Tiny 16-/14-/12-Bit SPI *nano*DAC+, with ±2 (16-Bit) LSB INL and 2 ppm/°C Reference

Data Sheet

AD5683R/AD5682R/AD5681R/AD5683

FEATURES

- **Ultrasmall package: 2 mm × 2 mm, 8-lead LFCSP**
- **High relative accuracy (INL): ±2 LSB maximum at 16 bits**
  - **AD5683R/AD5682R/AD5681R**
    - **Low drift, 2.5 V reference: 2 ppm/°C typical**
    - **Selectable span output: 2.5 V or 5 V**
  - **AD5683**
    - **External reference only**
    - **Selectable span output: V_{REF} or 2 × V_{REF}**
- **Total unadjusted error (TUE): 0.06% of FSR maximum**
  - **Offset error: ±1.5 mV maximum**
  - **Gain error: ±0.05% of FSR maximum**
- **Low glitch: 0.1 nV-sec**
- **High drive capability: 20 mA**
- **Low power: 1.2 mW at 3.3 V**
- **Independent logic supply: 1.62 V logic compatible**
- **Wide operating temperature range: −40°C to +105°C**
- **Robust 4 kV HBM ESD protection**

APPLICATIONS

- **Process controls**
- **Data acquisition systems**
- **Digital gain and offset adjustment**
- **Programmable voltage sources**

GENERAL DESCRIPTION

The AD5683R/AD5682R/AD5681R/AD5683, members of the *nano*DAC+® family, are low power, single-channel, 16-/14-/12-bit buffered voltage out digital-to-analog converters (DACs). The devices, except the AD5683, include an enabled by default internal 2.5 V reference, offering 2 ppm/°C drift. The output span can be programmed to be 0 V to V_{REF} or 0 V to 2 × V_{REF}. All devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design. The devices are available in a 2.00 mm × 2.00 mm, 8-lead LFCSP or a 10-lead MSOP.

The internal power-on reset circuit ensures that the DAC register is written to zero scale at power-up while the internal output buffer is configured in normal mode. The AD5683R/AD5682R/AD5681R/AD5683 contain a power-down mode that reduces the current consumption of the device to 2 µA (maximum) at 5 V and provides software selectable output loads while in power-down mode.

The AD5683R/AD5682R/AD5681R/AD5683 use a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz. Some devices also include asynchronous $\overline{RESET}$ pin and V_{LOGIC} pin options, allowing 1.8 V compatibility.

FUNCTIONAL BLOCK DIAGRAM

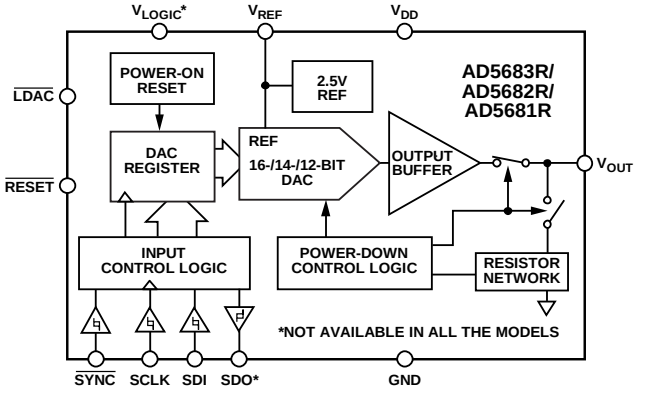

Figure 1. AD5683R/AD5682R/AD5681R MSOP
(For more information, see the Functional Block Diagrams—LFCSP section.)

Table 1. Single-Channel *nano*DAC+ Portfolio

Interface	Reference	16-Bit	14-Bit	12-Bit
SPI	Internal	AD5683R	AD5682R	AD5681R
	External	AD5683		
I²C	Internal	AD5693R	AD5692R	AD5691R
	External	AD5693		

PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL).
   AD5683R/AD5683 (16-bit): ±2 LSB maximum.
2. Low Drift, 2.5 V On-Chip Reference.
   2 ppm/°C typical temperature coefficient.
   5 ppm/°C maximum temperature coefficient.
3. Two Package Options.
   2.00 mm × 2.00 mm, 8-lead LFCSP.
   10-lead MSOP.

Rev. D **Document Feedback**

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Product Highlights ... 1
Revision History ... 2
Functional Block Diagrams—LFCSP ... 3
Specifications ... 4
AC Characteristics ... 6
Timing Characteristics ... 6
Absolute Maximum Ratings ... 8
Thermal Resistance ... 8
ESD Caution ... 8
Pin Configurations and Function Descriptions ... 9
Typical Performance Characteristics ... 11
Terminology ... 17
Theory of Operation ... 19
Digital-to-Analog Converter ... 19
Transfer Function ... 19
DAC Architecture ... 19
Serial Interface ... 21
SPI Serial Data Interface ... 21
Short Write Operation (AD5681R Only) ... 21
Internal Registers ... 23
Commands ... 23
Hardware $\overline{\text{LDAC}}$ ... 25
Hardware $\overline{\text{RESET}}$ ... 25
Thermal Hysteresis ... 26
Power-Up Sequence ... 26
Recommended Regulator ... 26
Layout Guidelines ... 26
Outline Dimensions ... 27
Ordering Guide ... 28

REVISION HISTORY

12/2016—Rev. C to Rev. D

Changed 1.8 V to 1.62 V, 1.8 V − 10% to 1.62 V, 5 V + 10% to 5.5 V, and 1.8 V ≤ V_{LOGIC} ≤ 2.7 V to 1.62 V ≤ V_{LOGIC} ≤ 2.7 V ..... Throughout
Changes to DC Power Supply Rejection Ratio, PSRR, Test Conditions/Comments Column, Table 2 ... 4

3/2016—Rev. B to Rev. C

Changes to Features Section ... 1
Changes to Specifications Section ... 4
Changes to Table 2 ... 5
Changes to AC Characteristics Section, Timing Characteristics Section, and Table 4 ... 6
Changes to Figure 4 ... 7
Changes to Table 7 ... 9
Changes to Table 8 ... 10
Changes to Terminology Section ... 17
Changes to SPI Serial Data Interface Section ... 21

10/2014—Rev. A to Rev. B

Changes to Table 1 ... 1
Changes to Figure 14 ... 11
Added Recommended Regulator Section ... 26
Changes to Ordering Guide ... 28

1/2014—Rev. 0 to Rev. A

Change to Features Section ... 1
Removed Endnote 2, Endnote 3, Endnote 5, and Endnote 6, Table 2; Renumbered Sequentially ... 5
Removed Endnote 2, Table 3; Renumbered Sequentially ... 6
Removed Endnote 1, Table 4; Renumbered Sequentially ... 6
Changes to Table 5 ... 8
Removed Solder Heat Reflow Section and Figure 53; Renumbered Sequentially ... 25

12/2013—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS—LFCSP

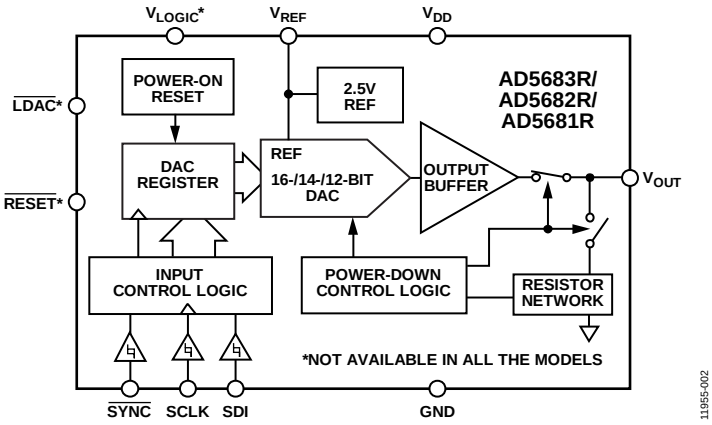


Figure 2. AD5683R/AD5682R/AD5681R LFCSP

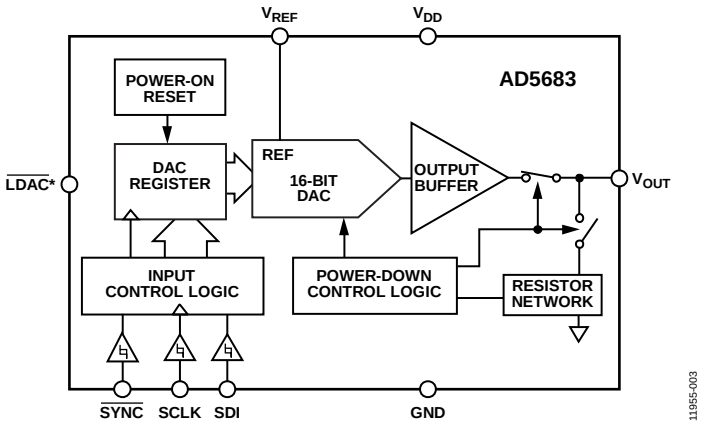


Figure 3. AD5683 LFCSP

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REF} = 2.5 V, V_{LOGIC}= 1.62 V to 5.5 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]					
AD5683R					
Resolution	16			Bits	
Relative Accuracy, INL				LSB	
A Grade			±8	LSB	
B Grade			±2	LSB	Gain = 2
			±3		Gain = 1
Differential Nonlinearity, DNL			±1	LSB	Guaranteed monotonic by design
AD5683					
Resolution	16			Bits	
Relative Accuracy, INL			±2	LSB	Gain = 2
			±3	LSB	Gain =1
Differential Nonlinearity, DNL			±1	LSB	Guaranteed monotonic by design
AD5682R					
Resolution	14			Bits	
Relative Accuracy, INL			±1	LSB	
Differential Nonlinearity, DNL			±1	LSB	Guaranteed monotonic by design
AD5681R					
Resolution	12			Bits	
Relative Accuracy, INL			±1	LSB	
Differential Nonlinearity, DNL			±1	LSB	Guaranteed monotonic by design
Zero-Code Error			1.25	mV	All 0s loaded to DAC register
Offset Error			±1.5	mV	
Full-Scale Error			±0.075	% of FSR	All 1s loaded to DAC register
Gain Error			±0.05	% of FSR	
Total Unadjusted Error, TUE			±0.16	% of FSR	Internal reference, gain = 1
			±0.14	% of FSR	Internal reference, gain = 2
			±0.075	% of FSR	External reference, gain = 1
			±0.06	% of FSR	External reference, gain = 2
Zero-Code Error Drift		±1		µV/°C	
Offset Error Drift		±1		µV/°C	
Gain Temperature Coefficient		±1		ppm/°C	
DC Power Supply Rejection Ratio, PSRR		0.2		mV/V	DAC code = midscale; V_{DD} = 5 V
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{REF}	V	Gain = 1
	0		2 × V_{REF}	V	Gain = 2
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 2 kΩ
Resistive Load	1			kΩ	C_L = 0 µF
Load Regulation		10		µV/mA	5 V, DAC code = midscale; −30 mA ≤ I_{OUT} ≤ +30 mA
		10		µV/mA	3 V, DAC code = midscale; −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current	20	30	50	mA	
Load Impedance at Rails[2]		20		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE OUTPUT					
Output Voltage	2.4975		2.5025	V	At ambient
Voltage Reference TC[3]					See the Terminology section
A-Grade		5	20	ppm/°C	
B-Grade		2	5	ppm/°C	
Output Impedance		0.05		Ω	
Output Voltage Noise		16.5		μV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		250		nV/√Hz	At ambient; f = 10 kHz, C_L = 10 nF
Capacitive Load Stability		5		μF	R_L = 2 kΩ
Load Regulation Sourcing		50		μV/mA	At ambient; V_{DD} ≥ 3 V
Load Regulation Sinking		30		μV/mA	At ambient
Output Current Load Capability		±5		mA	V_{DD} ≥ 3 V
Line Regulation		80		μV/V	At ambient
Thermal Hysteresis		125		ppm	First cycle
		25		ppm	Additional cycles
REFERENCE INPUT					
Reference Current		26		μA	$V_{REF} = V_{DD} = V_{LOGIC}$ = 5 V, gain = 1
		47		μA	$V_{REF} = V_{DD} = V_{LOGIC}$ = 5 V, gain = 2
Reference Input Range	1		V_{DD}	V	
Reference Input Impedance		120		kΩ	Gain = 1
		60		kΩ	Gain = 2
LOGIC INPUTS					
I_{IN}, Input Current			±1	μA	Per pin
V_{INL}, Input Low Voltage[4]			0.3 × V_{DD}	V	
V_{INH}, Input High Voltage[4]	0.7 × V_{DD}			V	
C_{IN}, Pin Capacitance		2		pF	
LOGIC OUTPUTS (SDO)[5]					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} − 0.4			V	I_{SOURCE} = 200 μA
Pin Capacitance		4		pF	
POWER REQUIREMENTS					
V_{LOGIC}[5]	1.62		5.5	V	
I_{LOGIC}[5]		0.25	3	μA	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND
V_{DD}	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}[6]					$V_{IH} = V_{DD}$, V_{IL} = GND
Normal Mode[7]		350	500	μA	Internal reference enabled
		110	180	μA	Internal reference disabled
Power-Down Modes[8]			2	μA	

[1] Linearity is calculated using a reduced code range: AD5683R and AD5683 (Code 512 to Code 65,535); AD5682R (Code 128 to Code 16,384); AD5681R (Code 32 to Code 4096). Output unloaded.
[2] When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 20 Ω typical channel resistance of the output devices; for example, when sinking 1 mA, the minimum output voltage = 20 Ω, 1 mA generates 20 mV. See Figure 38 (Headroom/Footroom vs. Load Current).
[3] Reference temperature coefficient is calculated as per the box method. See the Terminology section for more information.
[4] Substitute V_{LOGIC} for V_{DD} if device includes a V_{LOGIC} pin.
[5] The V_{LOGIC} and SDO pins are not available on all models.
[6] If the V_{LOGIC} pin is not available, $I_{DD} = I_{DD} + I_{LOGIC}$.
[7] Interface inactive. DAC active. DAC output unloaded.
[8] DAC powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REF} = 2.5 V, V_{LOGIC}= 1.62 V to 5.5 V, −40°C < T_A < +105°C, unless otherwise noted.[1]

Table 3.

Parameter	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Settling Time[2, 3]	5	7	µs	Gain = 1
Slew Rate	0.7		V/µs	
Digital-to-Analog Glitch Impulse[2]	0.1		nV-sec	±1 LSB change around major carry, gain = 2
Digital Feedthrough[2]	0.1		nV-sec	
Total Harmonic Distortion[2]	−83		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density	200		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise	6		µV p-p	0.1 Hz to 10 Hz; internal reference, DAC = zero scale
SNR	90		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SFDR	88		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SINAD	82		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] Temperature range = −40°C to +105°C, typical at 25°C.
[2] See the Terminology section.
[3] AD5683R/AD5683 to ±2 LSB, AD5682R to ±1 LSB, AD5681R to ±0.5 LSB.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, V_{LOGIC}= 1.62 V to 5.5 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 4.

		1.62 V ≤ V_{LOGIC} ≤ 2.7 V			2.7 V ≤ V_{LOGIC}[2] ≤ 5.5 V			Daisy Chain and Readback			
Parameter[1]	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SCLK Cycle Time	t_1	33			20			40			ns
SCLK High Time	t_2	16			10			20			ns
SCLK Low Time	t_3	16			10			20			ns
$\overline{SYNC}$ to SCLK Falling Edge Setup Time	t_4	15			10			20			ns
Data Setup Time	t_5	5			5			5			ns
Data Hold Time	t_6	5			5			5			ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	15			10			10			ns
Minimum $\overline{SYNC}$ High Time	t_8	20			20			40			ns
$\overline{SYNC}$ Falling Edge to SCLK Fall Ignore	t_9	16			10			10			ns
SDO Data Valid from SCLK Rising Edge	t_{10}									35	ns
$\overline{SYNC}$ Rising Edge to SCLK Falling Edge	t_{11}							10			ns
$\overline{SYNC}$ Rising Edge to SDO Disabled	t_{12}									60	ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge	t_{13}	25			25			25			ns
$\overline{LDAC}$ Pulse Width Low	t_{14}	20			15			15			ns
$\overline{RESET}$ Minimum Pulse Width Low	t_{15}	75			75			75			ns
$\overline{RESET}$ Pulse Activation Time	t_{16}	150			150			150			ns
$\overline{SYNC}$ Rising Edge to $\overline{SYNC}$ Rising Edge (DAC Updates)	t_{17}	1.9			1.7			1.7			µs
$\overline{LDAC}$ Falling Edge to $\overline{SYNC}$ Rising Edge	t_{18}	1.8			1.65			1.65			µs
Reference Power-Up[3]	$t_{REF_POWER_UP}$[4]		600			600			600		µs
Exit Shutdown[3]	$t_{SHUTDOWN}$[5]			6			6			6	µs

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Substitute V_{DD} for V_{LOGIC} on devices that do not include a V_{LOGIC} pin.
[3] Not shown in Figure 4.
[4] Same timing must be expected when powering up the device after V_{DD} = 2.7 V.
[5] Time required to exit power-down to normal mode of AD5683R/AD5682R/AD5681R operation; $\overline{SYNC}$ rising edge to 90% of DAC midscale value, with output unloaded.

Timing and Circuit Diagrams

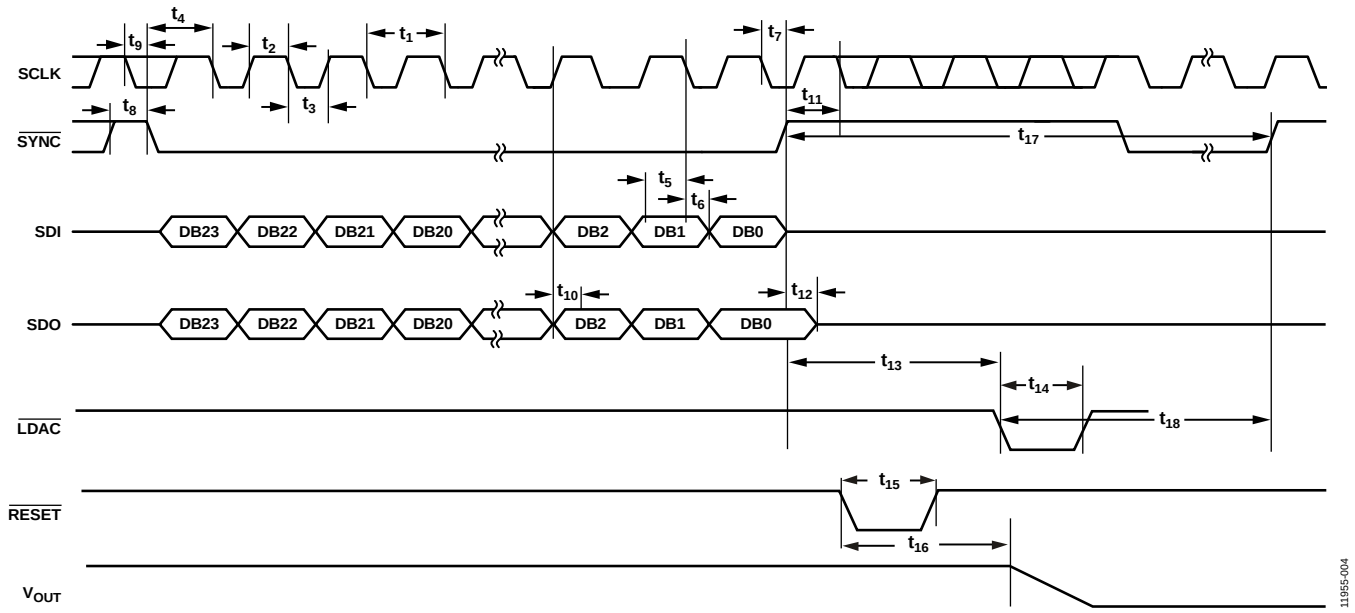


Figure 4. SPI Timing Diagram, Compatible with Mode 1 and Mode 2 (See the AN-1248 Application Note)

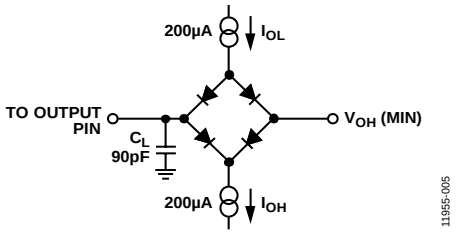


Figure 5. Load Circuit for Digital Output (SDO) Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V or +7 V (whichever is less)
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V or +7 V (whichever is less)
Digital Input Voltage to GND[1]	−0.3 V to V_{DD} + 0.3 V or +7 V (whichever is less)
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	135°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
ESD[2]	4 kV
FICDM[3]	1.25 kV

[1] Substitute VDD with VLOGIC on devices that include a VLOGIC pin.
[2] Human body model (HBM) classification.
[3] Field-Induced Charged-Device Model classification.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is defined by the JEDEC JESD51 standard, and the value is dependent on the test board and test environment.

Table 6. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP	90	25	°C/W
10-Lead MSOP	135	N/A	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

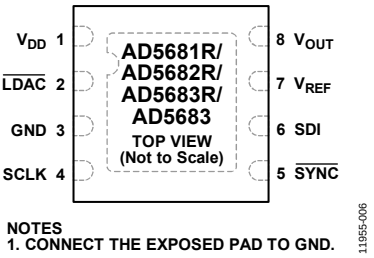


Figure 6. Pin Configuration, 8-Lead LFCSP, $\overline{LDAC}$ Option

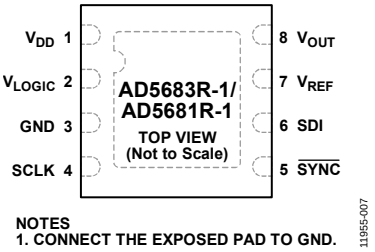


Figure 7. Pin Configuration, 8-Lead LFCSP, V_{LOGIC} Option

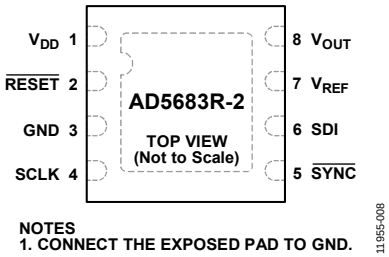


Figure 8. Pin Configuration, 8-Lead LFCSP, $\overline{RESET}$ Option

Table 7. Pin Function Descriptions, 8-Lead LFCSP

Pin No.				
$\overline{LDAC}$	V_{LOGIC}	$\overline{RESET}$	Mnemonic	Description
1	1	1	V_{DD}	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V. Decouple the supply to GND.
2	N/A	N/A	$\overline{LDAC}$	$\overline{LDAC}$ can be operated in asynchronous mode (see Figure 4). Pulsing this pin low allows the DAC register to be updated if the input register has new data. This pin can be tied permanently low; in this case, the DAC is automatically updated when new data is written to the input register.
N/A	2	N/A	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V to 5.5 V.
N/A	N/A	2	$\overline{RESET}$	Asynchronous Reset Input. The $\overline{RESET}$ input is low level sensitive. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored, the input and DAC registers are at their default values, and the output is connected to GND. Data written to the AD5683R is ignored. If not used, this pin can be tied to V_{LOGIC}.
3	3	3	GND	Ground Reference Point for All Circuitry on the Device.
4	4	4	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
5	5	5	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and SDI buffers and enables the input shift register. Data is transferred in on the falling edges of the next 24 clocks.
6	6	6	SDI	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
7	7	7	V_{REF}	AD5683R/AD5682R/AD5681R Reference Output. When using the internal reference, this is the reference output pin. The default for this pin is as a reference output. It is recommended that this pin be decoupled to GND with a 10 nF capacitor.
8	8	8	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.
0	0	0	EPAD	Exposed Pad. Connect the exposed pad to GND.

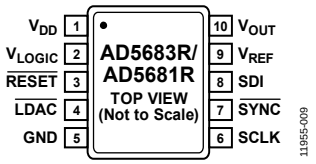


Figure 9. Pin Configuration, 10-Lead MSOP, V_{LOGIC} Option

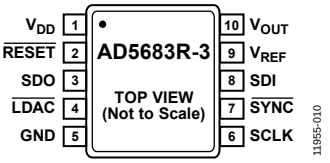


Figure 10. Pin Configuration, 10-Lead MSOP, SDO Option

Table 8. Pin Function Descriptions, 10-Lead MSOP

V_{LOGIC}	SDO	Mnemonic	Description
1	1	V_{DD}	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V. Decouple this pin to GND.
2	N/A	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V to 5.5 V. Decouple this pin to GND.
3	2	$\overline{RESET}$	Hardware Reset Pin. The $\overline{RESET}$ input is low level sensitive. When $\overline{RESET}$ is low, the device is reset and external pins are ignored. The input and DAC registers are loaded with a zero-scale value, and the write control register is loaded with default values. If not used, tie this pin to V_{LOGIC}.
N/A	3	SDO	Serial Data Output. Can be used for daisy chaining or readback commands.
4	4	$\overline{LDAC}$	Load DAC. Transfers the content of the input register to the DAC register. It can be operated in asynchronous mode (see Figure 4). This pin can be tied permanently low; in this case, the DAC register is automatically updated when new data is written to the input register.
5	5	GND	Ground Reference.
6	6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
7	7	$\overline{SYNC}$	Synchronization Data Input. When $\overline{SYNC}$ goes low, it enables the SCLK and SDI buffers and the input shift register.
8	8	SDI	Serial Data Input. Data is sampled on the falling edge of SCLK.
9	9	V_{REF}	Reference Input/Output. When using the internal reference, this is the reference output pin. The default for this pin is as a reference output. It is recommended that this pin be decoupled to GND with a 10 nF capacitor.
10	10	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.

TYPICAL PERFORMANCE CHARACTERISTICS

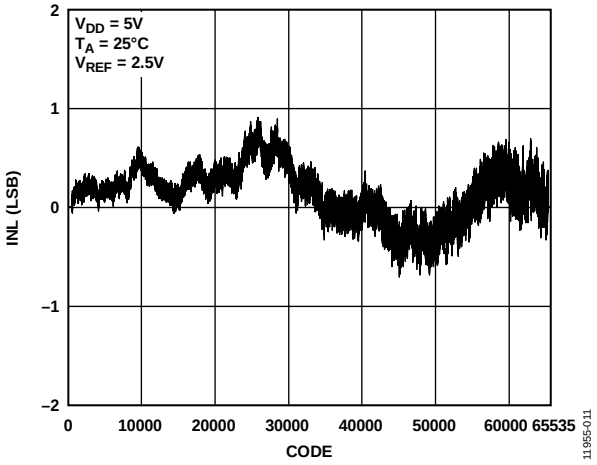


Figure 11. AD5683R/AD5683 INL

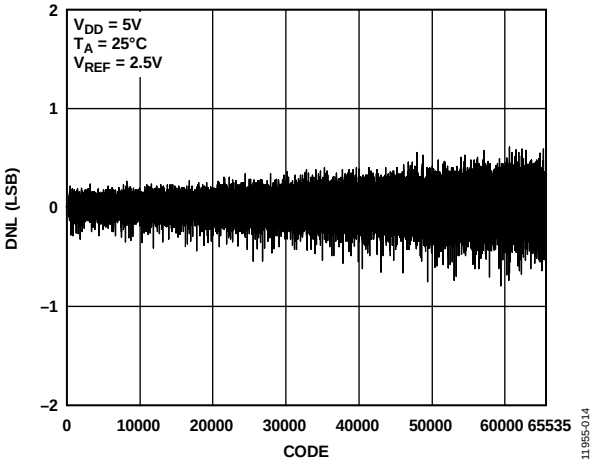


Figure 14. AD5683R/AD5683 DNL

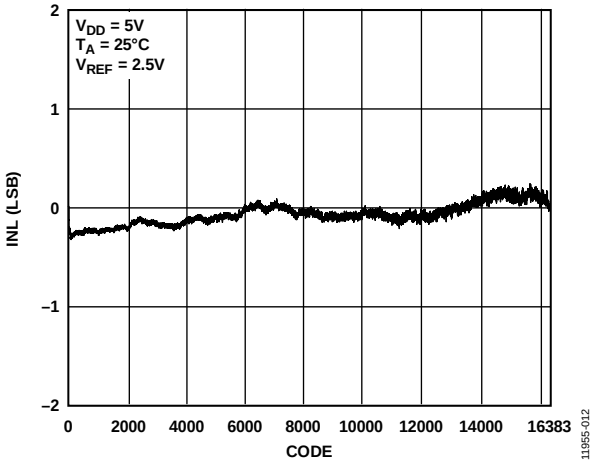


Figure 12. AD5682R INL

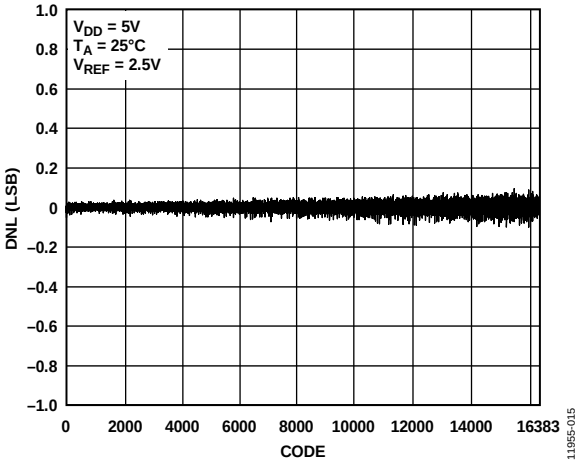


Figure 15. AD5682R DNL

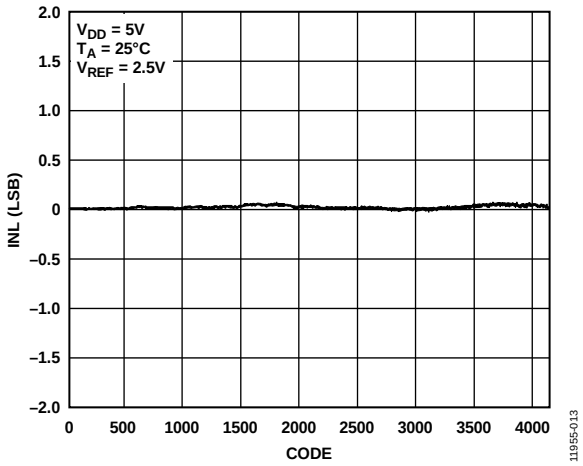


Figure 13. AD5681R INL

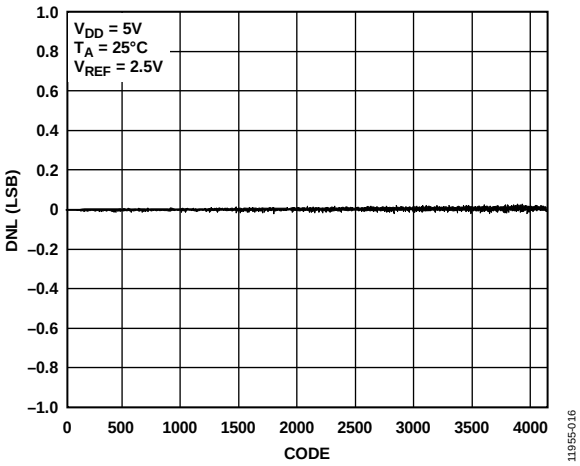


Figure 16. AD5681R DNL

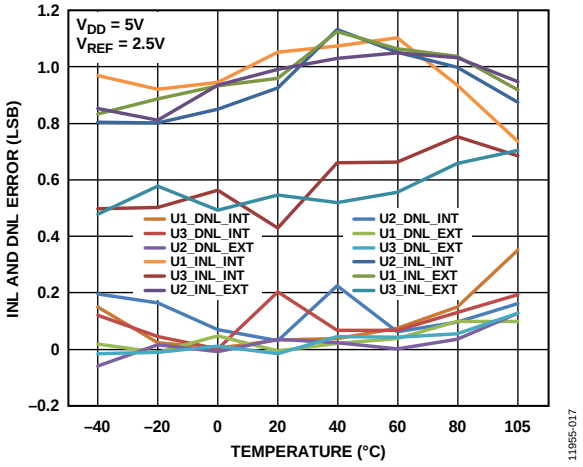


Figure 17. INL and DNL Error vs. Temperature (AD5683R/AD5683)

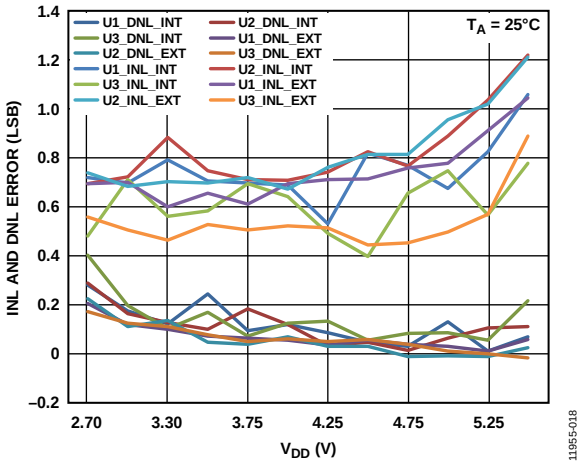


Figure 18. INL and DNL Error vs. Supply Voltage

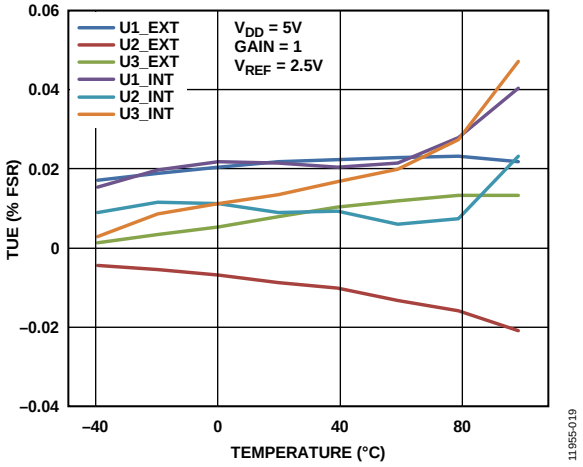


Figure 19. TUE vs. Temperature

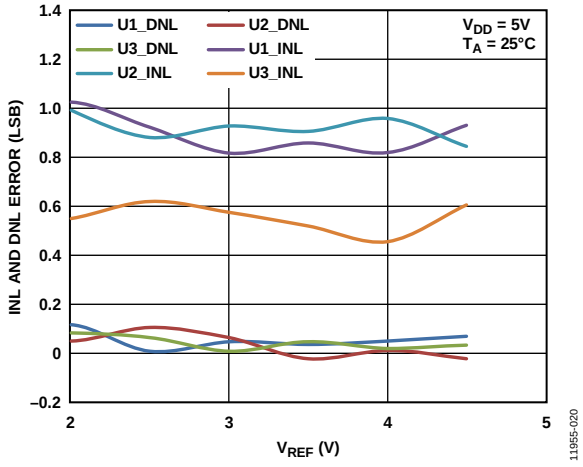


Figure 20. INL Error and DNL Error vs. V_{REF} (AD5683R/AD5683)

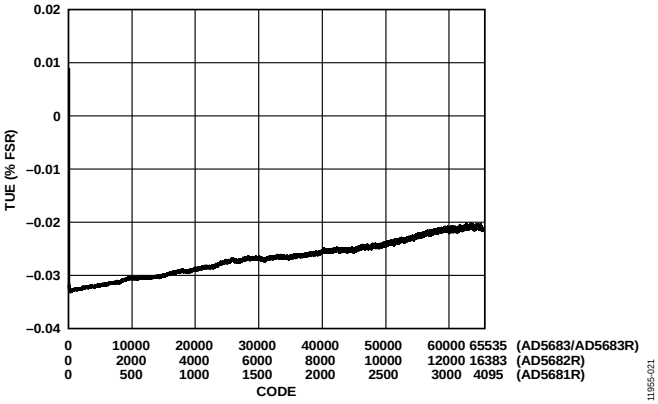


Figure 21. TUE vs. Code

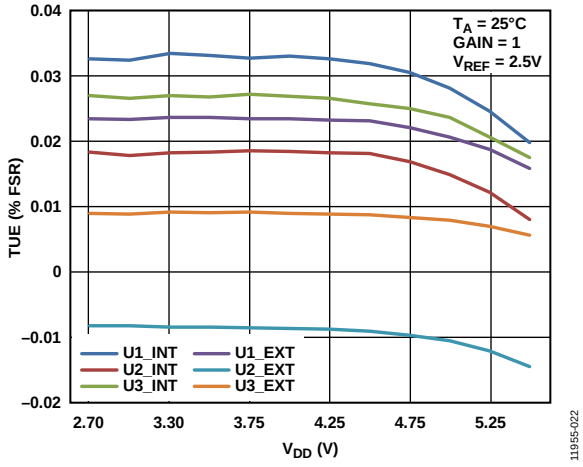


Figure 22. TUE vs. Supply

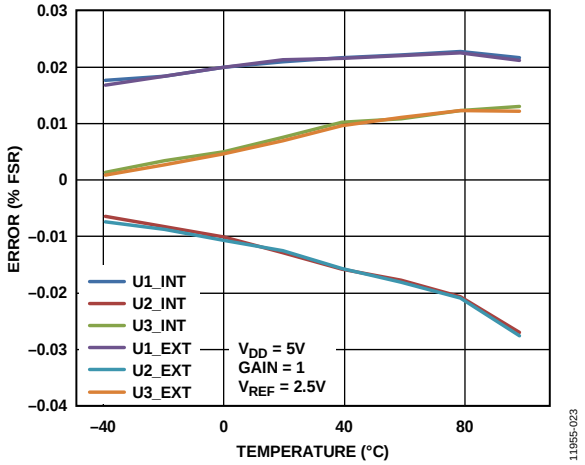


Figure 23. Gain Error and Full-Scale Error vs. Temperature

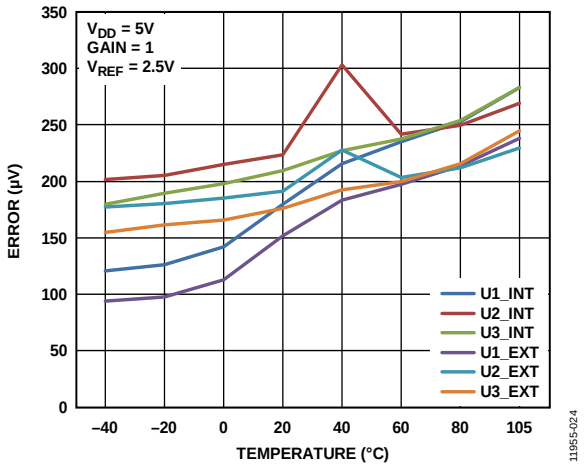


Figure 24. Zero Code Error and Offset Error vs. Temperature

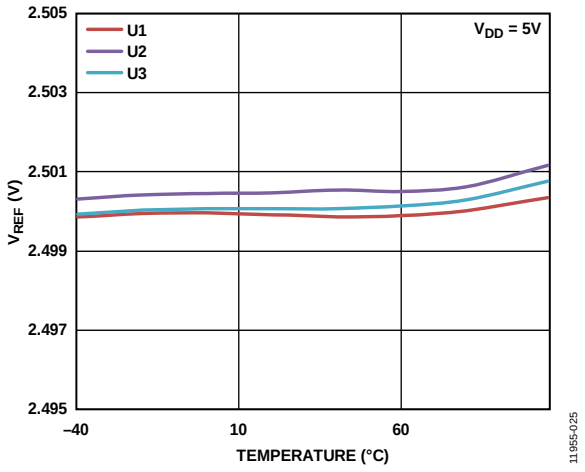


Figure 25. Internal Reference Voltage vs. Temperature (Grade B)

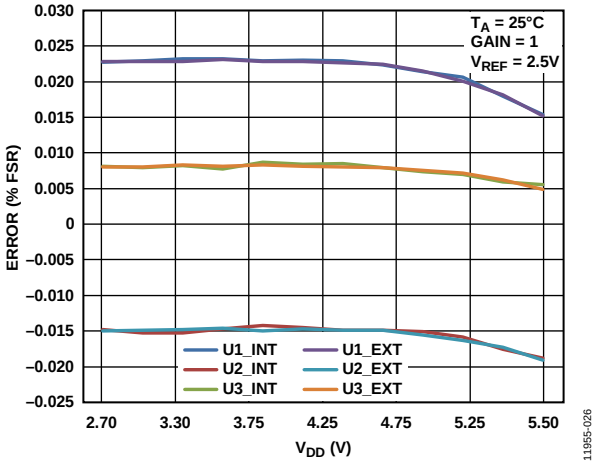


Figure 26. Gain Error and Full-Scale Error vs. Supply

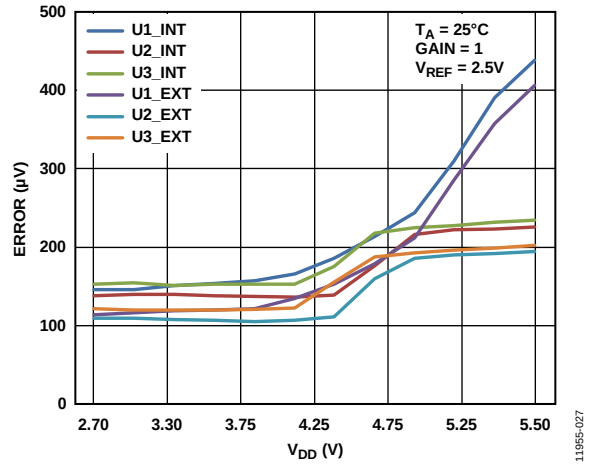


Figure 27. Zero Code Error and Offset Error vs. Supply

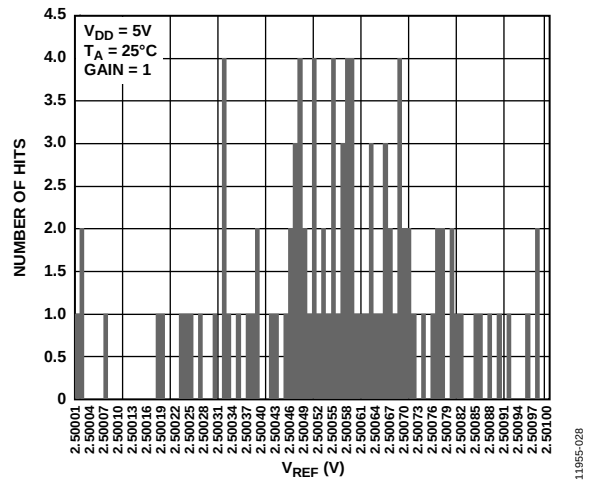


Figure 28. Reference Output Spread

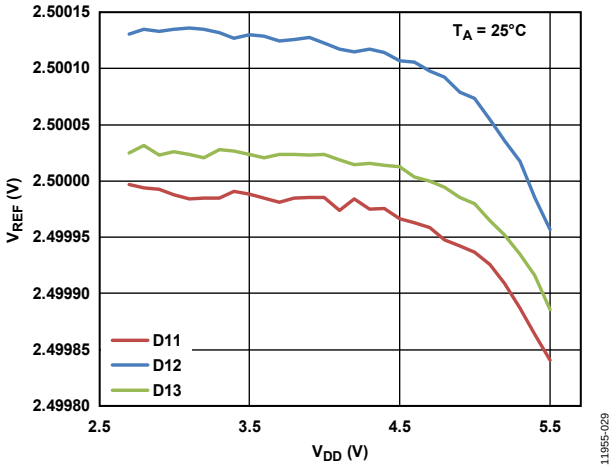


Figure 29. Internal Reference Voltage vs. Supply Voltage

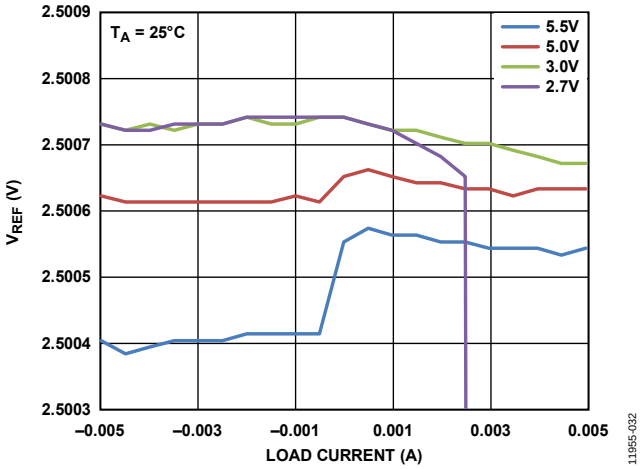


Figure 32. Internal Reference Voltage vs. Load Current

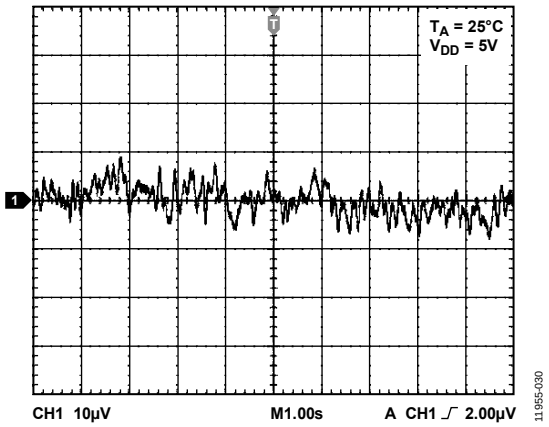


Figure 30. Internal Reference Noise, 0.1 Hz to 10 Hz

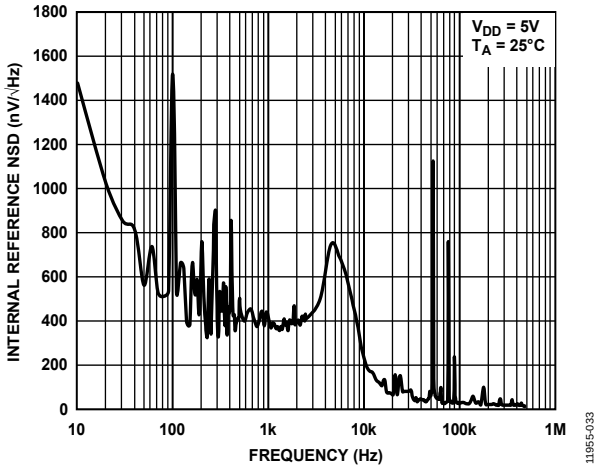


Figure 33. Internal Reference Noise Spectral Density vs. Frequency

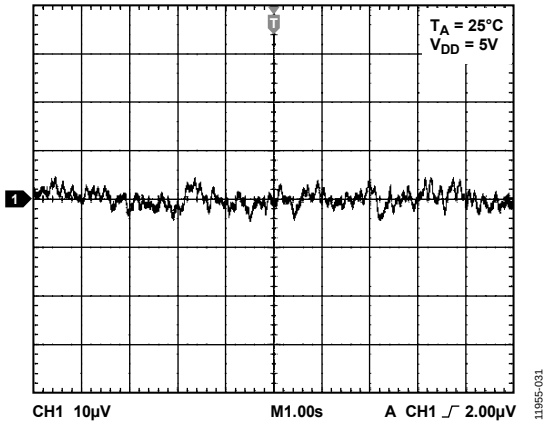


Figure 31. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference On

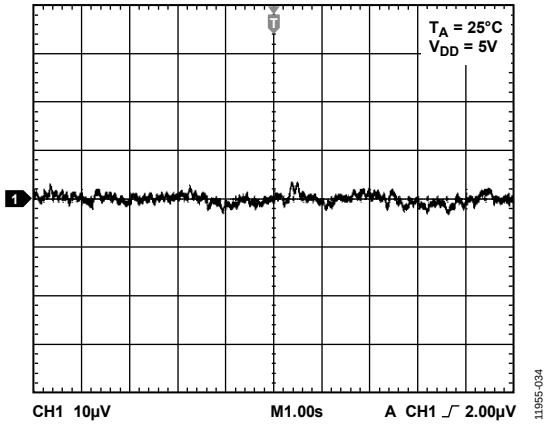


Figure 34. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

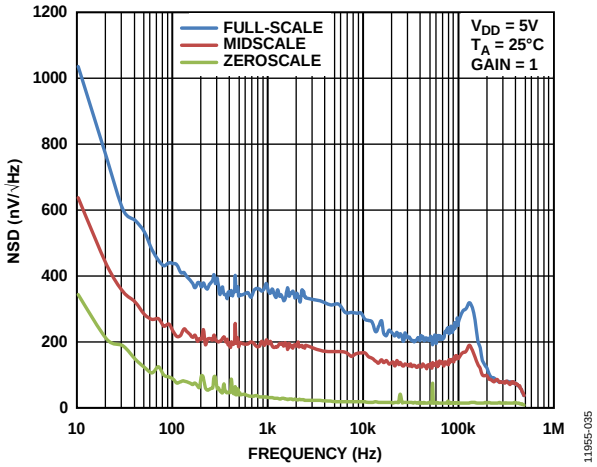


Figure 35. Noise Spectral Density vs. Frequency, Gain = 1

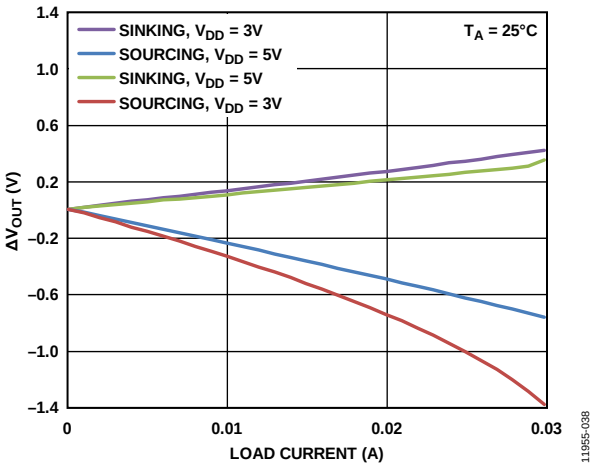


Figure 38. Headroom/Footroom vs. Load Current

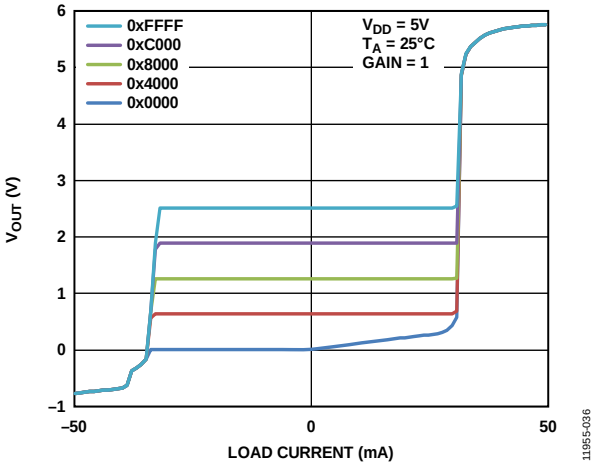


Figure 36. Source and Sink Capability, Gain = 1

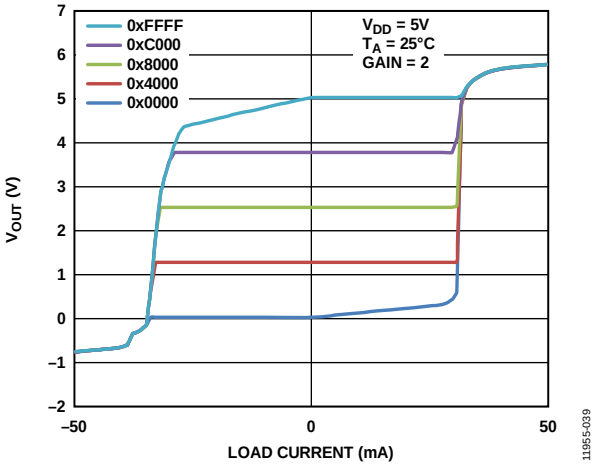


Figure 39. Source and Sink Capability, Gain = 2

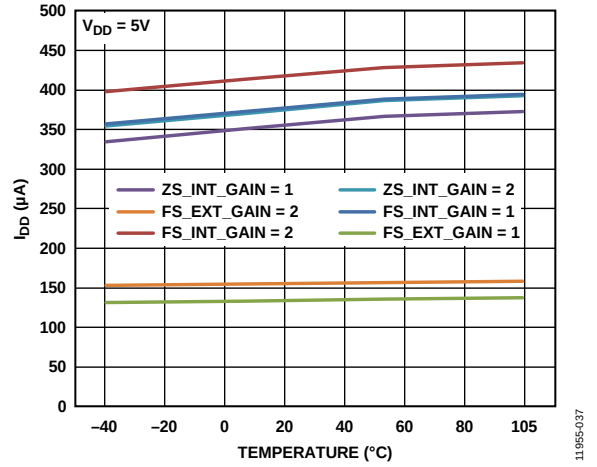


Figure 37. Supply Current vs. Temperature

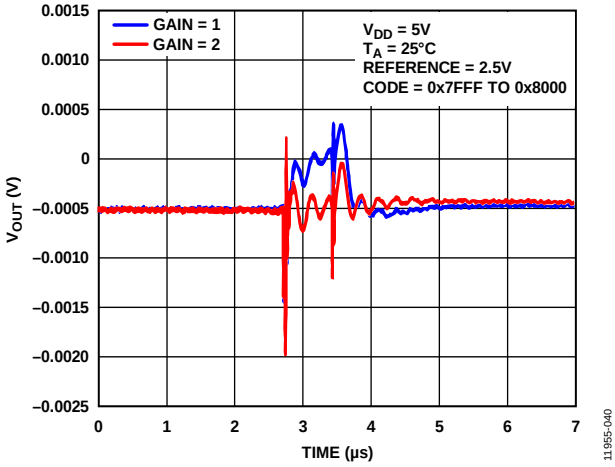


Figure 40. Digital-to-Analog Glitch Impulse

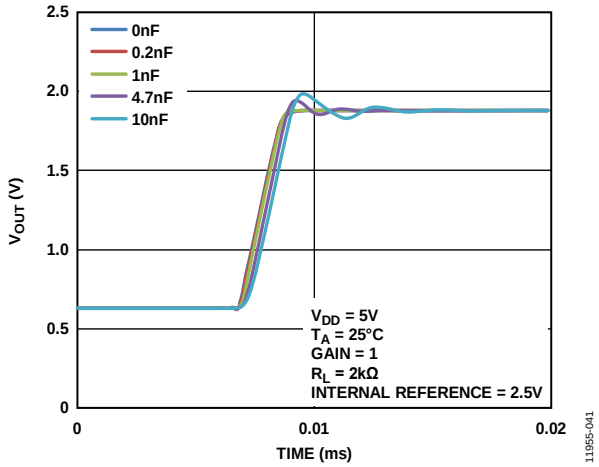


Figure 41. Capacitive Load vs. Settling Time, Gain = 1

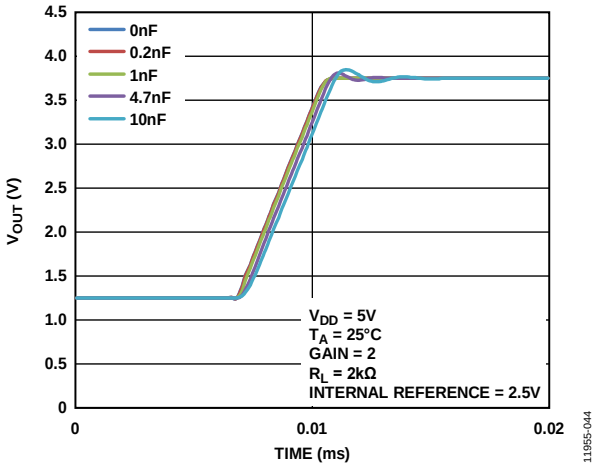


Figure 44. Capacitive Load vs. Settling Time, Gain = 2

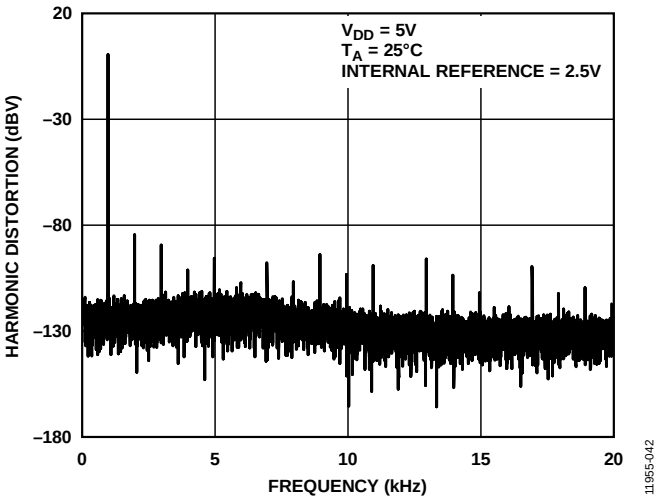


Figure 42. Total Harmonic Distortion at 1 kHz

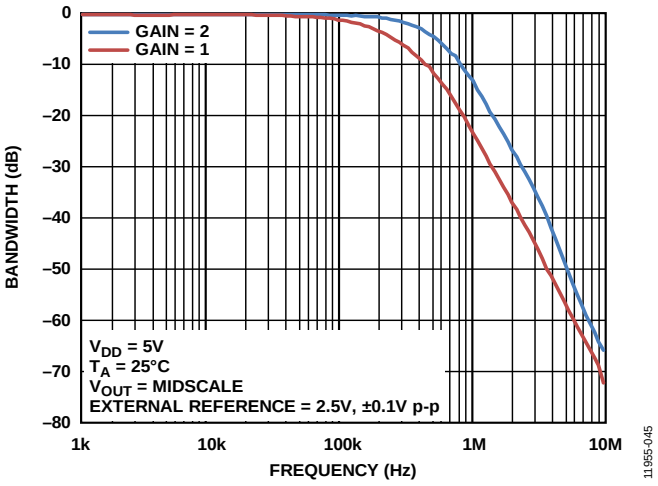


Figure 45. Multiplying Bandwidth, External Reference 2.5 V ± 0.1 V p-p, 10 kHz to 10 MHz

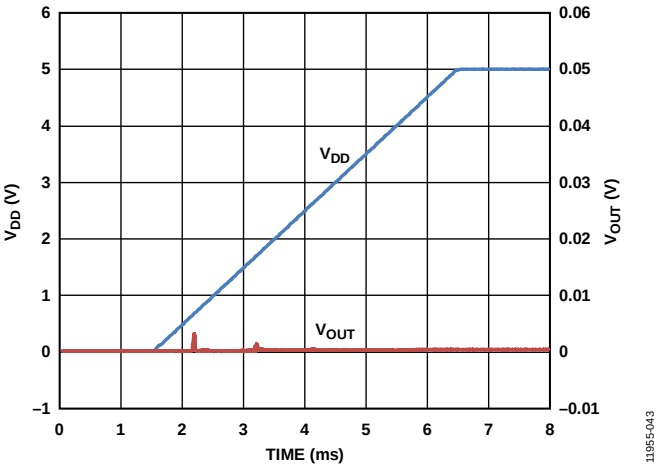


Figure 43. Power-On Reset to 0 V

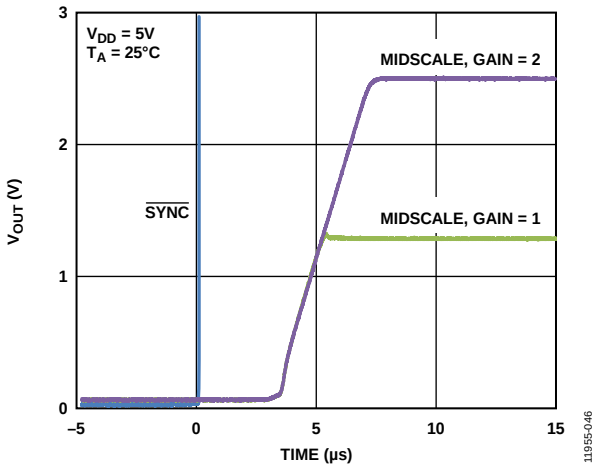


Figure 46. Exiting Power-Down to Midscale

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. See Figure 11, Figure 12, and Figure 13 for typical INL vs. code plots.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. See Figure 14, Figure 15, and Figure 16 for typical DNL vs. code plots.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output must be 0 V. The zero code error is always positive in the AD5683R/AD5682R/AD5681R because the output of the DAC cannot fall below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV. A plot of zero code error vs. temperature is shown in Figure 24.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output must be V_{REF} − 1 LSB or |2 × V_{REF}| − 1 LSB. Full-scale error is expressed in percent of full-scale range (% of FSR). See Figure 23 and Figure 26 for plots of full-scale error.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Zero-Code Error Drift
Zero-code error drift is a measurement of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5683R with Code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for mid-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ scale input change.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000), as shown in Figure 40.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. Digital feedthrough is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Output Noise Spectral Density
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. See Figure 31, Figure 34, and Figure 35 for a plot of noise spectral density. The noise spectral density for the internal reference is shown in Figure 30 and Figure 33.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this finite bandwidth. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
THD is the difference between an ideal sine wave and the attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:

V_{REFmax} is the maximum reference output measured over the total temperature range.

V_{REFmin} is the minimum reference output measured over the total temperature range.

V_{REFnom} is the nominal reference output voltage, 2.5 V.

TempRange is the specified temperature range, −40°C to +105°C.

Thermal Hysteresis

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5683R/AD5682R/AD5681R are single 16-bit, 14-bit, and 12-bit, serial input, voltage output DACs with a 2.5 V internal reference. The devices operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5683R/AD5682R/AD5681R in a 24-bit word format via a 3-wire serial interface. The AD5683R/AD5682R/AD5681R incorporate a power-on reset circuit that ensures that the DAC output powers up to a zero scale. The devices also have a software power-down mode that reduces the typical current consumption to 2 µA maximum.

TRANSFER FUNCTION

The internal reference is on by default. For users that need an external reference, the AD5683 is available. The input coding to the DAC is straight binary. The ideal output voltage is given by the following equations:

For the AD5683R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[\frac{D}{65,536}\right]$$

For the AD5682R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[\frac{D}{16,384}\right]$$

For the AD5681R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[\frac{D}{4096}\right]$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register.
Gain is the gain of the output amplifier. By default, it is set to ×1. The gain can also be set to ×2 using the gain bit in the write control register.

DAC ARCHITECTURE

The AD5683R/AD5682R/AD5681R/AD5683 implements segmented string DAC architecture with an internal output buffer. Figure 47 shows the internal block diagram.

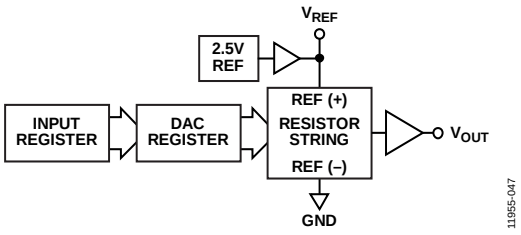


Figure 47. DAC Channel Architecture Block Diagram

The simplified segmented resistor string DAC structure is shown in Figure 48. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has same value, R, the string DAC is guaranteed monotonic.

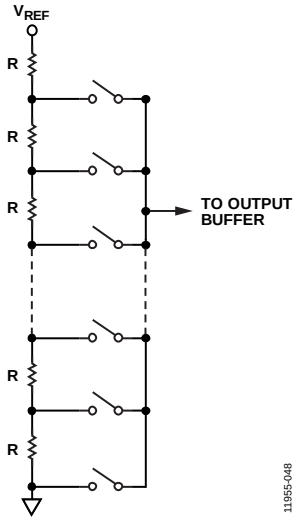


Figure 48. Simplified Resistor String Structure

Internal Reference

The AD5683R/AD5682R/AD5681R on-chip reference is on at power-up but can be disabled via a write to the write control register.

The AD5683R/AD5682R/AD5681R each have a 2.5 V, 2 ppm/°C reference, giving a full-scale output of 2.5 V or 5 V, depending on the state of the gain bit.

The internal reference is available at the V_{REF} pin. It is internally buffered and capable of driving external loads of up to 50 mA.

External Reference

The V_{REF} pin is an input pin in the AD5683. It can also be configured as an input pin on the AD5683R/AD5682R/AD5681R, allowing the use of an external reference if the application requires it.

In the AD5683R/AD5682R/AD5681R, the default condition of the on-chip reference is on at power-up. Before connecting an external reference to the pin, disable the internal reference by writing to the REF bit (Bit DB16) in the write control register.

Output Buffer

The output buffer is designed as an input/output rail-to-rail, which gives a maximum output voltage range of up to V_{DD}. The gain bit sets the segmented string DAC gain to ×1 or ×2, as shown in Table 12.

The output buffer voltage is determined by V_{REF}, the gain bit, and the offset and gain errors.

The output buffer can drive a 10 nF capacitance with a 2 kΩ resistor in parallel, as shown in Figure 41 and Figure 44. If a higher capacitance load is required, use the snubber method or a shunt resistor to isolate the load from the output amplifier. The slew rate is 0.7 V/μs with a ¼ to ¾ scale settling time of 5 μs.

SERIAL INTERFACE

The AD5683R/AD5682R/AD5681R/AD5683 uses a 3-wire serial interface that is compatible with some SPI modes, Mode 1 and Mode 2, as well as with completely synchronous interfaces such as SPORT. See Figure 4 for a timing diagram of a typical write sequence. See the AN-1248 Application Note for more information about the SPI interface.

SPI SERIAL DATA INTERFACE

Pulling low $\overline{\text{SYNC}}$ pin, the internal input shift register is enabled, the data in the SDI pin is sampled into the input shift register on the falling edge of SCLK. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word (24-bits) is loaded from the SDI pin (see Figure 4). When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded, following the instructions in Table 9.

Between consecutive data-words, $\overline{\text{SYNC}}$ must be held high for a minimum of 20 ns. Between consecutive DAC updates, $\overline{\text{SYNC}}$ must be held high for more than 20 ns to satisfy the DAC update condition as shown in Figure 4.

If $\overline{\text{SYNC}}$ is brought high after 24 falling clock edges, it is interpreted as a valid write, and the first 24 bits are loaded to the input shift register.

To minimize power consumption, it is recommended that all serial interface pins be operated close to the supply rails.

SHORT WRITE OPERATION (AD5681R ONLY)

The AD5681R SPI serial interface allows data to be transferred using a smaller number of clocks, if required. The last eight bits are don't care bits if the input or DAC registers are written as shown in Table 9. To increase the DAC update rate, the size of the data-word can be reduced.

If $\overline{\text{SYNC}}$ is brought high between 16 and 24 clock edges, this is interpreted as a valid write and only the first 16 bits are decoded, as shown in Figure 49. If $\overline{\text{SYNC}}$ is brought high before 16 falling clock edges, the serial write is ignored and the write sequence is considered invalid. If the DCEN bit is enabled, this functionality is not available (see Table 11).

SDO Pin

The serial data output pin (SDO), which is available only in the AD5683R, serves two purposes: to read back the contents of the DAC registers and to connect the device in daisy-chain mode.

The SDO pin contains a push-pull output that internally includes a weak pull-down resistor. The data is clocked out of SDO on the rising edge of SCLK, as shown in Figure 4, and the pin is active only when the DCEN bit is enabled in the write control register or automatically enabled during a readback command. In standby mode, the internal pull-down resistor forces a Logic 0 on the bus. Due to the high value of the internal pull-down resistor, other devices can have control over the SDO line if a parallel connection is made.

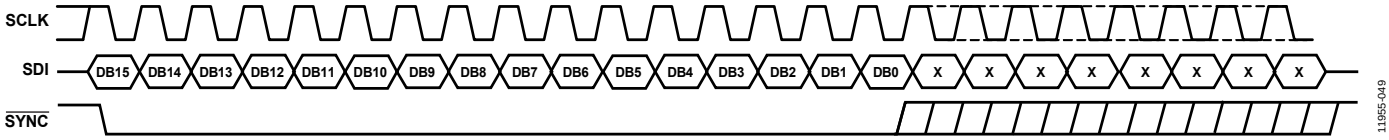


Figure 49. Short Write on the AD5681R

Daisy-Chain Connection

Daisy chaining minimizes the number of pins required from the controlling IC. As shown in Figure 50, the SDO pin of one package must be tied to the SDI pin of the next package. The clock period may need to be increased, as shown in Table 4, because of the propagation delay of the line between subsequent devices.

By default, the SDO pin is disabled. To enable daisy-chain operation, the DCEN bit must be set in the write control register (see Table 10).

When the daisy-chain mode is enabled (DCEN = 1), the AD5683R/AD5682R/AD5681R/AD5683 accept as a valid frame any data-word larger than 24 bits, decoding the last 24 bits received, as shown in Figure 51.

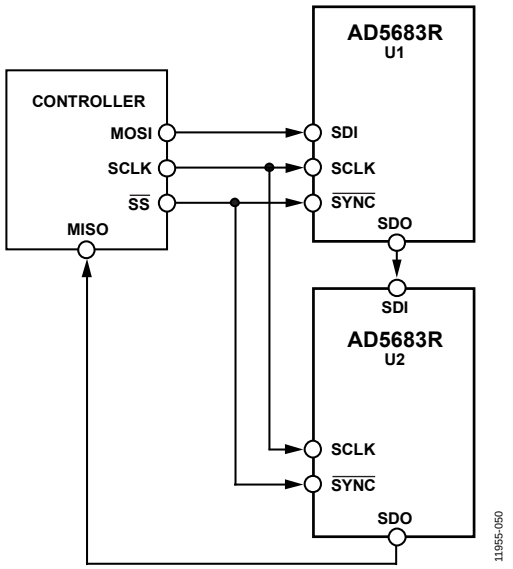


Figure 50. Daisy-Chain Connection

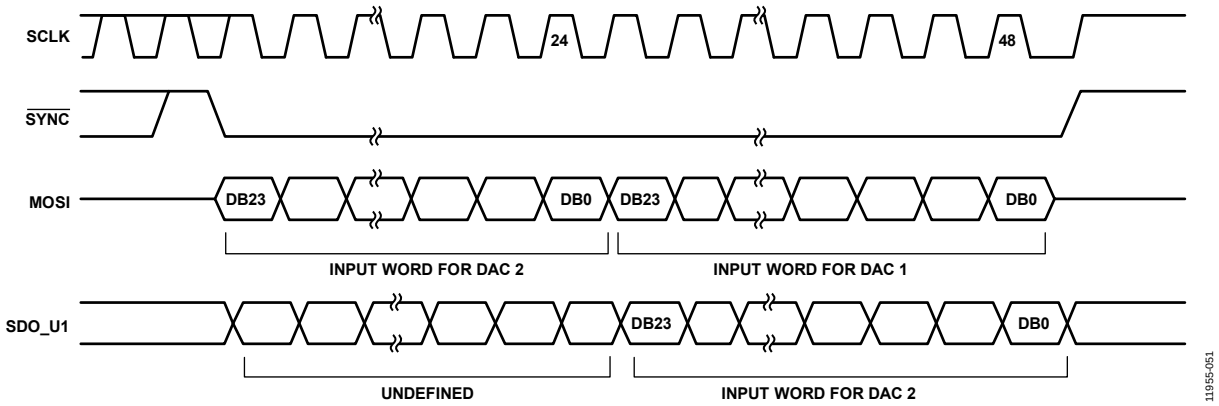


Figure 51. Daisy-Chain Timing Diagram

INTERNAL REGISTERS

Input Shift Register

The shift register of the AD5683R/AD5682R/AD5681R/AD5683 is 24 bits wide. Serial data is loaded MSB first (DB23) and the first four bits are the command bits, C3 to C0, followed by the data bits.

The data bits comprise a 20-bit, 18-bit, or 16-bit input code, followed by a number of don't care bits as shown in Table 9. The command is decoded on the rising edge of $\overline{SYNC}$.

Input Register

The input register acts as a buffer to preload new data. This register does not control the voltage in the V_{OUT} pin. There are two different ways to transfer the contents of the input register to the DAC register: by software or by hardware.

DAC Register

The DAC register controls the voltage in the V_{OUT} pin. This register can be updated by issuing a command or by transferring the contents of the input register to the DAC register.

COMMANDS

Write Input Register

The input register allows the preloading of a new value for the DAC register. The transfer from the input register to the DAC register can be triggered by hardware, by the $\overline{LDAC}$ pin, or by software using Command 2.

If new data is loaded into the DAC register directly using Command 3, the DAC register automatically overwrites the input register.

Update DAC Register

This command transfers the contents of the input register to the DAC register and, consequently, the V_{OUT} pin is updated.

This operation is equivalent to a software $\overline{LDAC}$.

Write DAC Register

The DAC register controls the output voltage in the DAC. This command updates the DAC register on completion of the write operation. The input register is refreshed automatically with the DAC register value.

Table 9. Command Operation

Command [DB23:DB20]				Data Bits [DB19:DB0][1]												
C3	C2	C1	C0	DB19	DB18	DB17	DB16	DB15	DB14	[DB13:DB8]	DB7	DB6	DB5	DB4	[DB3:DB0]	Operation
0	0	0	0	X	X	X	X	X	X	X…X	X	X	X	X	X…X	Do nothing
0	0	0	1	DB15	DB14	DB13	DB12	DB11	DB10	DB9…DB4	DB3[2]	DB2[2]	DB1[2,3]	DB0[2,3]	X…X	Write input register
0	0	1	0	X	X	X	X	X	X	X…X	X	X	X	X	X…X	Update DAC register (software $\overline{LDAC}$)
0	0	1	1	DB15	DB14	DB13	DB12	DB11	DB10	DB9…DB4	DB3[2]	DB2[2]	DB1[2,3]	DB0[2,3]	X…X	Write DAC and input register
0	1	0	0	DB19	DB18	DB17	DB16	DB15	DB14	0…0	0	0	0	0	0…0	Write control register
0	1	0	1	X	X	X	X	X	X	X…X	X	X	X	X	X…X	Readback input register

[1] X means don't care.
[2] This bit is a don't care bit for the AD5681R only.
[3] This bit is a don't care bit for the AD5682R only.

Write Control Register

The write control register sets the power-down and gain functions. It also enables/disables the internal reference and perform a software reset. See Table 10 for the write control register functionality.

Table 10. Write Control Register Bits

DB19	DB18	DB17	DB16	DB15	DB14
Reset	PD1	PD0	REF	Gain	DCEN

DCEN Bit

The daisy-chain enable bit (DCEN, Bit DB14) enables the SDO pin, allowing the device to operate in daisy-chain mode. This bit is automatically disabled when a readback command is executed. Enabling this bit disables the write short command feature in the AD5681R.

Table 11. Daisy-Chain Enable Bit (DCEN)

DB0	Mode
0	Standalone mode (default)
1	DCEN mode

Gain Bit

The gain bit selects the gain of the output amplifier. Table 12 shows how the output voltage range corresponds to the state of the gain bit.

Table 12. Gain Bit

Gain	Output Voltage Range
0	0 V to V_{REF} (default)
1	0 V to 2 × V_{REF}

REF Bit

The on-chip reference is on at power-up by default. This reference can be turned on or off by setting a software-programmable bit, DB16, in the write control register. Table 13 shows how the state of the bit corresponds to the mode of operation.

To reduce the power consumption, it is recommended to disable the internal reference if the device is placed in power-down mode.

Table 13. Reference Bit (REF)

REF	Reference Function
0	Reference enabled (default)
1	Reference disabled

PD0 and PD1 Bits

The AD5683R/AD5682R/AD5681R contain two separate mode of operation that are accessed by writing to the write control register.

In normal mode, the output buffer is directly connected to the V_{OUT} pin.

In power-down mode, the output buffer is internally disabled and the V_{OUT} pin output impedance can be selected to a well-known value, as shown in Table 14.

Table 14. Operation Modes

Operating Mode	PD1	PD0
Normal Mode	0	0
Power-Down Modes		
1 kΩ Output Impedance	0	1
100 kΩ Output Impedance	1	0
Three-State Output Impedance	1	1

In power-down mode, the device disables the output buffer but does not disable the internal reference. To achieve maximum power savings, it is recommend to disable the REF bit, if possible.

Disabling both the internal reference and the output buffer results in the supply current falling to 2 µA at 5 V.

The output stage is shown in Figure 52.

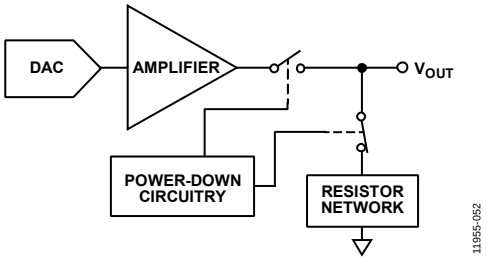


Figure 52. Output Stage During Power-Down

The output amplifier is shut down when the power-down mode is activated. However, unless the internal reference is powered down (using Bit DB16 in the write control register), the bias generator, reference, and resistor string remain on. When in power-down mode, the weak SDO resistor is also disconnected. The supply current falls to 2 µA at 5 V. The contents of the DAC register are unaffected when in power-down mode, and the DAC register can continue to be updated. The time that is required to exit power-down is typically 4 µs for V_{DD} = 5 V, or 600 µs if the reference is disabled.

Reset Bit

The write control register of the AD5683R/AD5682R/AD5681R contains a software reset function that resets the input and DAC registers to zero scale and resets the write control register to the default value. A software reset is initiated by setting the reset bit (Bit DB19) in the write control register to 1. When the software reset is complete, the reset bit is cleared to 0 automatically.

Readback Input Register

The AD5683R allows readback of the contents of the input register through the SDO pin by using Command 5 (see Table 9), as shown in Figure 53.

The SDO pin is automatically enabled for the duration of the read operation, after which it is disabled again, as shown in Table 15. If the DCEN bit was enabled before the read operation, the bit is reset after a readback operation. If the AD5683R was operating in daisy-chain mode, the user must enable the DCEN bit again.

Table 15. Write and Readback sequence

SDI	SDO	Action
0x180000	0x000000	Write 0x8000 to the input register
0x500000	0x000000	Prepare data read from the input register
0x000000	0xX8000X[1]	Clock out the data

[1] X mean don't care.

HARDWARE $\overline{\text{LDAC}}$

The DACs of the AD5683R/AD5682R/AD5681R/AD5683 have a double buffered interface consisting of an input register and a DAC register. The $\overline{\text{LDAC}}$ transfers data from the input register to the DAC register and, consequently, the output is updated.

Hold $\overline{\text{LDAC}}$ high while data is clocked into the input shift register. The DAC output is updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high. The output DAC is updated on the falling edge of $\overline{\text{LDAC}}$.

If $\overline{\text{LDAC}}$ is pulsed while the data is being clocked, the pulse is ignored.

HARDWARE $\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is an active low signal that sets the input and DAC registers to zero scale and the control registers to their default values. It is necessary to keep $\overline{\text{RESET}}$ low for 75 ns to complete the operation. When the $\overline{\text{RESET}}$ signal returns high, the output remains at the zero scale until a new value is programmed. While the $\overline{\text{RESET}}$ pin is low, the AD5683R/AD5681R ignore any new command.

If $\overline{\text{RESET}}$ is held low at power-up, the internal reference is not initialized correctly until the $\overline{\text{RESET}}$ pin is released.

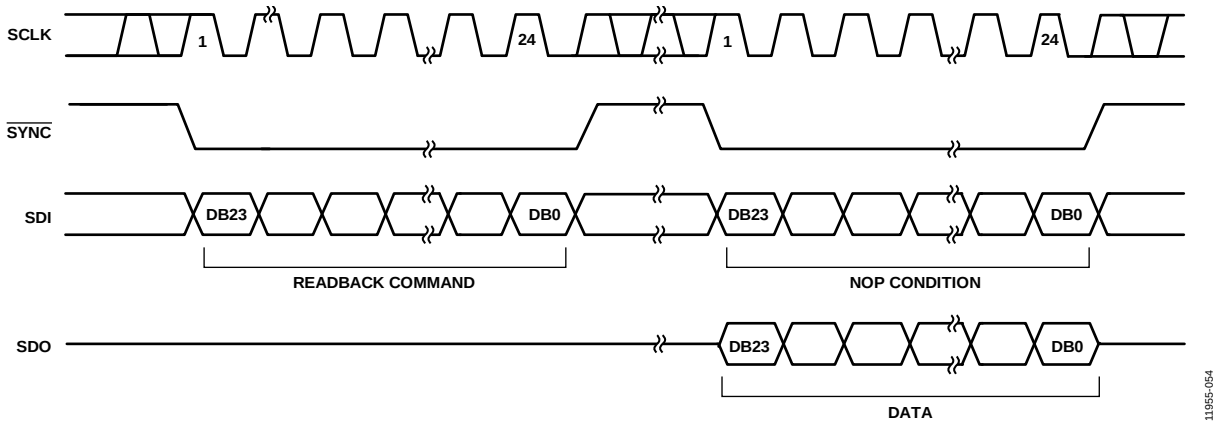


Figure 53. Readback Operation

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient.

The thermal hysteresis data is shown in Figure 54. It is measured by sweeping the temperature from ambient to −40°C, then to +105°C, and finally returning to ambient. The V_{REF} delta is next measured between the two ambient measurements; the result is shown in a solid line in Figure 54. The same temperature sweep and measurements were immediately repeated; the results are shown in a patterned line in Figure 54.

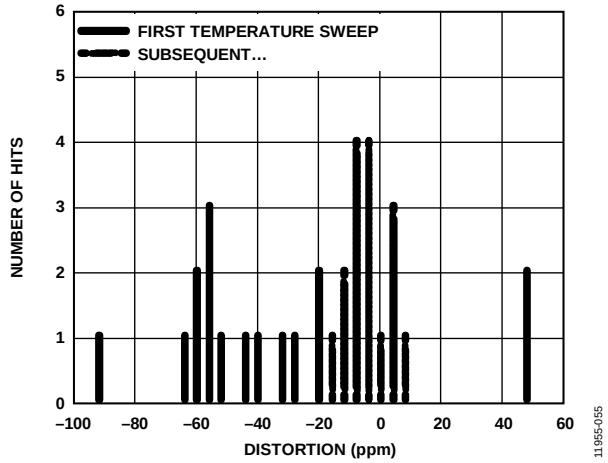


Figure 54. Thermal Hysteresis

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at the digital pins and analog pins, it is important to power GND first before applying any voltage to V_{DD}, V_{OUT}, and V_{LOGIC}. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally. The ideal power-up sequence is GND, V_{DD}, V_{LOGIC}, V_{REF}, followed by the digital inputs.

RECOMMENDED REGULATOR

The AD5683R/AD5682R/AD5681R/AD5683 use a 5 V (V_{DD}) supply as well as a digital logic supply (V_{LOGIC}).

The analog and digital supplies required for the AD5683R/AD5682R/AD5681R/AD5683 can be generated using Analog Devices, Inc., low dropout (LDO) regulators such as the ADP7118 and the ADP162, respectively, for analog and digital supplies.

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board (PCB) on which the ADCs are mounted must be designed such that the AD5683R/AD5682R/AD5681R/AD5683 lie on the analog plane.

Ensure that the AD5683R/AD5682R/AD5681R/AD5683 have ample supply bypassing of 10 µF, in parallel with a 0.1 µF capacitor on each supply that is located as near to the package as possible (ideally, right up against the device). The 10 µF capacitors are of the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The LFCSP packages of the AD5683R/AD5682R/AD5681R/AD5683 have an exposed pad beneath the device. Connect this pad to the GND supply of the device. For optimum performance, use special consideration when designing the motherboard and mounting the package. For enhanced thermal, electrical, and board level performance, solder the exposed pad on the bottom of the package to the corresponding thermal land pad on the PCB. Design thermal vias into the PCB land pad area to further improve heat dissipation.

The GND plane on the device can be increased (as shown in Figure 55) to provide a natural heat sinking effect.

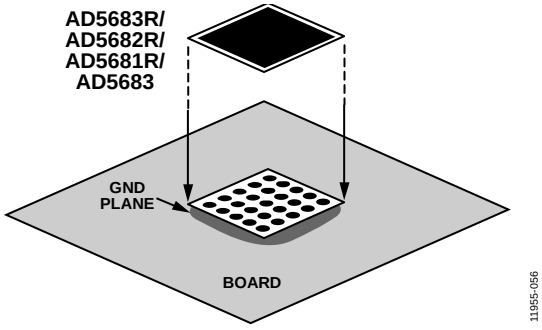


Figure 55. Pad Connection to Board

OUTLINE DIMENSIONS

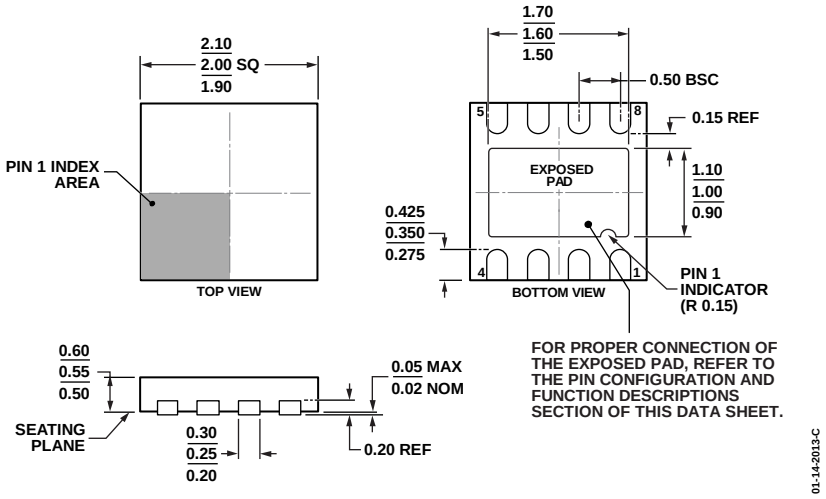
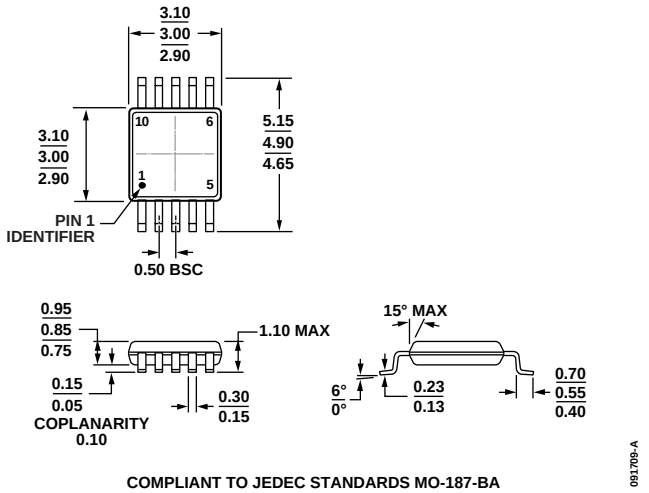


Figure 56. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultrathin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 57. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	Pinout	Temperature Range	Performance	Package Description	Package Option	Branding
AD5683RACPZ-RL7	16	$\overline{\text{LDAC}}$	−40°C to +105°C	A Grade	8-Lead LFCSP_UD	CP-8-10	94
AD5683RACPZ-1RL7	16	V_{LOGIC}	−40°C to +105°C	A Grade	8-Lead LFCSP_UD	CP-8-10	95
AD5683RACPZ-2RL7	16	$\overline{\text{RESET}}$	−40°C to +105°C	A Grade	8-Lead LFCSP_UD	CP-8-10	96
AD5683RARMZ	16	V_{LOGIC}	−40°C to +105°C	A Grade	10-Lead MSOP	RM-10	DHY
AD5683RARMZ-RL7	16	V_{LOGIC}	−40°C to +105°C	A Grade	10-Lead MSOP	RM-10	DHY
AD5683RBRMZ	16	V_{LOGIC}	−40°C to +105°C	B Grade	10-Lead MSOP	RM-10	DHZ
AD5683RBRMZ-RL7	16	V_{LOGIC}	−40°C to +105°C	B Grade	10-Lead MSOP	RM-10	DHZ
AD5683RBRMZ-3	16	SDO	−40°C to +105°C	B Grade	10-Lead MSOP	RM-10	DJ0
AD5683RBRMZ-3-RL7	16	SDO	−40°C to +105°C	B Grade	10-Lead MSOP	RM-10	DJ0
AD5683RBCPZ-RL7	16	$\overline{\text{LDAC}}$	−40°C to +105°C	B Grade	8-Lead LFCSP_UD	CP-8-10	97
AD5683RBCPZ-1RL7	16	V_{LOGIC}	−40°C to +105°C	B Grade	8-Lead LFCSP_UD	CP-8-10	DX
AD5683BCPZ-RL7	16	$\overline{\text{LDAC}}$	−40°C to +105°C	B Grade	8-Lead LFCSP_UD	CP-8-10	9A
AD5682RBCPZ-RL7	14	$\overline{\text{LDAC}}$	−40°C to +105°C	B Grade	8-Lead LFCSP_UD	CP-8-10	9B
AD5681RBCPZ-RL7	12	$\overline{\text{LDAC}}$	−40°C to +105°C	B Grade	8-Lead LFCSP_UD	CP-8-10	98
AD5681RBCPZ-1RL7	12	V_{LOGIC}	−40°C to +105°C	B Grade	8-Lead LFCSP_UD	CP-8-10	99
AD5681RBRMZ	12	V_{LOGIC}	−40°C to +105°C	B Grade	10-Lead MSOP	RM-10	DHX
AD5681RBRMZ-RL7	12	V_{LOGIC}	−40°C to +105°C	B Grade	10-Lead MSOP	RM-10	DHX
EVAL-AD5683RSDZ					Evaluation Board		

[1] Z = RoHS Compliant Part.

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D11955-0-12/16(D)

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