19-5216; Rev 3; 4/10

EVALUATION KIT AVAILABLE

Smart Card Interface

DS8113

General Description

The DS8113 smart card interface is a low-cost, analog front-end for a smart card reader, designed for all ISO 7816, EMV™, and GSM11-11 applications. The DS8113 supports 5V, 3V, and 1.8V smart cards. The DS8113 provides options for low active- and stop-mode power consumption, with as little as 10nA stop-mode current.

The DS8113 is designed to interface between a system microcontroller and the smart card interface, providing all power supply, ESD protection, and level shifting required for IC card applications.

An EMV Level 1 library (written for the MAXQ2000 microcontroller) and hardware reference design is available. Contact Maxim technical support at **https://support.maxim-ic.com/micro** regarding requirements for other microcontroller platforms. An evaluation kit, DS8113-KIT, is available to aid in prototyping and evaluation.

Applications

Consumer Set-Top Boxes
Access Control
Banking Applications
POS Terminals
Debit/Credit Payment Terminals
PIN Pads
Automated Teller Machines
Telecommunications
Pay/Premium Television

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS8113-RNG+	-40°C to +85°C	28 SO
DS8113-JNG+	-40°C to +85°C	28 TSSOP

Note: *Contact the factory for availability of other variants and package options.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Selector Guide appears at end of data sheet.

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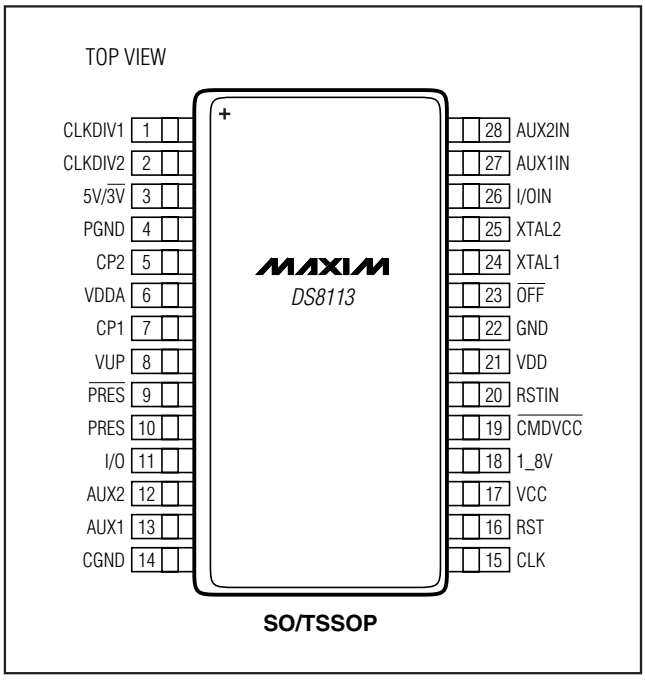
Features

- **Analog Interface and Level Shifting for IC Card Communication**
- **8kV (min) ESD (IEC) Protection on Card Interface**
- **Ultra-Low Stop-Mode Current, Less Than 10nA Typical**
- **Internal IC Card Supply-Voltage Generation:**
  5.0V ±5%, 80mA (max)
  3.0V ±8%, 65mA (max)
  1.8V ±10%, 30mA (max)
- **Automatic Card Activation and Deactivation Controlled by Dedicated Internal Sequencer**
- **I/O Lines from Host Directly Level Shifted for Smart Card Communication**
- **Flexible Card Clock Generation, Supporting External Crystal Frequency Divided by 1, 2, 4, or 8**
- **High-Current, Short-Circuit and High-Temperature Protection**
- **Low Active-Mode Current**

Pin Configuration



SO/TSSOP

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

Smart Card Interface

ABSOLUTE MAXIMUM RATINGS

Voltage Range on VDD Relative to GND.....-0.5V to +6.5V
Voltage Range on VDDA Relative to PGND.....-0.5V to +6.5V
Voltage Range on CP1, CP2, and VUP
Relative to PGND.....-0.5V to +7.5V
Voltage Range on All Other Pins
Relative to GND.....-0.5V to (V_{DD} + 0.5V)

Maximum Junction Temperature .....+125°C
Maximum Power Dissipation (T_A = -25°C to +85°C) 700mW
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Digital Supply Voltage	V_{DD}		2.7		6.0	V
Card Voltage-Generator Supply Voltage	V_{DDA}	$V_{DDA} > V_{DD}$	5.0		6.0	V
Reset Voltage Thresholds	V_{TH2}	Threshold voltage (falling)	2.35	2.45	2.60	V
	V_{HYS2}	Hysteresis	50.0	100	150	mV
CURRENT CONSUMPTION						
Active V_{DD} Current 5V Cards (Including 80mA Draw from 5V Card)	I_{DD_50V}	I_{CC} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V		80.75	85.00	mA
Active V_{DD} Current 5V Cards (Current Consumed by DS8113 Only)	I_{DD_IC}	I_{CC} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)		0.75	5.00	mA
Active V_{DD} Current 3V Cards (Including 65mA Draw from 3V Card)	I_{DD_30V}	I_{CC} = 65mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V		65.75	70.00	mA
Active V_{DD} Current 3V Cards (Current Consumed by DS8113 Only)	I_{DD_IC}	I_{CC} = 65mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)		0.75	5.00	mA
Active V_{DD} Current 1.8V Cards (Including 30mA Draw from 1.8V Card)	I_{DD_18V}	I_{CC} = 30mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V		30.75	35.00	mA
Active V_{DD} Current 1.8V Cards (Current Consumed by DS8113 Only)	I_{DD_IC}	I_{CC} = 30mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)		0.75	5.00	mA
Inactive-Mode Current	I_{DD}	Card inactive, active-high PRES, DS8113 not in stop mode		50.0	200	µA
Stop-Mode Current	I_{DD_STOP}	DS8113 in ultra-low-power stop mode ($\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V set to logic 1) (Note 3)		0.01	2.00	µA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK SOURCE							
Crystal Frequency		f_{XTAL}	External crystal	0		20	MHz
XTAL1 Operating Conditions		f_{XTAL1}		0		20	MHz
		V_{IL_XTAL1}	Low-level input on XTAL1	-0.3		0.3 x V_{DD}	V
		V_{IH_XTAL1}	High-level input on XTAL1	0.7 x V_{DD}		V_{DD} + 0.3	
External Capacitance for Crystal		C_{XTAL1}, C_{XTAL2}				15	pF
Internal Oscillator		f_{INT}			2.7		MHz
SHUTDOWN TEMPERATURE							
Shutdown Temperature		T_{SD}			+150		°C
RST PIN							
Card-Inactive Mode	Output Low Voltage	V_{OL_RST1}	I_{OL_RST} = 1mA	0		0.3	V
	Output Current	I_{OL_RST1}	V_{O_LRST} = 0V	0		-1	mA
Card-Active Mode	Output Low Voltage	V_{OL_RST2}	I_{OL_RST} = 200µA	0		0.3	V
	Output High Voltage	V_{OH_RST2}	I_{OH_RST} = -200µA	V_{CC} - 0.5		V_{CC}	V
	Rise Time	t_{R_RST}	C_L = 30pF			0.1	µs
	Fall Time	t_{F_RST}	C_L = 30pF			0.1	µs
	Shutdown Current Threshold	$I_{RST(SD)}$			-20		mA
	Current Limitation	$I_{RST(LIMIT)}$		-20		+20	mA
	RSTIN to RST Delay	$t_{D(RSTIN-RST)}$				2	µs
CLK PIN							
Card-Inactive Mode	Output Low Voltage	V_{OL_CLK1}	I_{OLCLK} = 1mA	0		0.3	V
	Output Current	I_{OL_CLK1}	V_{OLCLK} = 0V	0		-1	mA
Card-Active Mode	Output Low Voltage	V_{OL_CLK2}	I_{OLCLK} = 200µA	0		0.3	V
	Output High Voltage	V_{OH_CLK2}	I_{OHCLK} = -200µA	V_{CC} - 0.5		V_{CC}	V
	Rise Time	t_{R_CLK}	C_L = 30pF (Note 4)			8	ns
	Fall Time	t_{F_CLK}	C_L = 30pF (Note 4)			8	ns
	Current Limitation	$I_{CLK(LIMIT)}$		-70		+70	mA
	Clock Frequency	f_{CLK}	Operational	0		10	MHz
	Duty Factor	δ	C_L = 30pF	45		55	%
	Slew Rate	SR	C_L = 30pF	0.2			V/ns
VCC PIN							
Card-Inactive Mode	Output Low Voltage	V_{CC1}	I_{CC} = 1mA	0		0.3	V
	Output Current	I_{CC1}	V_{CC} = 0V	0		-1	mA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Card-Active Mode	Output Low Voltage	V_{CC2}	65mA < $I_{CC(5V)}$ < 80mA	4.55	5.00	5.25	V
			$I_{CC(5V)}$ < 65mA	4.75	5.00	5.25	
			$I_{CC(3V)}$ < 65mA	2.78	3.00	3.22	
			$I_{CC(1.8V)}$ < 30mA	1.65	1.80	1.95	
			5V card; current pulses of 40nC with I < 200mA, t < 400ns, f < 20MHz	4.6		5.4	
			3V card; current pulses of 24nC with I < 200mA, t < 400ns, f < 20MHz	2.75		3.25	
			1.8V card; current pulses of 12nC with I < 200mA, t < 400ns, f < 20MHz	1.62		1.98	
	Output Current	I_{CC2}	$V_{CC(5V)}$ = 0 to 5V			-80	mA
			$V_{CC(3V)}$ = 0 to 3V			-65	
			$V_{CC(1.8V)}$ = 0 to 1.8V			-30	
	Shutdown Current Threshold	$I_{CC(SD)}$			120		mA
	Slew Rate	V_{CCSR}	Up/down; C < 300nF (Note 5)	0.05	0.16	0.25	V/µs
DATA LINES (I/O AND I/OIN)							
I/O ⇔ I/OIN Falling Edge Delay		$t_{D(IO-IOIN)}$				200	ns
Pullup Pulse Active Time		t_{PU}				100	ns
Maximum Frequency		f_{IOMAX}				1	MHz
Input Capacitance		C_I				10	pF
I/O, AUX1, AUX2 PINS							
Card-Inactive Mode	Output Low Voltage	V_{OL_IO1}	I_{OL_IO} = 1mA	0		0.3	V
	Output Current	I_{OL_IO1}	V_{OL_IO} = 0V	0		-1	mA
	Internal Pullup Resistor	R_{PU_IO}	To V_{CC}	9	11	19	kΩ
Card-Active Mode	Output Low Voltage	V_{OL_IO2}	I_{OL_IO} = 1mA	0		0.3	V
	Output High Voltage	V_{OH_IO2}	I_{OH_IO} = < -20µA	0.8 x V_{CC}		V_{CC}	V
			I_{OH_IO} = < -40µA (3V/5V)	0.75 x V_{CC}		V_{CC}	
	Output Rise/Fall Time	t_{OT}	C_L = 30pF			0.1	µs
	Input Low Voltage	V_{IL_IO}		-0.3		+0.8	V
	Input High Voltage	V_{IH_IO}		1.5		V_{CC}	
	Input Low Current	I_{IL_IO}	V_{IL_IO} = 0V			600	µA
	Input High Current	I_{IH_IO}	V_{IH_IO} = V_{CC}			20	µA
	Input Rise/Fall Time	t_{IT}				1.2	µs
	Current Limitation	$I_{IO(LIMIT)}$	C_L = 30pF	-15		+15	mA
	Current When Pullup Active	I_{PU}	C_L = 80pF, V_{OH} = 0.9 x V_{DD}	-1			mA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/OIN, AUX1IN, AUX2IN PINS						
Output Low Voltage	V_{OL}	I_{OL} = 1mA	0		0.3	V
Output High Voltage	V_{OH}	No Load	0.9 x V_{DD}		V_{DD} + 0.1	V
		I_{OH} < -40µA	0.75 x V_{DD}		V_{DD} + 0.1	
Output Rise/Fall Time	t_{OT}	C_L = 30pF, 10% to 90%			0.1	µs
Input Low Voltage	V_{IL}		-0.3		0.3 x V_{DD}	V
Input High Voltage	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Low Current	I_{IL_IO}	V_{IL} = 0V			700	µA
Input High Current	I_{IH_IO}	V_{IH} = V_{DD}			10	µA
Input Rise/Fall Time	t_{IT}	V_{IL} to V_{IH}			1.2	µs
Integrated Pullup Resistor	R_{PU}	Pullup to V_{DD}	9	11	13	kΩ
Current When Pullup Active	I_{PU}	C_L = 30pF, V_{OH} = 0.9 x V_{DD}	-1			mA
CONTROL PINS (CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, 5V/$\overline{\text{3V}}$, 1_8V)						
Input Low Voltage	V_{IL}		-0.3		0.3 x V_{DD}	V
Input High Voltage	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Low Current	I_{IL_IO}	0 < V_{IL} < V_{DD}			5	µA
Input High Current	I_{IH_IO}	0 < V_{IH} < V_{DD}			5	µA
INTERRUPT OUTPUT PIN ($\overline{\text{OFF}}$)						
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0		0.3	V
Output High Voltage	V_{OH}	I_{OH} = -15µA	0.75 x V_{DD}			V
Integrated Pullup Resistor	R_{PU}	Pullup to V_{DD}	16	20	24	kΩ
PRES, $\overline{\text{PRES}}$ PINS						
Input Low Voltage	V_{IL_PRES}				0.3 x V_{DD}	V
Input High Voltage	V_{IH_PRES}		0.7 x V_{DD}			V
Input Low Current	I_{IL_PRES}	V_{IL_PRES} = 0V			40	µA
Input High Current	I_{IH_PRES}	V_{IH_PRES} = V_{DD}			40	µA

Smart Card Interface

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING							
Activation Time		t_{ACT}		50		220	µs
Deactivation Time		t_{DEACT}		50	80	100	µs
CLK to Card Start Time	Window Start	t_3		50		130	µs
	Window End	t_5		140		220	
PRES/$\overline{PRES}$ Debounce Time		$t_{DEBOUNCE}$		5	8	11	ms

Note 1: Operation guaranteed at -40°C and +85°C but not tested.

Note 2: IDD_IC measures the amount of current used by the DS8113 to provide the smart card current minus the load.

Note 3: Stop mode is enabled by setting $\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V to a logic-high.

Note 4: Parameters are guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the maximum rise and fall time is 10ns.

Note 5: Parameter is guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the minimum slew rate is 0.05V/µs and the maximum slew rate is 0.5V/µs.

Pin Description

PIN	NAME	FUNCTION
1, 2	CLKDIV1, CLKDIV2	Clock Divider. Determines the divided-down input clock frequency (presented at XTAL1 or from a crystal at XTAL1 and XTAL2) on the CLK output pin. Dividers of 1, 2, 4, and 8 are available.
3	5V/$\overline{3V}$	5V/3V Selection Pin. Allows selection of 5V or 3V for communication with an IC card. Logic-high selects 5V operation; logic-low selects 3V operation. The 1_8V pin overrides the setting on this pin if active. See Table 3 for a complete description of choosing card voltages.
4	PGND	Analog Ground
5, 7	CP2, CP1	Step-Up Converter Contact. Unused for the DS8113.
6	VDDA	Charge Pump Supply. Must be equal to or higher than V_{DD}. For the DS8113 this must be at least 5.0V.
8	VUP	Charge Pump Output. Unused for the DS8113.
9	$\overline{PRES}$	Card Presence Indicator. Active-low card presence inputs. When the presence indicator becomes active, a debounce timeout begins. After 8ms (typ) the $\overline{OFF}$ signal becomes active.
10	PRES	Card Presence Indicator. Active-high card presence inputs. When the presence indicator becomes active, a debounce timeout begins. After 8ms (typ) the $\overline{OFF}$ signal becomes active.
11	I/O	Smart Card Data-Line Output. Card data communication line, contact C7.
12, 13	AUX2, AUX1	Smart Card Auxiliary Line (C4, C8) Output. Data line connected to card reader contacts C4 (AUX1) and C8 (AUX2).
14	CGND	Smart Card Ground
15	CLK	Smart Card Clock. Card clock, contact C3.
16	RST	Smart Card Reset. Card reset output from contact C2.
17	VCC	Smart Card Supply Voltage. Decouple to CGND (card ground) with 2 x 100nF or 100 + 220nF capacitors (ESR < 100mΩ).
18	1_8V	1.8V Operation Selection. Active-high selection for 1.8V smart card communication. An active-high signal on this pin overrides any setting on the 5V/$\overline{3V}$ pin.
19	$\overline{CMDVCC}$	Activation Sequence Initiate. Active-low input from host.
20	RSTIN	Card Reset Input. Reset input from the host.
21	VDD	Supply Voltage
22	GND	Digital Ground
23	$\overline{OFF}$	Status Output. Active-low interrupt output to the host. Use a 20kΩ integrated pullup resistor to VDD.
24, 25	XTAL1, XTAL2	Crystal/Clock Input. Connect an input from an external clock to XTAL1 or connect a crystal across XTAL1 and XTAL2. For the low idle-mode current variant, an external clock must be driven on XTAL1.
26	I/OIN	I/O Input. Host-to-interface chip data I/O line.
27, 28	AUX1IN, AUX2IN	C4/C8 Input. Host-to-interface I/O line for auxiliary connections to C4 and C8.

Smart Card Interface

Detailed Description

The DS8113 is an analog front-end for communicating with 1.8V, 3V, and 5V smart cards. It is a dual input-voltage device, requiring one supply to match that of a host microcontroller and a separate +5V supply for generating correct smart card supply voltages. The DS8113 translates all communication lines to the correct voltage level and provides power for smart card operation. It is a low-power device, consuming very little current in active-mode operation (during a smart card communication session), and is suitable for use in battery-powered devices such as laptops and PDAs, consuming only 10nA in stop mode. See Figure 1 for a functional diagram.

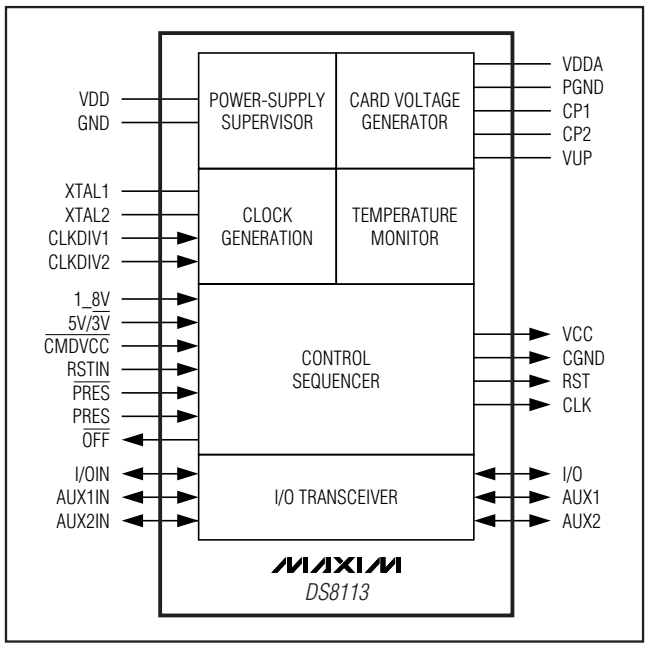


Figure 1. Functional Diagram

Power Supply

The DS8113 is a dual-supply device. The supply pins for the device are VDD, GND, VDDA, and PGND. V_{DD} should be in the range of 2.7V to 6.0V, and is the supply for signals that interface with the host controller. It should, therefore, be the same supply as used by the host controller. All smart card contacts remain inactive during power-on or power-off. The internal circuits are kept in the reset state until V_{DD} reaches $V_{TH2} + V_{HYS2}$ and for the duration of the internal power-on reset pulse, t_W. A deactivation sequence is executed when V_{DD} falls below V_{TH2}.

An internal regulator generates the 1.8V, 3V, or 5V card supply voltage (V_{CC}). The regulator should be supplied separately by VDDA and PGND. VDDA should be connected to a minimum 5.0V supply in order to provide the correct supply voltage for 5V smart cards.

Voltage Supervisor

The voltage supervisor monitors the V_{DD} supply. A 220µs reset pulse (t_W) is used internally to keep the device inactive during power-on or power-off of the V_{DD} supply. See Figure 2.

The DS8113 card interface remains inactive no matter the levels on the command lines until duration t_W after V_{DD} has reached a level higher than $V_{TH2} + V_{HYS2}$. When V_{DD} falls below V_{TH2}, the DS8113 executes a card deactivation sequence if its card interface is active.

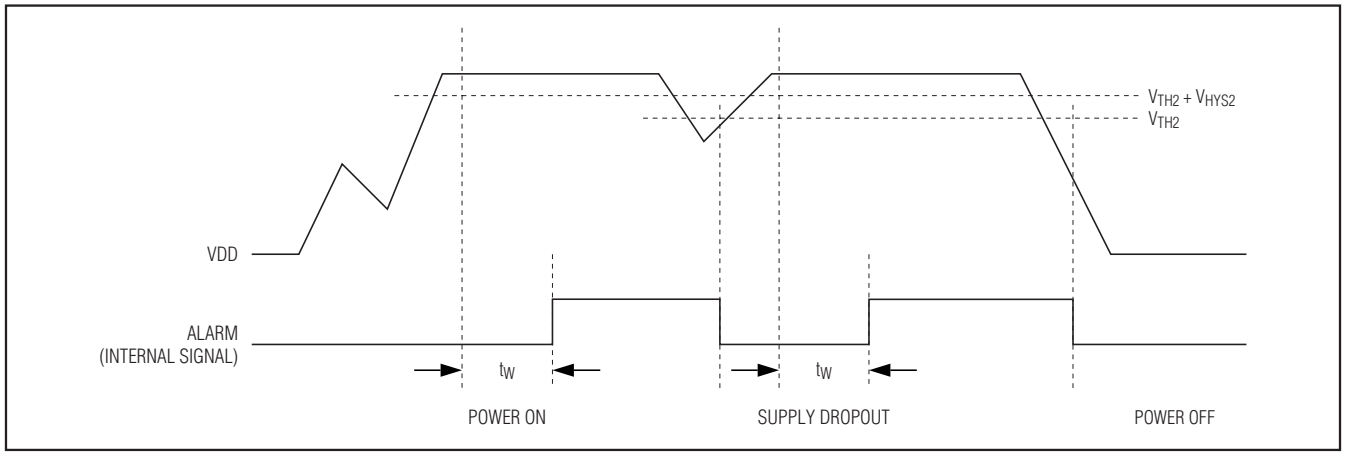


Figure 2. Voltage Supervisor Behavior

Clock Circuitry

The card clock signal (CLK) is derived from a clock signal input to XTAL1 or from a crystal operating at up to 20MHz connected between XTAL1 and XTAL2. The output clock frequency of CLK is selectable through inputs CLKDIV1 and CLKDIV2. The CLK signal frequency can be f_{XTAL}, $f_{XTAL}/2$, $f_{XTAL}/4$, or $f_{XTAL}/8$. See Table 1 for the frequency generated on the CLK signal given the inputs to CLKDIV1 and CLKDIV2.

Note that CLKDIV1 and CLKDIV2 must not be changed simultaneously; a delay of 10ns minimum between changes is needed. The minimum duration of any state of CLK is eight periods of XTAL1.

The frequency change is synchronous: during a transition of the clock divider, no pulse is shorter than 45% of the smallest period, and the first and last clock pulses about the instant of change have the correct width. When changing the frequency dynamically, the change is effective for only eight periods of XTAL1 after the command.

The f_{XTAL} duty factor depends on the input signal on XTAL1. To reach a 45% to 55% duty factor on CLK, XTAL1 should have a 48% to 52% duty factor with transition times less than 5% of the period.

With a crystal, the duty factor on CLK can be 45% to 55% depending on the circuit layout and on the crystal characteristics and frequency. In other cases, the duty factor on CLK is guaranteed between 45% and 55% of the clock period.

If the crystal oscillator is used or if the clock pulse on XTAL1 is permanent, the clock pulse is applied to the card as shown in the activation sequences in Figures 3 and 4. If the signal applied to XTAL1 is controlled by the host microcontroller, the clock pulse is applied to the card when it is sent by the system microcontroller (after completion of the activation sequence).

Table 1. Clock Frequency Selection

CLKDIV1	CLKDIV2	f_{CLK}
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

I/O Transceivers

The three data lines I/O, AUX1, and AUX2 are identical. This section describes the characteristics of I/O and I/OIN but also applies to AUX1, AUX1IN, AUX2, and AUX2IN.

I/O and I/OIN are pulled high with an 11kΩ resistor (I/O to VCC and I/OIN to VDD) in the inactive state. The first side of the transceiver to receive a falling edge becomes the master. When a falling edge is detected (and the master is decided), the detection of falling edges on the line of the other side is disabled; that side then becomes a slave. After a time delay $t_{D(EDGE)}$, an n transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side asserts a logic 1, a p transistor on the slave side is activated during the time delay t_{PU} and then both sides return to their inactive (pulled up) states. This active pullup provides fast low-to-high transitions. After the duration of t_{PU}, the output voltage depends only on the internal pullup resistor and the load current. Current to and from the card I/O lines is limited internally to 15mA. The maximum frequency on these lines is 1MHz.

Inactive Mode

The DS8113 powers up with the card interface in the inactive mode. Minimal circuitry is active while waiting for the host to initiate a smart card session.

- All card contacts are inactive (approximately 200Ω to GND).
- Pins I/OIN, AUX1IN, and AUX2IN are in the high-impedance state (11kΩ pullup resistor to VDD).
- Voltage generators are stopped.
- XTAL oscillator is running (if included in the device).
- Voltage supervisor is active.
- The internal oscillator is running at its low frequency.

Activation Sequence

After power-on and the reset delay, the host microcontroller can monitor card presence with signals $\overline{OFF}$ and $\overline{CMDVCC}$, as shown in Table 2.

Table 2. Card Presence Indication

$\overline{OFF}$	$\overline{CMDVCC}$	STATUS
High	High	Card present.
Low	High	Card **not** present.

Smart Card Interface

If the card is in the reader (if PRES is active), the host microcontroller can begin an activation sequence (start a card session) by pulling $\overline{CMDVCC}$ low. The following events form an activation sequence (Figure 3):

1) $\overline{CMDVCC}$ is pulled low.
2) The internal oscillator changes to high frequency (t_0).
3) The voltage generator is started (between t_0 and t_1).
4) V_{CC} rises from 0 to 5V, 3V, or 1.8V with a controlled slope ($t_2 = t_1 + 1.5 \times T$). T is 64 times the internal oscillator period (approximately 25µs).
5) I/O, AUX1, and AUX2 are enabled ($t_3 = t_1 + 4T$) (they were previously pulled low).
6) The CLK signal is applied to the C3 contact (t_4).
7) RST is enabled ($t_5 = t_1 + 7T$).

To apply the clock to the card interface:

1) Set RSTIN high.
2) Set $\overline{CMDVCC}$ low.
3) Set RSTIN low between t_3 and t_5; CLK will now start.
4) RST stays low until t_5, then RST becomes the copy of RSTIN.
5) RSTIN has no further effect on CLK after t_5.

If the applied clock is not needed, set $\overline{CMDVCC}$ low with RSTIN low. In this case, CLK starts at t_3 (minimum 200ns after the transition on I/O, see Figure 4); after t_5, RSTIN can be set high to obtain an answer to request (ATR) from an inserted smart card. Do not perform activation with RSTIN held permanently high.

Active Mode

When the activation sequence is completed, the DS8113 card interface is in active mode. The host microcontroller and the smart card exchange data on the I/O lines.

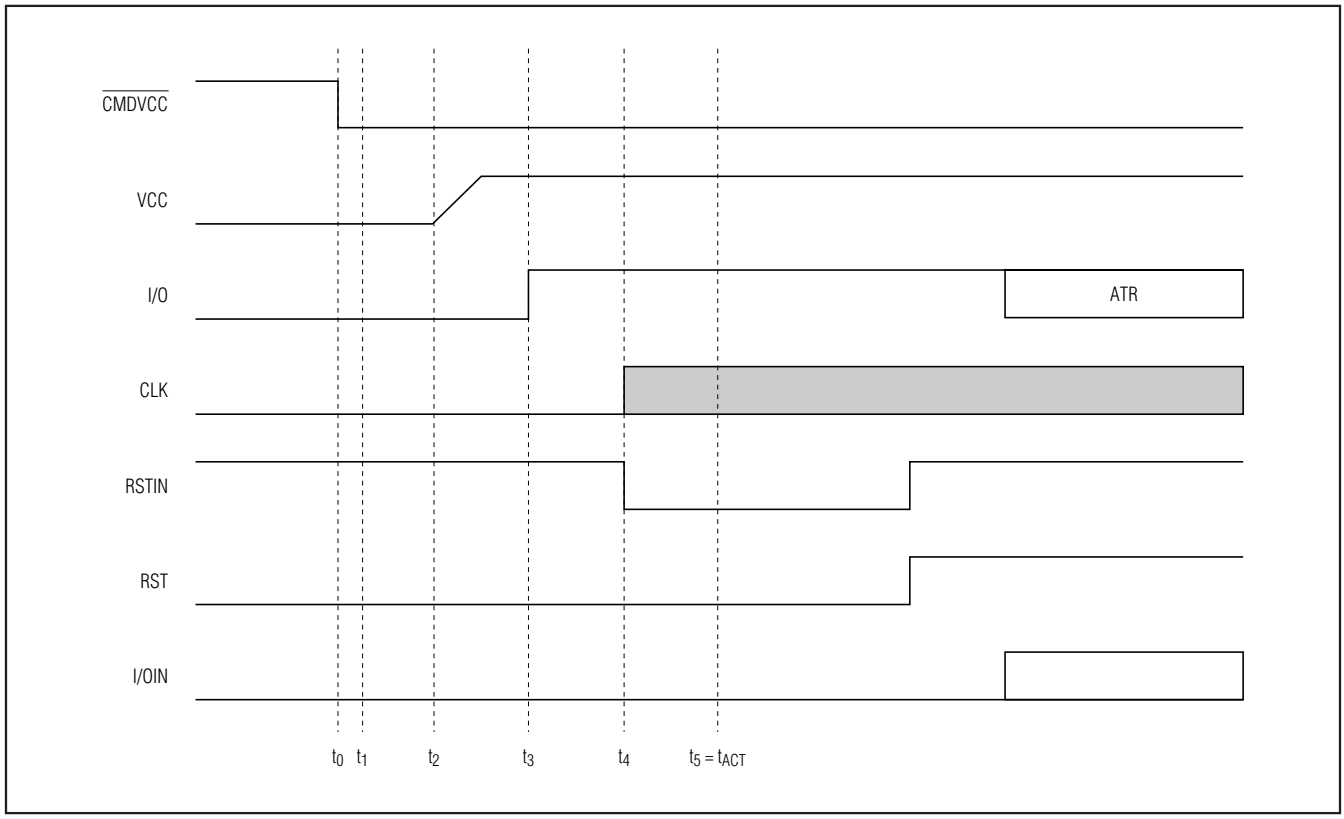


Figure 3. Activation Sequence Using RSTIN and $\overline{CMDVCC}$

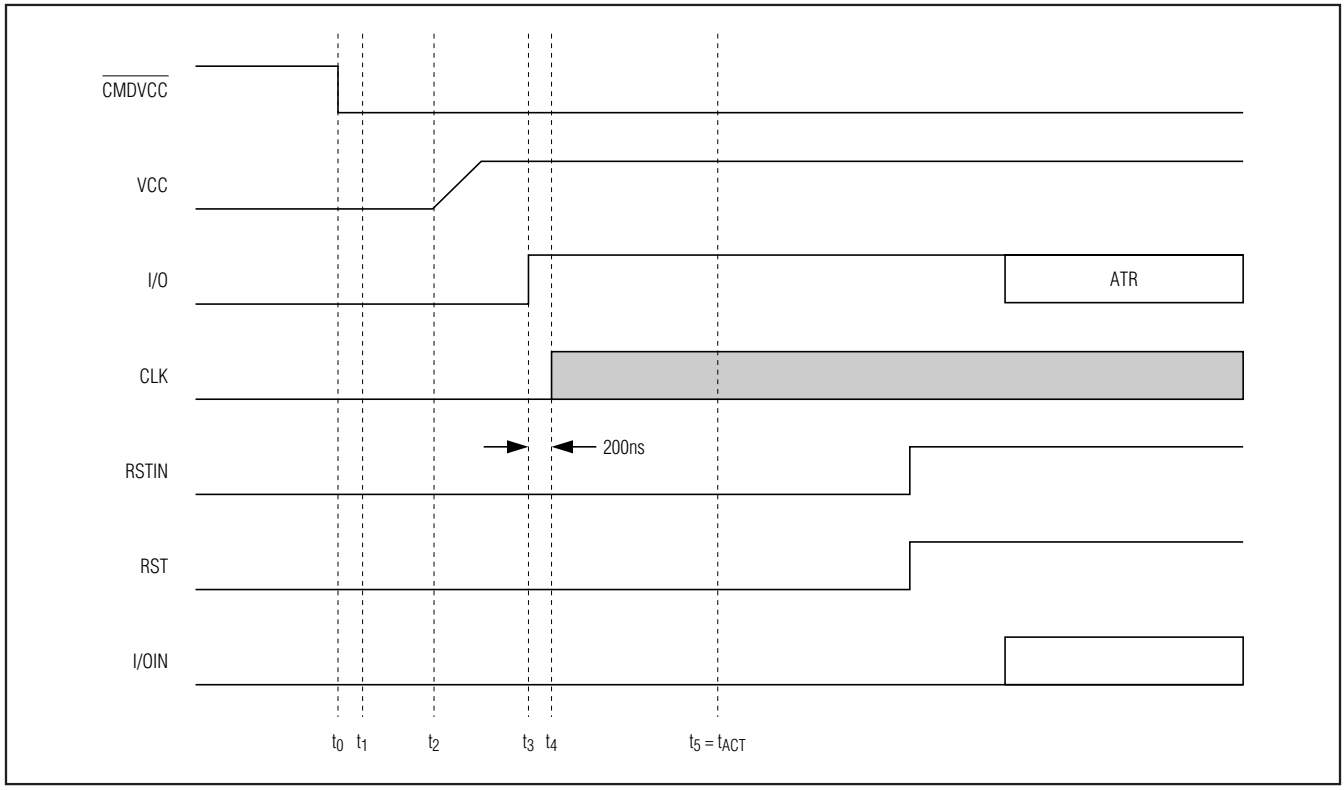


Figure 4. Activation Sequence at t_3

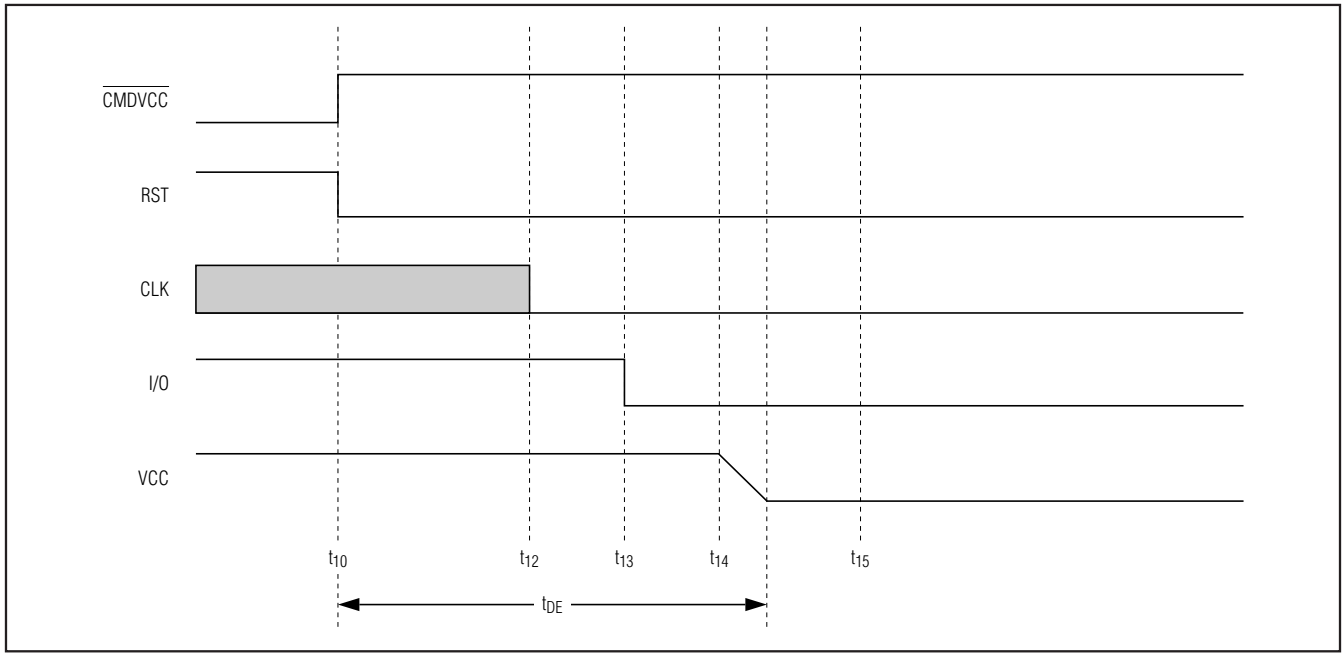


Figure 5. Deactivation Sequence

Smart Card Interface

Deactivation Sequence

When a session is completed, the host microcontroller sets the $\overline{CMDVCC}$ line high to execute an automatic deactivation sequence and returns the card interface to the inactive mode (Figure 5).

1) RST goes low (t_{10}).
2) CLK is held low ($t_{12} = t_{10} + 0.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25µs).
3) I/O, AUX1, and AUX2 are pulled low ($t_{13} = t_{10} + T$).
4) V_{CC} starts to fall ($t_{14} = t_{10} + 1.5 \times T$).
5) When V_{CC} reaches its inactive state, the deactivation sequence is complete (at t_{DE}).
6) All card contacts become low impedance to GND; I/OIN, AUX1IN, and AUX2IN remain at V_{DD} (pulled up through an 11kΩ resistor).
7) The internal oscillator returns to its lower frequency.

Vcc Generator

The V_{CC} generator has a capacity to supply up to 80mA continuously at 5V, 65mA at 3V, and 30mA at 1.8V. An internal overload detector triggers at approximately 120mA. Current samples to the detector are filtered. This allows spurious current pulses (with a duration of a few µs) up to 200mA to be drawn without causing deactivation. The average current must stay below the specified maximum current value. To maintain V_{CC} voltage accuracy, a 100nF capacitor (with an ESR < 100mΩ) should be connected to CGND and placed near the DS8113's VCC pin, and a 100nF or 220nF capacitor (220nF is the best choice) with the same ESR should be connected to CGND and placed near the smart card reader's C1 contact.

Fault Detection

The following fault conditions are monitored:

- Short-circuit or high current on VCC
- Removal of a card during a transaction
- V_{DD} dropping
- Card voltage generator operating out of the specified values (V_{DDA} too low or current consumption too high)
- Overheating

There are two different cases (Figure 6):

- **$\overline{CMDVCC}$ High Outside a Card Session.** Output $\overline{OFF}$ is low if a card is not in the card reader and high if a card is in the reader. The V_{DD} supply is monitored—a decrease in input voltage generates an internal power-on reset pulse but does not affect the $\overline{OFF}$ signal. Short-circuit and temperature detection is disabled because the card is not powered up.
- **$\overline{CMDVCC}$ Low Within a Card Session.** Output $\overline{OFF}$ goes low when a fault condition is detected, and an emergency deactivation is performed automatically (Figure 7). When the system controller resets $\overline{CMDVCC}$ to high, it may sense the $\overline{OFF}$ level again after completing the deactivation sequence. This distinguishes between a card extraction and a hardware problem ($\overline{OFF}$ goes high again if a card is present). Depending on the connector's card-present switch (normally closed or normally open) and the mechanical characteristics of the switch, bouncing can occur on the PRES signals at card insertion or withdrawal.

The DS8113 has a debounce feature with an 8ms typical duration (Figure 6). When a card is inserted, output $\overline{OFF}$ goes high after the debounce time delay. When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES and output $\overline{OFF}$ goes low.

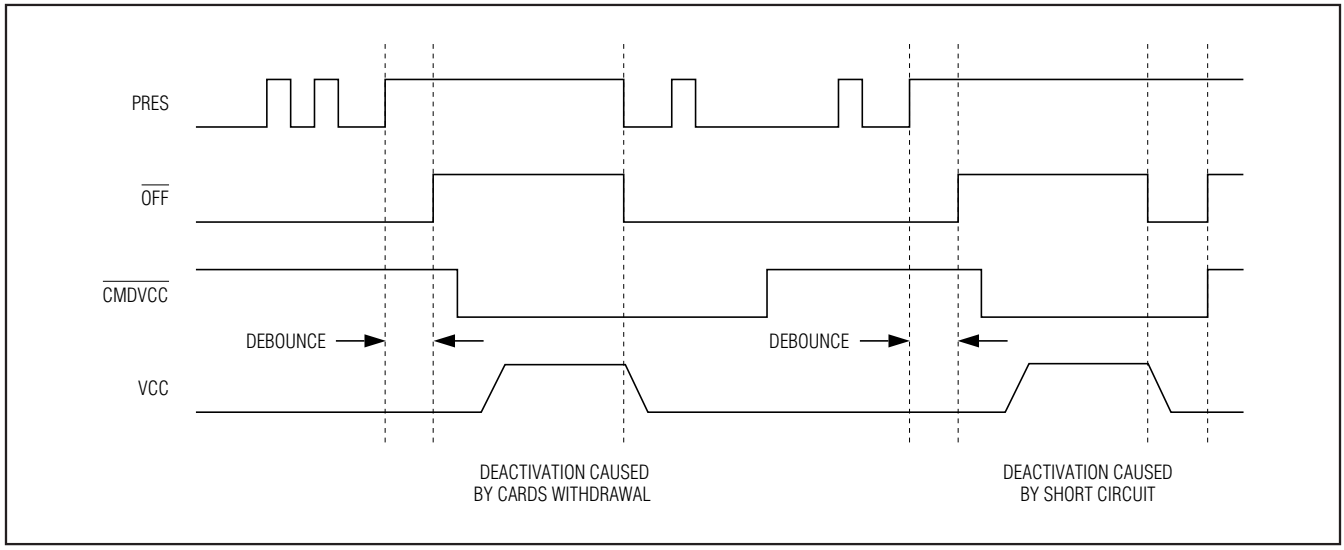


Figure 6. Behavior of PRES, OFF, CMDVCC, and VCC

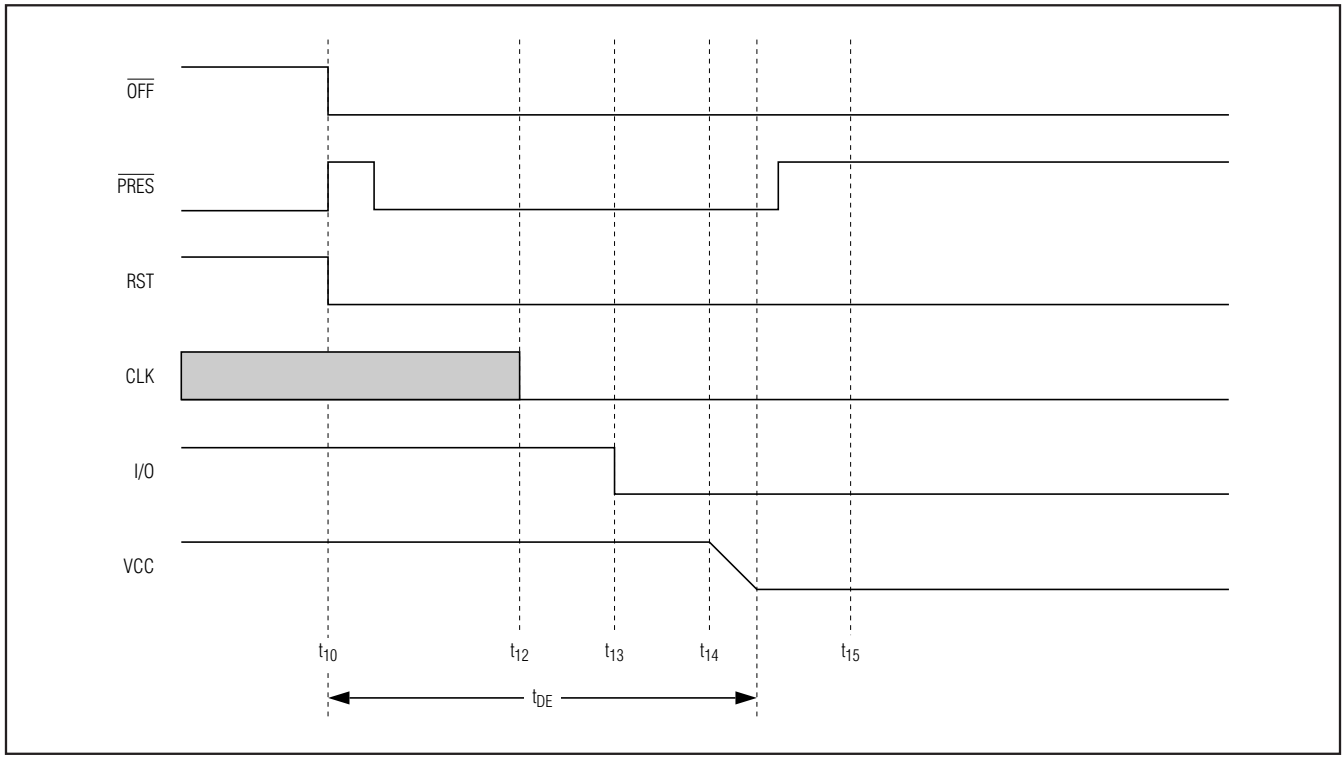


Figure 7. Emergency Deactivation Sequence (Card Extraction)

Smart Card Interface

Stop Mode (Low-Power Mode)

A low-power state, stop mode, can be entered by forcing the $\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V input pins to a logic-high state. Stop mode can only be entered when the smart card interface is inactive. In stop mode all internal analog circuits are disabled. The $\overline{OFF}$ pin follows the status of the PRES pin. To exit stop mode, change the state of one or more of the three control pins to a logic-low. An internal 220µs (typ) power-up delay and the 8ms PRES debounce delay are in effect and $\overline{OFF}$ is asserted to allow the internal circuitry to stabilize. This prevents smart card access from occurring after leaving the stop mode. Figure 8 shows the control sequence for entering and exiting stop mode. Note that an in-progress deactivation sequence always finishes before the DS8113 enters low-power stop mode.

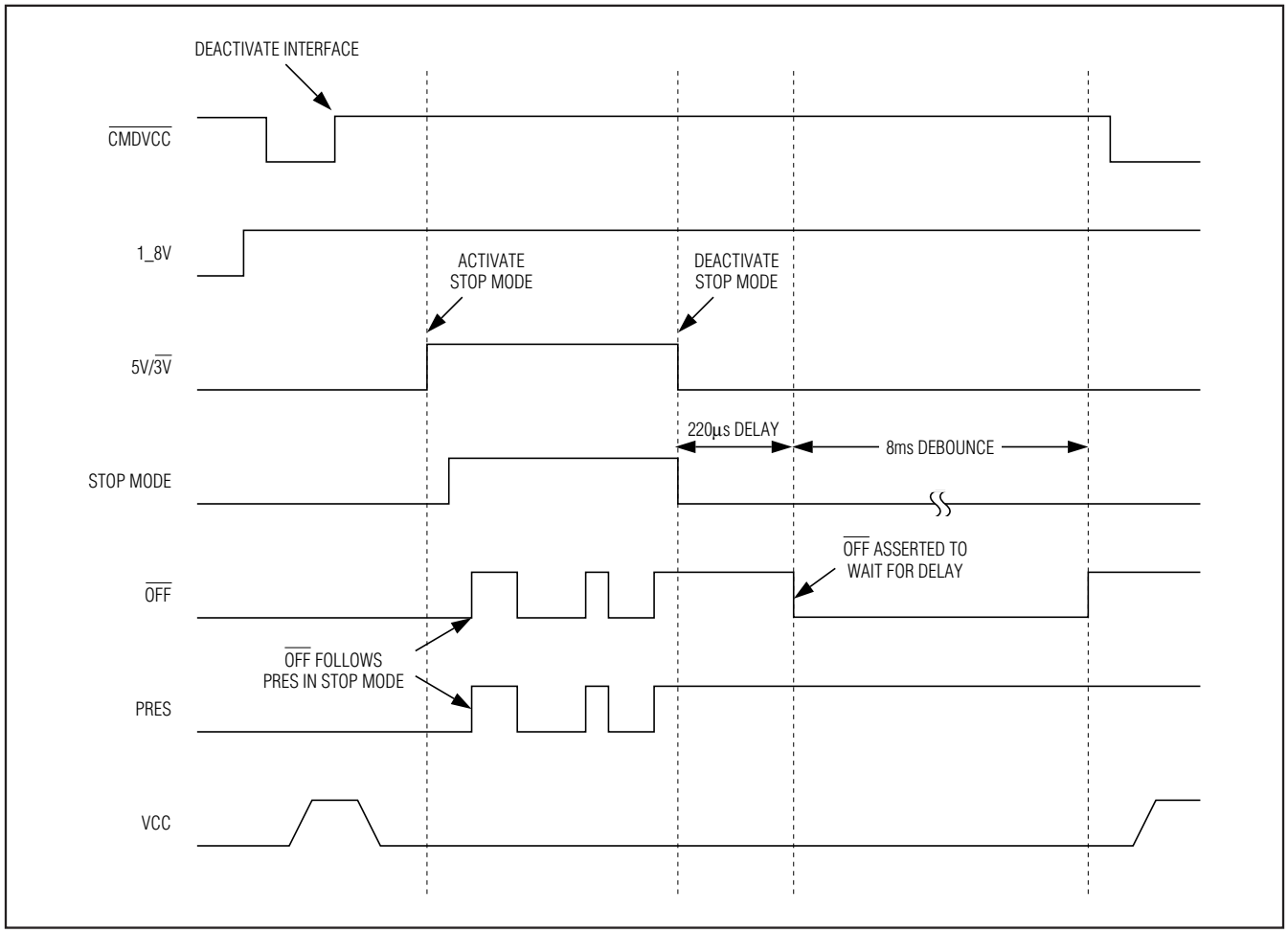


Figure 8. Stop-Mode Sequence

Smart Card Power Select

The DS8113 supports three smart card V_{CC} voltages: 1.8V, 3V, and 5V. The power select is controlled by the 1_8V and 5V/$\overline{3V}$ signals as shown in Table 3. The 1_8V signal has priority over 5V/$\overline{3V}$. When 1_8V is asserted high, 1.8V is applied to VCC when the smart card is active. When 1_8V is deasserted, 5V/$\overline{3V}$ dictates V_{CC} power range. V_{CC} is 5V if 5V/$\overline{3V}$ is asserted to a logic-high state, and V_{CC} is 3V if 5V/$\overline{3V}$ is pulled to a logic-low state. Care must be exercised when switching from one V_{CC} power selection to the other. If both 1_8V and 5V/$\overline{3V}$ are high with $\overline{CMDVCC}$ high at the same time, the DS8113 enters stop mode. To avoid accidental entry into stop mode, the state of 1_8V and 5V/$\overline{3V}$ must not be changed simultaneously. A minimum delay of 100ns should be observed between changing the states of 1_8V and 5V/$\overline{3V}$. See Figure 9 for the recommended sequence of changing the V_{CC} range.

Table 3. V_{CC} Select and Operation Mode

1_8V	5V/$\overline{3V}$	$\overline{CMDVCC}$	V_{CC} SELECT (V)	CARD INTERFACE STATUS
0	0	0	3	Activated
0	0	1	3	Inactivated
0	1	0	5	Activated
0	1	1	5	Inactivated
1	0	0	1.8	Activated
1	0	1	1.8	Inactivated
1	1	0	1.8	Reserved (Activated)
1	1	1	1.8	Not Applicable—Stop Mode

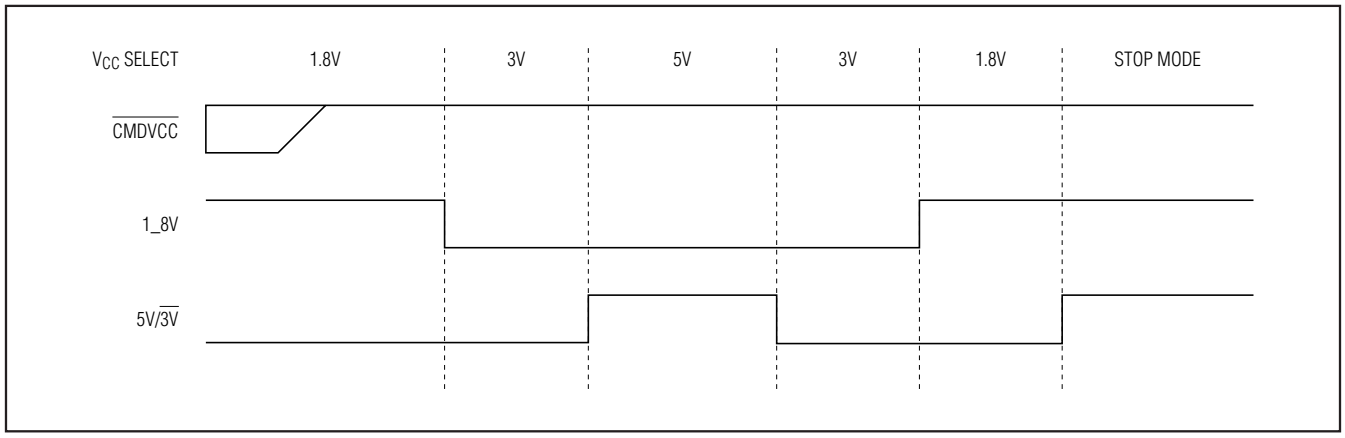


Figure 9. Smart Card Power Select

Smart Card Interface

Applications Information

Performance can be affected by the layout of the application. For example, an additional cross-capacitance of 1pF between card reader contacts C2 (RST) and C3 (CLK) or C2 (RST) and C7 (I/O) can cause contact C2 to be polluted with high-frequency noise from C3 (or C7). In this case, include a 100pF capacitor between contacts C2 and CGND.

Application recommendations include the following:

- Ensure there is ample ground area around the DS8113 and the connector; place the DS8113 very near to the connector; decouple the VDD and VDDA lines separately. These lines are best positioned under the connector, connected in a star on the main trace.
- The DS8113 and the host microcontroller must use the same VDD supply. Pins CLKDIV1, CLKDIV2, RSTIN, PRES, AUX1IN, I/OIN, AUX2IN, 5V/$\overline{3V}$, 1_8V, $\overline{CMDVCC}$, and $\overline{OFF}$ are referenced to VDD; if pin XTAL1 is to be driven by an external clock, also reference this pin to VDD.
- Trace C3 (CLK) should be placed as far as possible from the other traces.
- The trace connecting CGND to C5 (GND) should be straight (the two capacitors on C1 (VCC) should be connected to this ground trace).
- Avoid ground loops among CGND, PGND, and GND.

With all these layout precautions, noise should be kept to an acceptable level and jitter on C3 (CLK) should be less than 100ps. Reference layouts, designs, and an evaluation kit are available on request.

Selector Guide

PART	LOW STOP-MODE POWER	LOW ACTIVE-MODE POWER	PIN-PACKAGE
DS8113-RNG+	Yes	Yes	28 SO
DS8113-JNG+	Yes	Yes	28 TSSOP

Note: *Contact the factory for availability of other variants and package options.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 SO (300 mils)	W28+6	**21-0042**
28 TSSOP	U28+2	**21-0066**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/08	Initial release	—
1	2/08	In the *Recommended DC Operating Conditions* table, changed I/OIN, AUX1IN/AUX2IN specs to reference V_{DD} rather than V_{CC} and corrected I_{OH} to µA.	5
		In the *Pin Description*, removed references to active low from the PRES description.	7
2	5/08	In the *Recommended DC Operating Conditions* table, clarified specifications of V_{TH2}, f_{INT}, V_{CCSR}, and I_{IL_IO}.	2–5
3	4/10	Added the TSSOP package (see the *Ordering Information, Pin Configuration, Selector Guide,* and *Package Information* sections); added the lead temperature and updated the soldering temperature in the *Absolute Maximum Ratings*.	1, 2, 16

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