Serial EEPROM Series

# High Reliability Series EEPROMs I²C BUS

## BR24L□□-W Series,BR24S□□□-W Series

No.09001EDT04

ROHM's series of serial EEPROMs represent the highest level of reliability on the market. A double cell structure provides a failsafe method of data reliability, while a double reset function prevents data miswriting. In addition, gold pads and gold wires are used for internal connections, pushing the boundaries of reliability to the limit.
BR24L□□-W Series assort 1Kbit～64Kbit. BR24S□□□-W Series are possible to operate at high speed in low voltage and assort 8Kbit～256Kbit.

Contents

Serial EEPROM Series

# High Reliability Series EEPROMs I²C BUS

## BR24L□□-W Series

### ●Description

BR24L□□-W series is a serial EEPROM of I²C BUS interface method.

### ●Features

1) Completely conforming to the world standard I²C BUS. All controls available by 2 ports of serial clock(SCL) and serial data(SDA)
2) Other devices than EEPROM can be connected to the same port, saving microcontroller port
3) 1.8V~5.5V *1 single power source action most suitable for battery use
4) Page write mode useful for initial value write at factory shipment
5) Highly reliable connection by Au pad and Au wire
6) Auto erase and auto end function at data rewrite
7) Low current consumption
   At write operation (5V) : 1.2mA (Typ.) *2
   At read operation (5V) : 0.2mA (Typ.)
   At standby operation (5V) : 0.1μA (Typ.)
8) Write mistake prevention function
   Write (write protect) function added
9) Write mistake prevention function at low voltage
10) SOP8/SOP-J8/SSOP-B8/TSSOP-B8/MSOP8/TSSOP-B8J/VSON008X2030 compact package *3
11) Data rewrite up to 1,000,000 times
12) Data kept for 40 years
13) Noise filter built in SCL / SDA terminal
14) Shipment data all address FFh

*1 BR24L02-W, BR24L16-W, BR24L32-W : 1.7～5.5V
*2 BR24L32-W, BR24L64-W : 1.5mA
*3 Refer to following list

### ●Page write

| Number of Pages | 8Byte | 16Byte | 32Byte |
|---|---|---|---|
| Product number | BR24L01A-W<br>BR24L02-W | BR24L04-W<br>BR24L08-W<br>BR24L16-W | BR24L32-W<br>BR24L64-W |

### ●BR24L series

| Capacity | Bit format | Type | Power source Voltage | SOP8 | SOP-J8 | SSOP-B8 | TSSOP-B8 | MSOP8 | TSSOP-B8J | VSON008 X2030 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1Kbit | 128×8 | BR24L01A-W | 1.8～5.5V | ● | ● | ● | ● | ● | ● | ● |
| 2Kbit | 256×8 | BR24L02-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● |
| 4Kbit | 512×8 | BR24L04-W | 1.8～5.5V | ● | ● | ● | ● | ● | ● | ● |
| 8Kbit | 1K×8 | BR24L08-W | 1.8～5.5V | ● | ● | ● | ● | ● | ● | ● |
| 16Kbit | 2K×8 | BR24L16-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | |
| 32Kbit | 4K×8 | BR24L32-W | 1.7～5.5V | ● | ● | ● | ● | | | |
| 64Kbit | 8K×8 | BR24L64-W | 1.8～5.5V | ● | ● | | | | | |

**●Absolute maximum ratings (Ta=25℃)**

| Parameter | symbol | Limits | Unit |
|---|---|---|---|
| Impressed voltage | Vcc | -0.3～+6.5 | V |
| Permissible dissipation | Pd | 450 (SOP8) *1 | mW |
| | | 450 (SOP-J8) *2 | |
| | | 300 (SSOP-B8) *3 | |
| | | 330 (TSSOP-B8) *4 | |
| | | 310 (MSOP8) *5 | |
| | | 310 (TSSOP-B8J) *6 | |
| | | 300 (VSON008X2030) *7 | |
| Storage temperature range | Tstg | -65～+125 | ℃ |
| Action temperature range | Topr | -40～+85 | ℃ |
| Terminal voltage | - | -0.3～Vcc+1.0 | V |

When using at Ta=25℃ or higher, 4.5mW(*1,*2),
3.0mW(*3,*7) 3.3mW(*4),3.1mW(*5,*6) to be reduced per 1℃

**●Memory cell characteristics (Ta=25℃, Vcc=1.8～5.5V)*1**

| Parameter | Limits | | | Unit |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| Number of data rewrite times *2 | 1,000,000 | - | - | Times |
| Data hold years *2 | 40 | - | - | Years |

○Shipment data all address FFh
*1 BR24L02/16/32-W : 1.7~5.5V
*2 Not 100% TESTED

**●Recommended operating conditions**

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power source voltage | Vcc | 1.8～5.5 *1 | V |
| Input voltage | VIN | 0～Vcc | |

*1 BR24L02/16/32-W : 1.7~5.5V

**●Electrical characteristics (Unless otherwise specified, Ta=-40～+85℃, Vcc=1.8～5.5V) *1**

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| “HIGH” input voltage 1 | VIH1 | 0.7Vcc | - | Vcc +1.0 *2 | V | 2.5≦Vcc≦5.5V |
| “LOW” input voltage 1 | VIL1 | -0.3 *2 | - | 0.3 Vcc | V | 2.5≦Vcc≦5.5V |
| “HIGH” input voltage 2 | VIH2 | 0.8Vcc | - | Vcc +1.0 *2 | V | 1.8≦Vcc＜2.5V |
| “LOW” input voltage 2 | VIL2 | -0.3 *2 | - | 0.2 Vcc | V | 1.8≦Vcc＜2.5V |
| “HIGH” input voltage 3 *3 | VIH3 | 0.8Vcc | - | Vcc +1.0 | V | 1.7≦Vcc＜1.8V |
| “HIGH” input voltage 3 *4 | VIH3 | 0.9Vcc | - | Vcc +1.0 | V | 1.7≦Vcc＜1.8V |
| “LOW” input voltage 3 *2 | VIL3 | -0.3 | - | 0.1 Vcc | V | 1.7≦Vcc＜1.8V |
| “LOW” output voltage 1 | VOL1 | - | - | 0.4 | V | IOL=3.0mA, 2.5V≦Vcc≦5.5V, (SDA) |
| “LOW” output voltage 2 | VOL2 | - | - | 0.2 | V | IOL=0.7mA, 1.7V≦Vcc＜2.5V, (SDA) |
| Input leak current | ILI | -1 | - | 1 | μA | VIN=0V～Vcc |
| Output leak current | ILO | -1 | - | 1 | μA | VOUT=0V～Vcc, (SDA) |
| Current consumption at action | ICC1 | - | - | 2.0 *5 | mA | Vcc=5.5V,fSCL=400kHz, tWR=5ms, Byte write, Page write |
| | | | | 3.0 *6 | | |
| | ICC2 | - | - | 0.5 | mA | Vcc=5.5V,fSCL=400kHz Random read, current read,sequential read |
| Standby current | ISB | - | - | 2.0 | μA | Vcc=5.5V, SDA・SCL=Vcc A0, A1, A2=GND, WP=GND |

◎Radiation resistance design is not made.
*1 BR24L02/16/32-W : 1.7～5.5V, *2 BR24L16/32-W, *3 BR24L02/16-W, *4 BR24L32-W
*5 BR24L01A/02/04/08/16-W, *6 BR24L32/64-W

●**Action timing characteristics (Unless otherwise specified, Ta=-40～+85℃, Vcc=1.8～5.5V)**[*1]

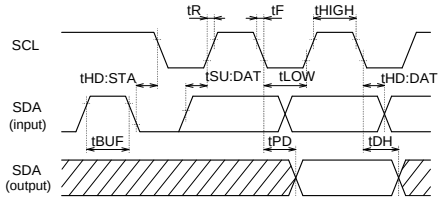
| Parameter | Symbol | FAST-MODE 2.5V≦Vcc≦5.5V | | | STANDARD-MODE 1.8V≦Vcc≦5.5V | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| SCL frequency | fSCL | - | - | 400 | - | - | 100 | kHz |
| Data clock “HIGH“ time | tHIGH | 0.6 | - | - | 4.0 | - | - | μs |
| Data clock “LOW“ time | tLOW | 1.2 | - | - | 4.7 | - | - | μs |
| SDA, SCL rise time [*2] | tR | - | - | 0.3 | - | - | 1.0 | μs |
| SDA, SCL fall time [*2] | tF | - | - | 0.3 | - | - | 0.3 | μs |
| Start condition hold time | tHD:STA | 0.6 | - | - | 4.0 | - | - | μs |
| Start condition setup time | tSU:STA | 0.6 | - | - | 4.7 | - | - | μs |
| Input data hold time | tHD:DAT | 0 | - | - | 0 | - | - | ns |
| Input data setup time | tSU:DAT | 100 | - | - | 250 | - | - | ns |
| Output data delay time | tPD | 0.1 | - | 0.9 | 0.2 | - | 3.5 | μs |
| Output data hold time | tDH | 0.1 | - | - | 0.2 | - | - | μs |
| Stop condition setup time | tSU:STO | 0.6 | - | - | 4.7 | - | - | μs |
| Bus release time before transfer start | tBUF | 1.2 | - | - | 4.7 | - | - | μs |
| Internal write cycle time | tWR | - | - | 5 | - | - | 5 | ms |
| Noise removal valid period (SDA, SCL terminal) | tI | - | - | 0.1 | - | - | 0.1 | μs |
| WP hold time | tHD:WP | 0 | - | - | 0 | - | - | ns |
| WP setup time | tSU:WP | 0.1 | - | - | 0.1 | - | - | μs |
| WP valid time | tHIGH:WP | 1.0 | - | -- | 1.0 | - | - | μs |

*1 BR24L02/16/32-W : 1.7～5.5V
*2 Not 100% tested

●**FAST-MODE and STANDARD-MODE**

FAST-MODE and STANDARD-MODE are of same actions, and mode is changed. They are distinguished by action speeds. 100kHz action is called STANDARD-MODE, and 400kHz action is called FAST-MODE. This action frequency is the maximum action frequency, so 100kHz clock may be used in FAST-MODE. When power source voltage goes down, action at high speed is not carried out, therefore, at Vcc=2.5V～5.5V , 400kHz, namely, action is made in FASTMODE. (Action is made also in STANDARD-MODE) Vcc=1.8V~2.5V is only action in 100kHz STANDARD-MODE.

**●Sync data input / output timing**




○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Fig.1-(a) Sync data input / output timing

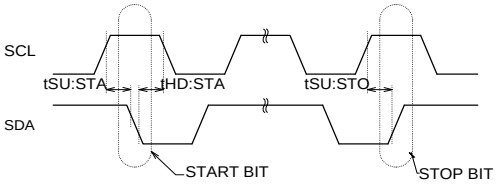



Fig.1-(b) Start-stop bit timing

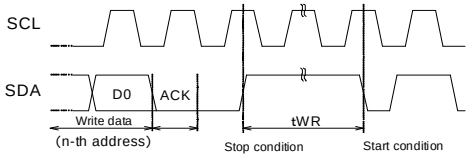



Fig.1-(c) Write cycle timing

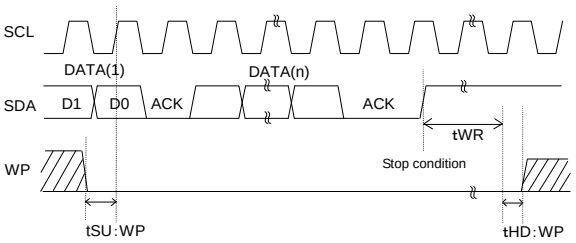
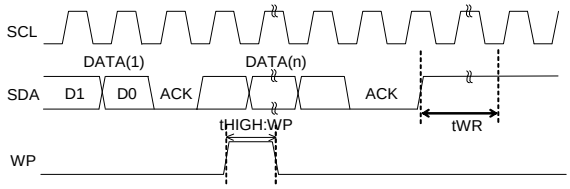



Fig.1-(d) WP timing at write execution




○At write execution, in the area from the D0 taken clock rise of the first DATA(1), to tWR, set WP="LOW".
○By setting WP "HIGH" in the area, write can be cancelled.
When it is set WP="HIGH" during tWR, write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

Fig.1-(e) WP timing at write cance

**●Block diagram**

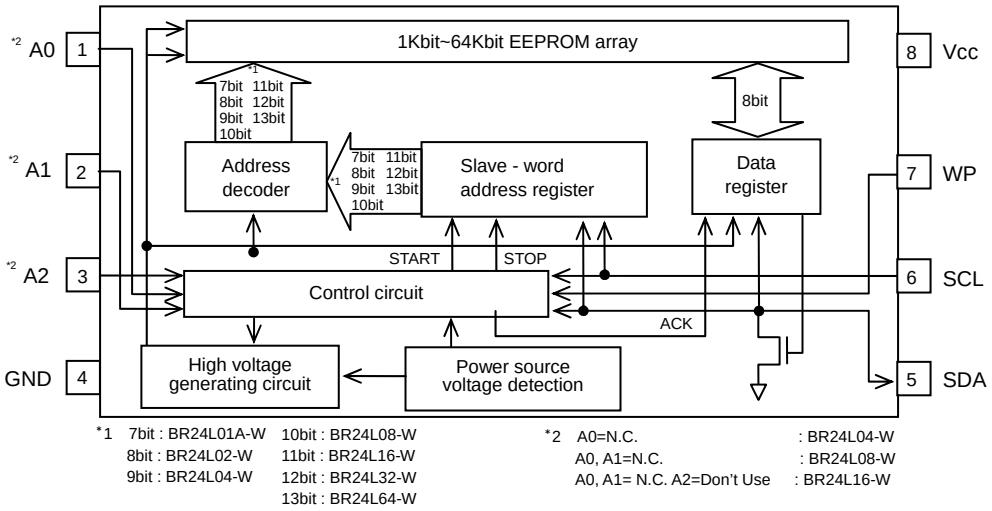
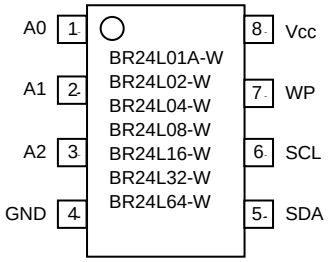



Fig.2 Block diagram

●Pin assignment and description




| Terminal name | Input / output | Function | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | BR24L01A-W | BR24L02-W | BR24L04-W | BR24L08-W | BR24L16-W | BR24L32-W | BR24L64-W |
| A0 | Input | Slave address setting | | Not connected | | | Slave address setting | |
| A1 | Input | Slave address setting | | | Not connected | | Slave address setting | |
| A2 | Input | Slave address setting | | | | Not used | Slave address setting | |
| GND | - | Reference voltage of all input / output, 0V | | | | | | |
| SDA | Input / output | Slave and word address, Serial data input serial data output | | | | | | |
| SCL | Input | Serial clock input | | | | | | |
| WP | Input | Write protect terminal | | | | | | |
| Vcc | - | Connect the power source. | | | | | | |

## ●Characteristic data (The following values are Typ. ones.)

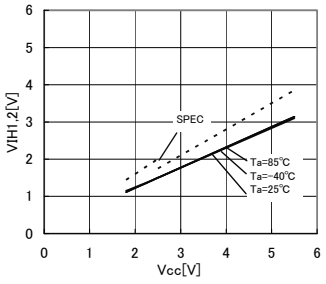


Fig.3 H input voltage VIH1,2

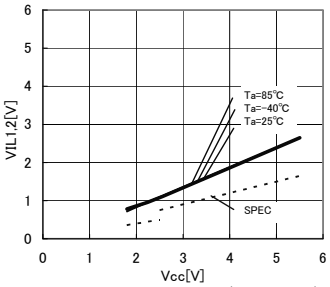


Fig.4 L input voltageVIL1,2 (SCL,SDA,WP)

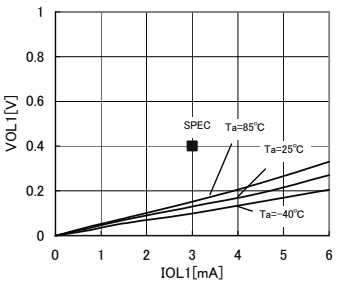


Fig.5 L output voltage VOL1-IOL1 (VCC=2.5V)

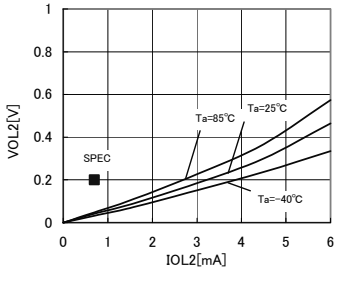


Fig.6 L output voltage VOL2-IOL2 (VCC=1.8V)

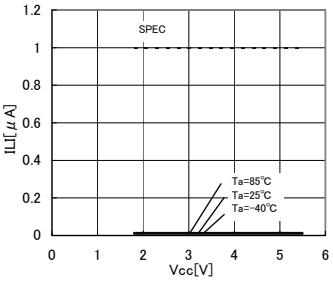


Fig.7 Input leak current ILI (SCL,WP)

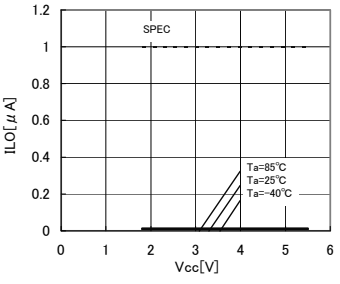


Fig.8 Output leak current ILO(SDA)

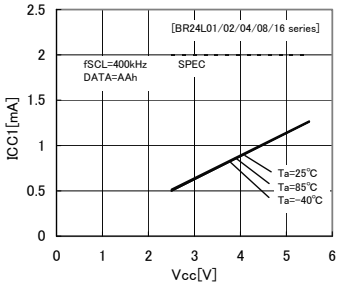


Fig.9 Current consumption at WRITE action ICC1 (fscl=400kHz)

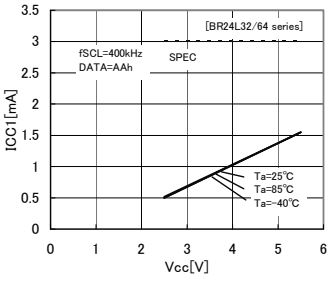


Fig.10 Current consumption at WRITE action ICC1 (fSCL=400kHz)

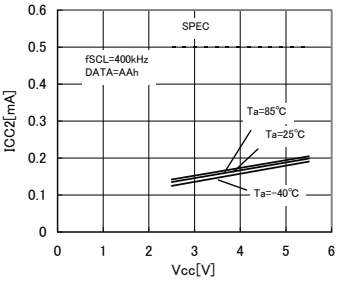


Fig.11 Current consumption at READ action ICC2 (fSCL=400kHz)

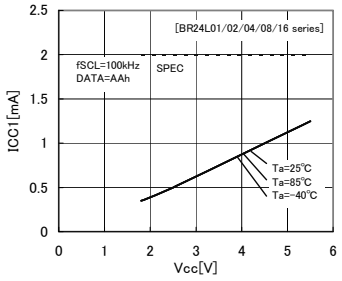


Fig.12 Current consumption at WRITE action ICC1 (fSCL=100kHz)

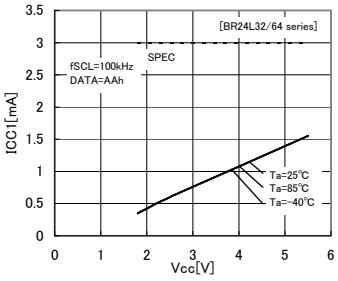


Fig.13 Current consumption at WRITE action ICC1 (fSCL=100kHz)

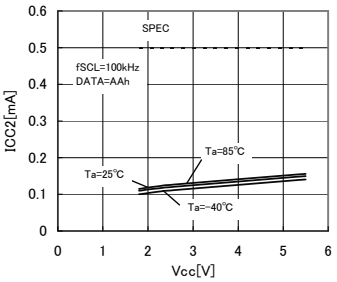


Fig.14 Current consumption at READ action ICC2 (fSCL=100kHz)

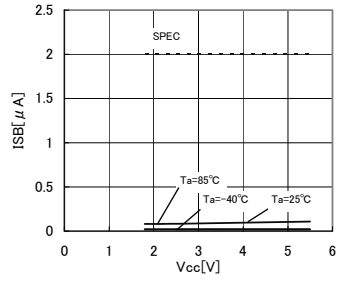


Fig.15 Standby current ISB

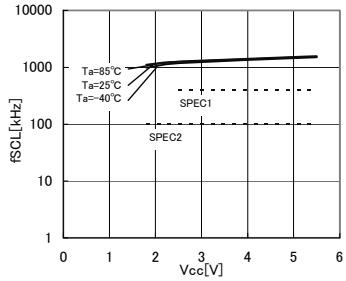


Fig.16 SCL frequency fSCL

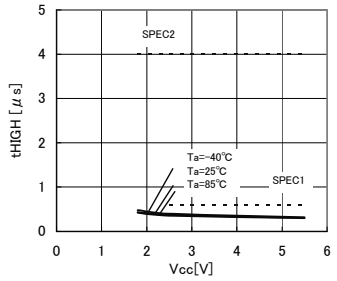


Fig.17 Data clock "H" time tHIGH

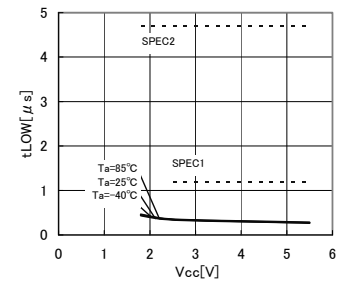


Fig.18 Data clock "L" time tLOW

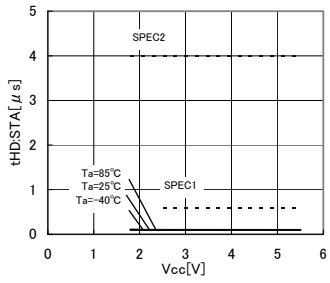


Fig.19 Start condition hold time tHD:STA

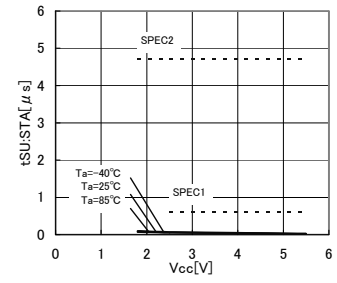


Fig.20 Start condition setup time tSU:STA

**●Characteristic data (The following values are Typ. ones).**

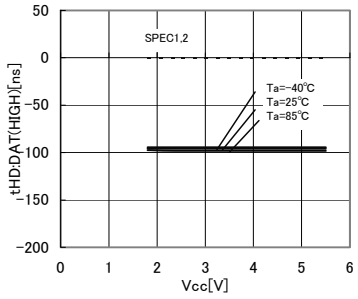



Fig.21 Input data hold time tHD:DAT(HIGH)

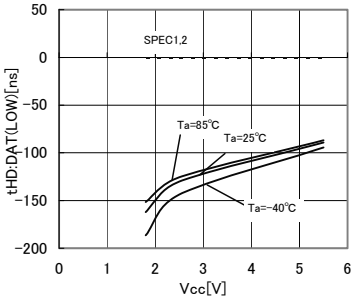



Fig.22 Input data hold time tHD:DAT(LOW)

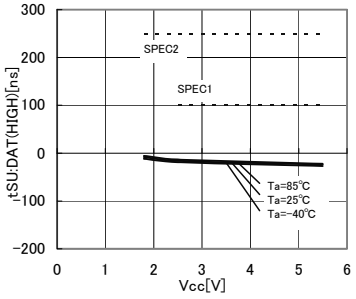



Fig.23 Input data setup time tSU:DAT(HIGH)

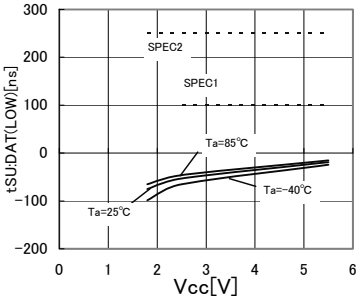



Fig.24 Input data setup time tSU:DAT(LOW)

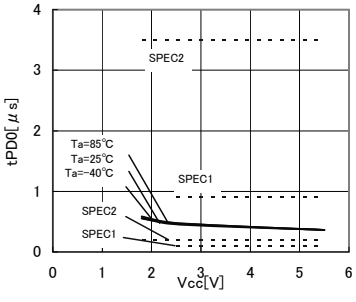



Fig.25 Output data delay time tPD0

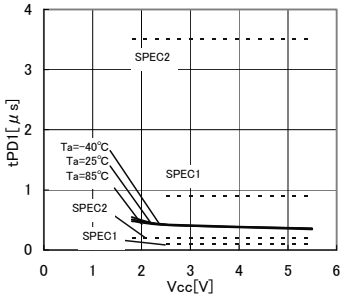



Fig.26 Output data delay time tPD1

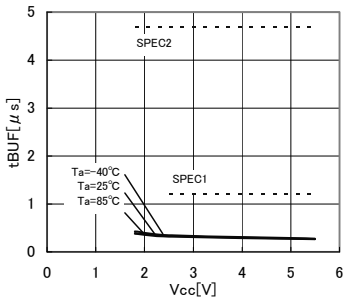



Fig.27 Bus release time before transfer start tBUF

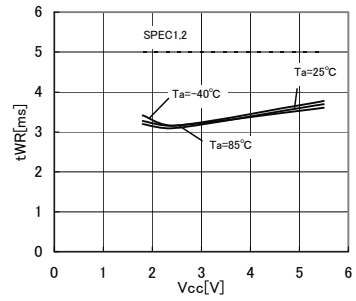



Fig.28 Internal write cycle time tWR

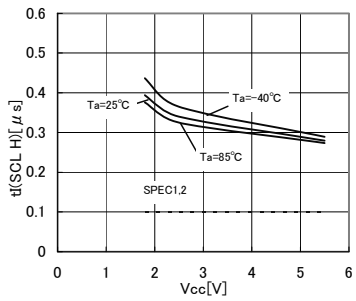



Fig.29 Noise removal valid time tI(SCL H)

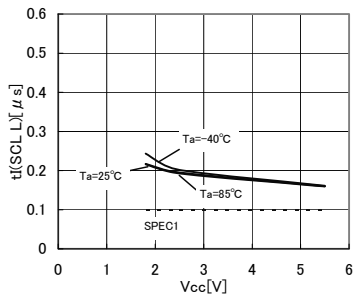



Fig.30 Noise removal valid time tI(SCL L)

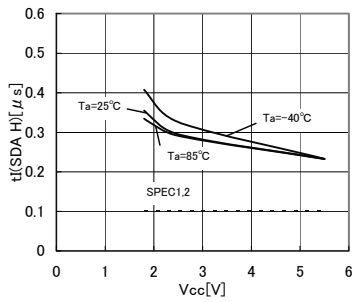



Fig.31 Noise removal valid time tI(SDA H)

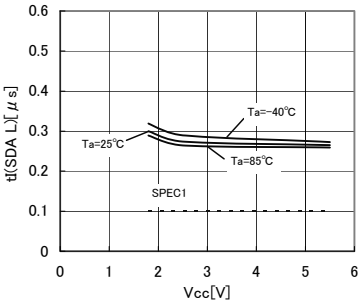



Fig.32 Noise removal valid time tI(SDA L)

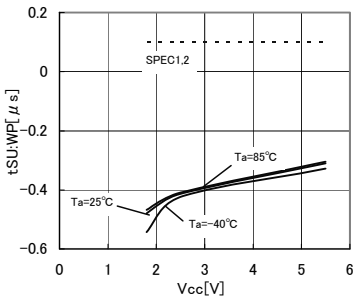



Fig.33 WP setup time tSU:WP

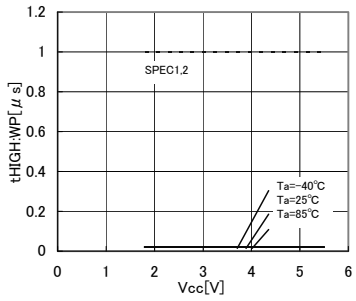



Fig.34 WP valid time tHIGH:WP

## ●I²C BUS communication

### ○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).
Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by address peculiar to devices. EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

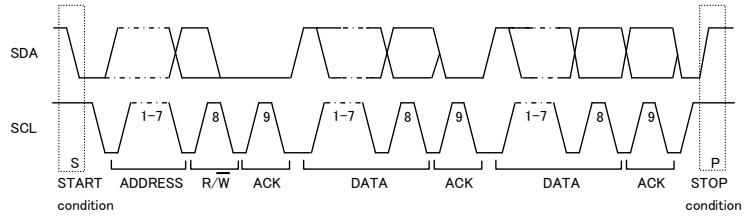



Fig.35 Data transfer timing

### ○Start condition (Start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this confdition is satisfied, any command is executed.

### ○Stop condition (stop bit recongnition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

### ○Acknowledge (ACK) signal

- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (μ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and μ-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write action outputs acknowledge signal (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'.
- When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop cindition (stop bit), and ends read action. And this IC gets in status.

### ○Device addressing

- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to '1010'.
- Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
- The most insignificant bit ($\overline{R}$/W --- READ / $\overline{WRITE}$) of slave address is used for designating write or read action, and is as shown below.

  Setting R / $\overline{W}$ to 0 ------- write (setting 0 to word address setting of random read)
  Setting R / $\overline{W}$ to 1 ------- read

| Type | Slave address | Maximum number of connected buses |
|---|---|---|
| BR24L01A-W | 1 0 1 0 A2 A1 A0 R/$\overline{W}$ | 8 |
| BR24L02-W | 1 0 1 0 A2 A1 A0 R/$\overline{W}$ | 8 |
| BR24L04-W | 1 0 1 0 A2 A1 PS R/$\overline{W}$ | 4 |
| BR24L08-W | 1 0 1 0 A2 P1 P0 R/$\overline{W}$ | 2 |
| BR24L16-W | 1 0 1 0 P2 P1 P0 R/$\overline{W}$ | 1 |
| BR24L32-W | 1 0 1 0 A2 A1 A0 R/$\overline{W}$ | 8 |
| BR24L64-W | 1 0 1 0 A2 A1 A0 R/$\overline{W}$ | 8 |

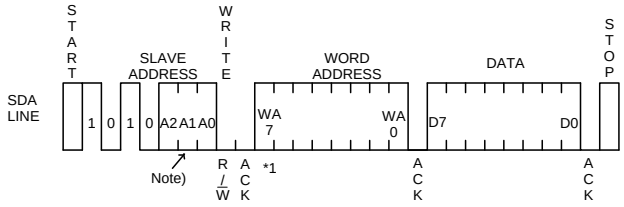
PS, P0～P2 are page select bits.

Note) Up to 4 units BR24L04-W, up to 2 units of BR24L08-W, and one unit of BR24L16-W can be connected.
Device address is set by 'H' and 'L' of each pin of A0, A1, and A2.

## ●Write Command

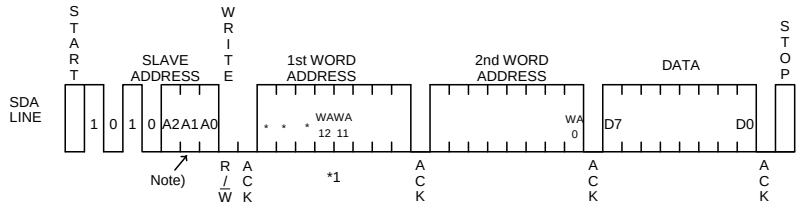
### ○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is specified per device of each capacity. Up to 32 arbitrary bytes can be written. (In the case of BR24L32 / L64-W)



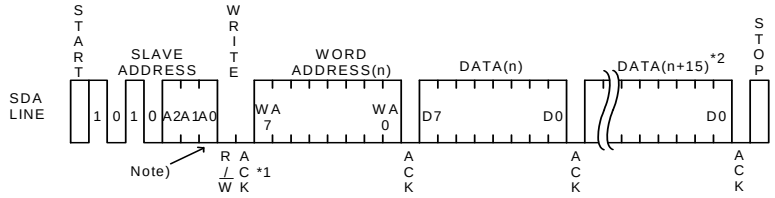

*1 As for WA7, BR24L01A-W becomes Don't care.

Fig.36 Byte write cycle (BR24L01A/02/04/08/16-W)



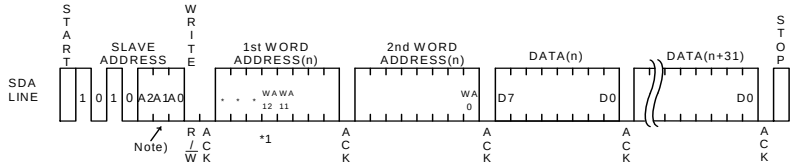

*1 As for WA12, BR24L32-W becomes Don't care.

Fig.37 Byte write cycle (BR24L32/64-W)




*1 As for WA7, BR24L01A-W becomes Don't care.
*2 As for BR24L01A/02-W becomes (n+7).

Fig.38 Page write cycle (BR24L01A/02/04/08/16-W)

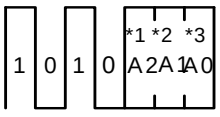



*1 As for WA12, BR24L32-W becomes Don't care.

Fig.39 Page write cycle (BR24L32/64-W)

・Data is written to the address designated by word address (n-th address)
・By issuing stop bit after 8bit data input, write to memory cell inside starts.
・When internal write is started, command is not accepted for tWR (5ms at maximum).
・By page write cycle, the following can be written in bulk : Up to 8 bytes ( BR24L01A-W, BR24L02-W)
: Up to 16bytes (BR24L04-W, BR24L08-W,BR24L16-W)
: Up to 32bytes (BR24L32-W, BR24L64-W)
And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to "Internal address increment" of "Notes on page write cycle" in P9/32.)
・As for page write cycle of BR24L01A-W and BR24L02-W, after the significant 5 bits (4 significant bits in BR24L01-W) of word address are designated arbitrarily, and as for page write command of BR24L04-W, BR24L08-W, and BR24L16-W, after page select bit (PS) of slave address is designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 4 bits (insignificant 3 bit in BR24L01A-W, and BR24L02-W) is incremented internally, and data up to 16 bytes (up to 8 bytes in BR24L01A-W and BR24L02-W) can be written.
・As for page write cycle of BR24L32-W and BR24L64-W, after the significant 7 bits (in the case of BR24L32-W) of word address, or the significant 8 bits (in the case of BR24L64-W) of word address are designated arbitrarily, by continuing data input of 2 byte or more, the address of insignificant 5 bits is incremented internally, and data up to 32 bytes can be written.

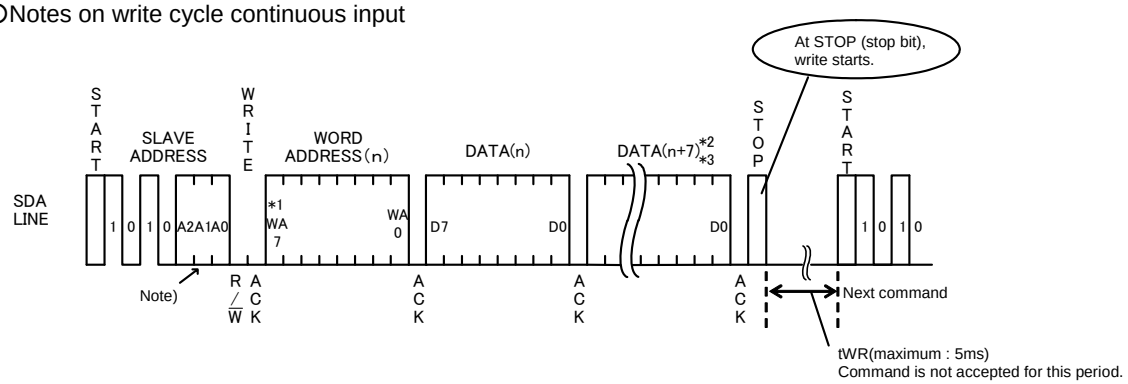
Note)




*1 In BR24L16-W, A2 becomes P2.
*2 In BR24L08-W, BR24L16-W, A1 becomes P1.
*3 In BR24L04-W, A0 becomes PS, and in BR24L08-W and BR24L16-W, A0 becomes P0.

Fig.40 Difference of slave address of each type

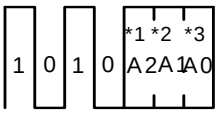
○Notes on write cycle continuous input




*1 BR24L01A-W becomes Don't care.
*2 BR24L04-W, BR24L08-W, and BR24L16-W become (n+15).
*3 BR24L32-W and BR24L64-W become (n+31).

Fig.41 Page write cycle

Note)




*1 In BR24L16-W, A2 becomes P2.
*2 In BR24L08-W, BR24L16-W, A1 becomes P1.
*3 In BR24L04-W, A0 becomes PS, and in BR24L08-W and in BR24L16-W, A0 becomes P0.

Fig.42 Difference of each type of slave address

○Notes on page write cycle

List of numbers of page write

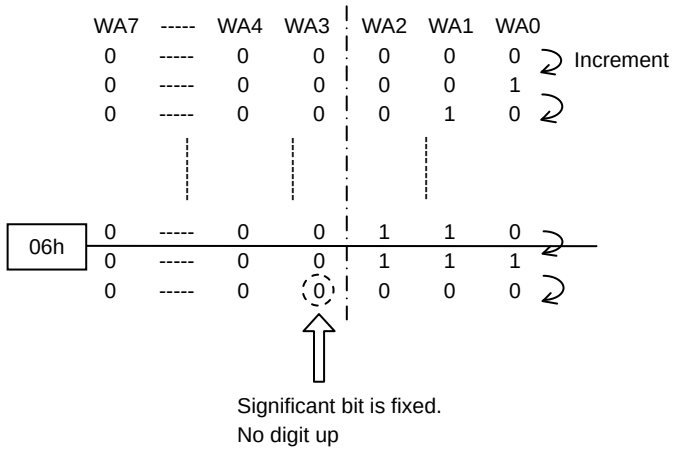
| Number of Pages | 8Byte | 16Byte | 32Byte |
|---|---|---|---|
| Product number | BR24L01A-W<br>BR24L02-W | BR24L04-W<br>BR24L08-W<br>BR24L16-W | BR24L32-W<br>BR24L64-W |

The above numbers are maximum bytes for respective types.
Any bytes below these can be written.

In the case BR24L02-W, 1 page=8bytes, but the page write cycle write time is 5ms at maximum for 8byte bulk write.
It does not stand 5ms at maximum × 8byte=40ms(Max.).

○Internal address increment

Page write mode (in the case of BR24L02-W)




For example, when it is started from address 06h,therefore, increment is made as below,
06h → 07h → 00h → 01h ---, which please note.

＊ 06h･･･06 in hexadecimal, therefore, 00000110 becomes a binary number.

○Write protect (WP) terminal

・Write protect (WP) function

When WP terminal is set Vcc (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.

At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', mistake write can be prevented.

During tWR, set the WP terminal always to 'L'. If it is set 'H', write is forcibly terminated.

## ●Read Command

### ○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.
Random read cycle is a command to read data by designating address, and is used generally.
Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.

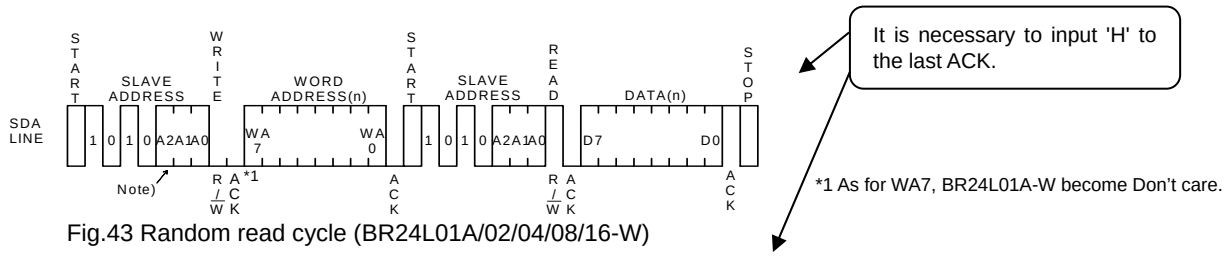



Fig.43 Random read cycle (BR24L01A/02/04/08/16-W)

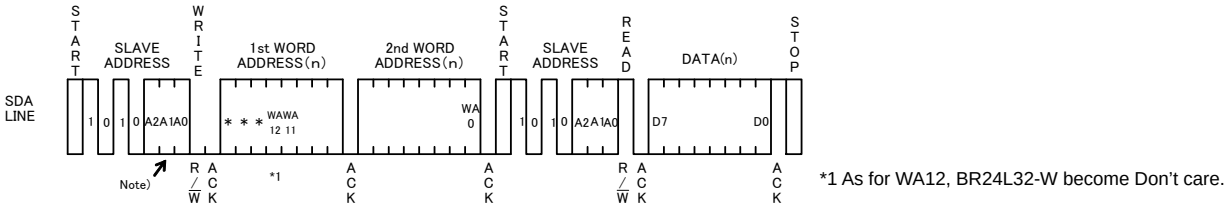



Fig.44 Random read cycle (BR24L32/64 -W)

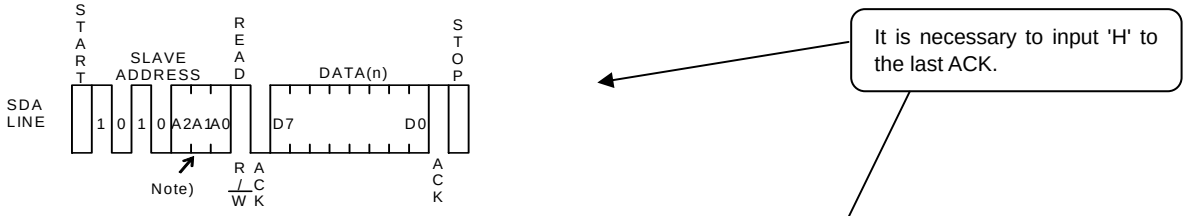



Fig.45 Current read cycle

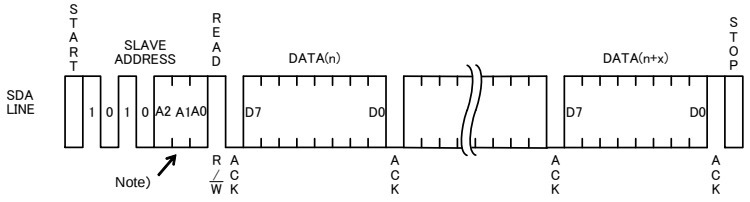
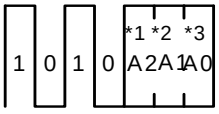



Fig.46 Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master ($\mu$-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H' .
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

Note)




*1 In BR24L16-W, A2 becomes P2.
*2 In BR24L08-W, BR24L16-W, A1 becomes P1.
*3 In BR24L04-W, A0 becomes PS, and in BR24L08-W and BR24L16-W, A0 becomes P0.

Fig.47 Difference of slave address of each type

**●Software reset**

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Fig.48(a), Fig.48(b), and Fig.48(c).) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

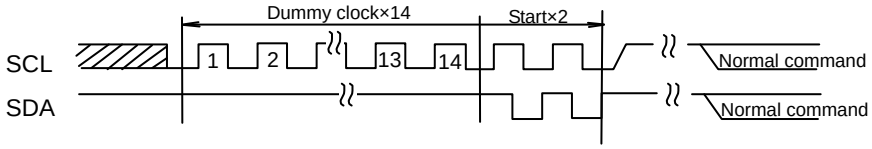



Fig.48-(a) The case of dummy clock +START+START+ command input

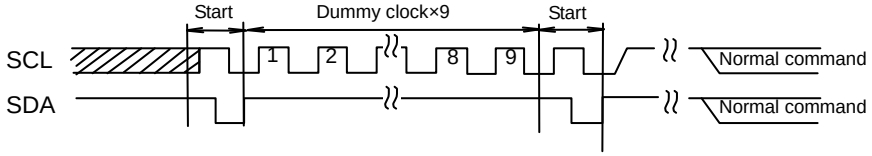
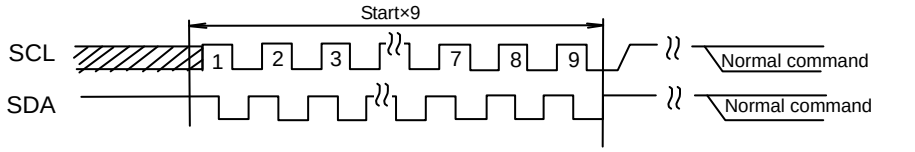



Fig.48-(b) The case of START +9 dummy clocks +START+ command input




* Start command from START input.

Fig.48-(c) START×9+ command input

**●Acknowledge polling**

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, R/$\overline{W}$ = 0, when to carry out current read cycle after write, slave address R/$\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

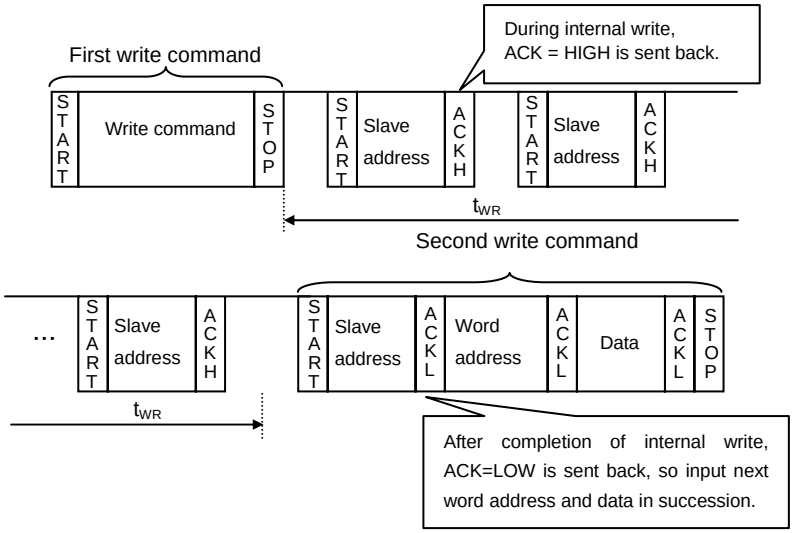



Fig.49 Case to continuously write by acknowledge polling

**●WP valid timing (write cancel)**

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.

WP input in this area becomes Don't care. Set the setup time to rise of D0 taken SCL 100ns or more. The area from the rise of SCL to take in D0 to the end of internal automatic write (tWR) is cancel valid area. And, when it is set WP='H' during tWR, write is ended forcibly, data of address under access is not guaranteed, therefore, write it once again. (Refer to Fig.50.) After execution of forced end by WP, standby status gets in, so there is no need to wait for tWR (5ms at maximum).

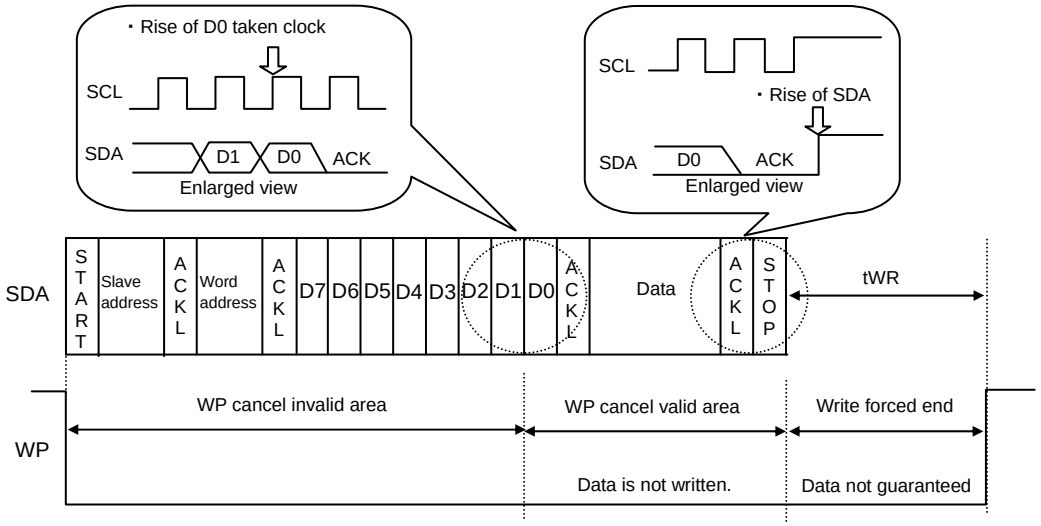



Fig.50 WP valid timing

**●Command cancel by start condition and stop condition**

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Refer to Fig. 51)

However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

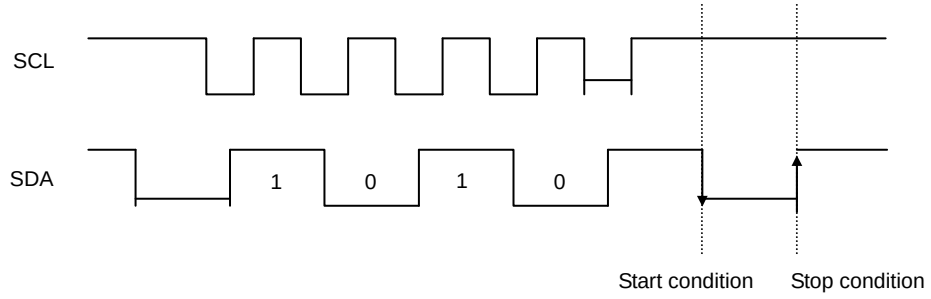



Fig.51 Case of cancel by start, stop condition during slave address input

**●I/O peripheral circuit**

○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value ($R_{PU}$), select an appropriate value to this resistance value from microcontroller $V_{IL}$, $I_L$, and $V_{OL}$-$I_{OL}$ characteristics of this IC. If $R_{PU}$ is large, action frequency is limited. The smaller the $R_{PU}$, the larger the consumption current at action.

○Maximum value of $R_{PU}$

The maximum value of $R_{PU}$ is determined by the following factors.

(1)SDA rise time to be determined by the capacitance (CBUS) of bus line of $R_{PU}$ and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by input leak total ($I_L$) of device connected to bus at output of 'H' to SDA bus and $R_{PU}$ should sufficiently secure the input 'H' level ($V_{IH}$) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$V_{CC} - I_L R_{PU} - 0.2Vcc \geqq V_{IH}$$

$$\therefore \quad R_{PU} = \frac{0.8Vcc - V_{IH}}{I_L}$$

Ex. ) When $V_{CC}$ =3V, $I_L$=10μA, $V_{IH}$=0.7 $V_{CC}$, from (2)

$$R_{PU} \leqq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leqq 300 \text{ [k}\Omega\text{]}$$

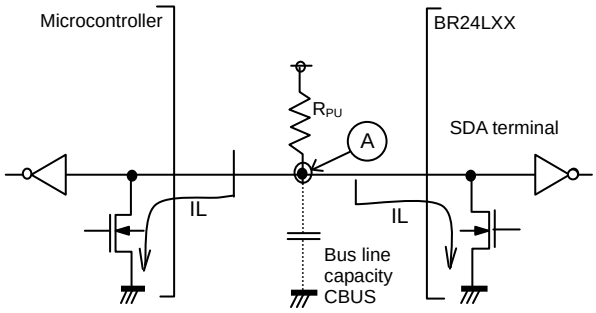



Fig.52 I/O circuit diagram

○Minimum value of $R_{PU}$

The minimum value of $R_{PU}$ is determined by the following factors.

(1)When IC outputs LOW, it should be satisfied that $V_{OLMAX}$=0.4V and $I_{OLMAX}$=3mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL} \qquad \therefore \quad R_{PU} \geqq \frac{V_C - V_{OL}}{I_{OL}}$$

(2)$V_{OLMAX}$=0.4V should secure the input 'L' level ($V_{IL}$) of microcontroller and EEPROM including recommended noise margin 0.1Vcc.

$V_{OLMAX} \leqq V_{IL}$-0.1 $V_{CC}$

Ex. ) When $V_{CC}$ =3V, $V_{OL}$=0.4V, $I_{OL}$=3mA, microcontroller, EEPROM $V_{IL}$=0.3$V_{CC}$ from (1)

$$R_{PU} \geqq \frac{3\text{-}0.4}{3 \times 10^{-3}}$$

$$\geqq 867 \text{ [}\Omega\text{]}$$

And

$V_{OL}$ = 0.4 [V]

$V_{IL}$ = 0.3×3

= 0.9 [V]

Therefore, the condition (2) is satisfied.

○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ ~ several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

**●A0, A1, A2, WP process**

○Process of device address terminals (A0,A1,A2)

Check whether the set device address coincides with device address input sent from the master side or not, and select one among plural devices connected to a same bus. Connect this terminal to pull up or pull down, or Vcc or GND. And, pins (N, C, PIN) not used as device address may be set to any of 'H' , 'L', and 'Hi-Z'.

| | | |
|---|---|---|
| Types with N.C.PIN | BR24L16/F/FJ/FV/FVT/FVM/FVJ-W | A0, A1, A2 |
| | BR24L08/F/FJ/FV/FVT/FVM/FVJ/NUX-W | A0, A1 |
| | BR24L04/F/FJ/FV/FVT/FVM/FVJ/NUX-W | A0 |

○Process of WP terminal

WP terminal is the terminal that prohibits and permits write in hardware manner. In 'H' status, only READ is available and WRITE of all address is prohibited. In the case of 'L', both are available. In the case of use it as an ROM, it is recommended to connect it to pull up or Vcc. In the case to use both READ and WRITE, control WP terminal or connect it to pull down or GND.

**●Cautions on microcontroller connection**

○Rs

In $I^2C$ BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

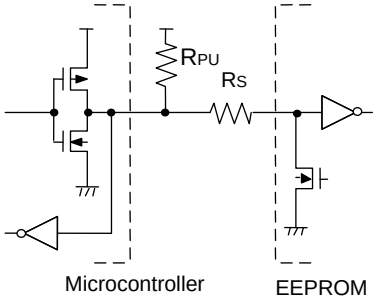



Fig.53 I/O circuit diagram

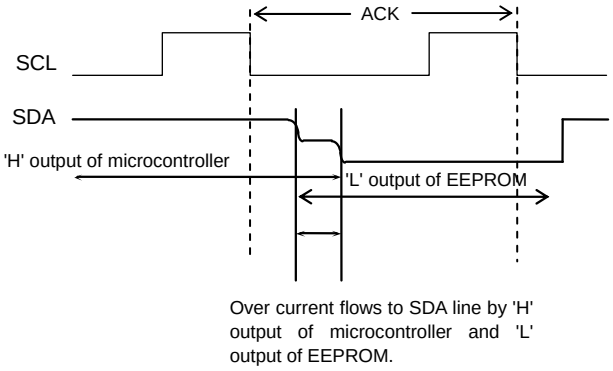



Fig.54 Input / output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by the following relations.

(1)SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level ($V_{IL}$) of microcontroller including recommended noise margin 0.1Vcc.

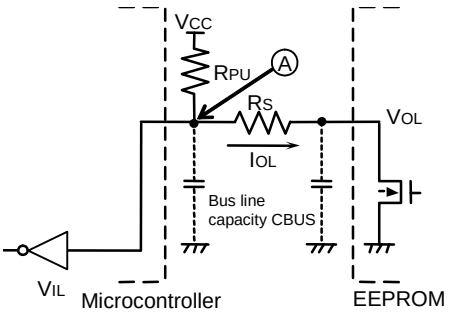



Fig.55 I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When $V_{CC}$=3V, $V_{IL}$=0.3$V_{CC}$, $V_{OL}$=0.4V, $R_{PU}$=20kΩ

$$\text{from(2)}, \quad R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67\ [k\Omega]$$

○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

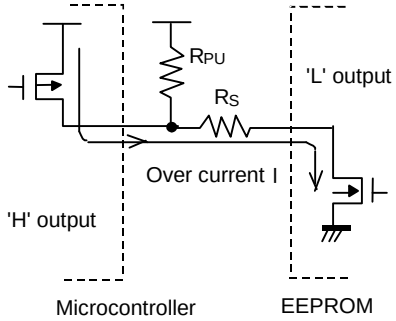



Fig.56 I/O circuit diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Example)When $V_{CC}$=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300\ [\Omega]$$

●**I²C BUS input / output circuit**

○Input (A0,A2,SCL)

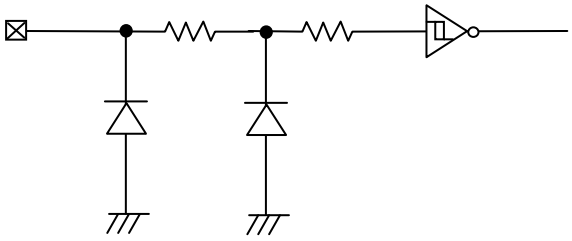


Fig.57 Input pin circuit diagram

○Input / output (SDA)

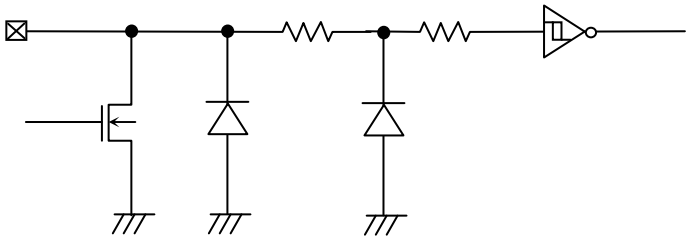


Fig.58 Input / output pin circuit diagram

○Input (A1, WP)

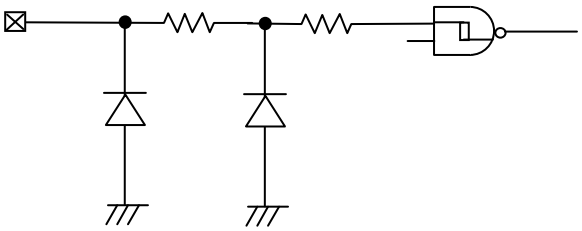


Fig.59 Input pin circuit diagram

●**Notes on power ON**

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of $t_R$, $t_{OFF}$, and Vbot for operating POR circuit.

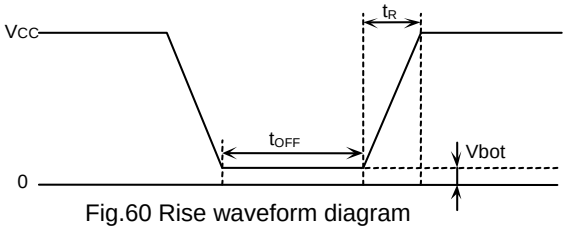



Fig.60 Rise waveform diagram

Recommended conditions of $t_R$, $t_{OFF}$, $V_{bot}$

| $t_R$ | $t_{OFF}$ | $V_{bot}$ |
|---|---|---|
| 10ms or below | 10ms or longer | 0.3V or below |
| 100ms or below | 10ms or longer | 0.2V or below |

3. Set SDA and SCL so as not to become 'Hi-Z'.
When the above conditions 1 and 2 cannot be observed, take the following countermeasures.
a) In the case when the above condition 1 cannot be observed. When SDA becomes 'L' at power on .
→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

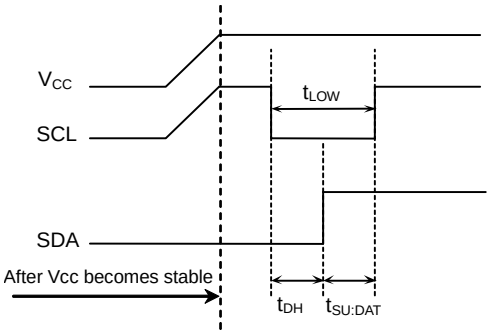



Fig.61 When SCL= 'H' and SDA= 'L'

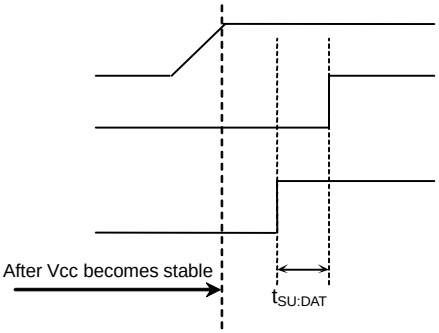



Fig.62 When SCL='L' and SDA='L'

b) In the case when the above condition 2 cannot be observed.
→After power source becomes stable, execute software reset(P11).

c) In the case when the above conditions 1 and 2 cannot be observed.
→Carry out a), and then carry out b).

**●Low voltage malfunction prevention function**

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

**●Vcc noise countermeasures**

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

**●Notes for use**

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Terminal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

Serial EEPROM Series

# High Reliability Series EEPROMs I²C BUS

## BR24S□□□-W Series

### ●Description

BR24S□□□-W series is a serial EEPROM of I2C BUS interface method.

### ●Features

1) Completely conforming to the world standard I²C BUS. All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
2) Other devices than EEPROM can be connected to the same port, saving microcontroller port.
3) 1.7～5.5V single power source action most suitable for battery use.
4) FAST MODE 400kHz at 1.7～5.5V
5) Page write mode useful for initial value write at factory shipment.
6) Highly reliable connection by Au pad and Au wire.
7) Auto erase and auto end function at data rewrite.
8) Low current consumption
   At write operation (5V) : 0.5mA (Typ.)
   At read operation (5V) : 0.2mA (Typ.)
   At standby operation (5V) : 0.1μA (Typ.)
9) Write mistake prevention function
   Write (write protect) function added
   Write mistake prevention function at low voltage
10) SOP8/SOP-J8/SSOP-B8/TSSOP-B8/MSOP8/TSSOP-B8J/VSON008X2030 compact package
11) Data rewrite up to 1,000,000 times
12) Data kept for 40 years
13) Noise filter built in SCL / SDA terminal
14) Shipment data all address FFh

### ●Page write

| Number of pages | 16Byte | 32Byte | 64Byte |
|---|---|---|---|
| Product number | BR24S08-W<br>BR24S16-W | BR24S32-W<br>BR24S64-W | BR24S128-W<br>BR24S256-W |

### ●BR24S series

| Capacity | Bit format | Type | Power source voltage | SOP8 | SOP-J8 | SSOP-B8 | TSSOP-B8 | MSOP8 | TSSOP-B8J | VSON008 X2030 |
|---|---|---|---|---|---|---|---|---|---|---|
| 8Kbit | 1K×8 | BR24S08-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● |
| 16Kbit | 2K×8 | BR24S16-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● |
| 32Kbit | 4K×8 | BR24S32-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● |
| 64Kbit | 8K×8 | BR24S64-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | |
| 128Kbit | 16K×8 | BR24S128-W | 1.7～5.5V | ● | ● | ● | ● | | | |
| 256Kbit | 32K×8 | BR24S256-W | 1.7～5.5V | ● | ● | | | | | |

**●Absolute maximum ratings (Ta=25℃)**

| Parameter | symbol | Limits | Unit |
|---|---|---|---|
| Impressed voltage | Vcc | -0.3～+6.5 | V |
| Permissible dissipation | Pd | 450 (SOP8) *1 | mW |
| | | 450 (SOP-J8) *2 | |
| | | 300 (SSOP-B8) *3 | |
| | | 330 (TSSOP-B8) *4 | |
| | | 310 (MSOP8) *5 | |
| | | 310 (TSSOP-B8J) *6 | |
| | | 300 (VSON008X2030) *7 | |
| Storage temperature range | Tstg | -65～+125 | ℃ |
| Action temperature range | Topr | -40～+85 | ℃ |
| Terminal voltage | - | -0.3～Vcc+1.0 | V |

*When using at Ta=25℃ or higher, 4.5mW(*1,*2), 3.0mW(*3,*7) 3.3mW(*4),3.1mW(*5,*6) to be reduced per 1℃

**●Memory cell characteristics (Ta=25℃, Vcc=1.7～5.5V)**

| Parameter | Limits | | | Unit |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| Number of data rewrite times *1 | 1,000,000 | - | - | Times |
| Data hold years *1 | 40 | - | - | Years |

*1 Not 100% TESTED

**●Recommended operating conditions**

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power source voltage | Vcc | 1.7～5.5 | V |
| Input voltage | VIN | 0～Vcc | |

**●Electrical characteristics**

(Unless otherwise specified, T=-40～+85℃, Vcc=1.7～5.5V)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ. | Max. | | |
| "H" Input Voltage1 | VIH1 | 0.7Vcc | - | Vcc+1.0 | V | |
| "L" Input Voltage1 | VIL1 | -0.3 | - | 0.3Vcc | V | |
| "L" Output Voltage1 | VOL1 | - | - | 0.4 | V | IOL=3.0mA , 2.5V≦Vcc≦5.5V (SDA) |
| "L" Output Voltage2 | VOL2 | - | - | 0.2 | V | IOL=0.7mA , 1.7V≦Vcc≦2.5V (SDA) |
| Input Leakage Current | ILI | -1 | - | 1 | μA | VIN=0～Vcc |
| Output Leakage Current | ILO | -1 | - | 1 | μA | VOUT=0～Vcc (SDA) |
| Current consumption at action | ICC1 | - | - | 2.0 | mA | Vcc=5.5V , fSCL =400kHz, tWR=5ms<br>Byte Write, Page Write BR24S08/16/32/64-W |
| | | - | - | 2.5 | | Vcc=5.5V , fSCL =400kHz, tWR=5ms<br>Byte Write, Page Write BR24S128/256-W |
| | ICC2 | - | - | 0.5 | mA | Vcc=5.5V , fSCL =400kHz<br>Random read, Current read, Sequential read |
| Standby Current | ISB | - | - | 2.0 | μA | Vcc=5.5V , SDA・SCL=Vcc<br>A0, A1, A2=GND, WP=GND |

○Radiation resistance design is not made.

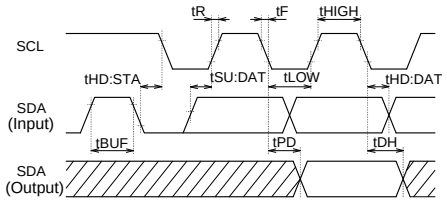
●**Action timing characteristics**

(Unless otherwise specified, T=-40～+85℃, Vcc=1.7～5.5V)

| Parameter | Symbol | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| SCL Frequency | fSCL | - | - | 400 | kHz |
| Data clock "High" time | tHIGH | 0.6 | - | - | μs |
| Data clock "Low" time | tLOW | 1.2 | - | - | μs |
| SDA, SCL rise time *1 | tR | - | - | 0.3 | μs |
| SDA, SCL fall time *1 | tF | - | - | 0.3 | μs |
| Start condition hold time | tHD:STA | 0.6 | - | - | μs |
| Start condition setup time | tSU:STA | 0.6 | - | - | μs |
| Input data hold time | tHD:DAT | 0 | - | - | ns |
| Input data setup time | tSU:DAT | 100 | - | - | ns |
| Output data delay time | tPD | 0.1 | - | 0.9 | μs |
| Output data hold time | tDH | 0.1 | - | - | μs |
| Stop condition data setup time | tSU:STO | 0.6 | - | - | μs |
| Bus release time before transfer start | tBUF | 1.2 | - | - | μs |
| Internal write cycle time | tWR | - | - | 5 | ms |
| Noise removal valid period (SDA,SCL terminal) | tI | - | - | 0.1 | μs |
| WP hold time | tHD:WP | 0 | - | - | ns |
| WP setup time | tSU:WP | 0.1 | - | - | μs |
| WP valid time | tHIGH:WP | 1.0 | - | - | μs |

*1 : Not 100% TESTED

## ●Sync data input/output timing




○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Fig.1-(a) Sync data input / output timing

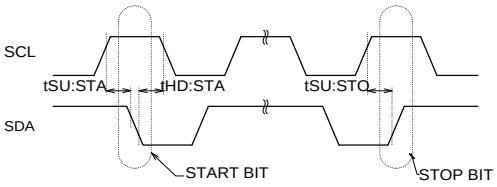



Fig.1-(b) Start - stop bit timing

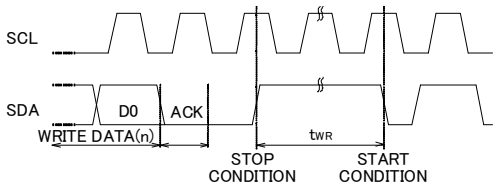



Fig.1-(c) Write cycle timing

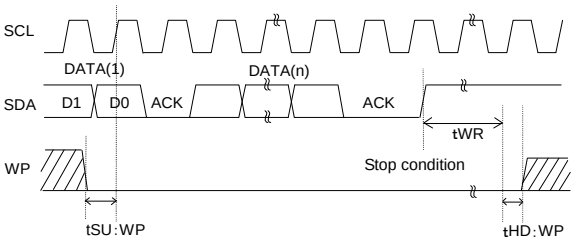
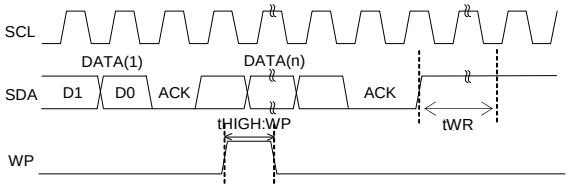


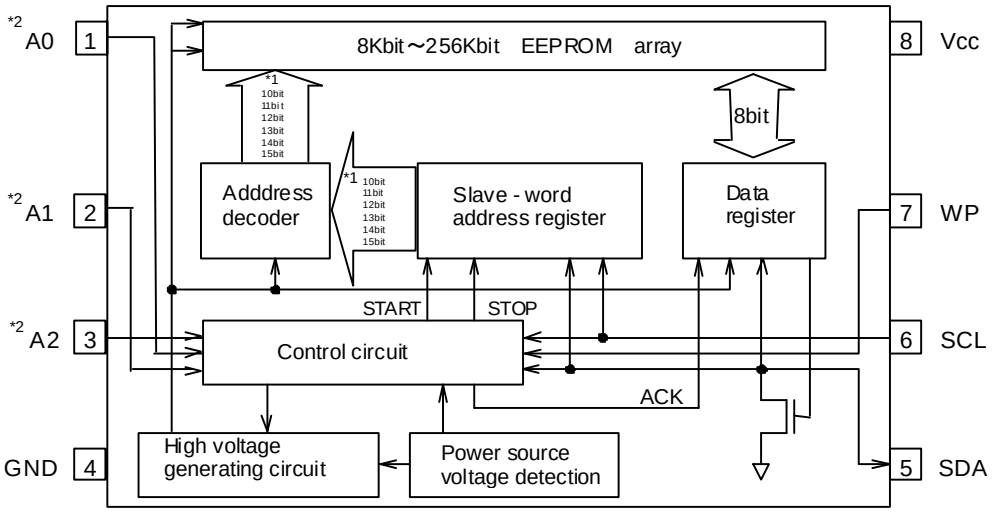

Fig.1-(d) WP timing at write execution




○At write execution, in the area from the D0 taken clock rise of the first DATA(1), to tWR, set WP= 'LOW'.
○By setting WP "HIGH" in the area, write can be cancelled.
When it is set WP = 'HIGH' during tWR, write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

Fig.1-(e) WP timing at write cancel

## ●Block diagram

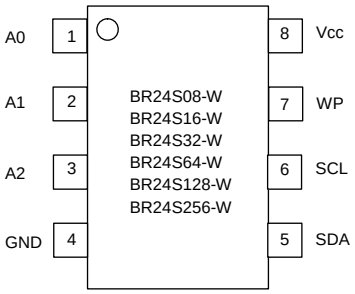



*1 10bit: BR24S08-W
11bit: BR24S16-W
12bit: BR24S32-W
13bit: BR24S64-W
14bit: BR24S128-W
15bit: BR24S256-W

*2 A0, A1= Don't use: BR24S08-W
A0, A1, A2= Don't use: BR24S16-W

Fig.2 Block diagram

**●Pin assignment and description**




| Terminal name | Input/ Output | Function | | |
|---|---|---|---|---|
| | | BR24S08-W | BR24S16-W | BR24S32/64/128/256-W |
| A0 | Input | Don't use | Don't use | Slave address setting |
| A1 | Input | Don't use | Don't use | Slave address setting |
| A2 | Input | Slave address setting | Don't use | Slave address setting |
| GND | - | Reference voltage of all input / output, 0V. | | |
| SDA | Input / Output | Slave and word address,<br>Serial data input serial data output | | |
| SCL | Input | Serial clock input | | |
| WP | Input | Write protect terminal | | |
| Vcc | - | Connect the power source. | | |

**●Characteristic data (The following values are Typ. ones.)**

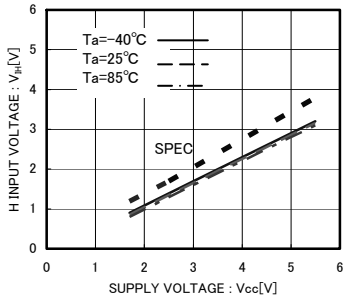



Fig.3 'H' input voltage $V_{IH}$
(A0,A1,A2,SCL,SDA,WP)

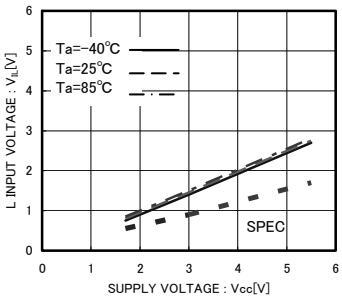



Fig.4 'L' input voltage $V_{IL}$
(A0,A1,A2,SCL,SDA,WP)

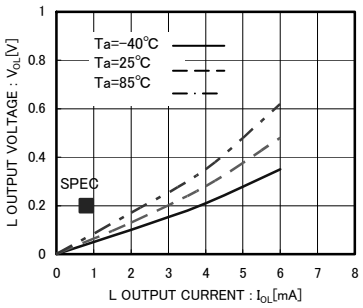



Fig.5 'L' output voltage $V_{OL}$-$I_{OL}$(Vcc=1.7V)

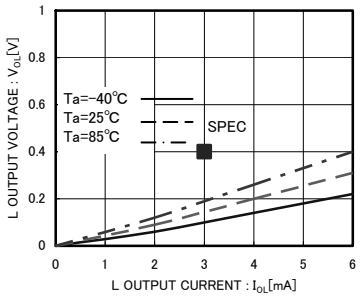



Fig.6 'L' output voltage $V_{OL}$-$I_{OL}$(Vcc=2.5V)

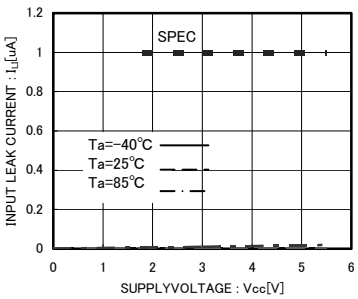



Fig.7 Input leak current $I_{LI}$
(A0,A,A2,SCL,WP)

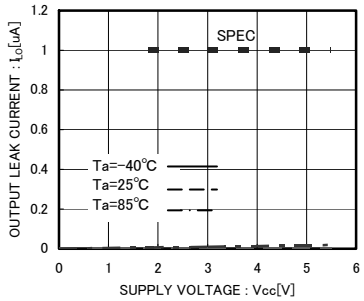



Fig.8 Output leak current $I_{LO}$(SDA)

## ●Characteristic data (The following values are Typ. ones.)

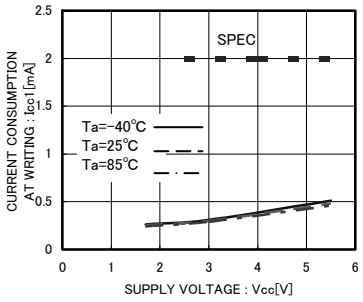



Fig.9 Current consumption at WRITE operation $I_{CC}1$
($f_{SCL}$=400kHz BR24S16/32/64-W)

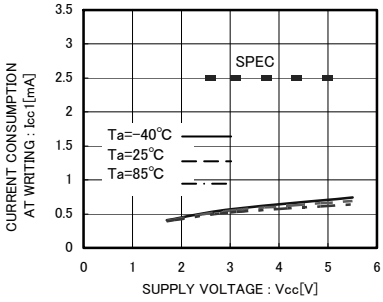



Fig.10 Current consumption at WRITE operation Icc1
($f_{SCL}$=400kHz BR24S128/256-W)

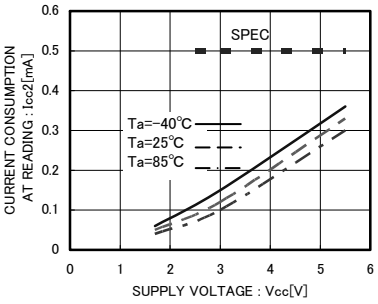



Fig.11 Current consumption at READ operation $I_{CC}2$
($f_{SCL}$=400kHz)

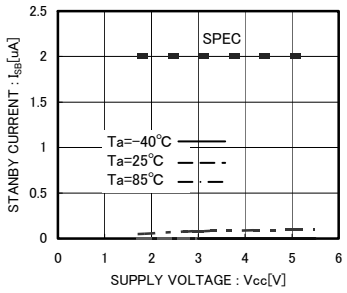



Fig.12 Stanby operation $I_{SB}$

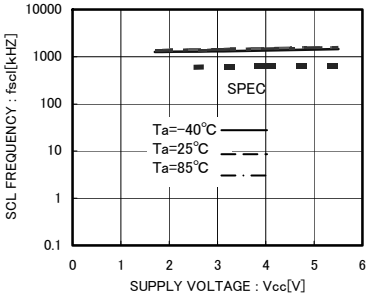



Fig.13 SCL frequency $f_{SCL}$

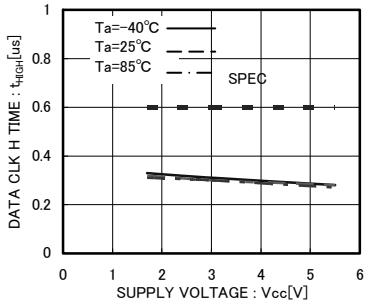



Fig.14 Data clock High Period $t_{HIGH}$

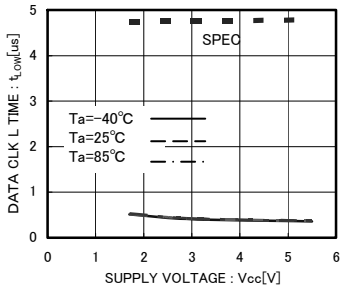



Fig.15 Data clock Low Period $t_{LOW}$

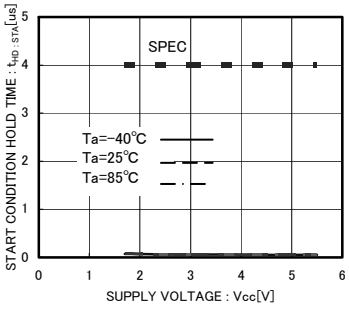



Fig.16 Start Condition Hold Time $t_{HD:STA}$

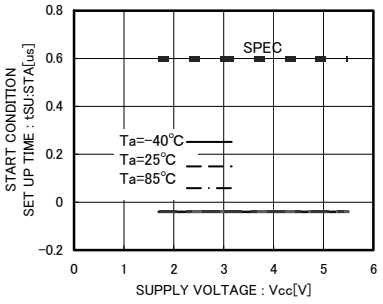



Fig.17 Start Condition Setup Time $t_{SU:STA}$

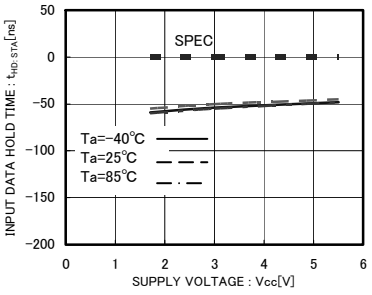



Fig.18 Input Data Hold Time $t_{HD:DAT}$(HIGH)

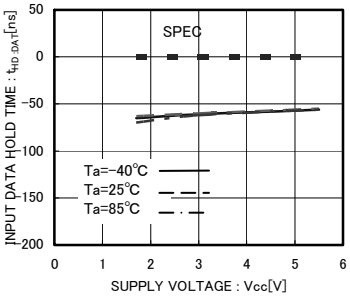



Fig.19 Input Data Hold Time $t_{HD:DAT}$(LOW)

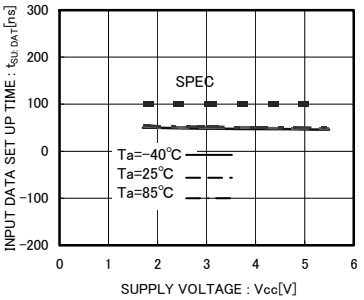



Fig.20 Input Data Setup Time $t_{SU:DAT}$(HIGH)

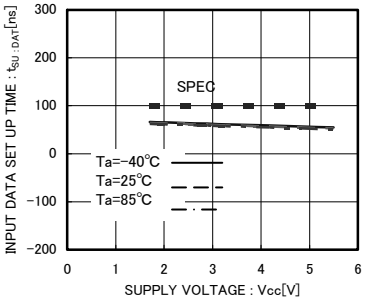



Fig.21 Input Data setup time $t_{SU:DAT}$(LOW)

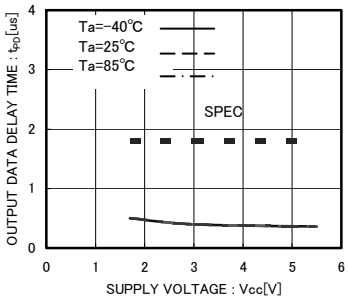



Fig.22 'L' Data output delay time $t_{PD}0$

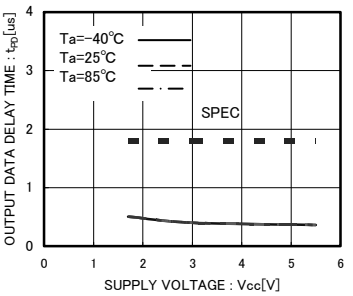



Fig.23 'H' Data output delay time $t_{PD}1$

## ●Characteristic data (The following values are Typ. ones.)

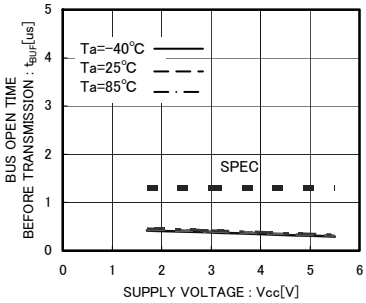



Fig.24 BUS open time before transmission $t_{BUF}$

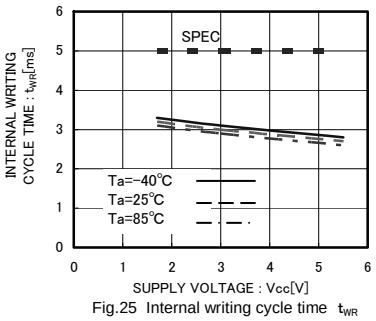



Fig.25 Internal writing cycle time $t_{WR}$

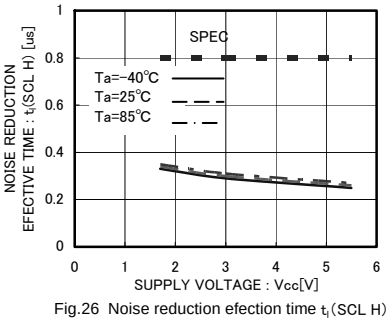



Fig.26 Noise reduction efection time $t_f$(SCL H)

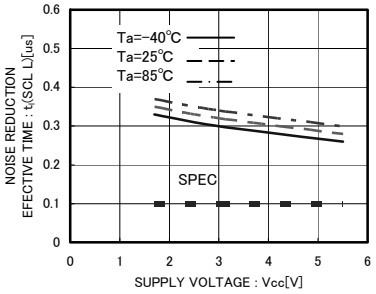



Fig.27 Noise reduction efective time $t_f$(SCL L)

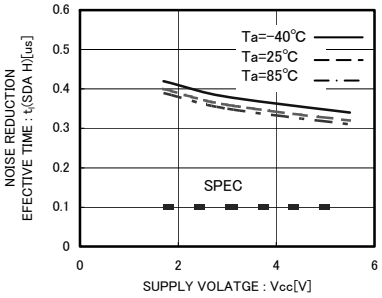



Fig.28 Noise resuction efecctive time $t_f$(SDA H)

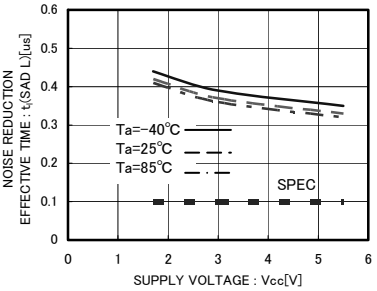



Fig.29 Noise reduction efective time $t_f$(SDA L)

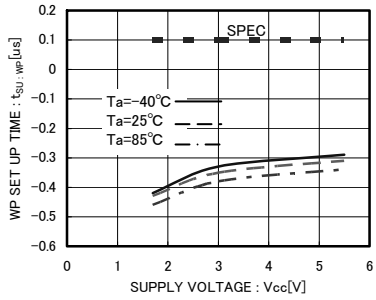



Fig.30 WP setup time $t_{SU:WP}$

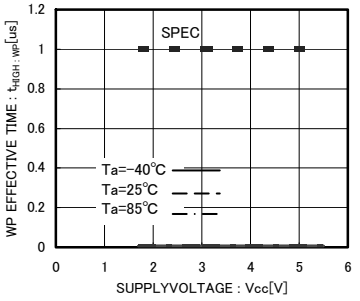



Fig.31 WP efective time $t_{HIGH:WP}$

## ●I²C BUS communication

### ○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte.
I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).
Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by addresses peculiar to devices.
EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

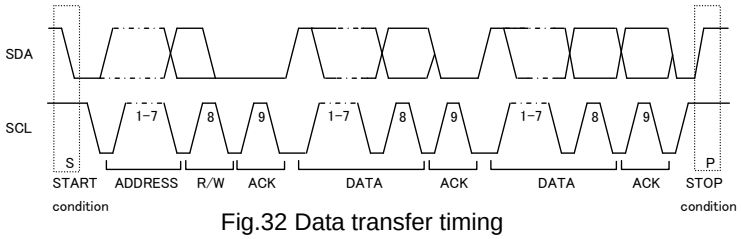



Fig.32 Data transfer timing

### ○Start condition (start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command is executed.

### ○Stop condition (stop bit recognition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

### ○Acknowledge (ACK) signal

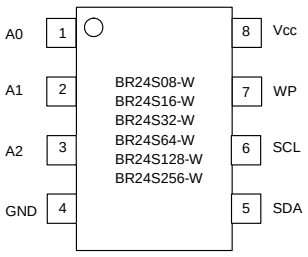
- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device ($\mu$-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and $\mu$-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write action outputs acknowledge signal) (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'.
- When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master ($\mu$-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read action. And this IC gets in standby status.

### ○Device addressing

- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to '1010'.
- Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
- The most insignificant bit (R/$\overline{W}$ --- READ/$\overline{WRITE}$) of slave address is used for designating write or read action, and is as shown below.

Setting R/$\overline{W}$ to 0 --- write (setting 0 to word address setting of random read)
Setting R/$\overline{W}$ to 1 --- read

| Type | Slave address | | | | | | | | Maximum number of connected buses |
|---|---|---|---|---|---|---|---|---|---|
| BR24S08-W | 1 | 0 | 1 | 0 | A2 | P1 | P0 | R/$\overline{W}$ | 2 |
| BR24S16-W | 1 | 0 | 1 | 0 | P2 | P1 | P0 | R/$\overline{W}$ | 1 |
| BR24S32-W, BR24S64-W<br>BR24S128-W, BR24S256-W | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/$\overline{W}$ | 8 |




P0～P2 are page select bits.
Note) Up to 2 units of BR24S08-W, up to 1 units of BR24S16-W, and up to 8 units of BR24S32/64/128/256-W can be connected.
Device address is set by 'H' and 'L' of each pin of A0, A1, and A2.

**●Write Command**

○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is specified per device of each capacity.
Up to 64 arbitrary bytes can be written. (In the case of BR24S128/256-W)

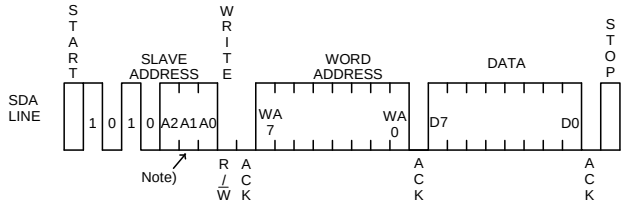
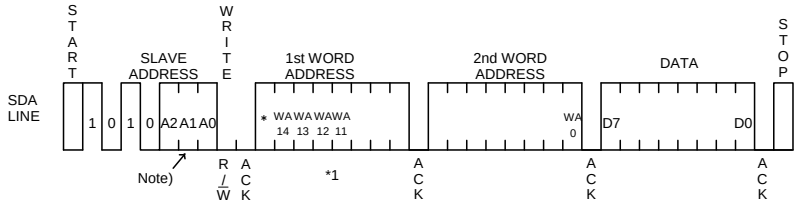



Fig.33 Byte write cycle (BR24S08/16-W)




*1 As for WA12, BR24S32-W becomes Don't care.
As for WA13, BR24S32/64-W becomes Don't care.
As for WA14, BR24S32/64/128-W becomes Don't care.

Fig.34 Byte write cycle (BR24S32/64/128/256-W)

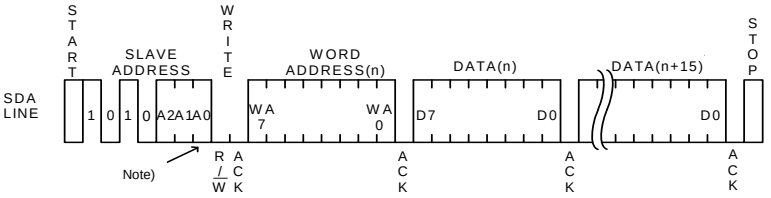
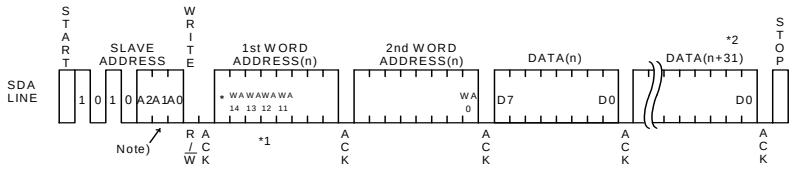



Fig.35 Page write cycle (BR24S08/16-W)



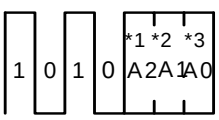

*1 As for WA12, BR24S32-W becomes Don't care.
As for WA13, BR24S32/64-W becomes Don't care.
As for WA14, BR24S32/64/128-W becomes Don't care.

*2 As for BR24S128/256-W becomes (n+63).

Fig.36 Page write cycle (BR24S32/64/128/256-W)

・Data is written to the address designated by word address (n-th address).
・By issuing stop bit after 8bit data input, write to memory cell inside starts.
・When internal write is started, command is not accepted for tWR (5ms at maximum).
・By page write cycle, the following can be written in bulk: Up to 16 bytes (BR24S08-W, BR24S16-W)
: Up to 32 bytes (BR24S32-W, BR24S64-W)
: Up to 64 bytes (BR24S128-W, BR24S256-W)
And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to "Internal address increment of "Notes on page write cycle" in P24/32.)
・As for page write command of BR24S08-W and, BR24S16-W, after page select bit(PS) of slave address is designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 4 bits is incremented internally, and data up to 16 bytes can be written.
・As for page write cycle of BR24S32-W and BR24S64-W , after the significant 7 bits (in the case of BR24S32-W) of word address, or the significant 8 bits (in the case of BR24S64-W) of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 5 bits is incremented internally, and data up to 32 bytes can be written.
・As for page write cycle of BR24S128-W and BR24S256-W, after the significant 9 bit (in the case of BR24S128-W) of word address, or the significant 10bit (in the case of BR24S256-W) of word address are designated arbitrarily, by continuing data input of 64 bytes or more.

Note)




*1 In BR24S16-W, A2 becomes P2
*2 In BR24S08/16-W, A1 becomes P1
*3 In BR24S08/16-W, A0 becomes P0

Fig.37 Difference of slave address each type

○Notes on write cycle continuous input

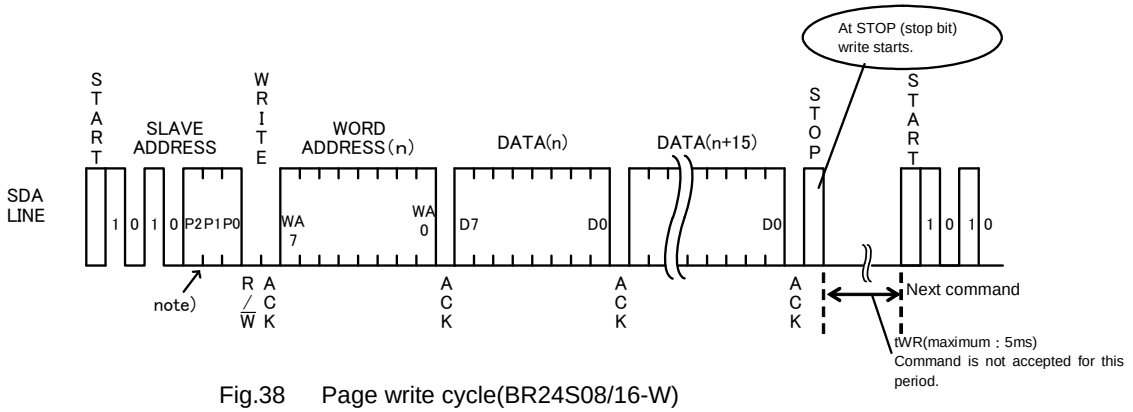
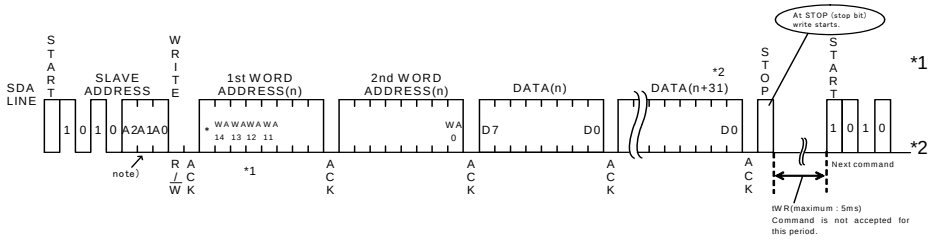



Fig.38 Page write cycle(BR24S08/16-W)




*1 As for WA12, BR24S32-W becomes Don't care.
As for WA13, BR24S32/64-W becomes Don't care.
As for WA14, BR24S32/64/128-W becomes Don't care.

*2 As for BR24S128/256-W becomes (n+63).

Fig.39 Page write cycle(BR24S32/64/128/256-W)

○Notes on page write cycle

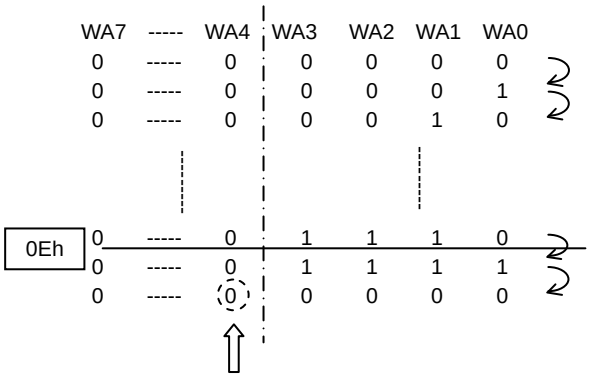
List of numbers of page write

| Number of pages | 16Byte | 32Byte | 64Byte |
|---|---|---|---|
| Product number | BR24S08-W<br>BR24S16-W | BR24S32-W<br>BR24S64-W | BR24S128-W<br>BR24S256-W |

The above numbers are maximum bytes for respective types. Any bytes below these can be written.
In the case of BR24S256-W, 1 page = 64bytes, but the page write cycle write time is 5ms at maximum for 64byte bulk write.
It does not stand 5ms at maximum × 64byte = 320ms(Max.).

○Internal address increment

Page write mode (in the case of BR24S16-W)




Significant bit is fixed.
No digit up

For example, when it is started from address 0Eh, therefore, increment is made as below,
0Eh→0Fh→00h→01h･･･, which please note.

* 0Eh･･･16 in hexadecimal, therefore, 00001110 becomes a binary number.

○Write protect (WP) terminal

・Write protect (WP) function

When WP terminal is set Vcc (H level), data rewrite of all address is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.
At extremely low voltage at power ON/OFF, by setting the WP terminal 'H', mistake write can be prevented.
During tWR, set the WP terminal always to 'L'. If it is set 'H', write is forcibly terminated.

## ●Read Command

### ○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.
Random read cycle is a command to read data by designating address, and is used generally.
Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.

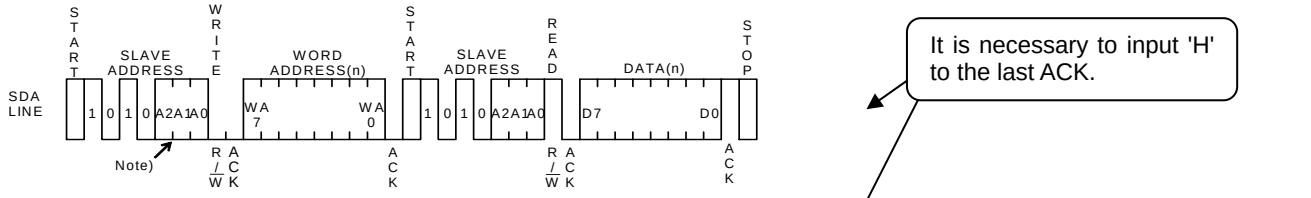



Fig.40 Random read cycle (BR24S08/16-W)

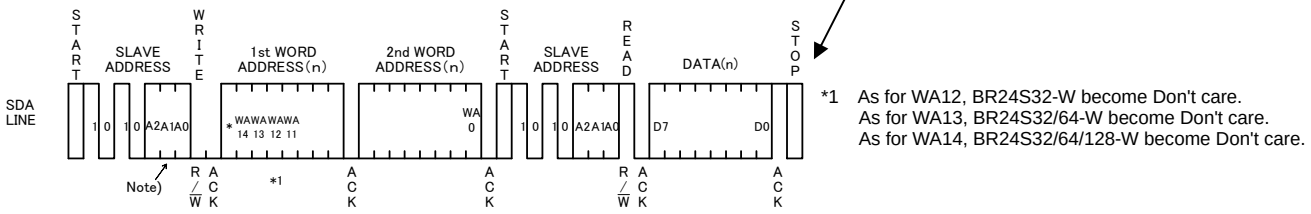



Fig.41 Random read cycle (BR24S32/64/128/256-W)

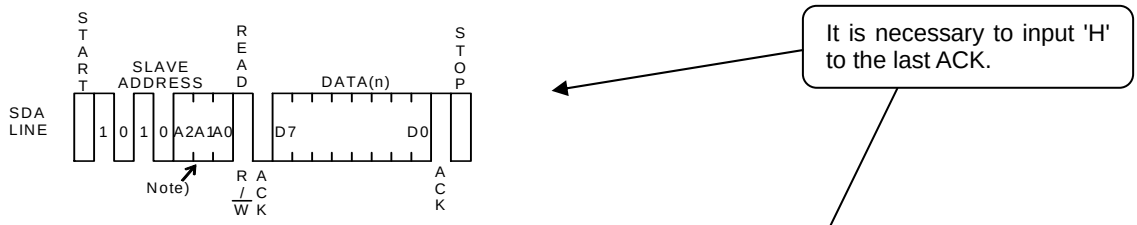



Fig.42 Current read cycle

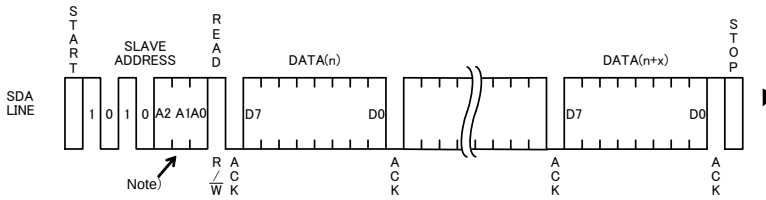
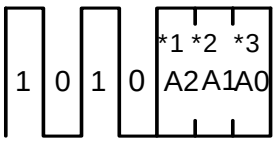



Fig.43 Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master ($\mu$-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H'.
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

Note)




*1 BR24S16-W A2 becomes P2.
*2 BR24S08/16-W A1 becomes P1.
*3 BR24S08/16-W A0 becomes P0.

Fig.44 Difference of slave address of each type

**●Software reset**

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kids of them are shown in the figure below. (Refer to Fig.45(a), Fig.45(b), Fig.45(c).) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

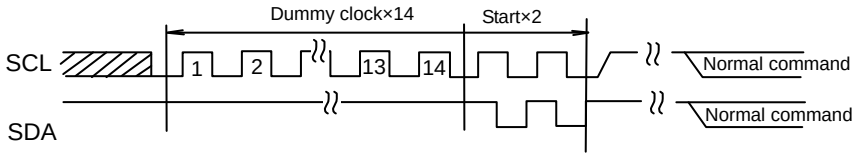



Fig.45-(a) The case of 14 Dummy clock + START + START+ command input

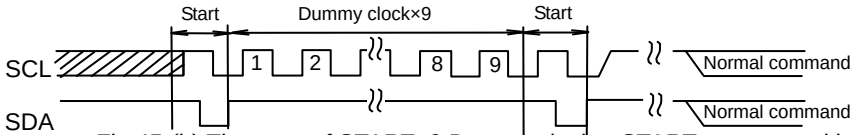
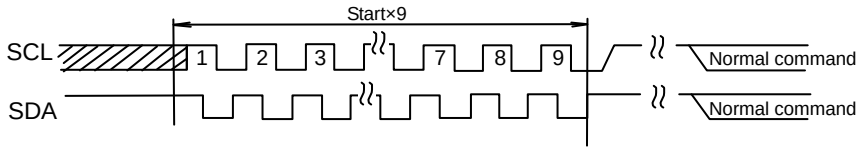



Fig.45-(b) The case of START+9 Dummy clock + START + command input




* Start command from START input.

Fig.45-(c) START × 9 + command input

**●Acknowledge polling**

During internal write, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, R/$\overline{W}$ = 0, when to carry out current read cycle after write, slave address R/$\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data so forth.

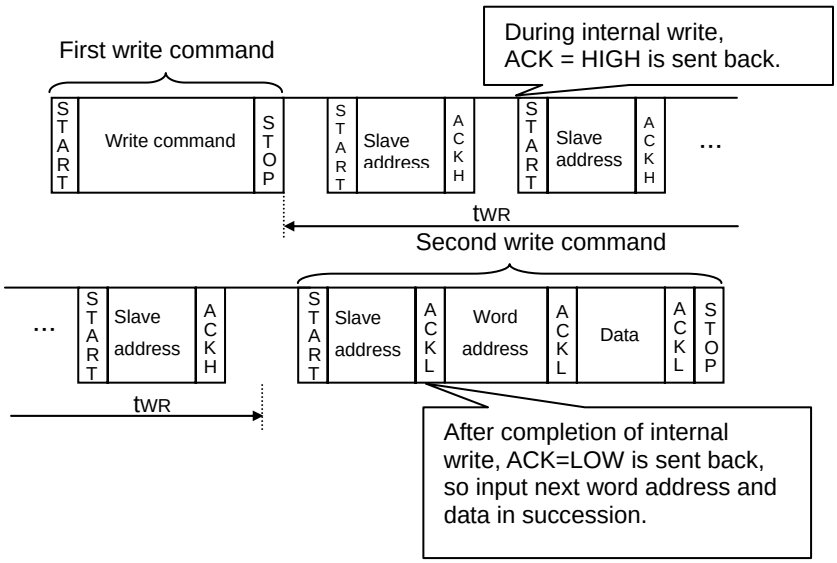



Fig.46 Case to continuously write by acknowledge polling

**●WP valid timing (write cancel)**

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.

WP input in this area becomes Don't care. Set the setup time to rise of D0 taken 100ns or more. The area from the rise of SCL to take in D0 to the end of internal automatic write (tWR) is cancel valid area. And, when it is set WP='H' during tWR, write is ended forcibly, data of address under access is not guaranteed, therefore, write it once again.(Refer to Fig.47.) After execution of forced end by WP standby status gets in, so there is no need to wait for tWR (5ms at maximum).

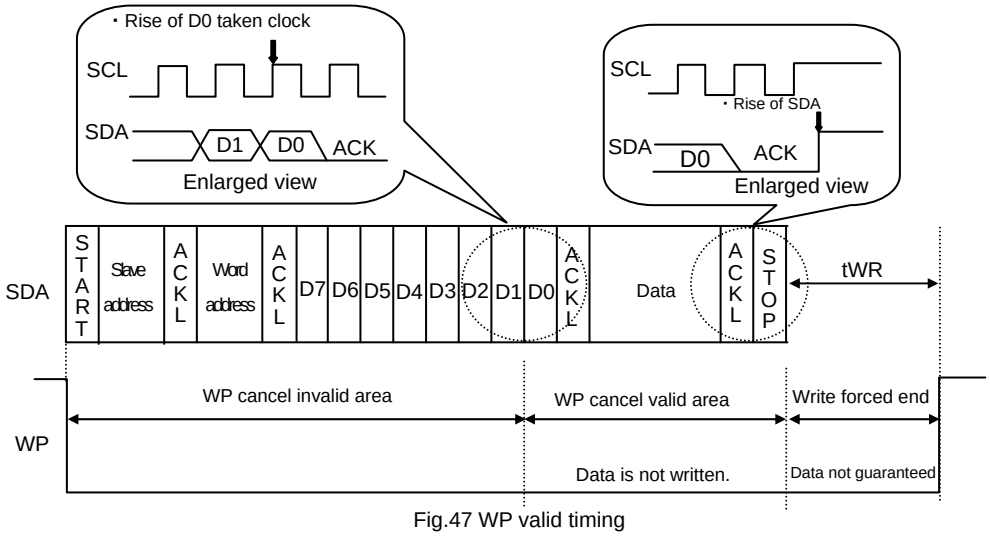



Fig.47 WP valid timing

**●Command cancel by start condition and stop condition**

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Refer to Fig. 48.)

However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

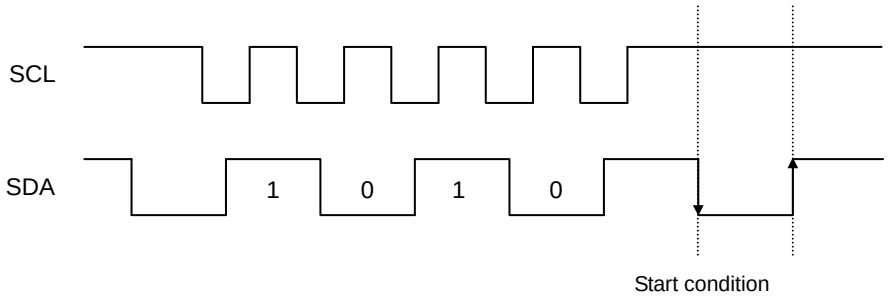



Fig.48 Case of cancel by start, stop condition during slave address input

## ●I/O peripheral circuit

### ○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value ($R_{PU}$), select an appropriate value to this resistance value from microcontroller $V_{IL}$, $I_L$, and $V_{OL}$-$I_{OL}$ characteristics of this IC. If $R_{PU}$ is large, action frequency is limited. The smaller the $R_{PU}$, the larger the consumption current at action.

### ○Maximum value of $R_{PU}$

The maximum value of $R_{PU}$ is determined by the following factors.

(1)SDA rise time to be determined by the capacitance (CBUS) of bus line of $R_{PU}$ and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by input leak total ($I_L$) of device connected to bus output of 'H' to SDA bus and $R_{PU}$ should sufficiently secure the input 'H' level ($V_{IH}$) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$Vcc - I_L R_{PU} - 0.2Vcc \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8Vcc - V_{IH}}{I_L}$$

Ex.) When Vcc = 3V, $I_L$=10μA, $V_{IH}$ = 0.7Vcc

from(2)

$$R_{PU} \leqq \frac{0.8\times3 - 0.7\times3}{10\times10^{-6}}$$

$$\leqq 300 \ [k\Omega]$$

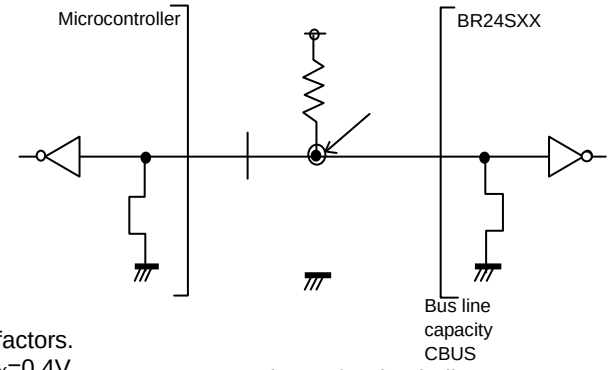



Fig.49 I/O circuit diagram

### ○Minimum value of $R_{PU}$

The minimum value of $R_{PU}$ is determined by the following factors.

(1)When IC outputs LOW, it should be satisfied that $V_{OLMAX}$=0.4V and $I_{OLMAX}$=3mA.

$$\frac{Vcc - V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{Vcc - V_{OL}}{I_{OL}}$$

(2)$V_{OLMAX}$=0.4V should secure the input 'L' level ($V_{IL}$) of microcontroller and EEPROM including recommended noise margin 0.1Vcc.

$$V_{OLMAX} \leqq V_{IL}\text{-}0.1\ Vcc$$

Ex.) When Vcc= 3V, $V_{OL}$0.4V, $I_{OL}$=3mA, microcontroller, EEPROM $V_{IL}$=0.3Vcc

from(1),

$$R_{PU} \geqq \frac{3-0.4}{3\times10}$$

$$\geqq 867 \quad [\Omega]$$

And

$V_{OL}$=0.4 [V]

$V_{IL}$=0.3×3

=0.9 [V]

Therefore, the condition (2) is satisfied.

### ○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ ~ several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

## ●A0, A1, A2, WP process

### ○Process of device address terminals (A0,A1,A2)

Check whether the set device address coincides with device address input sent from the master side or not, and select one among plural devices connected to a same bus. Connect this terminal to pull up or pull down, or Vcc or GND. And, pins(Don't use PIN) not used as device address may be set to any of 'H' , 'L', and 'Hi-Z'.

| | | |
|---|---|---|
| Types with Don't use PIN | BR24S08F/FJ/FV/FVT/FVM/FVJ/NUX-W | A0, A1 |
| | BR24S16F/FJ/FV/FVT/FVM/FVJ/NUX-W | A0, A1, A2 |

### ○Process of WP terminal

WP terminal is the terminal that prohibits and permits write in hardware manner. In 'H' status, only READ is available and WRITE of all address is prohibited. In the case of 'L', both are available. In the case of use it as an ROM, it is recommended to connect it to pull up or Vcc. In the case to use both READ and WRITE, control WP terminal or connect it to pull down or GND.

**●Cautions on microcontroller connection**

○Rs

In $I^2C$ BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

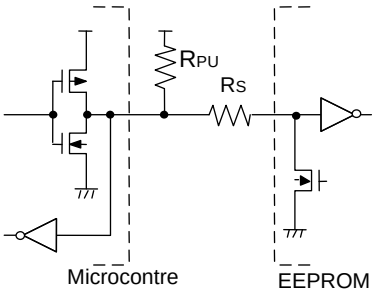
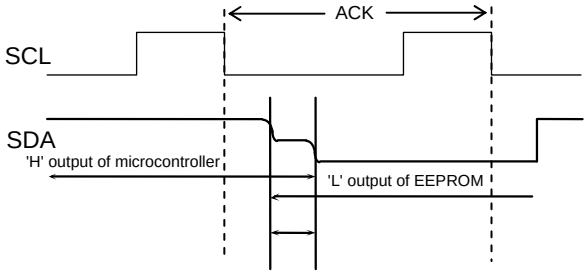



Fig.50 I/O circuit diagram




Over current flows to SDA line by 'H' output of microcontroller and 'L' output of EEPROM.

Fig.51 Input/output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by following relations.

(1)SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA shoulder be tR or below.
And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level ($V_{IL}$) of microcontroller including recommended noise margin 0.1Vcc.

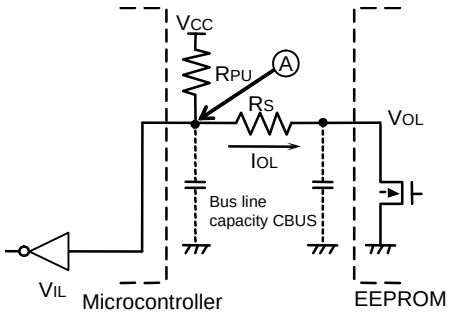



Fig.52 I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example） When $V_{CC}$=3V, $V_{IL}$=0.3$V_{CC}$, $V_{OL}$=0.4V, $R_{PU}$=20kΩ

$$\text{from(2)}, \quad R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67\ [k\Omega]$$

○Maximum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

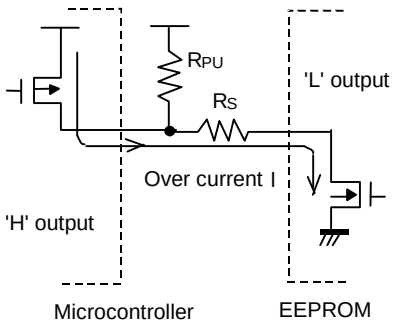



Fig.53 I/O circuit diagram

$$\frac{V_{CC}}{RS} \leqq I$$

$$\therefore \quad RS \geqq \frac{V_{CC}}{I}$$

Example） When $V_{CC}$=3V, I=10mA

$$RS \geqq \frac{3}{10\times10\text{-}3}$$

## ●I²C BUS input / output circuit

○Input (A0, A1, A2, SCL, WP)

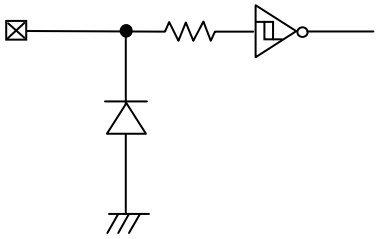


Fig.54 Input pin circuit diagram

○Input/Output (SDA)

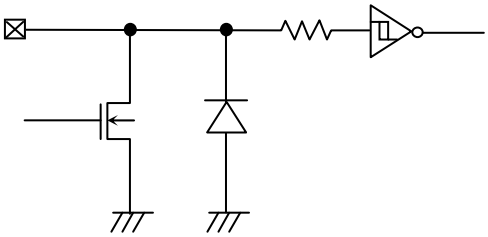


Fig.55 Input /output pin circuit diagram

## ●Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following condition at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of tR, tOFF, and Vbot for operating POR circuit.

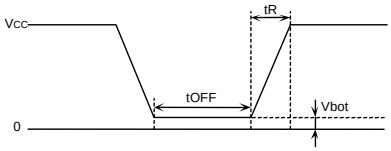



Fig.56 Rise waveform diagram

Recommended conditions of tR,tOFF,Vbot

| tR | tOFF | Vbot |
|---|---|---|
| 10ms or below | 10ms or longer | 0.3V or below |
| 100ms or below | 10ms or longer | 0.2V or below |

3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

a) In the case when the above conditions 1 cannot be observed. When SDA becomes 'L' at power on .

→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

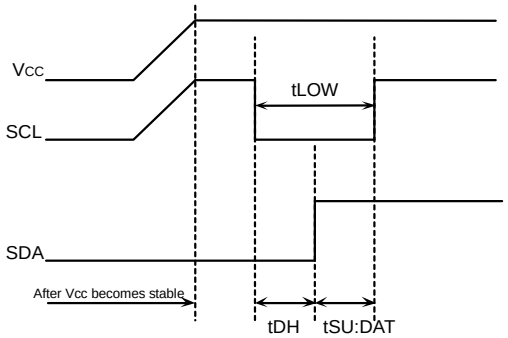



Fig.57 When SCL='H' and SDA='L'

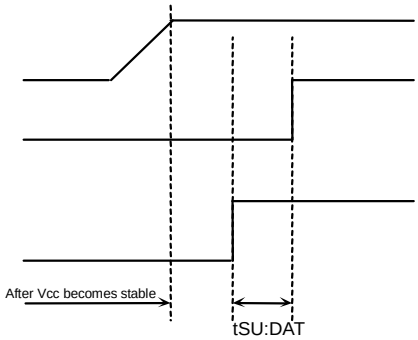



Fig.58 When SCL='H' and SDA='L'

b) In the case when the above condition 2 cannot be observed.

→After power source becomes stable, execute software reset(P26).

c) In the case when the above conditions 1 and 2 cannot be observed.

→Carry out a), and then carry out b).

**●Low voltage malfunction prevention function**

LVCC circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

**●Vcc noise countermeasures**

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

**●Notes for use**

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Terminal design

In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

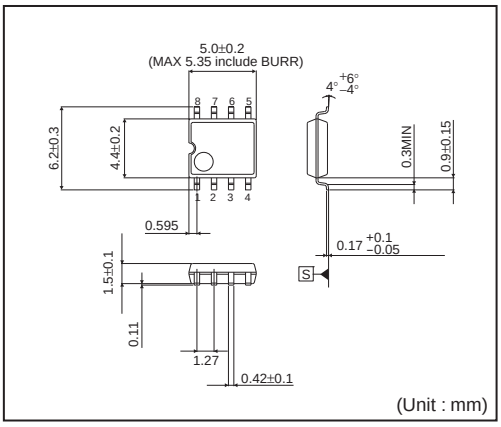
(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

## ●Ordering part number

| B R | 2 4 | S | 2 5 6 | F | - | W | E 2 |
|---|---|---|---|---|---|---|---|
| Part No. | BUS type<br>24 : $I^2C$ | Operating temperature/ Power source voltage<br>L: -40℃~+85℃/ 1.8V ~ 5.5V<br>S: -40℃~+85℃/ 1.7V ~ 5.5V | Capacity<br>01=1K 16=16K<br>02=2K 32=32K<br>04=4K 64=64K<br>08=8K 128=128K<br>256=256K | Package<br>F : SOP8<br>FJ : SOP-J8<br>FV : SSOP-B8<br>FVM : MSOP8<br>FVT :TSSOP-B8<br>FVJ :TSSOP-B8J<br>NUX : VSON008X2030 | | Double cell | Packaging and forming specification<br>E2: Embossed tape and reel<br>TR: Embossed tape and reel |

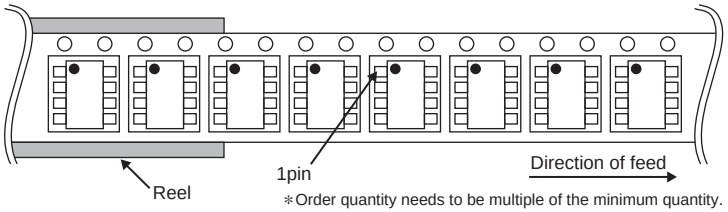
## ●Package specifications

### SOP8



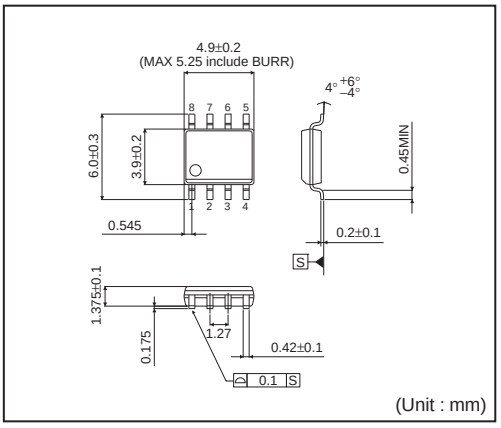

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



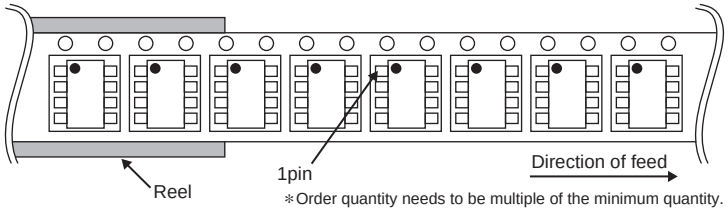

∗Order quantity needs to be multiple of the minimum quantity.

### SOP-J8



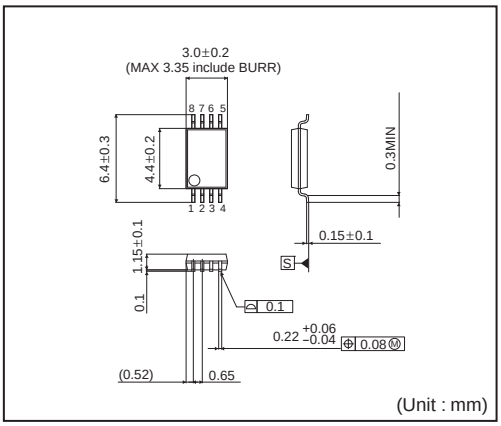

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



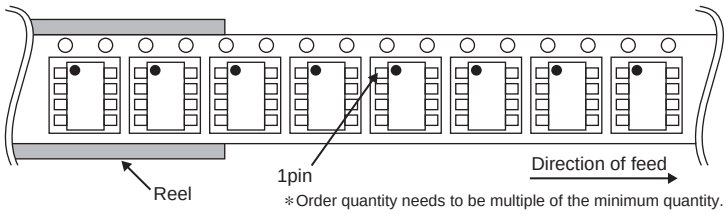

∗Order quantity needs to be multiple of the minimum quantity.

### SSOP-B8



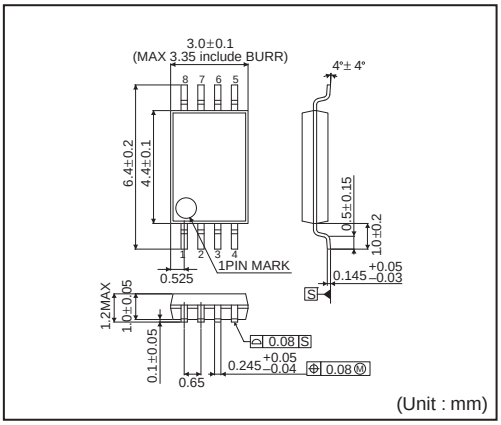

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



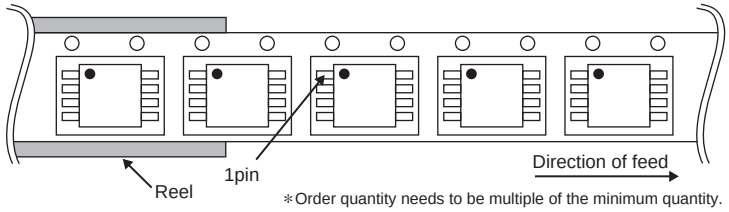

∗Order quantity needs to be multiple of the minimum quantity.

### TSSOP-B8



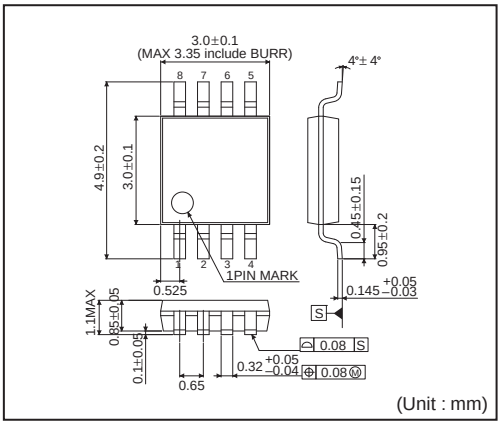

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



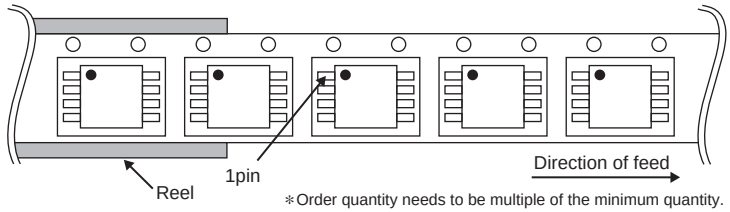

∗Order quantity needs to be multiple of the minimum quantity.

### TSSOP-B8J



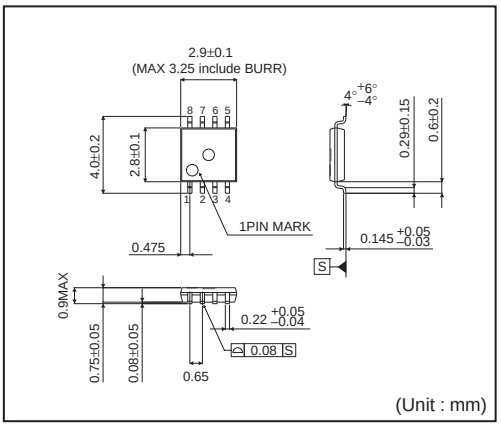

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



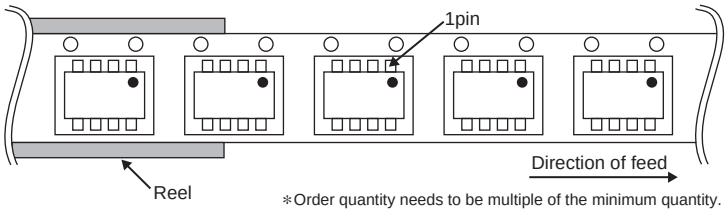

∗Order quantity needs to be multiple of the minimum quantity.

### MSOP8



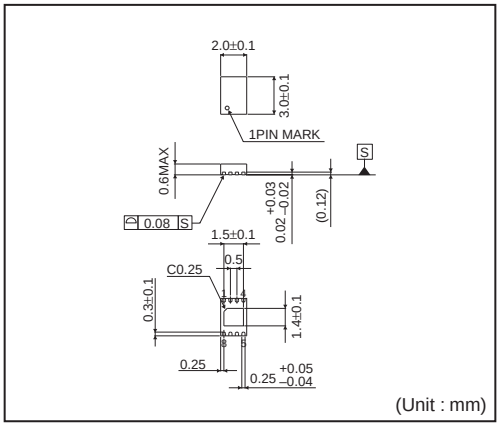

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |



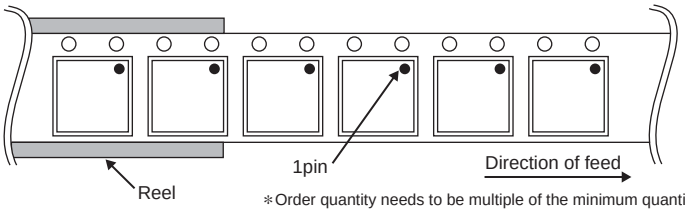

∗Order quantity needs to be multiple of the minimum quantity.

### VSON008X2030




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 4000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.

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