

# IS31FL3730

## AUDIO MODULATED MATRIX LED DRIVER

December 2011

### GENERAL DESCRIPTION

IS31FL3730 is a LED matrix driver which features an audio modulation display mode and a general LED dot matrix display mode. The default configuration of IS31FL3730 is to drive a single 8×8 LED matrix. However, IS31FL3730 may be configured to drive either one or two 8×8, 7×9, 6×10, or 5×11 dot matrix display(s). The intensity of any matrix picture can be modulated by an audio signal.

In matrix display mode, the rows and columns of the matrix are internally scanned, requiring only one time programming of the individual LED on or off state, thus eliminating the need for real time system resource utilization to perform the row and column scanning function.

In the general purpose mode, the ON or OFF condition of each individual LED in the display matrix is programmed via an I2C interface.

IS31FL3730 is available in QFN-24 (4mm × 4mm). It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

### FEATURES

- 2.7V to 5.5V supply
- I2C interface, automatic address increment function
- Internal reset register
- Programmable single or dual 8×8, 7×9, 6×10, or 5×11 LED matrix display mode
- One-time programming, internal scan
- Audio modulated display intensity with digitally programmable input gain
- Internal registers to digitally adjust display intensity
- Modulate LED brightness with 128 different items in PWM
- One address pin with 4 logic levels to allow four I2C slave addresses
- Over-temperature protection
- QFN-24 (4mm × 4mm) package

### APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

### TYPICAL APPLICATION CIRCUIT

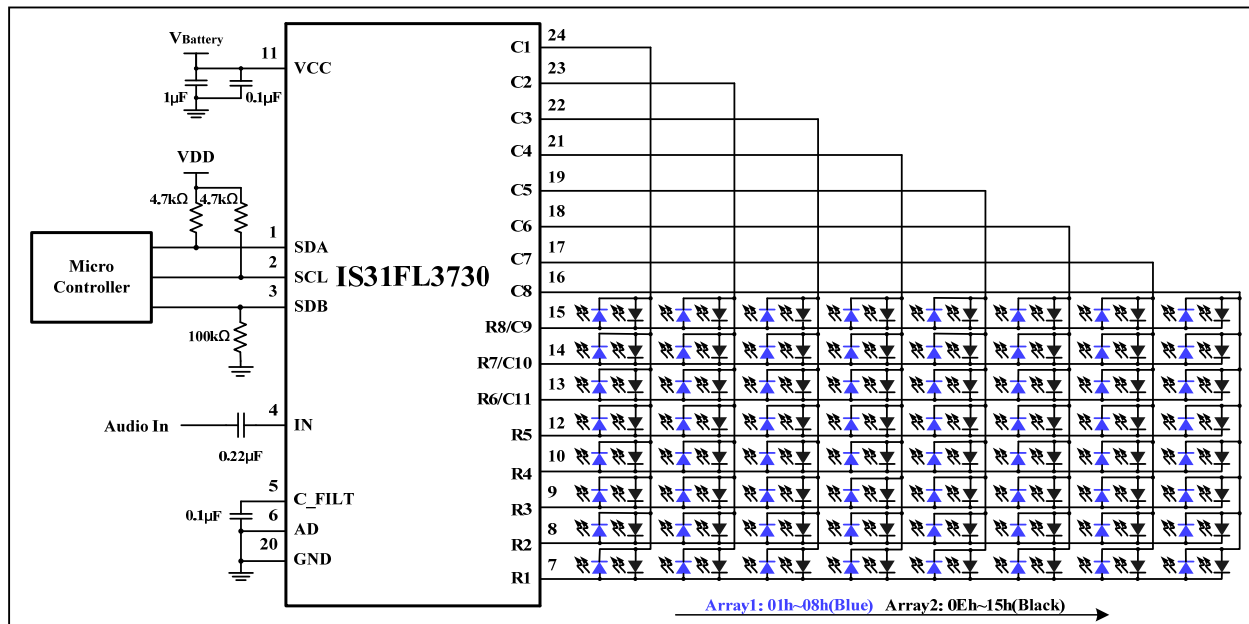


Figure 1 Typical Application Circuit Dual 8×8

**Note:** The IC should be placed far away from the mobile antenna in order to prevent the EMI.

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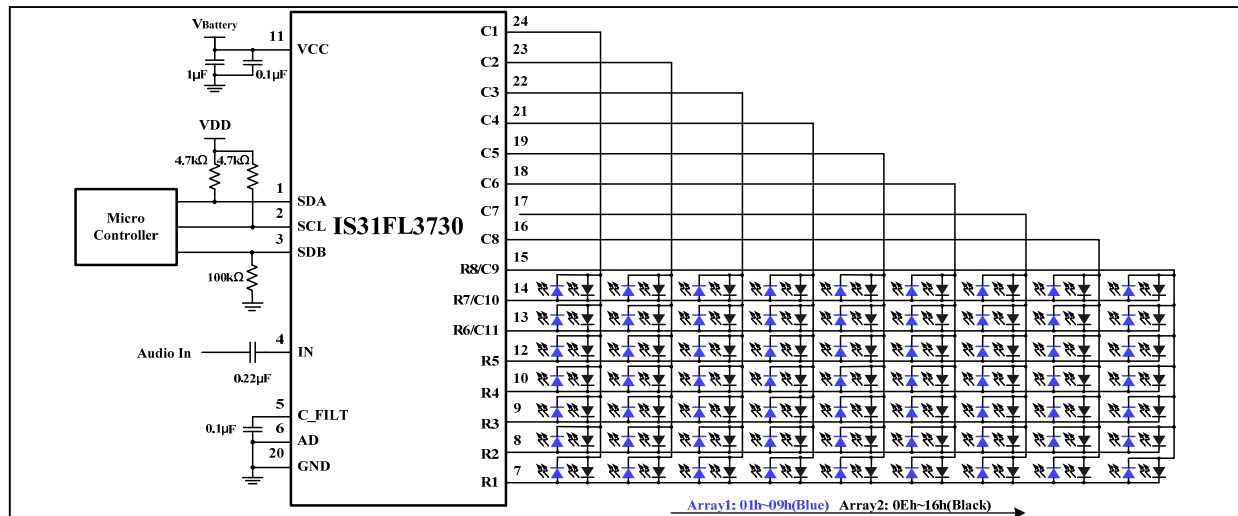


Figure 2 Typical Application Circuit Dual 7×9

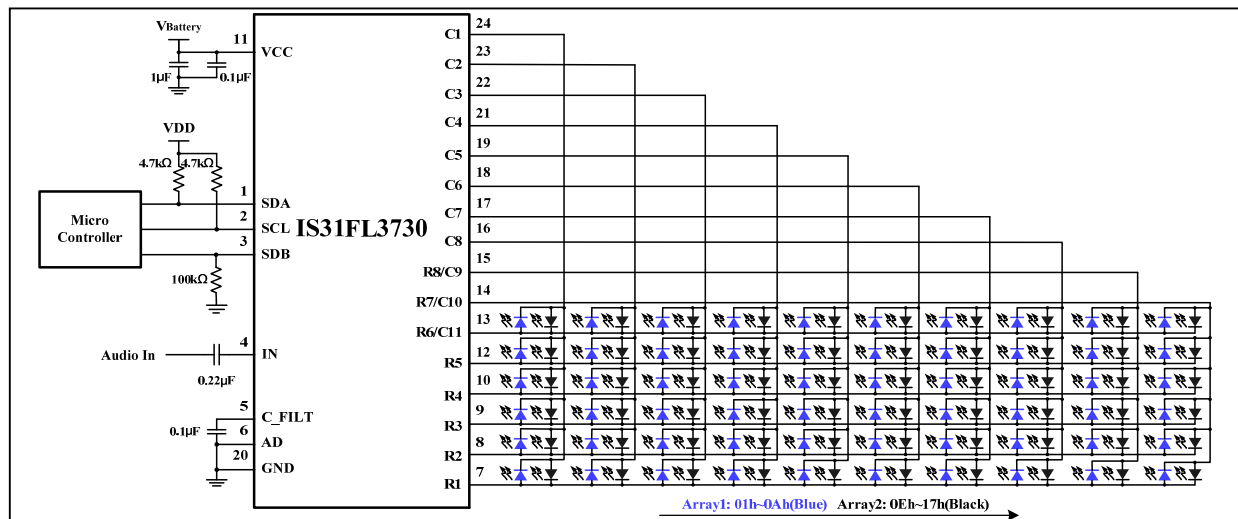


Figure 3 Typical Application Circuit Dual 6×10

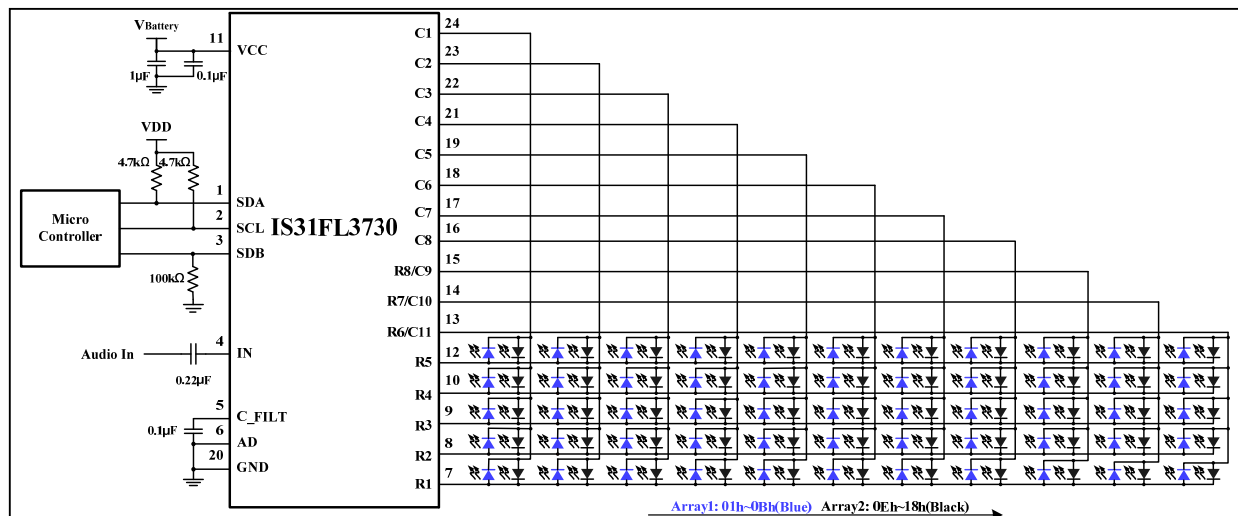
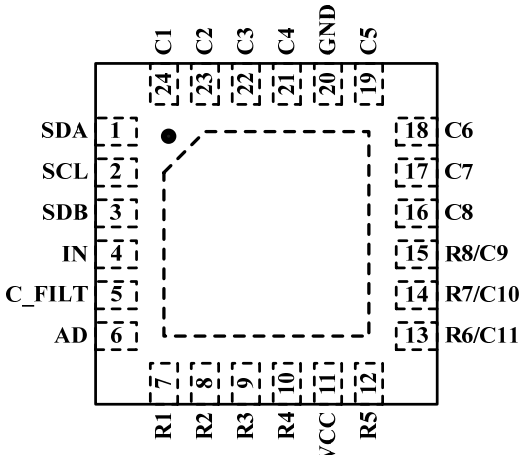


Figure 4 Typical Application Circuit Dual 5×11

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## PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	

## PIN DESCRIPTION

No.	Pin	Description
1	SDA	I2C serial data.
2	SCL	I2C serial clock.
3	SDB	Shutdown the chip when pull to low.
4	IN	Audio input.
5	C_FILT	Filter cap for audio control.
6	AD	I2C address setting.
7~10, 12	R1~R5	Row control.
11	VCC	Power supply.
13~15	R6/C11, R7/C10, R8/C9	Row/column control.
16~19, 21~24	C8~C5, C4~C1	Column control.
20	GND	Ground.
	Thermal Pad	Connect to GND.

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# IS31FL3730

## ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3730-QFLS2-TR	QFN-24, Lead-free	2500

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## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{CC}+0.3V$
Maximum junction temperature, $T_{JMAX}$	150°C
Storage temperature range, $T_{STG}$	-65°C ~ +150°C
Operating temperature range, $T_A$	-40°C ~ +85°C

### Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted. Typical value are  $T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = 3.6\text{V}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply voltage		2.7		5.5	V
$I_{CC}$	Quiescent power supply current	$V_{IN} = 0V$ , without audio input, all LEDs off		7.0		mA
$I_{SD}$	Shutdown current	$V_{SDB} = 0V$		0.2	1.0	$\mu\text{A}$
		$V_{SDB} = V_{CC}$ , software shutdown		1.7	3.0	
$I_{OUT}$	Output current of R1~R8, C1~C8	Matrix display mode without audio modulation Lighting Effect Register(0Dh) = 0xxx 0000		40 (Note 1)		mA
		Matrix display mode with audio modulation $V_{IN} = 2.5V_{P-P}$ , 1kHz square wave Audio Gain = 0dB		40 (Note 1)		
$V_{HR}$	Current sink headroom voltage R1~R8, C1~C8	$I_{sink} = 320\text{mA}$ (Note 2)		300		mV
	Current source headroom voltage R1~R8, C1~C8	$I_{source} = 40\text{mA}$		200		
$t_{SCAN}$	Period of row and column scanning (Figure 10)			32		$\mu\text{s}$
$t_{SCANOL}$	Non-overlap blanking time during row and column scan (Figure 10)			1		$\mu\text{s}$

## Logic Electrical Characteristics (SDA, SCL, AD)

$V_{IL}$	Logic "0" input voltage	$V_{CC} = 2.7V$			0.4	V
$V_{IH}$	Logic "1" input voltage	$V_{CC} = 5.5V$	1.4			V
$I_{IL}$	Logic "0" input current	$V_{IN} = 0V$		5 (Note 3)		nA
$I_{IH}$	Logic "1" input current	$V_{IN} = V_{CC}$		5 (Note 3)		nA

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## DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{SCL}$	Serial-Clock frequency				400	kHz
$t_{BUF}$	Bus free time between a STOP and a START condition		1.3			$\mu s$
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			$\mu s$
$t_{SU, STA}$	Repeated START condition setup time		0.6			$\mu s$
$t_{SU, STO}$	STOP condition setup time		0.6			$\mu s$
$t_{HD, DAT}$	Data hold time				0.9	$\mu s$
$t_{SU, DAT}$	Data setup time		100			ns
$t_{LOW}$	SCL clock low period		1.3			$\mu s$
$t_{HIGH}$	SCL clock high period		0.7			$\mu s$
$t_R$	Rise time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns
$t_F$	Fall time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns

**Note 1:** Due to the row and column scanning sequence, the average current of an individual LED in the display is  $I_{OUT}/8$  when configured to drive a single matrix. When configured to drive two matrices, the average current of an individual LED in the display is  $I_{OUT}/16$ .

**Note 2:** All row drivers are on.

**Note 3:** Guaranteed by design.

**Note 4:** Cb = total capacitance of one bus line in pF.  $I_{SINK} \leq 6mA$ .  $t_R$  and  $t_F$  measured between  $0.3 \times V_{CC}$  and  $0.7 \times V_{CC}$ .



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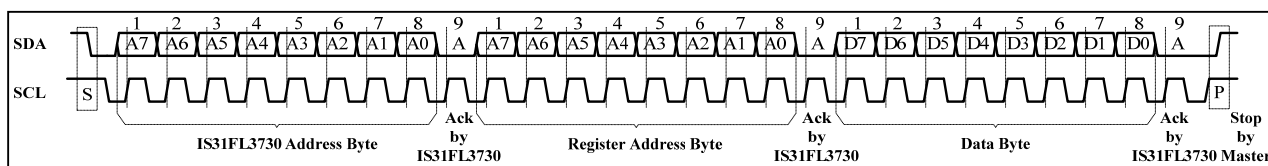


Figure 7 Writing to IS31FL3730(Typical)

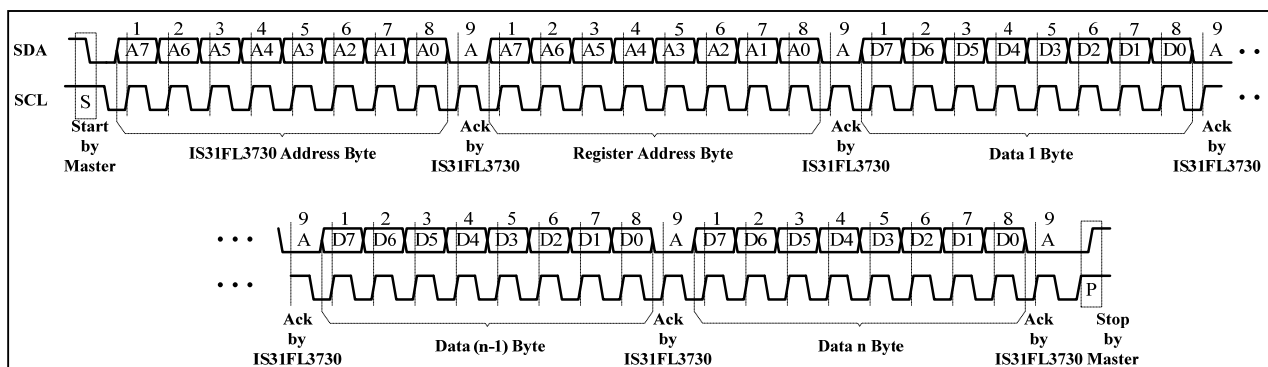


Figure 8 Writing to IS31FL3730(Automatic Address Increment)

## REGISTER DEFINITION

Table2 Register Function

Address	Name	Function	Table	Default
00h	Configuration Register	Set operation mode of IS31FL3730	3	0000 0000
01h~0Bh	Matrix 1 Data Register	Store the on or off state of each LED	4	0000 0000
0Eh~18h	Matrix 2 Data Register	Store the on or off state of each LED	5	
0Ch	Update Column Register	Make the Data Register update the data	-	xxxx xxxx
0Dh	Lighting Effect Register	Store the intensity control settings	6	0000 0000
19h	PWM Register	Modulate LED light with 128 different items	7	1000 0000
FFh	Reset Register	Reset all registers to default value	-	xxxx xxxx

Table3 00h Configuration Register

Bit	D7	D6:D5	D4:D3	D2	D1	D0
Name	SSD	Reserved	DM	A_EN	ADM	
Default	0	00	00	0	0	0

The Configuration Register sets operation mode of IS31FL3730.

**SSD** Software Shutdown Enable  
 0 Normal operation  
 1 Software shutdown mode

**DM** Display Mode  
 00 Matrix 1 only  
 01 Matrix 2 only  
 11 Matrix 1 and Matrix 2

**A\_EN** Audio Input Enable  
 0 Matrix intensity is controlled by the current setting in the Lighting Effect Register (0Dh)  
 1 Enable audio signal to modulate the intensity of the matrix

**ADM** Matrix Mode Selection  
 00 8×8 dot matrix display mode  
 01 7×9 dot matrix display mode  
 10 6×10 dot matrix display mode  
 11 5×11 dot matrix display mode



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**Table4 01h~0Bh Matrix 1 Data Register(C1~C11)**

Bit	D7:D0
Name	R8:R1
Default	00000000

**Table5 0Eh~18h Matrix 2 Data Register(C1~C11)**

Bit	D7:D0
Name	R8:R1
Default	00000000

The Data Registers (Matrix 1/Matrix 2) store the on or off state of each LED in the Matrix.

**Rx** LED State

0 LED off

1 LED on

11×2 registers are assigned to C1~C11 columns respectively; the LED at a particular (row, column) location will be turned on when the respective data is set to “1”. When configured for more than 8 column operation, only the required numbers of LSBs are used in each data register. For example, in 5×11 dot matrix mode, only bits R1 thru R5 are used, and bits R6 thru R8 are ignored.

## 0Ch Update Column Register

The data sent to the Data Registers will be stored in temporary registers. A write operation of any 8-bit value to the Update Column Register is required to update the Data Registers (01h~0Bh, 0Eh~18h).

**Table6 0Dh Lighting Effect Register**

Bit	D7	D6:D4	D3:D0
Name	Reserved	AGS	CS
Default	0	000	0000

The Lighting Effect Register stores the intensity control settings for all of the LEDs in the Matrix.

**AGS** Audio Input Gain Selection

000: Gain= 0dB

001: Gain= +3dB

010: Gain= +6dB

011: Gain= +9dB

100: Gain= +12dB

101: Gain= +15dB

110: Gain= +18dB

111: Gain= -6dB

**CS** Full Current Setting for Each Row Output

0000: 40mA

0001: 45mA

... ..

0111: 75mA

1000: 5mA

1001: 10mA

... ..

1110: 35mA

**Table7 19h PWM Register**

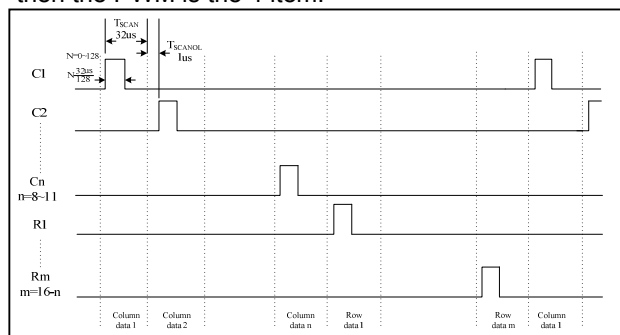
Bit	D7	D6:D0
Default	1	0000000

The PWM Register can modulate LED light with 128 different items.

When the D7 set to “1”, the PWM is the 128 item.

When the D7 set to “0”, D6:D0 set the PWM from the 0 item to the 127 item.

For example, if the data in PWM Register is 0000 0100, then the PWM is the 4 item.



**Figure 9** PWM Timing Diagram

## FFh Reset Register

Once user writes any 8-bit data to the Reset Register, IS31FL3730 will reset all registers to default value. On initial power-up, the IS31FL3730 registers are reset to their default values for a blank display.

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## APPLICATION INFORMATION

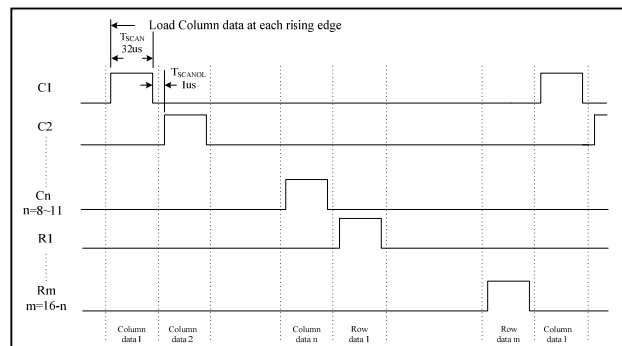
### GENERAL PURPOSE DOT MATRIX DISPLAY MODE

The general purpose dot matrix display timing diagram is shown in Figure 10. IS31FL3730 may be configured to drive displays of different dimensions from 8×8 to 5×11. Furthermore, IS31FL3730 may be configured to drive one or two LED matrices of the same dimension. Therefore, the overall row and column scan time can vary based on the final LED matrix configuration.

In any LED matrix configuration, a single line (column or row) of LEDs is illuminated for 32μs before IS31FL3730 moves on to the next line of LEDs (Figure 10).

**Example 1:** When the IS31FL3730 is configured in the general purpose dual 8×8 dot matrix display mode, column controls C8:C1 scans the eight columns of Matrix 1 then row controls R8:R1 scans the eight rows of Matrix 2 at a rate of 1.89kHz, or 528μs per frame. Each line is active for 32μs. The non-overlap interval between adjacent lines is 1μs.

**Example 2:** When configured to drive a single 7×9 dot matrix display (Matrix 1), the column controls C9:C1 scan the nine columns every 297μs. Also note that in this case, the Data Registers' MSB will be ignored.



**Figure 10** Dot Matrix Display Timing Diagram

### DUAL 8×8 DOT MATRIX DISPLAY MODE

The application example in Figure 1 shows the IS31FL3730 in the dual 8×8 LED dot matrix display mode.

The Matrix 1 LED columns have common cathodes and are connected to the C1:C8 outputs. The rows are connected to the row drivers. The Matrix 2 LED rows have common cathodes and connected to the R1:R8. The columns are connected to the C1:C8. Each of the 128 LEDs can be addressed separately.

### DUAL 5×11 DOT MATRIX DISPLAY MODE

By setting the ADM bits of the Configuration Register (00h) to “11” and the DM bits to “11”, the IS31FL3730 will operate in the dual 5×11 LED dot matrix display mode.

The Matrix 1 LED columns have common cathodes and are connected to the C1:C11 outputs. The rows are connected to the row drivers. The Matrix 2 LED rows have common cathodes and are connected to the R1:R5 outputs. The columns are connected to the column drivers. Each of the 110 LEDs can be addressed separately. The three MSBs (D7:D5) of each Data Register (01h~0Bh, 0Eh~18h) are ignored.

### DOT MATRIX DISPLAY MODE WITH AUDIO MODULATION

When the IS31FL3730 operates in any of the dot matrix modes, if the bit A\_EN in Configuration Register (00h) is set to “1”, the brightness of LED image can be modulated by audio signal not controlled by the CS bit in Lighting Effect Register (0Dh).

An external capacitor, C\_FILT is required to control the rate at which the display intensity will change. The rate of change is computed using the formula:  $\Delta T = C \times 500k\Omega$ . A value of 0.1μF provides a good effect by allowing the display to fade from full intensity to off in approximately 50ms. Smaller capacitance will cause the intensity to change more quickly, and, conversely, a larger capacitance will cause the display intensity to change at a slower rate.

### SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

### SOFTWARE SHUTDOWN

By setting SSD bit of the Configuration Register (00h) to “1”, the IS31FL3730 will operate in software shutdown mode, wherein they consume only 1.7μA (Typ.) current. When the IS31FL3730 is in software shutdown mode, all current sources and digital drivers are switched off, so that the matrix is blanked.

### HARDWARE SHUTDOWN

The chip enters hardware shutdown mode when the SDB pin is pulled low.

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## CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
<b>Preheat &amp; Soak</b>	
Temperature min (T <sub>smin</sub> )	150°C
Temperature max (T <sub>smax</sub> )	200°C
Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> )	217°C
Time at liquidous (t <sub>L</sub> )	60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

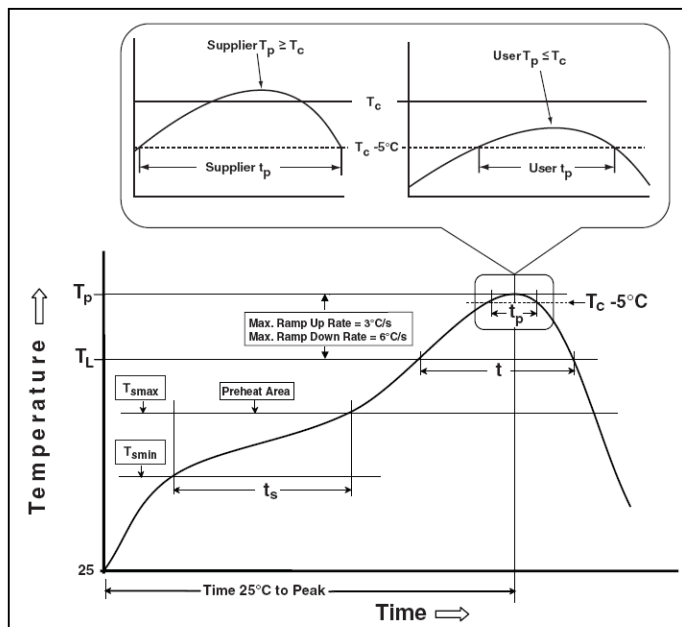
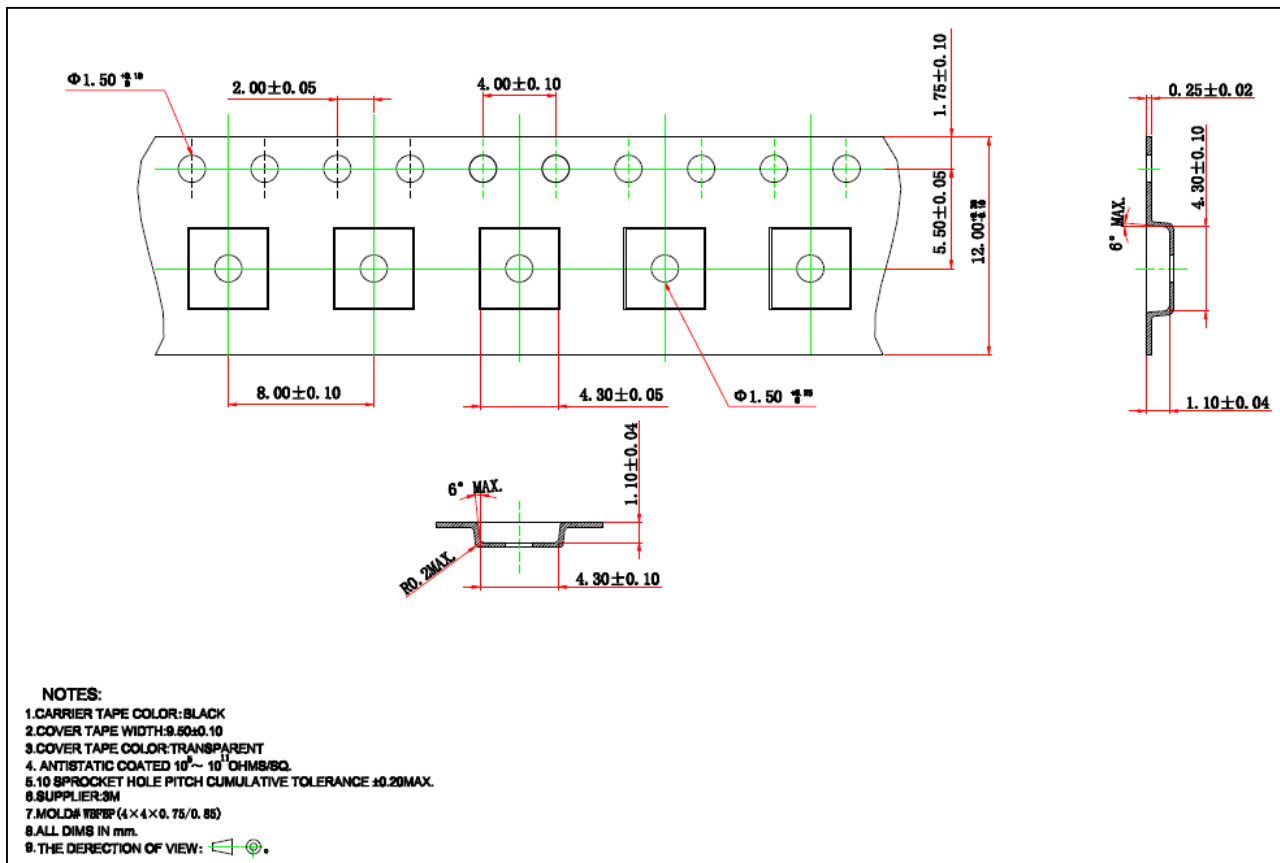


Figure 11 Classification profile

# IS31FL3730

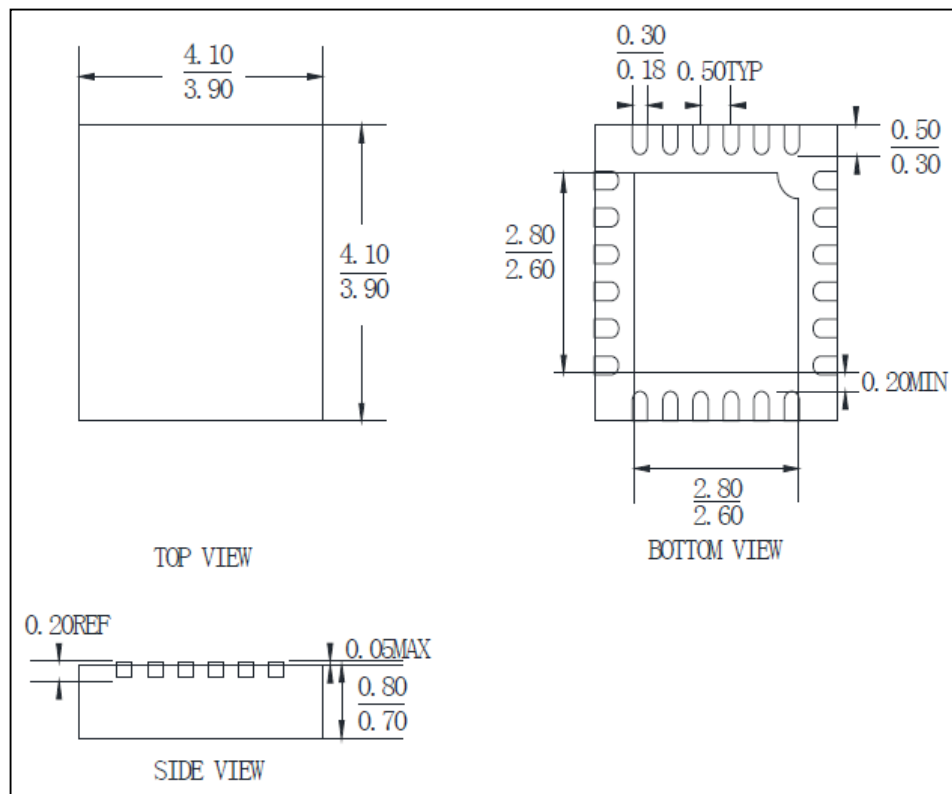
## TAPE AND REEL INFORMATION



# IS31FL3730

## PACKAGE INFORMATION

### QFN-24



**Note:** All dimensions in millimeters unless otherwise stated.

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