NCL30030

Combination Power Factor Correction and Quasi-Resonant Flyback Controllers for LED Lighting

This combination IC integrates power factor correction (PFC) and quasi−resonant flyback functionality necessary to implement a compact and highly efficient LED driver for high performance LED lighting applications.

The PFC stage utilizes a proprietary multiplier architecture to achieve low harmonic distortion and near−unity power factor while operating in a Critical Conduction Mode (CrM). The circuit incorporates all the features necessary for building a robust and compact PFC stage while minimizing the number of external components.

The quasi−resonant current−mode flyback stage features a proprietary valley−lockout circuitry, ensuring stable valley switching. This system works down to the 4th valley and toggles to a frequency foldback mode with a minimum frequency clamp beyond the 4th valley to eliminate audible noise. Skip mode operation allows excellent efficiency in light load conditions while consuming very low standby power consumption.

Common General Features

- Wide V_{CC} Range from 9 V to 30 V with Built−in Overvoltage Protection
- High−Voltage Startup Circuit
- Integrated High−Voltage Brown−Out Detector
- Fault Input for Severe Fault Conditions, NTC Compatible (Latch and Auto−Recovery Options)
- 0.5 A / 0.8 A Source / Sink Gate Drivers
- Internal Temperature Shutdown

PFC Controller Features

- Critical Conduction Mode with a Multiplier
- Accurate Overvoltage Protection
- Optional Bi−Level Line−Dependent Output Voltage (2:1 / 1.77:1 Versions)
- Fast Line / Load Transient Compensation
- Boost Diode Short−Circuit Protection
- Feed−Forward for Improved Operation across Line and Load
- Adjustable PFC Disable Threshold Based on Output Power

QR Flyback Controller Features

- Valley Switching Operation with Valley−Lockout for Noise−Free Operation
- Frequency Foldback with Minimum Frequency Clamp for Highest Performance in Standby Mode
- Minimum Frequency Clamp Eliminates Audible Noise
- Timer−Based Overload Protection (Latched or Auto−Recovery options)
- Adjustable Overpower Protection
- Winding and Output Diode Short−Circuit Protection
- 4 ms Soft−Start Timer
- These are Pb−Free Devices

Typical Applications

- High Power LED Drivers
- Commercial LED ballasts
- LED Signage Power Supplies
- Adapters
- Open Frame Power Supplies
- LED Electronic Control Gear

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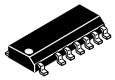
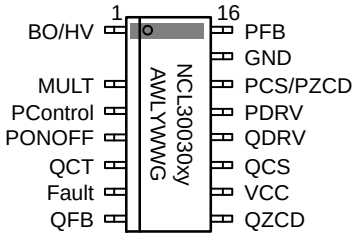


SOIC−16 NB MISSING PIN 2
CASE 751DT

MARKING DIAGRAM



NCL30030 = Specific Device Code
x = A or B
y = 1, 2 or 3
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.

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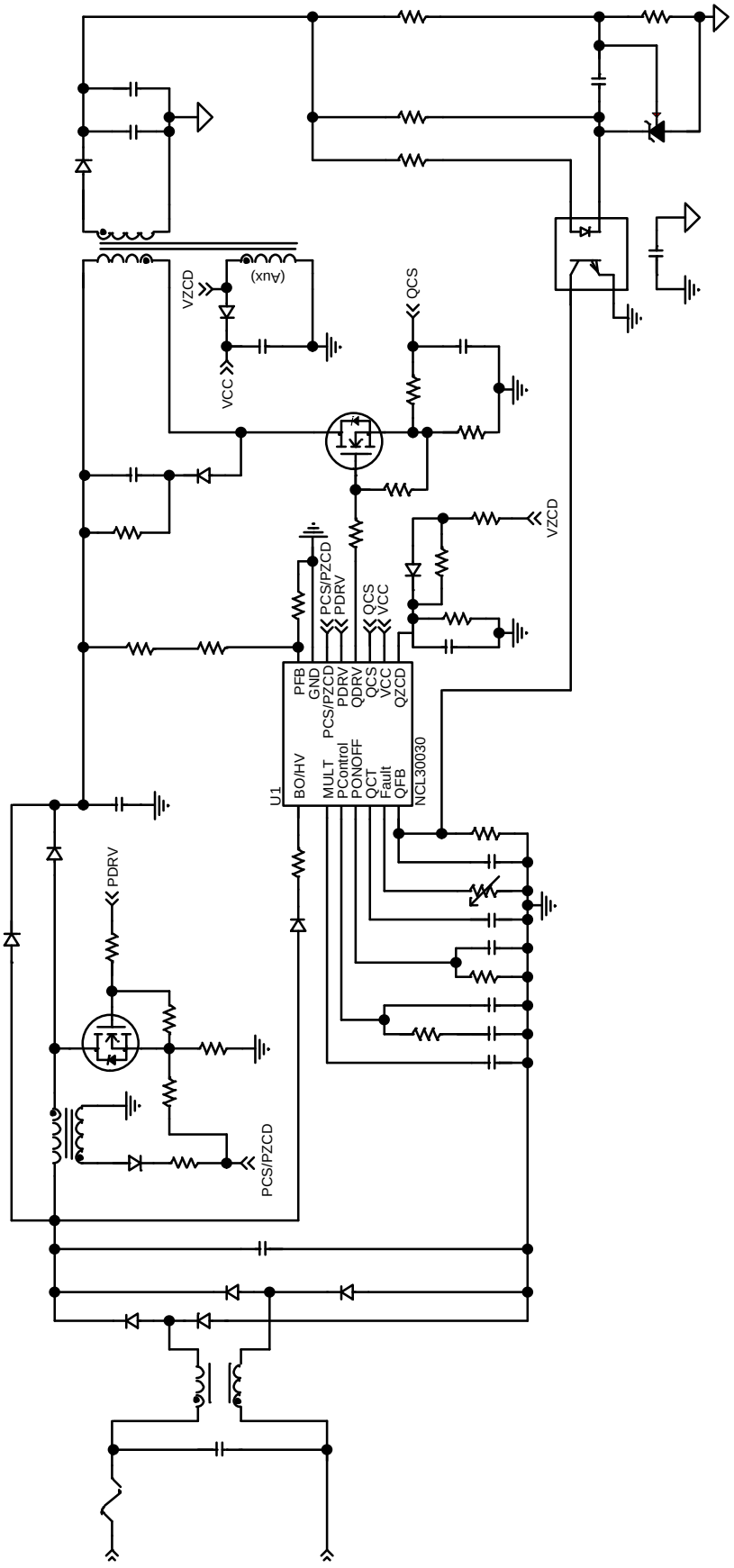

Figure 1. NCL30030 Typical Application Circuit

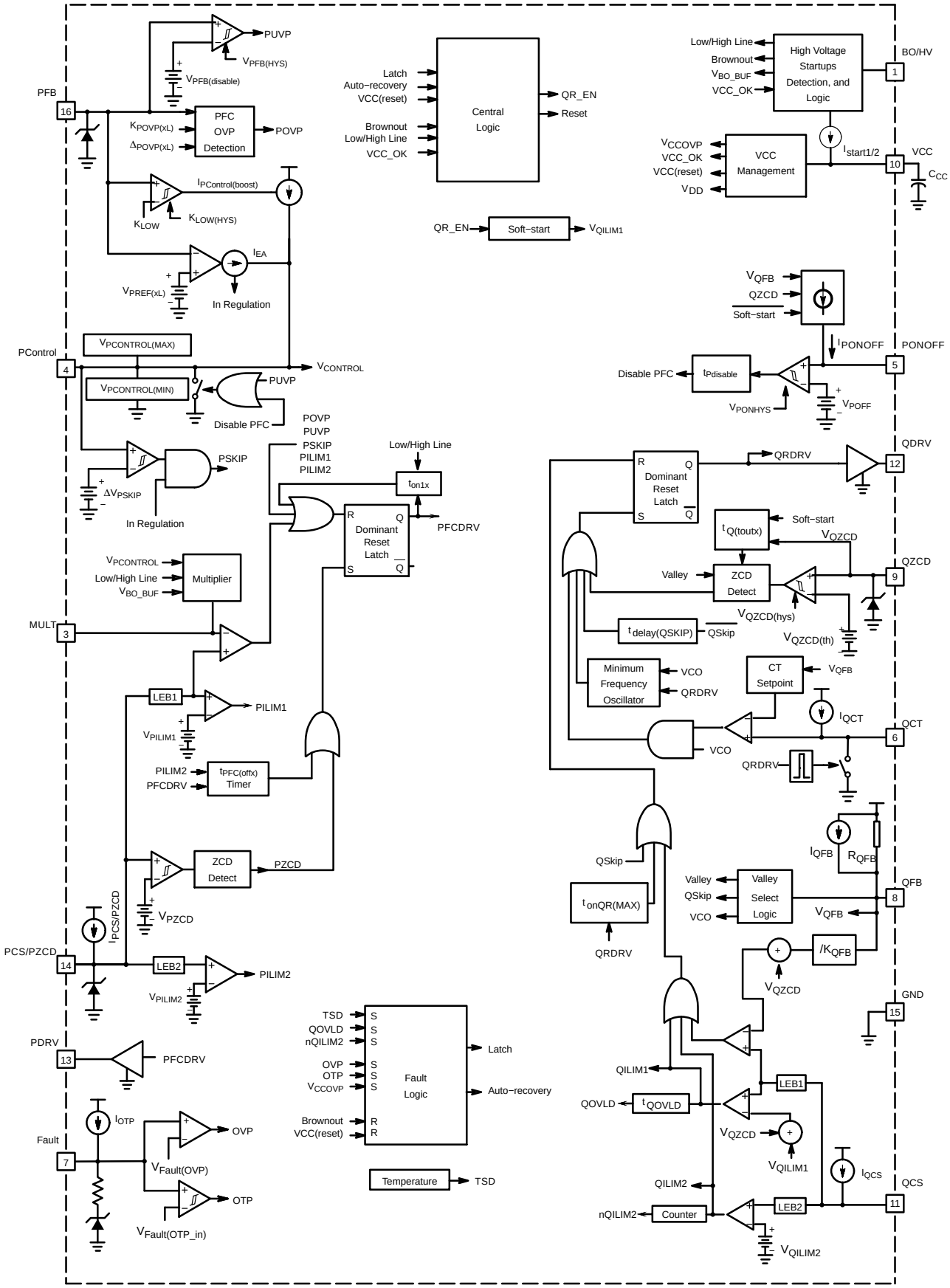

Figure 2. NCL30030 Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin Out	Name	Function
1	BO/HV	Performs input brown−out detection and line voltage range detection.
2		Removed for creepage distance.
3	MULT	This is the output of the multiplication of the BO and Control signals. A capacitor should be put on this pin for filtering. Suggested values from 1 nF − 20 nF.
4	PControl	Output of the PFC transconductance error amplifier. A compensation network is connected between this pin and ground to set the loop bandwidth.
5	PONOFF	A resistor between this pin and ground sets the PFC turn off threshold. The voltage on this pin is compared to an internal voltage signal proportional to the output power. The PFC disabled threshold is determined by the resistor on this pin and the internal pull–up current source, I_{PONOFF}.
6	QCT	An external capacitor sets the frequency in VCO mode for the QR flyback controller.
7	Fault	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor. Fault detection triggers a latch or auto−recovery depending on device option.
8	QFB	Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler.
9	QZCD	Input to the demagnetization detection comparator for the QR Flyback controller. Also used to set the overpower compensation.
10	VCC	Supply input.
11	QCS	Input to the cycle−by−cycle current limit comparator for the QR Flyback section.
12	QDRV	QR flyback controller switch driver.
13	PDRV	PFC controller switch driver.
14	PCS/PZCD	Input to the cycle−by−cycle current limit comparator for the PFC section. Also used to perform the demagnetization detection for the PFC controller.
15	GND	Ground reference.
16	PFB	PFC feedback input from external resistor divider used to sense the PFC bulk voltage. This pin voltage is compared to an internal reference. There are three different reference voltage combinations depending on ac mains voltage and version of the part.

Table 2. NCL30030 DEVICE OPTIONS

Device	Flyback Overload Protection	Fault OTP	PFC Reference Voltage (High Line / Low Line)
NCL30030B1DR2G	Auto−Recovery	Auto−Recovery	3.55 / 2 V
NCL30030B2DR2G	Auto−Recovery	Auto−Recovery	4 / 2 V
NCL30030B3DR2G	Auto−Recovery	Auto−Recovery	4 / 4 V
NCL30030A1DR2G*	Latch	Latch	3.55 / 2 V
NCL30030A2DR2G*	Latch	Latch	4 / 2 V
NCL30030A3DR2G*	Latch	Latch	4 / 4 V

*Please contact local sales representative for availability

Table 3. MAXIMUM RATINGS (Notes 1 through 6)

Rating	Pin	Symbol	Value	Unit
High Voltage Brownout Detector Input Voltage	1	$V_{BO/HV}$	−0.3 to 700	V
High Voltage Brownout Detector Input Current	1	$I_{BO/HV}$	20	mA
PFC Low Voltage Feedback Input Voltage	16	V_{PFB}	−0.3 to 9	V
PFC Low Voltage Feedback Input Current	16	I_{PFB}	0.5	mA
PFC Zero Current Detection and Current Sense Input Voltage (Note 1)	14	$V_{PCS/PZCD}$	−0.3 to $V_{PCS/PZCD(MAX)}$	V
PFC Zero Current Detection and Current Sense Input Current	14	$I_{PCS/PZCD}$	−2/+5	mA
PFC Control Input Voltage	4	$V_{PControl}$	−0.3 to 5	V
PFC Control Input Current	4	$I_{PControl}$	10	mA
Supply Input Voltage	10	$V_{CC(MAX)}$	−0.3 to 30	V
Supply Input Current	10	$I_{CC(MAX)}$	30	mA
Supply Input Voltage Slew Rate	10	dV_{CC}/dt	1	V/μs
Fault Input Voltage	7	V_{Fault}	−0.3 to (V_{CC} + 1.25)	V
Fault Input Current	7	I_{Fault}	10	mA
PFC Multiplier pin	3	V_{MULT}	−0.3 to 10	V
PFC Multiplier pin	3	I_{MULT}	3	mA
QR Flyback Zero Current Detection Input Voltage	9	V_{QZCD}	−0.9 to (V_{CC} + 1.25)	V
QR Flyback Zero Current Detection Input Current	9	I_{QZCD}	−2/+5	mA
QR Feedback Input Voltage	6	V_{QCT}	−0.3 to 10	V
QR Feedback Input Current	6	I_{QCT}	10	mA
QR Flyback Current Sense Input Voltage	11	V_{QCS}	−0.3 to 10	V
QR Flyback Current Sense Input Current	11	I_{QCS}	10	mA
QR Flyback Feedback Input Voltage	8	V_{QFB}	−0.3 to 10	V
QR Flyback Feedback Input Current	8	I_{QFB}	10	mA
PFC Driver Maximum Voltage (Note 2)	13	V_{PDRV}	−0.3 to $V_{PDRV(high2)}$	V
PFC Driver Maximum Current	13	$I_{PDRV(SRC)}$ $I_{PDRV(SNK)}$	500 800	mA
Flyback Driver Maximum Voltage (Note 2)	12	V_{QDRV}	−0.3 to $V_{QDRV(high2)}$	V
Flyback Driver Maximum Current	12	$I_{QDRV(SRC)}$ $I_{QDRV(SNK)}$	500 800	mA
PFC ON/OFF Threshold Adjust Input Voltage	5	V_{PONOFF}	−0.3 to 10	V
PFC ON/OFF Threshold Adjust Input Current	5	I_{PONOFF}	10	mA
Operating Junction Temperature	N/A	T_J	−40 to 125	°C
Storage Temperature Range	N/A	T_{STG}	–60 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{PCS/PZCD(MAX)}$ is the maximum voltage of the pin shown in the electrical table. When the voltage on this pin exceeds 5 V, the pin sinks a current equal to ($V_{PCS/PZCD}$ − 5 V)/(2 kΩ). A $V_{PSC/PZCD}$ of 7 V generates a sink current of approximately 1 mA.
2. Maximum driver voltage is limited by the driver clamp voltage, $V_{XDRV(high2)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.
3. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
4. This device contains Latch−up protection and has been tested per JEDEC JESD78D, Class I and exceeds +100/−100 mA.
5. Low Conductivity Board. As mounted on 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC51−1 conductivity test PCB. Test conditions were under natural convection of zero air flow.
6. Pin 1 is rated to the maximum voltage of the part, or 700 V.

Table 3. MAXIMUM RATINGS (Notes 1 through 6)

Rating	Symbol	Value	Unit
Power Dissipation (T_A = 75°C, 1 Oz Cu, 0.155 Sq Inch Printed Circuit Copper Clad) Plastic Package SOIC−16NB	P_D	550	mW
Thermal Resistance, Junction to Ambient 1 Oz Cu Printed Circuit Copper Clad) Plastic Package SOIC−16NB	$R_{\theta JA}$	145	°C/W
ESD Capability (Note 6) Human Body Model per JEDEC Standard JESD22−A114F. Machine Model per JEDEC Standard JESD22−A115−A. Charge Device Model per JEDEC Standard JESD22−C101E.	 HBM MM CDM	 3000 200 750	V

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Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/HV}$ = 120 V, V_{Fault} = open, V_{PFB} = 1.9 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, C_{MULT} = 2 nF, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS							
Supply Voltage Startup Threshold Minimum Operating Voltage Operating Hysteresis Internal Latch / Logic Reset Level Transition from I_{start1} to I_{start2}	 V_{CC} increasing V_{CC} decreasing $V_{CC(on)} - V_{CC(off)}$ V_{CC} decreasing V_{CC} increasing, $I_{HV/HV}$ = 650 μA	10	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(HYS)}$ $V_{CC(reset)}$ $V_{CC(inhibit)}$	 16 8.2 7.7 4.5 0.3	 17 8.8 – 5.5 0.7	 18 9.4 – 7.5 0.95	V
Blanking Duration After $V_{CC(off)}$		10	$t_{UVLO(blank)}$	3	–	25	μs
Startup Current in Inhibit Mode	V_{CC} = 0 V	10	$I_{start1A}$	0.20	0.50	0.65	mA
Startup Current Operating Mode	$V_{CC} = V_{CC(on)} - 0.5$ V, $V_{BO/HV}$ = 100 V	10	 $I_{start2A}$	 2.5	 –	 5	mA
Minimum Startup Voltage	$I_{start2A}$ = 1 mA, $V_{CC} = V_{CC(on)} - 0.5$ V	1	$V_{BO/HV(MIN)}$	–	–	40	V
V_{CC} Overvoltage Protection Threshold		10	$V_{CC(OVP)}$	27	28	29	V
V_{CC} Overvoltage Protection Delay		10	$t_{delay(VCC_OVP)}$	20.0	30.0	40.0	μs
Supply Current Before Startup, Fault or Latch Flyback in Skip, PFC Disabled Flyback in Skip, PFC in Skip Flyback Enabled, QDRV Low, PFC Disabled Flyback Enabled, QDRV Low, PFC in Skip PFC and Flyback switching at 70 kHz PFC and Flyback switching at 70 kHz	 $V_{CC} = V_{CC(on)} - 0.5$ V V_{QFB} = 0.35 V V_{QFB} = 0.35 V, $V_{PControl} < V_{PSKIP}$ V_{QZCD} = 1 V V_{QZCD} = 1 V, $V_{PControl} < V_{PSKIP}$ $C_{QDRV} = C_{PDRV}$ = open	10	 I_{CC2} I_{CC3a} I_{CC3b} I_{CC4} I_{CC5} I_{CC6} I_{CC7}	 – – – – – – –	 0.15 0.3 0.5 0.85 1.1 1.5 2.8	 0.28 0.43 1.03 1.38 1.83 4.03 5.23	mA
BROWN−OUT DETECTION							
System Startup Threshold	$V_{BO/HV}$ increasing	1	$V_{BO(start)}$	102	111	120	V
System Shutdown Threshold	$V_{BO/HV}$ decreasing	1	$V_{BO(stop)}$	86	101	116	V
Brown−out Hysteresis	$V_{BO/HV}$ increasing	1	$V_{BO(hys)}$	4	–	16	V
Brown−out Detection Blanking Time	$V_{BO/HV}$ decreasing, duration below $V_{BO(stop)}$ for a Brown−out fault	1	$t_{BO(stop)}$	43	54	65	ms
Brown−out Drive Disable Threshold	$V_{BO/HV}$ decreasing, threshold to disable drive	1	$V_{BO(DRV_disable)}$	20	30	40	V
Line Level Detection Threshold	$V_{BO/HV}$ increasing	1	$V_{lineselect}$	216	240	264	V
High to Low Line Mode Selector Timer	$V_{BO/HV}$ decreasing	1	$t_{high\ to\ low\ line}$	43	54	65	ms
Low to High Line Mode Selector Timer	$V_{BO/HV}$ increasing	1	$t_{low\ to\ high\ line}$	200	350	450	μs
Brownout Pin Off State Leakage Current	$V_{BO/HV}$ = 500 V	1	$I_{BO/HV(off)}$	–	–	42	μA
PFC MAXIMUM OFF TIME TIMER							
Maximum Off Time	 $V_{PCS/PZCD} > V_{PILIM2}$	13	$t_{PFC(off1)}$ $t_{PFC(off2)}$	100 700	200 1000	300 1300	μs
PFC CURRENT SENSE							
Fixed Cycle by Cycle Current Sense Threshold		14	V_{PILIM1}	1.35	1.5	1.65	V
Cycle by Cycle Leading Edge Blanking Duration		14	$t_{PCS(LEB1)}$	250	325	400	ns
Cycle by Cycle Current Sense Propagation Delay		14	$t_{PCS(delay1)}$	–	100	400	ns
Abnormal Overcurrent Fault Threshold		14	V_{PILIM2}	1.8	2	2.2	V
Abnormal Overcurrent Fault Leading Edge Blanking Duration		14	$t_{PCS(LEB2)}$	100	175	250	ns
Abnormal Overcurrent Fault Propagation Delay		14	$t_{PCS(delay2)}$	–	100	200	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/HV}$ = 120 V, V_{Fault} = open, V_{PFB} = 1.9 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, C_{MULT} = 2 nF, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
PFC CURRENT SENSE							
Multipler Cycle by Cycle Current Sense Offset	BO = 180, PFB = 1.5 V	14	V_{PILIM_MULT}	−12	−	10	mV
Multiplier Cycle by Cycle Current Sense Propagation Delay	BO = 180 V, PFB = 1.5 V	14	$t_{PCS(delay_mult)}$	10	100	200	ns
Pull−up Current Source	$V_{PCS/PZCD}$ = 2.5 V	14	$I_{PCS/PZCD}$	0.7	1.0	1.3	μA
PFC REGULATION BLOCK							
PFC Reference Voltage See Table 2 for Options	$V_{BO/HV} > V_{BO(lineselect)}$ $V_{BO/HV} < V_{BO(lineselect)}$	16	$V_{PREF(HL)}$ $V_{PREF(LL)}$	3.47 3.92 1.95 3.92	3.55 4.00 2 4	3.62 4.08 2.05 4.08	V
Error Amplifier Current Source Sink Source Sink	PFC Enabled V_{PFB} = 0.96 x $V_{PREF(HL)}$ V_{PFB} = 1.04 x $V_{PREF(HL)}$ V_{PFB} = 0.96 x $V_{PREF(LL)}$ V_{PFB} = 1.04 x $V_{PREF(LL)}$	4	 $I_{EA(SRCHL)}$ $I_{EA(SNKHL)}$ $I_{EA(SRCLL)}$ $I_{EA(SNKLL)}$	 16 16 10 10	 32 32 20 20	 48 48 30 30	μA
Open Loop Error Amplifier Transconductance	V_{PFB} = $V_{PREF(LL)}$ +/− 4 % V_{PFB} = $V_{PREF(HL)}$ +/− 4 %	4	g_m g_{m_HL}	100 100	200 200	300 300	μS
Maximum Control Voltage	V_{PFB} * $K_{LOW(PFCxL)}$, $C_{PControl}$ = 10 nF	4	$V_{PControl(MAX)}$	–	4.5	–	V
Minimum Control Voltage (Lower clamp)	V_{PFB} * $K_{POVP(xL)}$, $C_{PControl}$ = 10 nF	4	$V_{PControl(MIN)}$	–	0.6	–	V
EA Output Control Voltage Range	$V_{PControl(MAX)}$ − $V_{PControl(MIN)}$	4	$\Delta V_{PControl}$	3.7	3.9	4.1	V
Ratio between the V_{out} Low Detect Threshold and the Regulation Level	V_{PFB} decreasing, V_{BOOST} / $V_{PREF(HL)}$ V_{PFB} decreasing, V_{BOOST} / $V_{PREF(LL)}$	16	$K_{LOW(PFCHL)}$ $K_{LOW(PFCLL)}$	0.940 0.940	0.945 0.945	0.950 0.950	
Ratio between the V_{out} Low Exit Threshold and the Regulation Level	V_{PFB} increasing	16	$K_{LOW(HYSHL)}$ $K_{LOW(HYSLL)}$	0.950 0.950	0.960 0.960	0.965 0.965	
Source Current During V_{out} Low Detect		4	$I_{PControl(boost)}$	190	240	290	μA
PFC In Regulation Threshold	$V_{PControl}$ increasing	4	$I_{In_Regulation}$	−6.5	–	0	μA
Resistance of Internal Pull Down Switch	$I_{PControl}$ = 5 mA	4	$R_{PControl}$	4	25	50	Ω
PFC SKIP MODE							
Delta Between Skip Level and Lower Clamp PControl Voltages	$V_{PControl}$ decreasing, measured from $V_{PControl(MIN)}$	4	ΔV_{PSKIP}	5	25	50	mV
PFC Skip Hysteresis	$V_{PControl}$ increasing	4	$V_{PSKIP(HYS)}$	25	50	75	mV
Delay Exiting Skip Mode	Apply 1 V step from $V_{PControl(MIN)}$	4	$t_{delay(PSKIP)}$	–	50	60	μs
PFC FAULT PROTECTION							
Ratio between the Hard Overvoltage Protection Threshold and Regulation Level	V_{PFB} increasing $K_{POVP(LL)}$ = V_{PFB}/$V_{PREF(LL)}$ $K_{POVP(HL)}$ = V_{PFB}/$V_{PREF(HL)}$	16	 $K_{POVP(LL)}$ $K_{POVP(HL)}$	 1.06 1.05	 1.08 1.06	 1.10 1.08	
Soft Overvoltage Protection Threshold	$V_{PSOVP(LL)}$ = soft overvoltage level $\Delta_{POVP(LL)}$ = K_{POVP}*$V_{PREF(LL)}$ − $V_{PSOVP(LL)}$ $\Delta_{POVP(HL)}$ = K_{POVP}*$V_{PREF(HL)}$ − $V_{PSOVP(HL)}$	16	 $\Delta_{POVP(LL)}$ $\Delta_{POVP(HL)}$	 20 20	 – –	 55 55	mV
PFC Feedback Pin Disable Threshold	V_{PFB} decreasing	16	$V_{PFB(disable)}$	0.225	0.30	0.35	V
PFC Feedback Pin Enable Threshold	V_{PFB} increasing	16	$V_{PFB(enable)}$	0.275	0.35	0.40	V
PFC Feedback Pin Hysteresis	V_{PFB} increasing	16	$V_{PFB(HYS)}$	25	50	–	mV
PFC Feedback Disable Delay		16	$t_{delay(PFB)}$	20	30	40	μs
PFC ON TIME CONTROL							
PFC Maximum On	$V_{PControl}$ = $V_{PControl(MAX)}$ $V_{BO/HV}$ = 163 V $V_{BO/HV}$ = 325 V	13	 t_{on1a} t_{on1b}	 12.5 4.25	 15 5.00	 17.5 5.75	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
PFC DISABLE							
Voltage to Current Conversion Ratio	V_{QFB} = 3 V, Low Line V_{QFB} = 3 V, High Line	5	$I_{ratio1(QFB/PON)}$ $I_{ratio2(QFB/PON)}$	13 13	15 15	17 17	μA
PFC Disable Threshold	V_{PONOFF} decreasing	5	V_{POFF}	1.9	2.0	2.1	V
PFC Enable Hysteresis	V_{QFB} = increasing	5	V_{PONHYS}	0.135	0.160	0.185	V
PONOFF Operating Mode Voltage	t_{demag}/T = 70%, R_{PONOFF} = 191 kΩ, C_{PONOFF} = 1 nF V_{QFB} = 1.8 V (decreasing) V_{QFB} = 3 V (decreasing)	5	 $V_{PONOFF1}$ $V_{PONOFF2}$	 1.08 1.8	 1.20 2.0	 1.32 2.2	V
PFC Disable Timer	Disable Timer	5	$t_{Pdisable}$	450	500	550	ms
PFC Enable Filter Delay		5	$t_{Penable(filter)}$	50	100	150	μs
PFC Enable Timer	PONOFF Increasing	5	$t_{Penable}$	200	–	500	μs
PFC MULTIPLIER							
Multiplier maximum BO=180V	PControl = open, BO = 180 V	3	MULT_max_180	0.85	1	1.15	V
Multiplier maximum BO = 360V	PControl = open, BO = 360 V	3	MULT_max_360	0.425	0.5	0.575	V
Multiplier output	PControl = 2.5 V, BO = 180 V	3	VmultLL	0.425	0.5	0.575	V
Multiplier output	PControl = 2.5 V, BO = 360 V	3	VmultHL	0.2125	0.25	0.2875	V
Multiplier linearity with respect to BO at low line. (VMULT180/180V)/(VMULT120/120V)	PControl = 2.5 V, BO = 180 V and BO = 120 V	3	Mult_linearityLL	0.98	1	1.02	
Multiplier linearity with respect to BO at high line. (VMULT360/360V)/VMULT300/300V)	PControl = 2.5 V, BO = 360 V and BO = 300 V	3	Mult_linearityHL	0.99	1	1.01	
PFC GATE DRIVE							
Rise Time (10−90%)	V_{PDRV} from 10% to 90% of V_{CC}	13	$t_{PDRV(rise)}$	–	40	80	ns
Fall Time (90−10%)	90% to 10% of V_{PDRV}	13	$t_{PDRV(fall)}$	–	20	40	ns
Driver Resistance Source Sink		13	 $R_{PDRV(SRC)}$ $R_{PDRV(SNK)}$	 – –	 13 7	 – –	Ω
Current Capability Source Sink	 V_{PDRV} = 2 V V_{PDRV} = 10 V	13	 $I_{PDRV(SRC)}$ $I_{PDRV(SNK)}$	 – –	 500 800	 – –	mA
High State Voltage	V_{CC} = $V_{CC(off)}$ + 0.2 V, R_{PDRV} = 10 kΩ V_{CC} = 26 V, R_{PDRV} = 10 kΩ	13	$V_{PDRV(high1)}$ $V_{PDRV(high2)}$	8 10	– 12	– 14	V
Low State Voltage	V_{Fault} = 4 V	13	$V_{PDRV(low)}$	–	–	0.25	V
PFC ZERO CURRENT DETECTION							
Zero Current Detection Threshold	$V_{PCS/PZCD}$ rising $V_{PCS/PZCD}$ falling	14	$V_{PZCD(rising)}$ $V_{PZCD(falling)}$	675 200	750 250	825 300	mV
Hysteresis on Voltage Threshold	$V_{PZCD(rising)}$ – $V_{PZCD(falling)}$	14	$V_{PZCD(HYS)}$	375	500	625	mV
Propagation Delay	Measure from $V_{PCS/PZCD}$ = $V_{PZCD(falling)}$ to PDRV rising	14	t_{PZCD}	50	100	170	ns
Input Voltage Excursion Upper Clamp Negative Clamp	 $I_{PCS/PZCD}$ = 1 mA $I_{PCS/PZCD}$ = −2 mA	14	 $V_{PCS/PZCD(MAX)}$ $V_{PCS/PZCD(MIN)}$	 6.5 −0.9	 7 −0.7	 7.5 0	V
Minimum detectable ZCD Pulse Width	Between $V_{PZCD(rising)}$ and $V_{PZCD(falling)}$ to PDRV	14	t_{SYNC}	–	70	200	ns
ZCD blanking time	Measured DRV off to DRV on	14	T_{Pzcd_blank}	450	700	1000	ns
QR FLYBACK GATE DRIVE							
Rise Time (10−90%)	V_{QDRV} from 10 to 90%	12	$t_{QDRV(rise)}$	–	40	80	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/HV}$ = 120 V, V_{Fault} = open, V_{PFB} = 1.9 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, C_{MULT} = 2 nF, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
QR FLYBACK GATE DRIVE							
Fall Time (90−10%)	90 to 10% of V_{QDRV}	12	$t_{QDRV(fall)}$	–	20	40	ns
Driver Resistance Source Sink		12	 $R_{QDRV(SRC)}$ $R_{QDRV(SNK)}$	 – –	 13 7	 – –	Ω
Current Capability Source Sink	 V_{QDRV} = 2 V V_{QDRV} = 10 V	12	 $I_{QDRV(SRC)}$ $I_{QDRV(SNK)}$	 – –	 500 800	 – –	mA
High State Voltage	V_{CC} = $V_{CC(off)}$ + 0.2 V, R_{QDRV} = 10 kΩ V_{CC} = 26 V, R_{QDRV} = 10 kΩ	12	$V_{QDRV(high1)}$ $V_{QDRV(high2)}$	8 10	– 12	– 14	V
Low State Voltage	V_{Fault} = 4 V	12	$V_{QDRV(low)}$	–	–	0.25	V
QR FLYBACK FEEDBACK							
Internal Pull−Up Current Source		8	I_{QFB}	46.75	50	53.25	μA
Feedback Input Open Voltage		8	$V_{QFB(open)}$	4.5	5.0	5.5	V
V_{QFB} to Internal Current Setpoint Division Ratio		8	K_{QFB}	3.8	4.0	4.2	
QFB Pull Up Resistor	V_{QFB} = 0.4 V	8	R_{QFB}	340	400	460	kΩ
Valley Thresholds Transition from 1st to 2nd valley Transition from 2nd to 3rd valley Transition from 3rd to 4th valley Transition from 4th valley to VCO Transition from VCO to 4th valley Transition from 4th to 3rd valley Transition from 3rd to 2nd valley Transition from 2nd to 1st valley	 V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing	8	 V_{H2D} V_{H3D} V_{H4D} V_{HVCOD} V_{HVCOI} V_{H4I} V_{H3I} V_{H2I}	 1.316 1.128 0.846 0.752 1.316 1.504 1.692 1.880	 1.400 1.200 0.900 0.800 1.400 1.600 1.800 2.000	 1.484 1.272 0.954 0.848 1.484 1.696 1.908 2.120	V
Skip Threshold	V_{QFB} decreasing	8	V_{QSKIP}	0.35	0.40	0.45	V
Skip Hysteresis	V_{QFB} increasing	8	$V_{QSKIP(HYS)}$	25	50	75	mV
Delay Exiting Skip Mode to 1st QDRV Pulse	Apply 1 V step from V_{QSKIP}	8	$t_{delay(QSKIP)}$	–	–	10	μs
Maximum On Time		12	$t_{onQR(MAX)}$	26	32	38	μs
QR FLYBACK TIMING CAPACITOR							
QCT Operating Voltage Range	V_{QFB} = 0.5 V	6	$V_{QCT(peak)}$	3.815	4.000	4.185	V
On Time Control Source Current	V_{QCT} = 0 V	6	I_{QCT}	18	20	22	μA
Minimum voltage on QCT Input		6	$V_{QCT(min)}$	–	–	90	mV
Minimum Operating Frequency in VCO Mode	V_{QCT} = $V_{QCT(peak)}$ + 100 mV	6	$f_{VCO(MIN)}$	23.5	27	30.5	kHz
QR FLYBACK DEMAGNETIZATION INPUT							
QZCD threshold voltage	V_{QZCD} decreasing	9	$V_{QZCD(th)}$	35	55	90	mV
QZCD hysteresis	V_{QZCD} increasing	9	$V_{QZCD(HYS)}$	15	35	55	mV
Demagnetization Propagation Delay	V_{QZCD} step from 4.0 V to −0.3 V	9	t_{DEM}	–	150	250	ns
Input Voltage Excursion Upper Clamp Negative Clamp	 I_{QZCD} = 5.0 mA I_{QZCD} = −2.0 mA	9	 $V_{QZCD(MAX)}$ $V_{QZCD(MIN)}$	 12.4 −0.9	 12.7 −0.7	 13.5 0	V
Blanking Delay After Turn−Off		9	$t_{ZCD(blank)}$	2	3	4	μs
Timeout After Last Demagnetization Detection	During soft−start After soft−start	12	$t_{Q(tout1)}$ $t_{Q(tout2)}$	80 5.1	100 6	120 6.9	μs
QR FLYBACK CURRENT SENSE							
Current Sense Voltage Threshold	V_{QCS} increasing V_{QCS} increasing, V_{QZCD} = 1 V	11	$V_{QILIM1a}$ $V_{QILIM1b}$	0.760 0.760	0.800 0.800	0.840 0.840	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/HV}$ = 120 V, V_{Fault} = open, V_{PFB} = 1.9 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, C_{MULT} = 2 nF, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
QR FLYBACK CURRENT SENSE							
Cycle by Cycle Leading Edge Blanking Duration	Minimum on time minus $t_{delay(ILIM_QR)}$	11	$t_{QCS(LEB1)}$	220	275	350	ns
Cycle by Cycle Current Sense Propagation Delay		11	$t_{QCS(delay1)}$	–	125	175	ns
Immediate Fault Protection Threshold	V_{QCS} increasing, V_{QFB} = 4 V	11	V_{QILIM2}	1.125	1.200	1.275	V
Abnormal Overcurrent Fault Leading Edge Blanking Duration		11	$t_{QCS(LEB2)}$	90	120	150	ns
Abnormal Overcurrent Fault Propagation Delay		11	$t_{QCS(delay2)}$	–	125	175	ns
Number of Consecutive Abnormal Overcurrent Detections to Enter Fault Mode		11	n_{QILIM2}	–	4	–	
Minimum Peak Current Level in VCO Mode	V_{QFB} = 0.4 V, V_{QCS} increasing	11	$I_{peak(VCO)}$	11	12.5	14	%
Set point decrease for V_{QZCD} = −250 mV	V_{QCS} Increasing, V_{QFB} = 4 V	11	$V_{OPP(MAX)}$	28	31.25	33	%
Overpower Protection Delay		11	$t_{QOPP(delay)}$	–	125	175	ns
Pull−up Current Source	V_{QCS} = 1.5 V	11	I_{QCS}	0.7	1.0	1.3	μA
QR FLYBACK FAULT PROTECTION							
Soft−Start Period	Measured from 1st QDRV pulse to V_{QCS} = V_{QILIM1}	11	t_{SSTART}	2.8	4.0	5.0	ms
Flyback Overload Fault Timer	V_{QCS} = V_{QILIM1}	11	t_{QOVLD}	60	80	100	ms
COMMON FAULT PROTECTION							
Overvoltage Protection (OVP) Threshold	V_{Fault} increasing	7	$V_{Fault(OVP)}$	2.79	3.00	3.21	V
Delay Before Fault Confirmation Used for OVP Detection Used for OTP Detection	 V_{Fault} increasing V_{Fault} decreasing	7	 $t_{delay(Fault_OVP)}$ $t_{delay(Fault_OTP)}$	 22.5 22.5	 30.0 30.0	 37.5 37.5	μs
Overtemperature Protection (OTP) Threshold (Note 7)	V_{Fault} decreasing	7	$V_{Fault(OTP_in)}$	0.38	0.40	0.42	V
Overtemperature Protection (OTP) Exiting Threshold (Note 7)	V_{Fault} increasing, B version	7	$V_{Fault(OTP_out)}$	0.874	0.920	0.966	V
OTP Pull−up Current Source (Note 7)	V_{Fault} = $V_{Fault(OTP_in)}$ + 0.2 V	7	$I_{Fault(OTP)}$	42.5	45.5	48.5	μA
Fault Input Clamp Voltage	V_{Fault} = open	7	$V_{Fault(clamp)}$	1.5	1.75	2.0	V
Fault Input Clamp Series Resistor		7	$R_{Fault(clamp)}$	1.32	1.55	1.82	kΩ

7. NTC with R_{110} = 8.8 kΩ (TTC03-474)]

THERMAL PROTECTION

Thermal Shutdown	Temperature increasing	N/A	T_{SHDN}	−	150	−	°C
Thermal Shutdown Hysteresis	Temperature decreasing	N/A	$T_{SHDN(HYS)}$	−	40	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DETAILED OPERATING DESCRIPTION

INTRODUCTION

The NCL30030 is a combination critical mode (CrM) power factor correction (PFC) and quasi−resonant (QR) flyback controller optimized for high performance LED driver applications.

HIGH VOLTAGE STARTUP CIRCUIT

The NCL30030 integrates a high voltage startup circuit accessible by the BO/HV pin. The BO/HV input is also used for monitoring the ac line voltage and detecting brown−out faults. The startup circuit is rated at a maximum voltage of 700 V to support higher voltages used in commercial lighting such as 277 and 347 VAC.

A startup regulator consists of a constant current source that supplies current from the ac input terminals (V_{in}) to the supply capacitor on the V_{CC} pin (C_{CC}). The startup circuit current ($I_{start2A}$) is typically 3.75 mA. $I_{start2A}$ is disabled if the VCC pin is below $V_{CC(inhibit)}$. In this condition the startup current is reduced to $I_{start1A}$, typically 0.5 mA. The internal high voltage startup circuit eliminates the need for external startup components. In addition, the startup regulator helps increase the system efficiency as it uses negligible power in the normal operation mode.

Once C_{CC} is charged to the startup threshold, $V_{CC(on)}$, typically 17 V, the startup regulator is disabled and the controller is enabled. The startup regulator will remain disabled until V_{CC} falls below the minimum operating voltage threshold, $V_{CC(off)}$, typically 8.8 V. Once reached, the PFC and flyback controllers are disabled reducing the bias current consumption of the IC. The startup circuit is then are then enabled allowing V_{CC} to charge back up.

A dedicated comparator monitors V_{CC} when the QR stage is enabled and latches off the controller if V_{CC} exceeds $V_{CC(OVP)}$, typically 28 V.

The controller is disabled once a fault is detected. The controller will restart the next time V_{CC} reaches $V_{CC(on)}$ and all non−latching faults have been removed.

The supply capacitor provides power to the controller during power up. The capacitor must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the controller will turn off. The operating IC bias current, I_{CC4}, and gate charge load at the drive outputs must be considered to correctly size C_{CC}. The increase in current consumption due to external gate charge is calculated using Equation 1.

$$I_{CC(gatecharge)} = f \cdot Q_G \qquad \text{(eq. 1)}$$

where f is the operating frequency and Q_G is the gate charge of the external MOSFETs.

LINE VOLTAGE SENSE

The BO/HV pin provides access to the brown−out and line voltage detectors. The brown−out detector detects mains interruptions and the line voltage detector determines the presence of either 120 V or 230 V ac mains. Depending on the detected input voltage range device parameters are internally adjusted to optimize the system performance.

This pin can connect after the rectifier bridge to achieve full wave rectification as shown in Figure 3. A diode is used to prevent the pin from going below ground. A low value resistor in series with the BO/HV pin can be used for protection. A low value resistor is needed to reduce the voltage offset while sensing the line voltage.

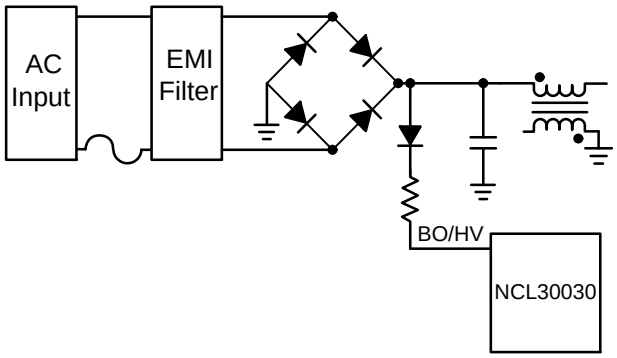


Figure 3. Brown−out and Line Voltage Detectors Configuration

The flyback stage is enabled once $V_{BO/HV}$ is above the brown−out threshold, $V_{BO(start)}$, typically 111 V, and V_{CC} reaches $V_{CC(on)}$. The high voltage startup is immediately enabled when the voltage on $V_{BO/HV}$ crosses over the brown−out start threshold, $V_{BO(start)}$, to ensure that device is enabled quickly upon exiting a brown−out state. Figure 4 shows typical power up waveforms.

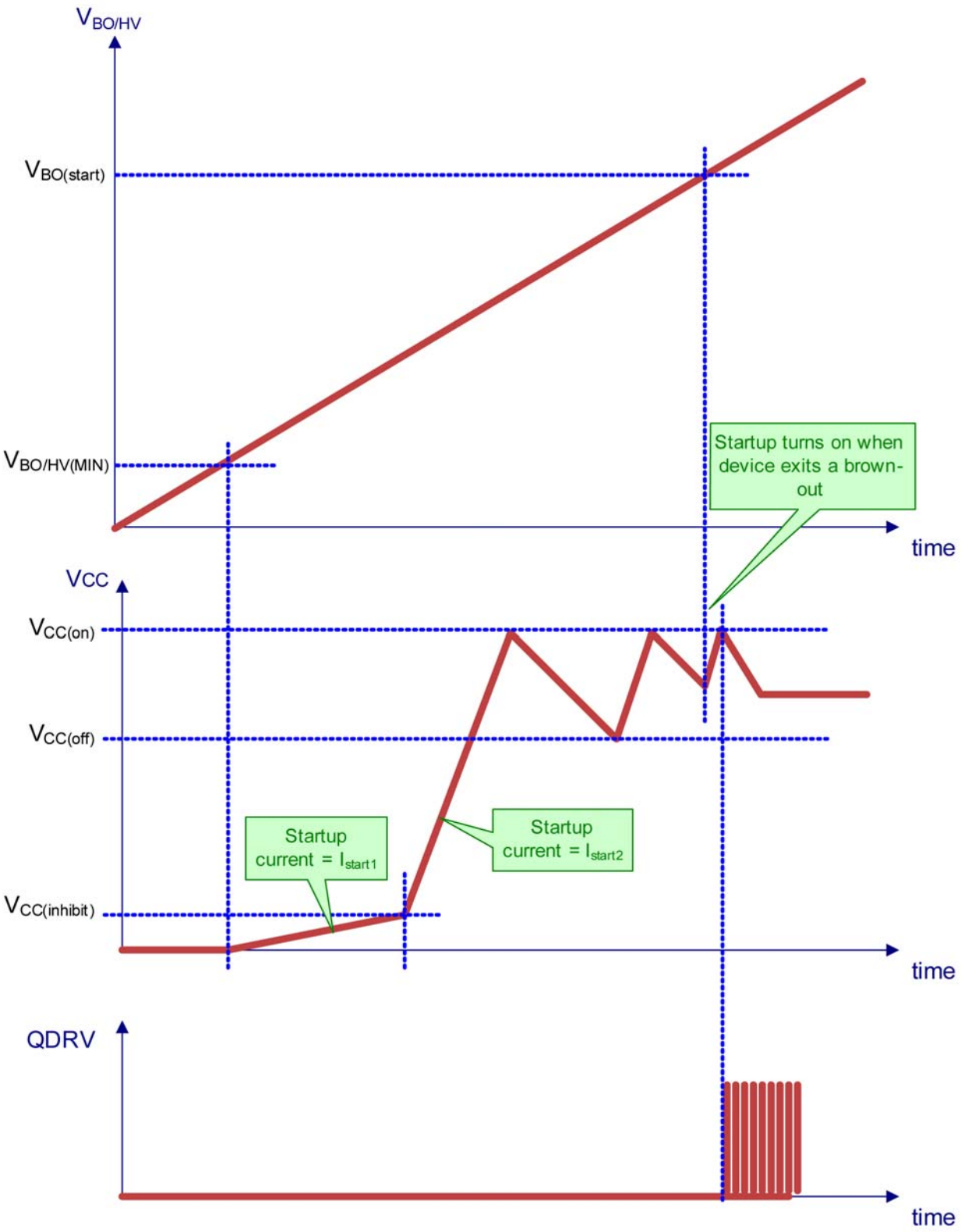


Figure 4. Startup Timing Diagram

A timer is enabled once $V_{BO/HV}$ drops below its stop threshold, $V_{BO(stop)}$, typically 101 V. If the timer, t_{BO}, expires the device will begin monitoring the voltage on $V_{BO/HV}$ and disable the PFC and flyback stages when that voltage is below the Brown−out Drive Disable threshold, $V_{BO(DRV_disable)}$, typically 30 V. This ensures that device switching is stopped in a low energy state which minimizes inductive voltage kick from the EMI components and ac mains. The timer, t_{BO}, typically 54 ms, is set long enough to ignore a single cycle drop−out.

LINE VOLTAGE DETECTOR

The input voltage range is detected based on the peak voltage measured at the BO/HV pin. Discrete values are selected for the PFC stage gain (feedforward) depending on the input voltage range. The controller compares $V_{BO/HV}$ to an internal line select threshold, $V_{BO(lineselect)}$, typically 240 V. Once $V_{BO/HV}$ exceeds $V_{BO(lineselect)}$, the PFC stage operates in “high line” (Commercial US − 277 Vac) or “230 Vac” mode. In high line mode the maximum on time is reduced by a factor of 3, resulting in a maximum output power independent of input voltage.

The default power−up mode of the controller is low line. The controller switches to “high line” mode if $V_{BO/HV}$ exceeds the line select threshold for longer than the low to high line timer, $t_{(low\ to\ high\ line)}$, typically 300 μs, as long as it was not previously in high line mode. If the controller has switched from “high line” to “low line” mode, the low to high line timer, $t_{(low\ to\ high\ line)}$, is inhibited until $V_{BO/HV}$ falls below $V_{BO(stop)}$. This prevents the controller from toggling back to “high line” until at least one $V_{BO(stop)}$ transition has occurred. The timer and logic is included to prevent unwanted noise from toggling the operating line level.

In “high line” mode the high to low line timer, $t_{(high\ to\ low\ line)}$, (typically 54 ms) is enabled once $V_{BO/HV}$ falls below $V_{BO(lineselect)}$. It is reset once $V_{BO/HV}$ exceeds $V_{BO(lineselect)}$. The controller switches back to “low line” mode if the high to low line timer expires.

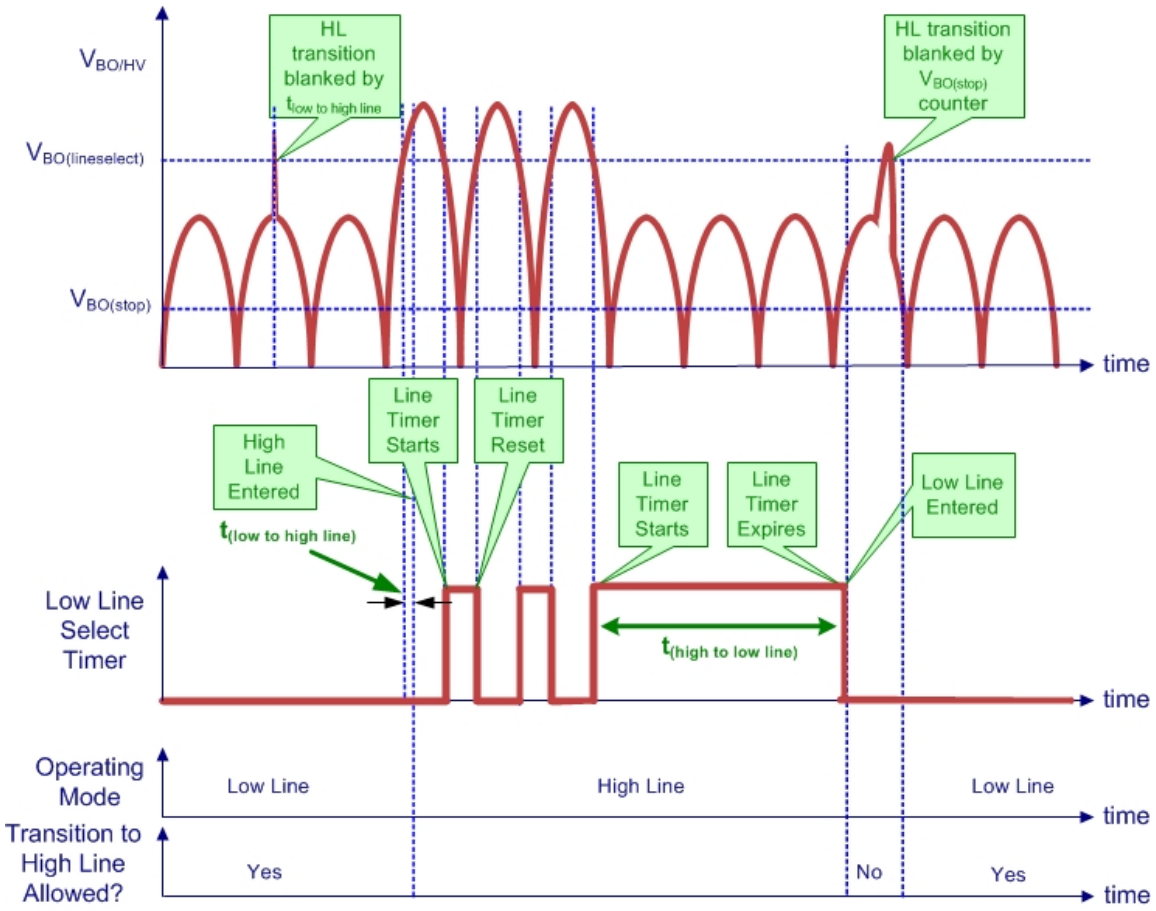


Figure 5. Line Detector Waveforms

FAULT INPUT

The NCL30030 includes a dedicated fault input accessible via the Fault pin. The controller will enter triple hiccup mode when the pin is pulled above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. The controller is disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP_in)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 6 shows the architecture of the Fault input.

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source $I_{Fault(OTP)}$, (typically 45.5 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP_in)}$. Part option A latches off the controller after an overtemperature fault is detected. For part option B the controller is re−enabled once the fault is removed such that V_{Fault} increases above $V_{Fault(OTP_out)}$ and V_{CC} reaches $V_{CC(on)}$. Figure 7 shows typical waveforms related to the latch option where as Figure 8 shows waveforms of the auto−recovery option.

An active clamp prevents the Fault pin voltage from reaching the upper latch threshold if the pin is open. To reach the upper threshold, the external pull−up current has to be higher than the pull−down capability of the clamp (set by $R_{Fault(clamp)}$ at $V_{Fault(clamp)}$). The upper fault threshold is intended to be used for an overvoltage fault using a Zener diode and a resistor in series from the auxiliary winding voltage, V_{AUX}. The controller goes into a triple hiccup once V_{Fault} exceeds $V_{Fault(OVP)}$.

The Fault input signal is filtered to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, $t_{delay(Fault_OVP)}$ and $t_{delay(Fault_OTP)}$ are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay.

A bypass capacitor is usually connected between the Fault and GND pins and it will take some time for V_{Fault} to reach its steady state value once $I_{Fault(OTP)}$ is enabled. Therefore, a lower fault (i.e. overtemperature) is ignored during soft−start. In Option B, $I_{Fault(OTP)}$ remains enabled while the lower fault is present independent of V_{CC} in order to provide temperature hysteresis. The upper OVP fault detection is enabled and remains active as long as the QR flyback is enabled.

Once the controller is latched, it is reset if a brown−out condition is detected or if V_{CC} is cycled down to its reset level, $V_{CC(reset)}$. In the typical application these conditions occur only if the ac voltage is removed from the system. Prior to reaching $V_{CC(reset)}$, $V_{fault(clamp)}$ is set at 0 V.

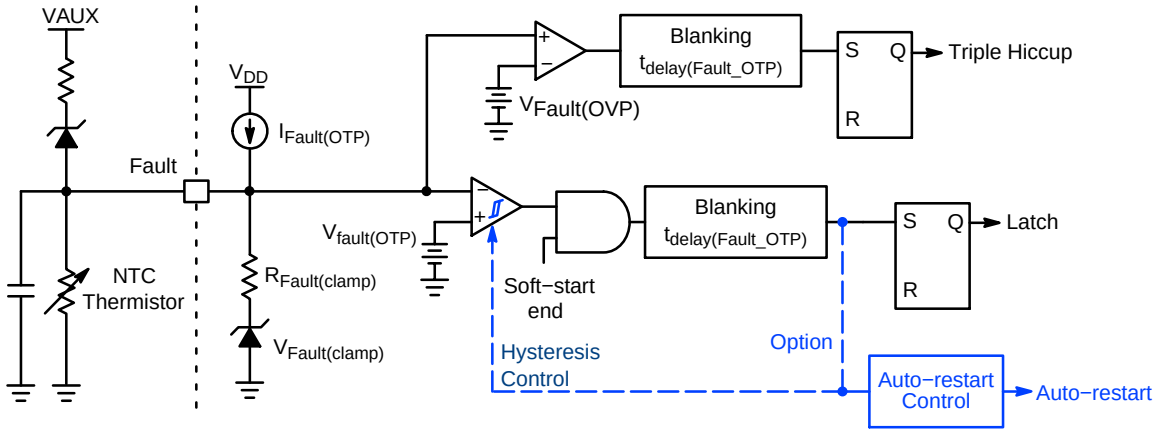


Figure 6. Fault Detection Schematic

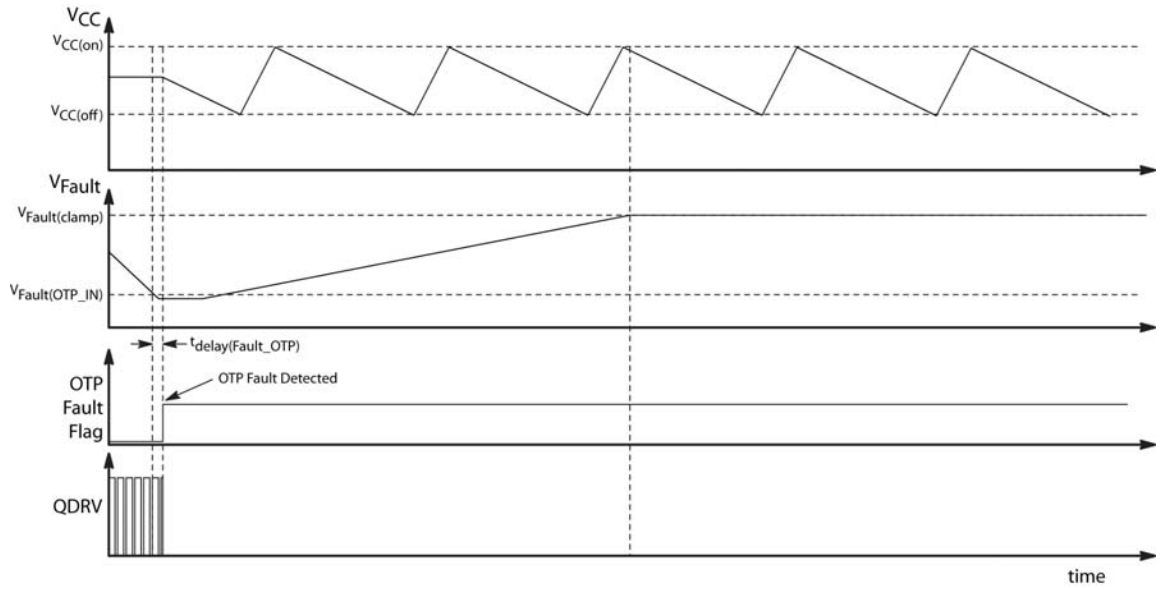


Figure 7. Latch−off Function Timing Diagram

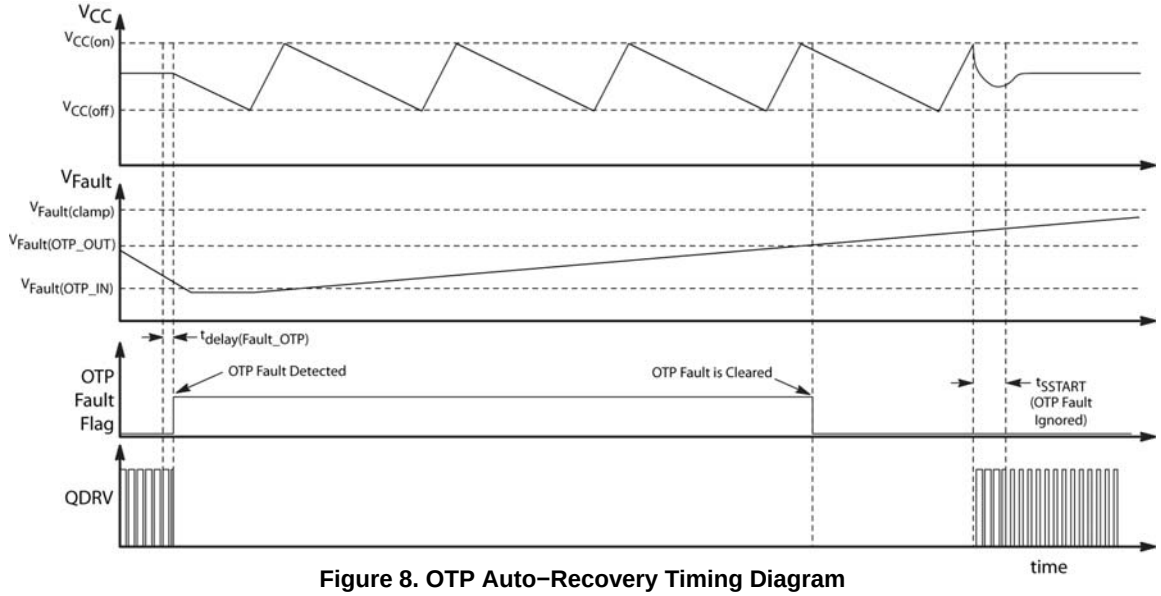


Figure 8. OTP Auto−Recovery Timing Diagram

QR FLYBACK VALLEY LOCKOUT

The NCL30030 integrates a quasi−resonant (QR) flyback controller. The power switch turn−off of the QR converter is determined by the peak current set by the feedback loop. The switch turn−on is determined by the transformer demagnetization. The demagnetization is detected by monitoring the transformer auxiliary winding voltage.

Turning on the power switch once the transformer is demagnetized or reset reduces switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lump capacitance eventually settling at the input voltage. A QR controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce switching losses and electromagnetic interference (EMI).

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. That is, a load reduction increases the operating frequency. This traditionally requires a maximum frequency clamp to limit the operating frequency. This causes the controller to become unstable and jump (or hesitate) between two valleys generating audible noise. The NCL30030 incorporates a patent pending valley lockout circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly. Like a traditional QR flyback controller, the frequency increases when the load decreases. Once a higher valley is selected the frequency decreases very rapidly. It

will continue to increase if the load is further reduced. This technique extends QR operation over a wider output power range while maintaining good efficiency and limiting the maximum operating frequency. Figure 9 shows a qualitative frequency vs output power relationship.

Figure 10 shows the internal arrangement of the valley detection circuitry. An internal counter increments each time a valley is detected. The operating valley (1st, 2nd, 3rd or 4th) is determined by the QFB voltage. As V_{QFB} decreases or increases, the valley comparators toggle one after another to select the proper valley. The activation of an "n" valley comparator blanks the "n−1" or "n+1" valley comparator output depending if V_{QFB} decreases or increases, respectively.

A valley is detected once V_{QZCD} falls below the QR flyback demagnetization threshold, $V_{QZCD(th)}$, typically 55 mV. The controller will switch once the valley is detected or increment the valley counter depending on QFB voltage.

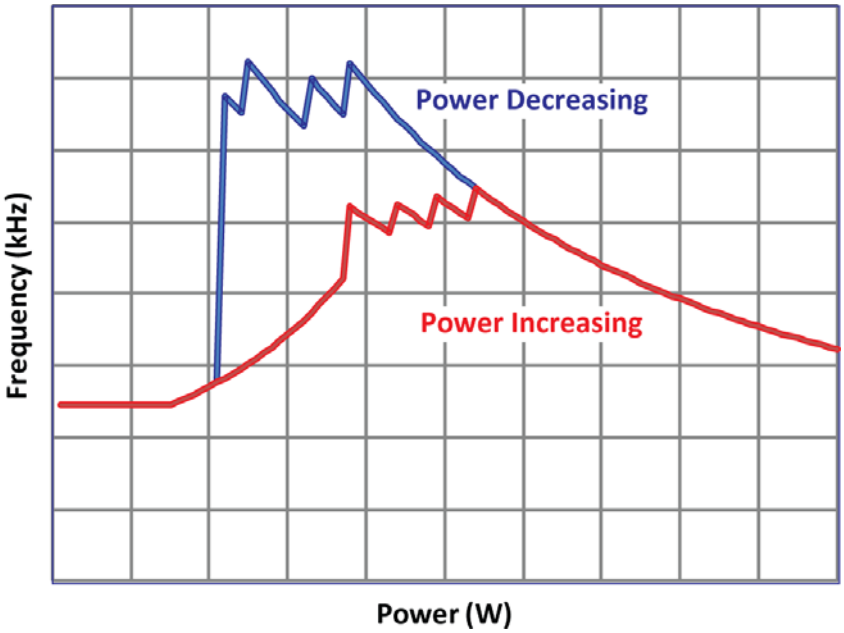


Figure 9. Valley Lockout Frequency vs Output Power Relationship

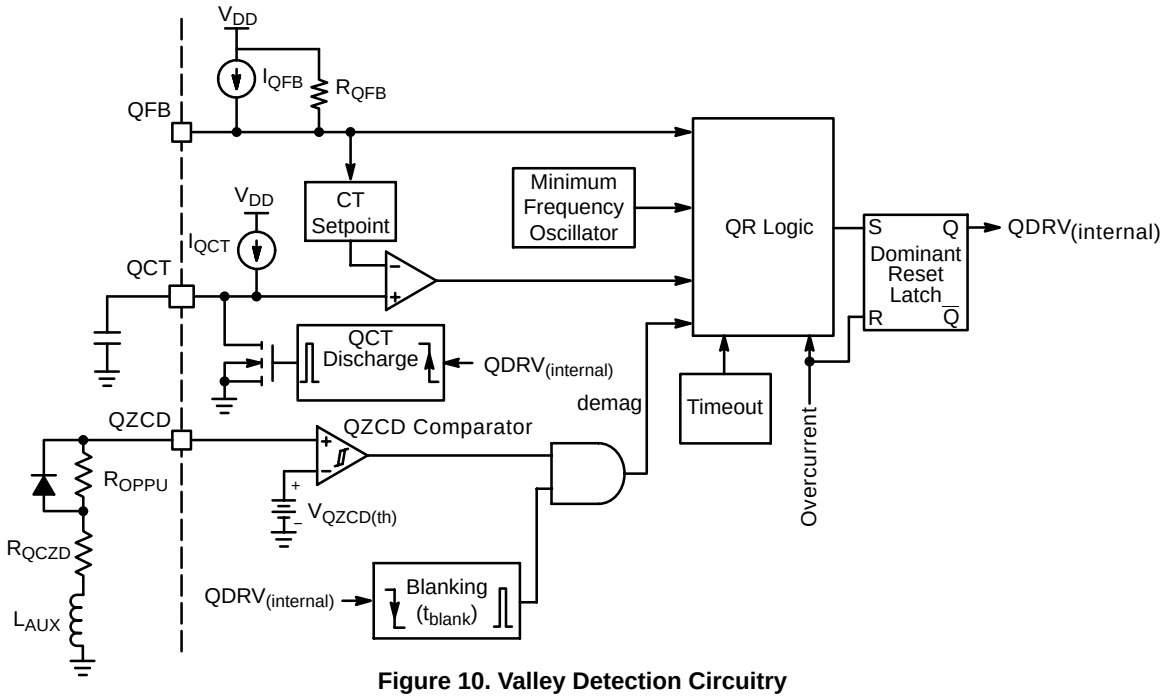


Figure 10. Valley Detection Circuitry

Figure 11 shows the operating valley versus V_{QFB}. Once a valley is asserted by the valley selection circuitry, the controller is locked in this valley until V_{QFB} decreases or increases such that V_{QFB} reaches the next valley threshold. A decrease in output power causes the controller to switch from “n” to “n+1” valley until reaching the 4th valley.

A further reduction of output power causes the controller to enter the voltage control oscillator (VCO) mode once V_{QFB} falls below V_{HVCOD}. In VCO mode the peak current is set to $V_{QILIM1}*KI_{peak(VCO)}$ as shown in Figure 12. The operating frequency in VCO mode is adjusted to deliver to required output power.

A hysteresis between valleys provides noise immunity and helps stabilize the valley selection in case of small perturbations on V_{QFB}.

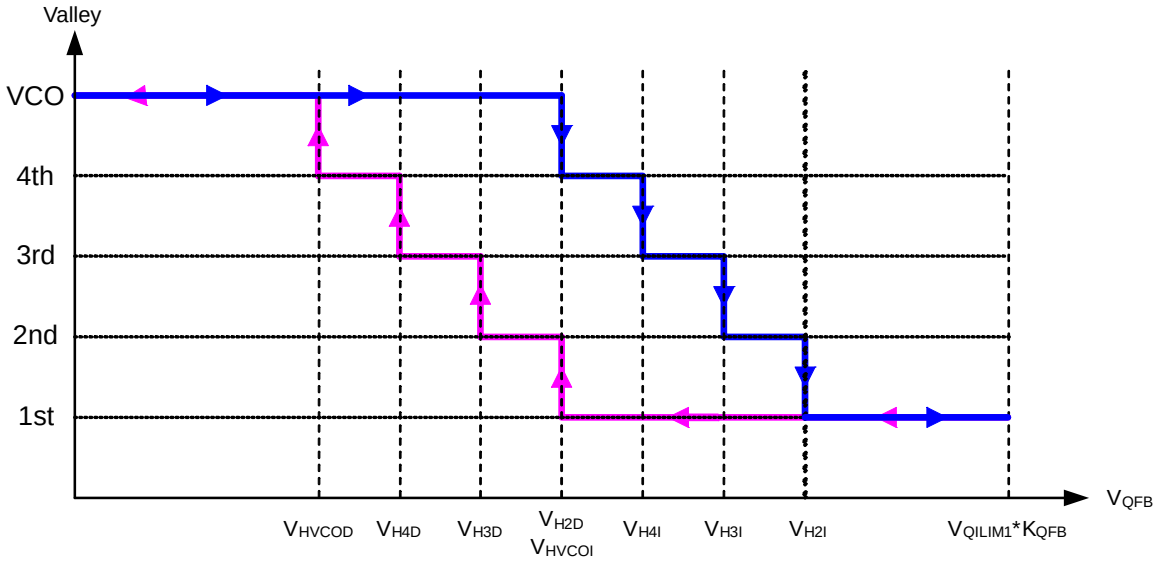


Figure 11. Selected Operating Valley versus V_{QFB}

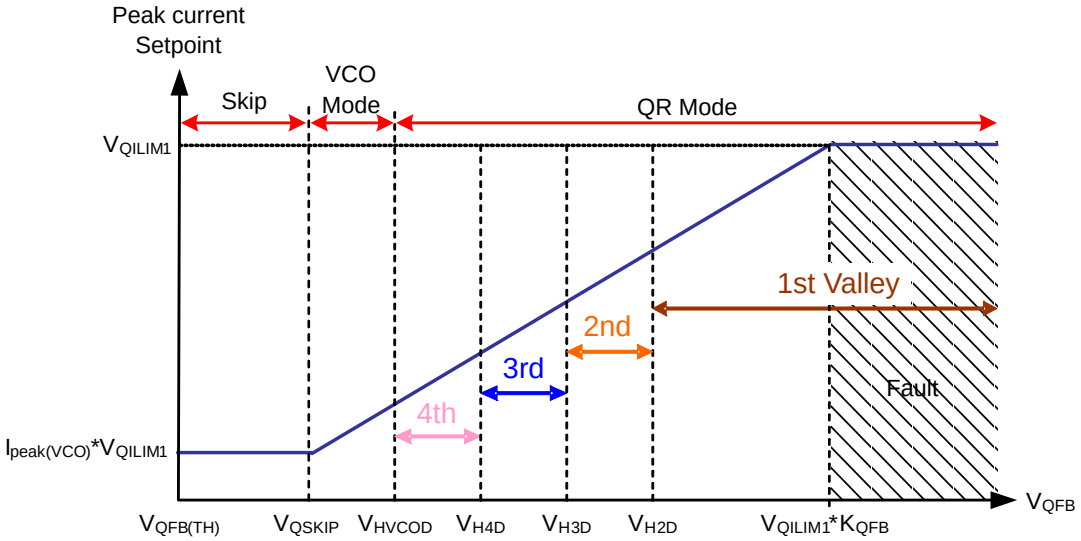


Figure 12. Operating Valley versus V_{QFB}

Figures 13 through 16 show drain voltage, V_{QFB} and V_{QCT} simulation waveforms for a reduction in output power. The transitions between 2nd to 3rd, 3rd to 4th and 4th valley to VCO mode are observed without any instabilities or valley jumping.

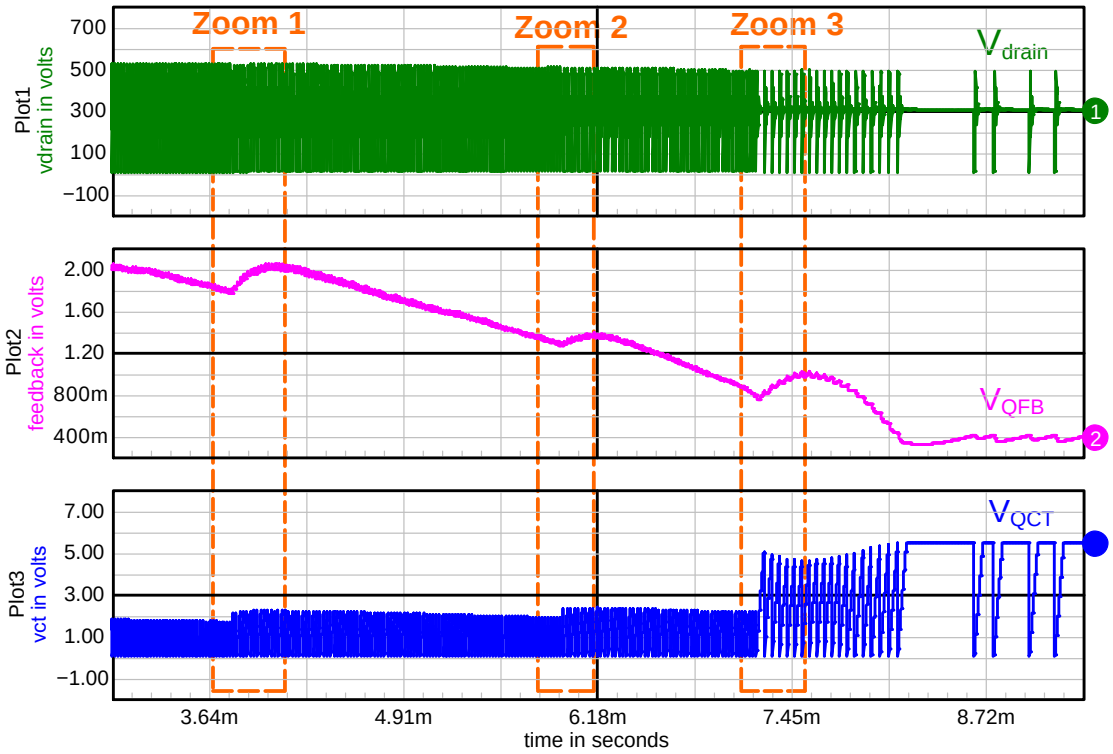


Figure 13. Operating Mode Transitions Between 2nd to 3rd, 3rd to 4th and 4th Valley to VCO Mode

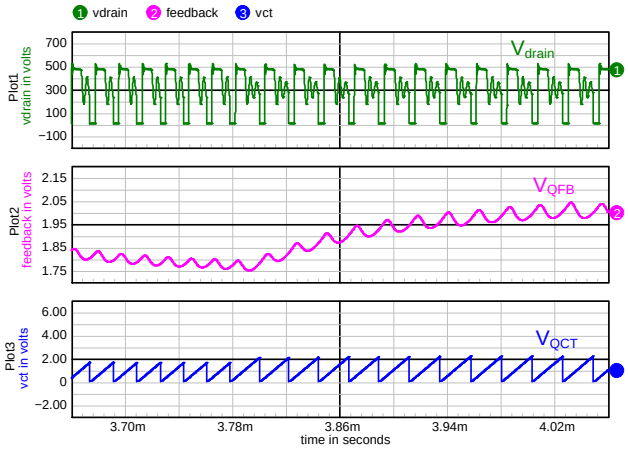


Figure 14. Zoom 1: 2nd to 3rd Valley Transition

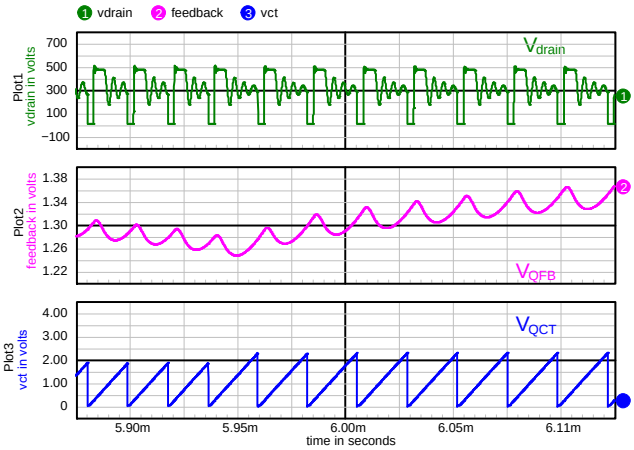


Figure 15. Zoom 2: 3rd to 4th Valley Transition

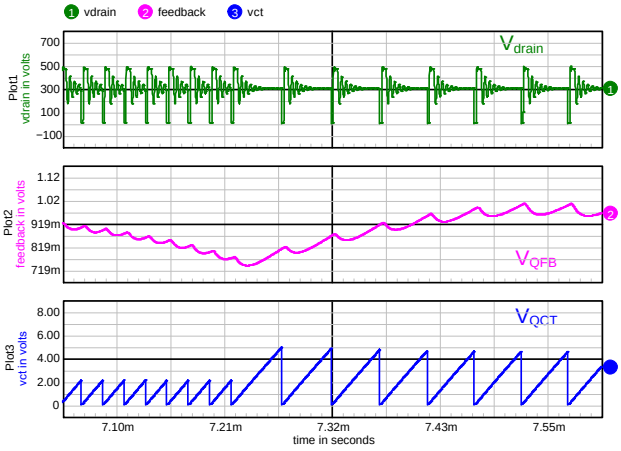


Figure 16. Zoom 3: 4th Valley to VCO Mode Transition

VCO MODE

The controller enters VCO mode once V_{QFB} falls below V_{HVCOD} and remains in VCO until V_{QFB} exceeds V_{HVCOI}. In VCO mode the peak current is set to V_{QILIM1}*$I_{peak(VCO)}$ and the operating frequency is linearly dependent on V_{QFB}. The product of V_{QILIM1}*$I_{peak(VCO)}$ is typically 12.5%. A minimum frequency clamp, $f_{VCO(MIN)}$, typically 27 kHz, prevents operation in the audible range. Further reduction in output power causes the controller to enter skip operation. The minimum frequency clamp is only enabled when operating in VCO mode.

The VCO mode operating frequency is set by the timing capacitor connected between the QCT and GND pins. This capacitor is charged with a constant current source, I_{QCT}, typically 20 μA.

The capacitor voltage, V_{QCT}, is compared to an internal voltage level, $V_{f(QFB)}$, inversely proportional to V_{QFB} The relationship between and $V_{f(QFB)}$ and V_{QFB} is given by Equation 2).

$$V_{f(QFB)} = 5 - 2 \cdot V_{QFB} \qquad \text{(eq. 2)}$$

A drive pulse is generated once V_{QCT} exceeds $V_{f(QFB)}$ followed by the immediate discharge of the timing capacitor. The timing capacitor is also discharged once the minimum frequency clamp is reached. Figure 17 shows simulation waveforms of $V_{f(QFB)}$, V_{QDRV} and output current while operating in VCO mode.

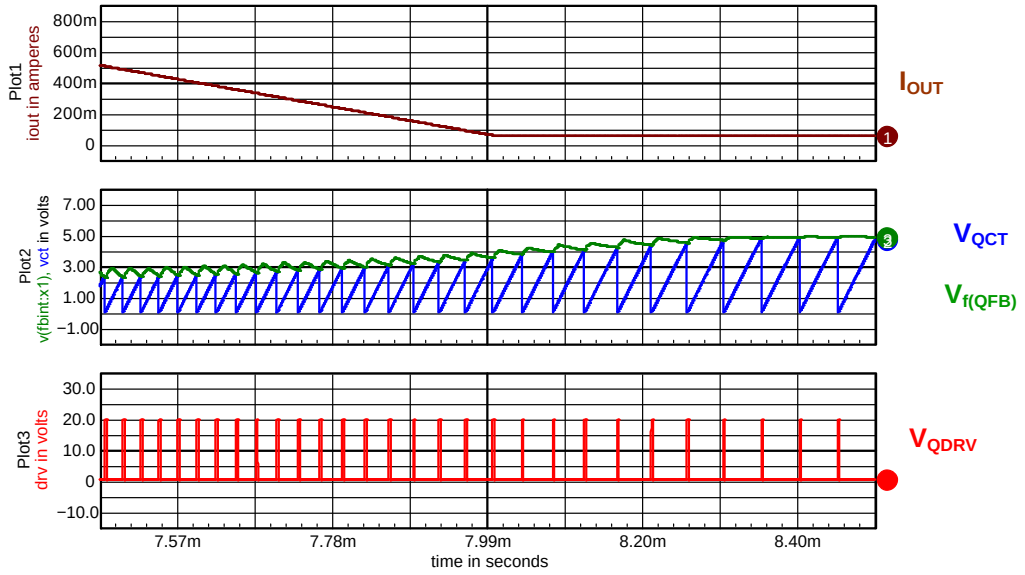


Figure 17. VCO Mode Operating Waveforms

FLYBACK TIMEOUT

In case of extremely damped oscillations, the QZCD comparator may be unable to detect the valleys. In this condition, drive pulses will stop waiting for the next valley or ZCD event. The NCL30030 ensures continued operation by incorporating a maximum timeout period after the last demagnetization detection. The timeout signal is a substitute for the ZCD signal for the valley counter. Figure 18 shows the timeout period generator circuit schematic. The steady state timeout period, $t_{Q(tout2)}$, is set at 6 μs to limit the frequency step.

During startup, the voltage offset added by the overpower compensation diode, D_{OPP}, prevents the QZCD Comparator from accurately detecting the valleys. In this condition, the steady state timeout period will be shorter than the inductor demagnetization period causing continuous current mode (CCM) operation. CCM operation lasts for a few cycles until the voltage on the QZCD pin is high enough to detect the valleys. A longer timeout period, $t_{Q(tout1)}$, (typically 100 μs) is set during soft−start to limit CCM operation. Figures 19 and 20 show the timeout period generator related waveforms.

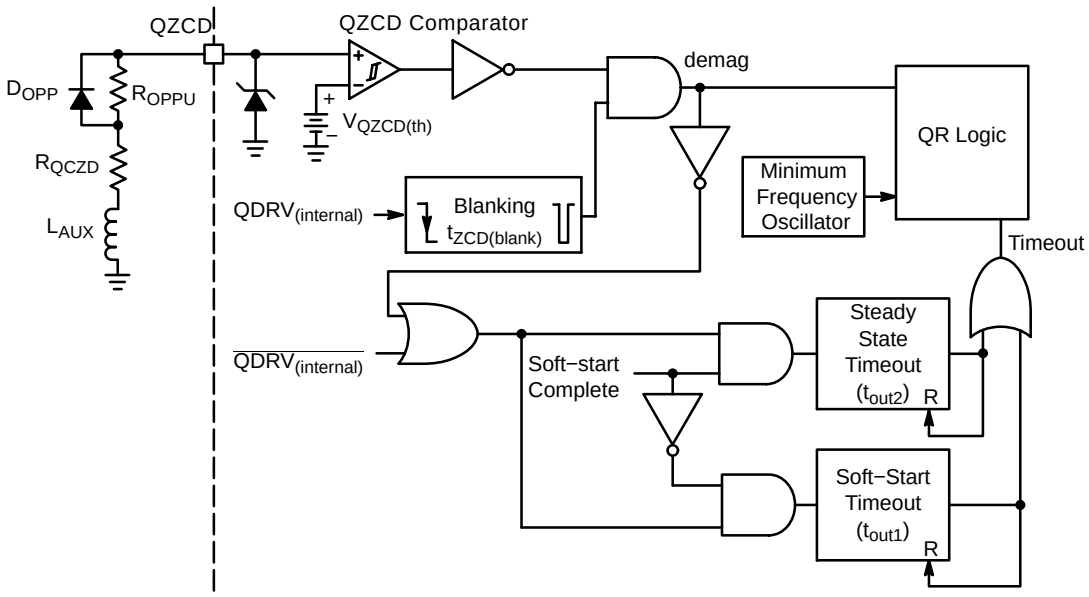


Figure 18. Timeout Period Generator Circuit Schematic

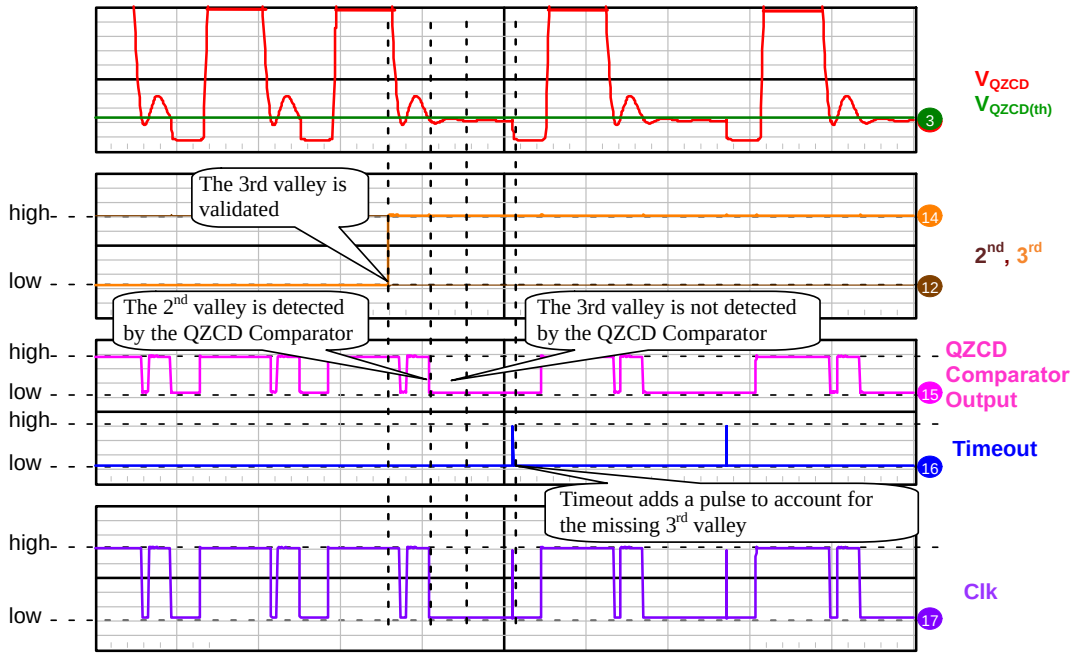


Figure 19. Timeout Operation With a Missing 3rd Valley

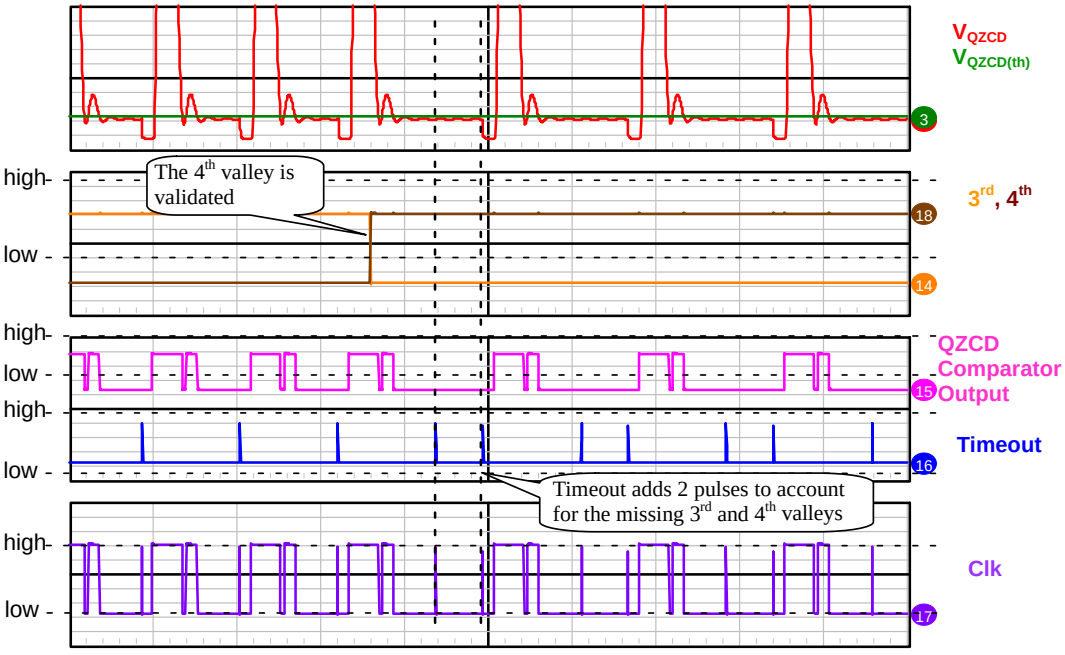


Figure 20. Timeout Operation With Missing 3rd and 4th Valleys

QR FLYBACK CURRENT SENSE AND OVERLOAD

The power switch on time is modulated by comparing a ramp proportional to the switch current to V_{QFB}/K_{QFB} using the PWM Comparator. The switch current is sensed across a current sense resistor, $R_{SENSE,}$ and the resulting voltage is applied to the QCS pin. The current signal is blanked by a leading edge blanking (LEB) circuit. The blanking period eliminates the leading edge spike and high frequency noise during the switch turn−on event. The LEB period, $t_{QCS(LEB1)}$, is typically 275 ns. The drive pulse terminates once the current sense signal exceeds V_{QFB}/K_{QFB}.

The Maximum Peak Current Comparator compares the current sense signal to a reference voltage to limit the maximum peak current of the system. The maximum peak current reference voltage, V_{QILIM1}, is typically 0.8 V. The maximum peak current setpoint is reduced by the overpower compensation circuitry. An overload condition causes the output of the Maximum Peak Current Comparator to transition high and enable the overload timer. Figure 21 shows the implementation of the current sensing circuitry.

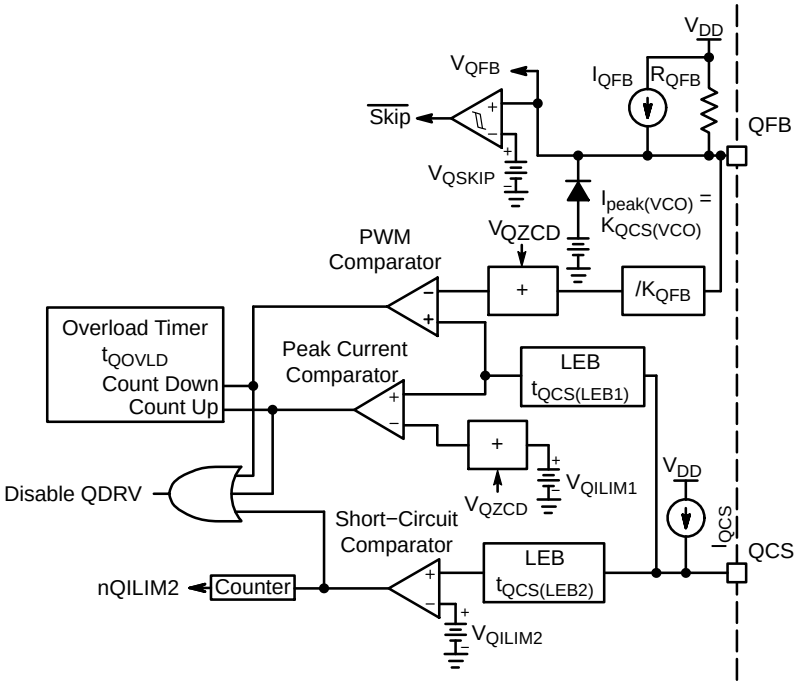


Figure 21. Current Sensing Circuitry Schematic

The overload timer integrates the duration of the overload fault. That is, the timer count increases while the fault is present and reduces its count once it is removed. The overload timer duration, t_{QOVLD}, is typically 80 ms. If both the PWM and Maximum Peak Current Comparators toggle at the same time, the PWM Comparator takes precedence and the overload timer counts down. The controller can latch (option A) or allow for auto−recovery (option B) once the overload timer expires. Auto−recovery requires a V_{CC} triple hiccup before the controller restarts. Figures 22 and 23 show operating waveforms for latched and auto−recovery overload conditions.

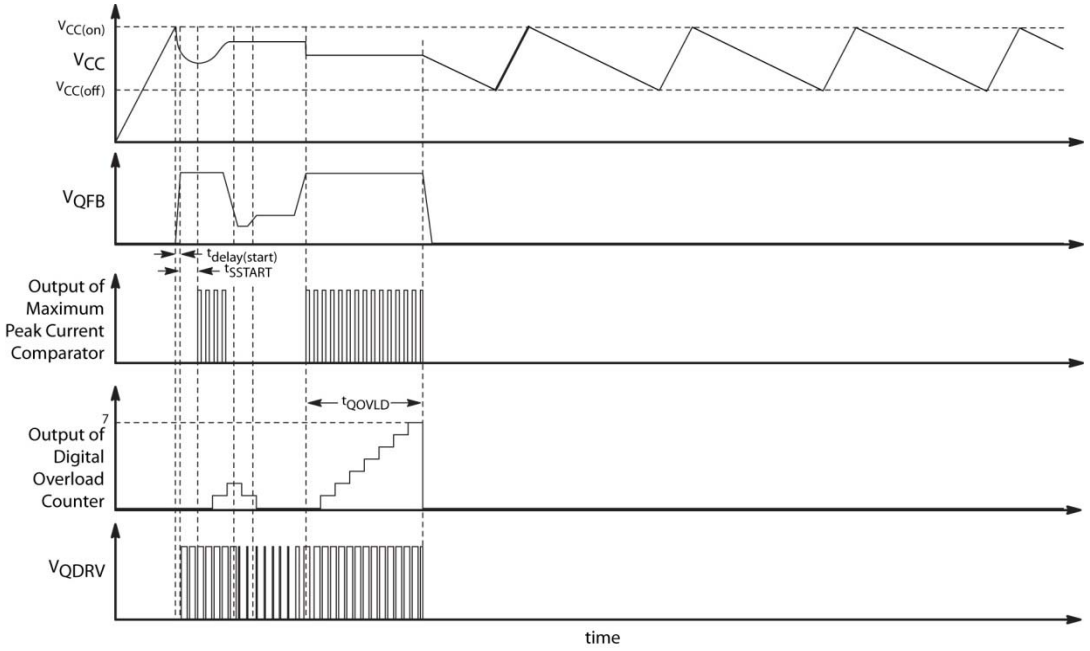


Figure 22. Latched Overload Operation

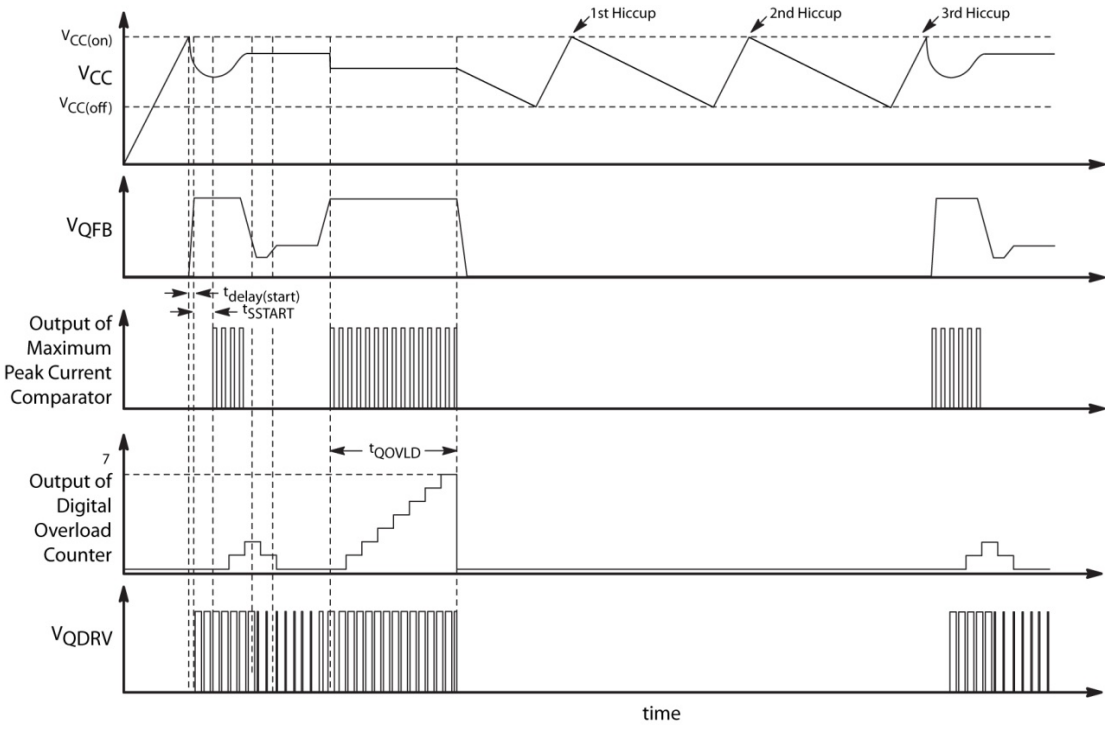


Figure 23. Auto−Recovery Overload Operation

A severe overload fault like a secondary side winding short−circuit causes the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{QILIM1}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the system current can get extremely high causing system damage.

The NCL30030 protects against this fault by adding an additional comparator, Fault Overcurrent Comparator. The current sense signal is blanked with a shorter LEB duration, $t_{QCS(LEB2)}$, typically 120 ns, before applying it to the Fault Overcurrent Comparator. The voltage threshold of the comparator, V_{QILIM2}, typically 1.2 V, is set 50% higher than V_{QILIM1}, to avoid interference with normal operation. Four

consecutive faults detected by the Fault Overcurrent Comparator causes the controller to enter triple−hiccup auto−recovery mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a QDRV pulse occurs without activating the Fault Overcurrent Comparator. A 1 μA (typically) pull−up current source, I_{QCS}, pulls up the QCS pin to disable the controller if the pin is left open.

QR FLYBACK SOFT−START

Soft−start is achieved by ramping up an internal reference, V_{SSTART}, and comparing it to current sense signal. V_{SSTART} ramps up from 0 V once the controller powers up. The soft−start duration, t_{SSTART}, is typically 4 ms.

During soft−start the timeout duration is extended and the lower latch or OTP Comparator signal (typically for overtemperature) is blanked. Soft−start ends once V_{SSTART} exceeds the peak current sense signal threshold.

QR FLYBACK OVERPOWER COMPENSATION

The input voltage of the QR flyback stage varies with the line voltage and operating mode of the PFC converter. At low line the PFC bulk voltage is 220 V and at high line it will be 390 V or 440 V, depending on the version of the part. Additionally, the PFC can be disabled at which point the PFC bulk voltage is set by the rectified peak line voltage.

An integrated overpower circuit provides a relative constant output power across PFC bulk voltage, V_{bulk}. It also reduces the variation on V_{QFB} during the PFC stage enable or disable transitions. Figure 24 shows the circuit schematic for the overpower detector.

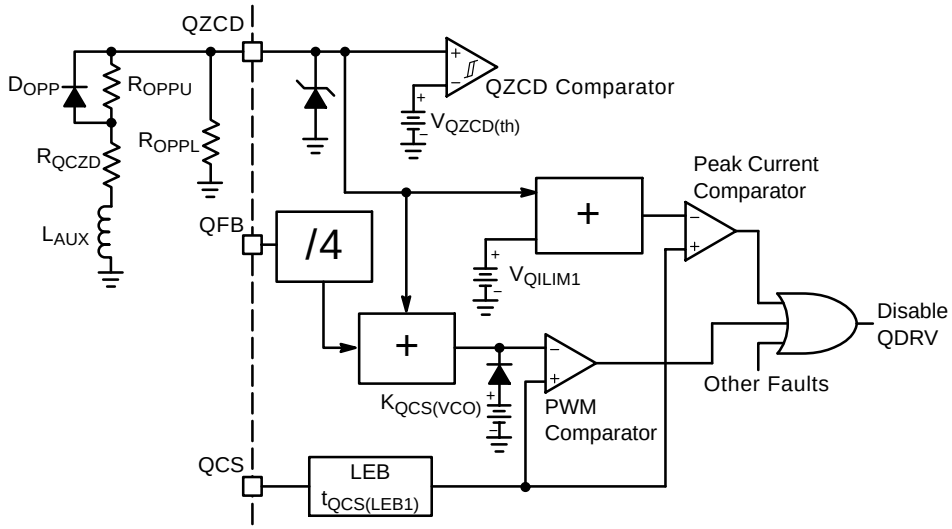


Figure 24. Overpower Compensation Circuit Schematic

The auxiliary winding voltage during the power switch on time is a reflection of the input voltage scaled by the primary to auxiliary winding turns ratio, $N_{P,AUX}$, as shown in Figure 25.

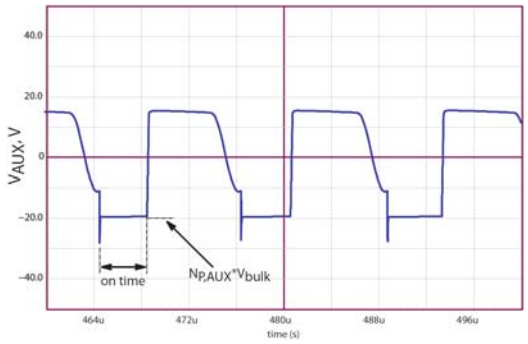


Figure 25. Auxiliary Winding Voltage Waveform

Overpower compensation is achieved by scaling down the on−time reflected voltage and applying it to the QZCD pin. The voltage is scaled down using R_{OPPU} and R_{OPPL}. The negative voltage applied to the pin is referred to as V_{OPP}.

The internal current setpoint is the sum of V_{OPP} and peak current sense threshold, V_{QILIM1}. V_{OPP} is also subtracted from V_{QFB} to compensate for the PWM Comparator delay and improve the PFC on/off accuracy.

The current setpoint is calculated using Equation 3. For example, a V_{OPP} of −0.15 V results in a current setpoint of 0.65 V.

$$\text{Current setpoint} = V_{QILIM1} + V_{OPP} \qquad \text{(eq. 3)}$$

To ensure optimal zero−crossing detection, a diode is needed to bypass R_{OPPU} during the off−time. Equation 4 is used to calculate R_{OPPU} and R_{OPPL}.

$$\frac{R_{QZCD} + R_{OPPU}}{R_{OPPL}} = -\frac{N_{P,AUX} \cdot V_{bulk} - V_{OPP}}{V_{OPP}} \qquad \text{(eq. 4)}$$

R_{OPPU} is selected once a value is chosen for R_{OPPL}. R_{OPPL} is selected large enough such that enough voltage is available for the zero crossing detection during the off−time.

It is recommended to have at least 8 V applied on the QZCD pin for good detection. The maximum voltage is internally clamped to V_{CC}. The off−time voltage on the QZCD is given by Equation 5.

$$V_{QZCD} = -\frac{R_{OPPL}}{R_{OZCD} + R_{OPPL}} \cdot (V_{AUX} - V_F) \quad \text{(eq. 5)}$$

Where V_{AUX} is the voltage across the auxiliary winding and V_F is the D_{OPP} forward voltage drop.

The ratio between R_{QZCD} and R_{OPPL} is given by Equation 6. It is obtained combining Equations 4 and 5.

$$\frac{R_{OZCD}}{R_{OPPL}} = \frac{V_{AUX} - V_F - V_{QZCD}}{V_{QZCD}} \quad \text{(eq. 6)}$$

A design example is shown below:

System Parameters:
V_{AUX} = 18 V
V_F = 0.6 V
$N_{P,AUX}$ = 0.18

The ratio between R_{QZCD} and R_{OPPL} is calculated using Equation 6 for a minimum V_{QZCD} of 8 V.

$$\frac{R_{OZCD}}{R_{OPPL}} = \frac{18 - 0.6 - 8}{8} \approx 1.2$$

R_{QZCD} is arbitrarily set to 1 kΩ. R_{OPPL} is also set to 1 kΩ because the ratio between the resistors is close to 1.

The NCL30030 maximum overpower compensation or peak current setpoint reduction is 31.25% for a V_{OPP} of −250 mV. We will use this value for the following example:

Substituting values in Equation 4 and solving for R_{OPPU} we obtain,

$$\frac{R_{QZCD} + R_{OPPU}}{R_{OPPL}} = -\frac{0.18 \cdot 370 - (-0.25)}{(-0.25)} = 271$$

$$R_{OPPU} = 271 \cdot R_{OPPL} - R_{QZCD}$$

$$R_{OPPU} = 271 \cdot 1k - 1k = 270k$$

POWER FACTOR CORRECTION

The PFC stage operates in critical conduction mode (CrM). In CrM the PFC inductor current, $I_L(t)$, reaches zero at the end of each switch cycle. Figure 26 shows the PFC inductor current while operating in CrM. High power factor and low harmonic distortion is achieved by shaping the input current, $I_{in}(t)$, such that it is sinusoidal and in phase with the ac line voltage, $V_{in}(t)$.

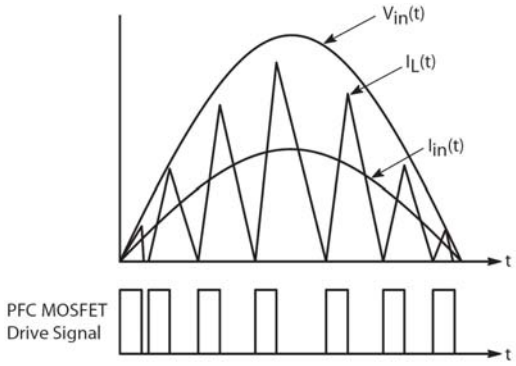


Figure 26. Inductor Current in CrM

To achieve unity power factor and low harmonic distortion the NCL30030 uses a peak current mode control architecture where the cycle−by−cycle current limit is set by a multiplier circuit. A block diagram of the control architecture is shown in Figure 27. The control works by generating a DC current proportional to the instantaneous AC line voltage and multiplying that current with the error voltage generated from the feedback error amplifier.

The multiplication factor is determined by the output of a comparator which measures the error voltage against a high frequency ramping signal. As the error voltage approaches its maximum value, the multiplication factor approaches 1. The output of the comparator toggles a switch to modulate the DC current from the current generator. The modulated current then feeds a resistor to set the peak current limit and hence control the duty cycle for every switching period. An external capacitor on the MULT pin is used to filter ripple caused by the modulation.

This control architecture is effectively a dual loop control method where the current generator shapes the peak current setpoint such that it follows the AC input while the error voltage adjusts the peak current to ensure that bulk voltage regulation is maintained.

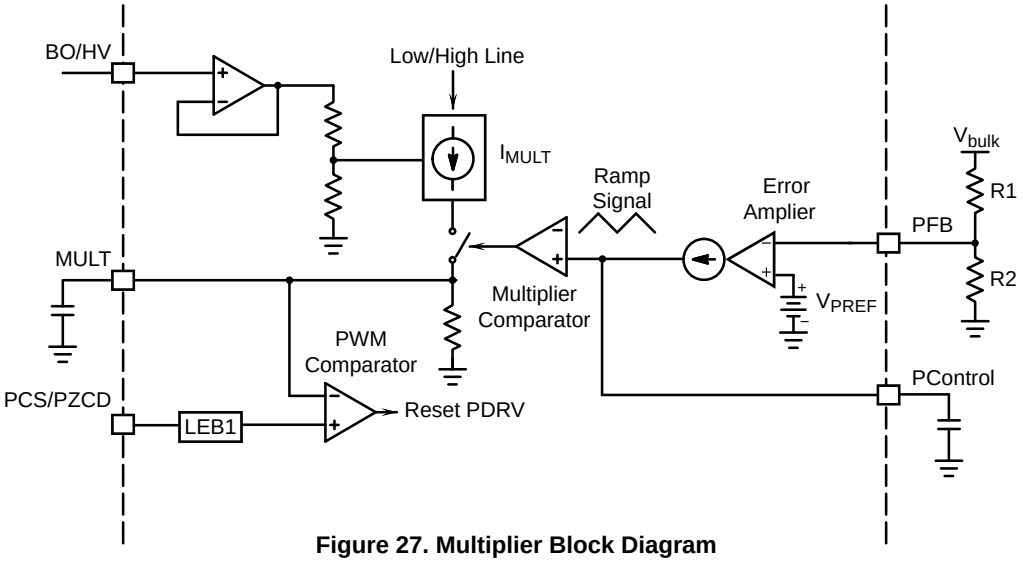


Figure 27. Multiplier Block Diagram

PFC FEEDBACK

The PFC feedback circuitry is shown in Figure 28. A resistor divider consisting of R1 and R2 scales down the PFC output voltage, V_{bulk}, to generate a PFC feedback signal. The feedback signal is applied to the inverting input of a transconductance error amplifier which regulates V_{bulk} by comparing the PFC feedback signal to an internal reference voltage, V_{PREF}. The reference is connected to the non−inverting input of the error amplifier and is trimmed during manufacturing to achieve an accuracy of ±2% across temperature.

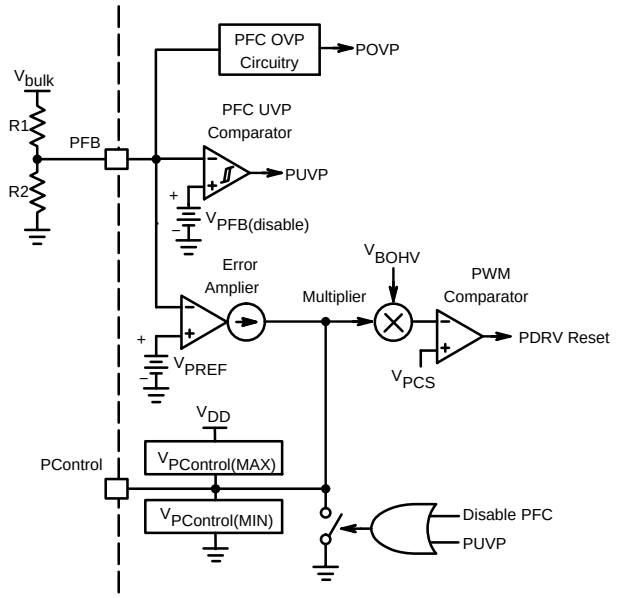


Figure 28. PFC Regulation Circuit Schematic

PFC ERROR AMPLIFIER

A transconductance amplifier has a voltage−to−current gain, g_m. That is, the amplifier's output current is controlled by the differential input voltage. The NCL30030 amplifier has a typical g_m of 200 μS. The PControl pin provides access to the amplifier output for compensation. The compensation network is ground referenced allowing the PFC feedback signal to detect undervoltage and overvoltage conditions as shown in Figure 28.

The compensation network on the PControl pin is selected to filter the bulk voltage ripple such that a constant control voltage is maintained across the ac line cycle. A capacitor between the PControl pin and ground sets a pole. A pole at or below 20 Hz is enough to filter the ripple voltage for a 50 and 60 Hz system. The low frequency pole, f_p, of the system is calculated using Equation 7.

$$f_p = \frac{gm}{2\pi C_{PControl}} \quad \text{(eq. 7)}$$

where, $C_{PControl}$ is the capacitor on the PControl pin to ground.

The output of the error amplifier is held low when the PFC is disabled by means of an internal pull−down transistor. The pull down transistor is disabled once the PFC stage is enabled. An internal voltage clamp is then enabled to quickly raise $V_{PControl}$ to its minimum voltage, $V_{PControl(min)}$, typically 0.6 V.

PFC TRANSIENT RESPONSE

The PFC bandwidth is set low enough to achieve good power factor. However, a low bandwidth system is slow and fast load transients can result in large output voltage excursions. The NCL30030 incorporates dedicated circuitry to help maintain regulation of the output voltage independent of load transients.

An undervoltage detector monitors the ratio between V_{PFB} and $V_{PREF(xL)}$. Once the ratio between V_{PFB} and $V_{PREF(xL)}$ exceeds $K_{LOW(PFCxL)}$, typically 5.5%, a pull−up current source on the PControl pin, $I_{PControl(boost)}$, is enabled to speed up the charge of the compensation network. This results in an increased on−time and thus output power. $I_{PControl(boost)}$ is typically 240 μA. The boost current source

is disabled once the ratio between V_{PFB} and $V_{PREF(xL)}$ drops below $K_{LOW(PFCxL)}$, typically 4%.

The boost current source becomes active as soon as the PFC is enabled. Coupled with the lower control clamp, the boost current source assists in rapidly bringing $V_{PControl}$ to its set point to allow the bulk voltage to quickly reach regulation. Achieving regulation is detected by monitoring the error amplifier output current. The error amplifier output current drops to zero once the PFC output voltage reaches the target regulation level.

The maximum PFC output voltage is limited by the overvoltage protection circuitry. The NCL30030 incorporates both soft and hard overvoltage protection. The hard overvoltage protection function immediately terminates and prevents further PFC drive pulses when V_{PFB} exceeds the hard−OVP level, V_{POVP} ($V_{PREF(xL)}$*$K_{POVP(xL)}$). Soft−OVP reduces the on−time proportional to the delta between V_{PFB} and the hard−OVP level. Soft−OVP is enabled once the delta, $\Delta_{POVP(xL)}$, between V_{PFB} and the hard−OVP level is between 20 and 55 mV. Figure 29 shows a block diagram of the boost and Soft−OVP circuits.

During power up, $V_{PControl}$ exceeds the regulation level due to the system's inherently low bandwidth. This causes the bulk voltage to rapidly increase and exceed its regulation. The on time starts to decrease when soft−OVP is activated. Once the bulk voltage decreases to its regulation level the PFC on time is no longer controlled by the soft−OVP circuitry.

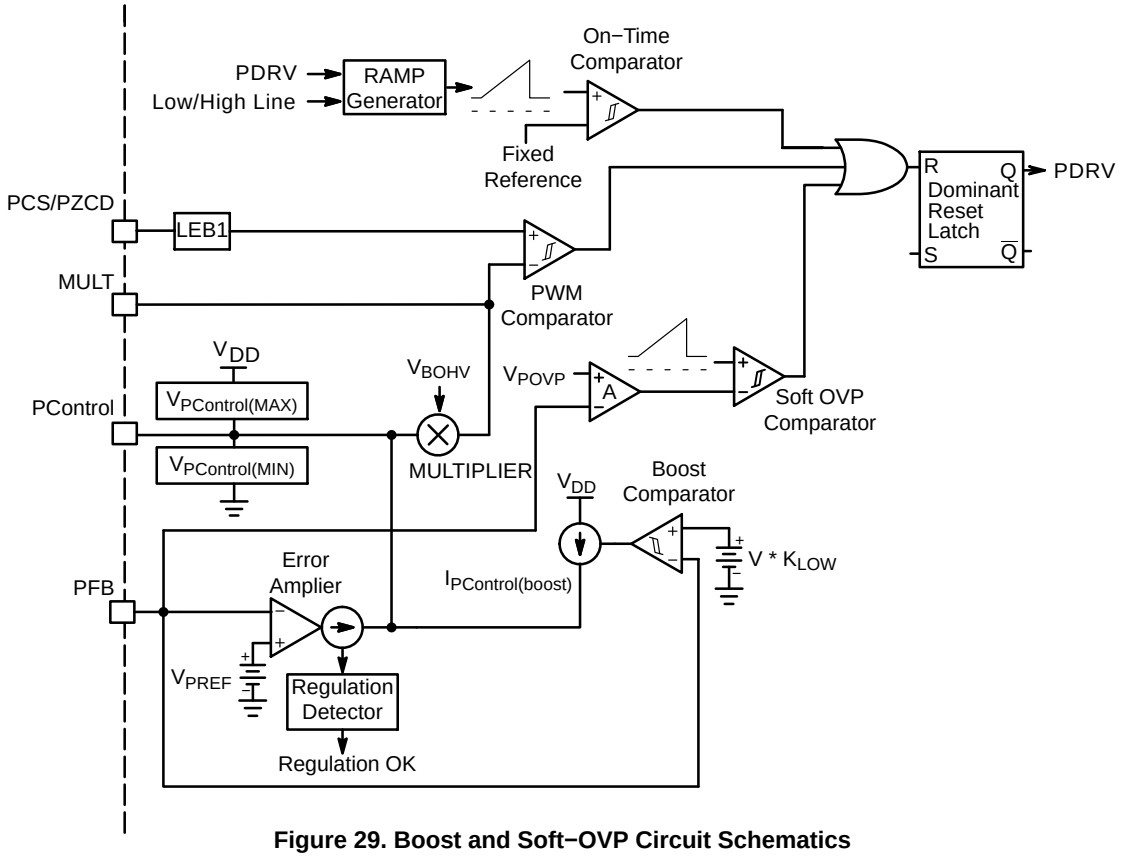


Figure 29. Boost and Soft−OVP Circuit Schematics

PFC CURRENT SENSE AND ZERO CURRENT DETECTION

The NCL30030 uses a novel architecture combining the PFC current sense and zero current detectors (ZCD) in a single input terminal. Figure 30 shows the circuit schematic of the current sense and ZCD detectors.

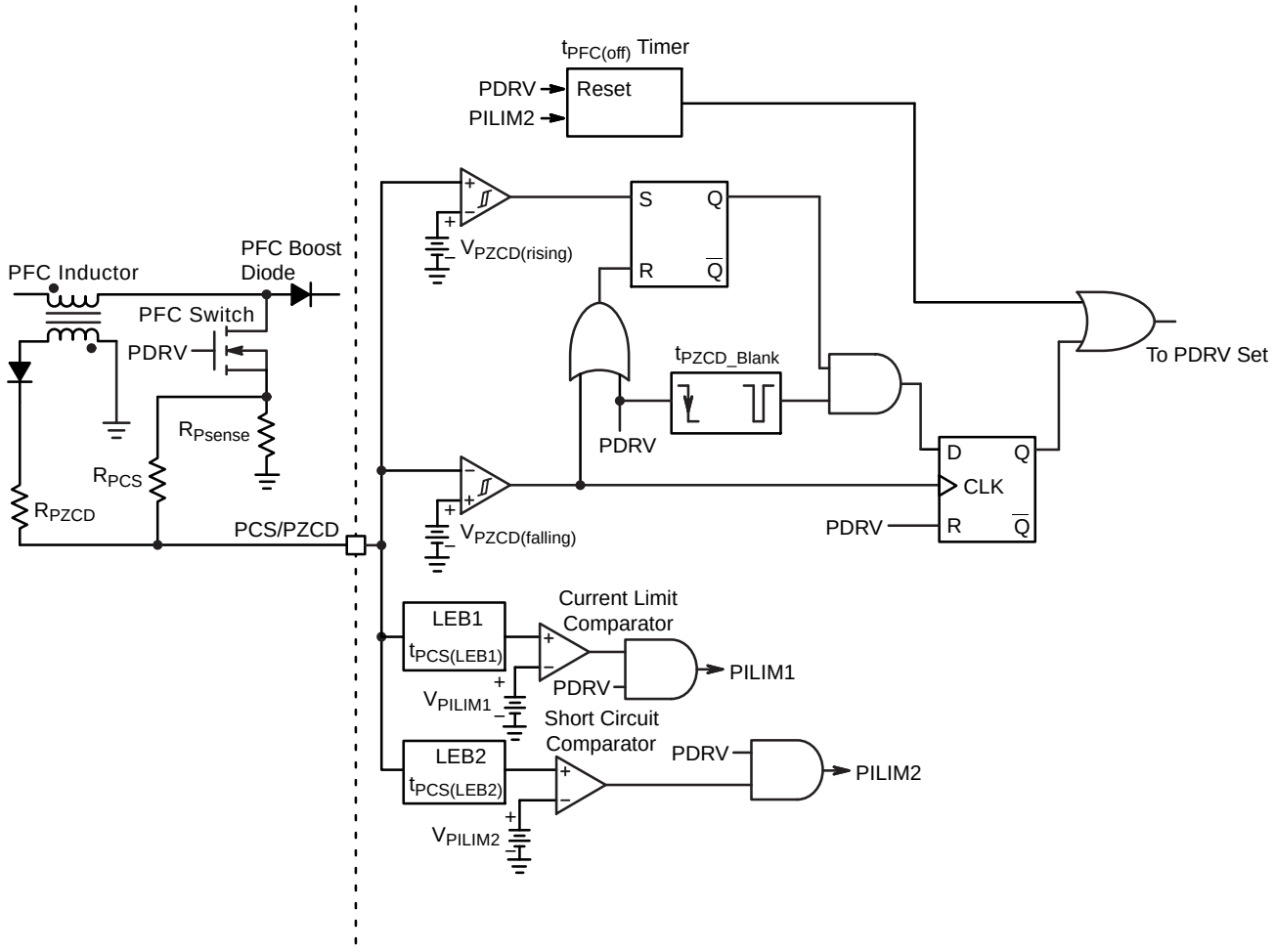


Figure 30. PFC Current Sense and ZCD Detectors Schematic

PFC CURRENT SENSE

The PFC Switch current is sensed across a sense resistor, R_{Psense}, and the resulting voltage ramp is applied to the PCS/PZCD pin. The current signal is blanked by a leading edge blanking (LEB) circuit. The blanking period eliminates the leading edge spike and high frequency noise during the switch turn−on event. The LEB period, $t_{PCS(LEB1)}$, is typically 325 ns. The Current Limit Comparator disables the PFC driver once the current sense signal exceeds the PFC current sense reference, V_{PILIM1}, typically 1.5 V.

A severe overload fault like a PFC boost diode short circuit causes the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{PILIM1}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the system current can get extremely high causing system damage.

The NCL30030 protects against this fault by adding an additional comparator, PFC Short Circuit Comparator. The current sense signal is blanked with a shorter LEB duration, $t_{PCS(LEB2)}$, typically 175 ns, before applying it to the PFC Short Circuit Comparator. The voltage threshold of the comparator, V_{PILIM2}, typically 2 V, is set 33% higher than V_{PILIM1}, to avoid interference with normal operation. Whenever a fault is detected by the Short Circuit Comparator, the watchdog timer increases to 1 ms allowing the system time to recover from the excessive over current. The next PFC drive pulse is then initiated when the watchdog timer expires.

PFC ZERO CURRENT DETECTION

The off−time in a CrM PFC topology varies with the instantaneous line voltage and is adjusted every switching cycle to allow the inductor current to reach zero before the next switching cycle begins. The inductor is demagnetized once its current reaches zero. Once the inductor is demagnetized the drain voltage of the PFC switch begins to drop. The inductor demagnetization is detected by sensing the voltage across the inductor using an auxiliary winding. This winding is commonly known as a zero crossing detector (ZCD) winding. This winding provides a scaled version of the inductor voltage. Figure 31 shows the ZCD winding arrangement.

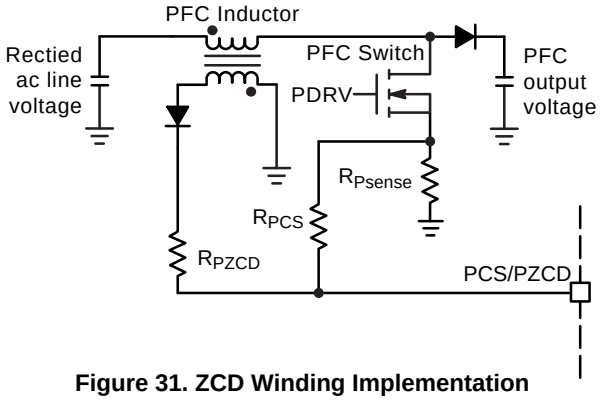


Figure 31. ZCD Winding Implementation

The ZCD voltage, V_{ZCD}, is positive while the PFC Switch is off and current flows through the PFC inductor. V_{ZCD} drops to and rings around zero volts once the inductor is demagnetized. The next switching cycle begins once a negative transition is detected on the PCS/PZCD pin. A positive transition (corresponding to the PFC switch turn off) arms the ZCD detector to prevent false triggering. The arming of the ZCD detector, $V_{PZCD(rising)}$, is typically 0.75 V. The trigger threshold, $V_{PZCD(falling)}$, is typically 0.25 V. The NCL30030 also incorporates a blanking period, T_{PZCD_Blank} which prevents detection of a ZCD event for 700 ns after the PFC switch turn off.

The PCS/PZCD pin is internally clamped to 5 V with a Zener diode and a 2 kΩ resistor. A resistor in series with the PCS/PZCD pin is required to limit the current into pin. The Zener diode also prevents the voltage from going below ground. Figure 32 shows typical ZCD waveforms.

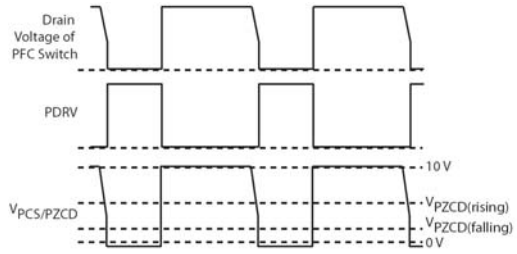


Figure 32. ZCD Winding Waveforms

During startup there are no ZCD transitions to set the PFC PWM Latch and generate a PDRV pulse. A watchdog timer, $t_{PFC(off1)}$, starts the drive pulses in the absence of ZCD transitions. Its duration is typically 200 μs. The timer is also useful if the line voltage transitions from low line to high line and while operating at light load because the amplitude of the ZCD signal may be too small to cross the ZCD arming threshold. The watchdog timer is reset at the beginning of a PFC drive pulse. It is disabled during a PFC hard overvoltage and feedback input short circuit condition.

PFC ENABLE & DISABLE

In some applications it is desired to disable the PFC at lighter loads to increase the overall system efficiency. The NCL30030 integrates a novel architecture that allows the user to program the PFC disable threshold based on the percentage of QR output power. The PFC enable circuitry is inactive until the QR flyback soft start period has ended. A voltage to current (V−I) converter generates a current proportional to V_{QFB}. This current is pulse width modulated by the demagnetization time of the flyback controller to generate a current, I_{PONOFF}, proportional to the output power. An external resistor, R_{PONOFF}, between the PONOFF and GND pins is used to scale the output power signal. A capacitor, C_{PONOFF}, in parallel with R_{PONOFF} is required to average the signal on this pin. A good compromise between voltage ripple and speed is achieved by setting the time constant of C_{PONOFF} and R_{PONOFF} to 160 μs.

The PONOFF pin voltage, V_{PONOFF}, is compared to an internal reference, V_{POFF} (typically 2 V) to disable the PFC stage. In high power SSL applications it is often desired to control the PFC disable point from the secondary side. An optocoupler can be used as a logic disable to ground the PONOFF pin when the PFC needs to be disabled.

Once V_{PONOFF} decreases below V_{POFF}, the PFC disable timer, $t_{Pdisable}$, is enabled. The PFC disable timer is typically 500 ms. The PFC stage is disabled once the timer expires. The PFC stage is enabled once V_{PONOFF} exceeds V_{POFF} by V_{PONHYS} for a period longer than the PFC enable filter, $t_{Penable(filter)}$, typically 100 μs. A shorter delay for the PFC enable threshold is used to reduce the bulk capacitor requirements during a step load response. Figure 33 shows the block diagram of the PFC disable circuit.

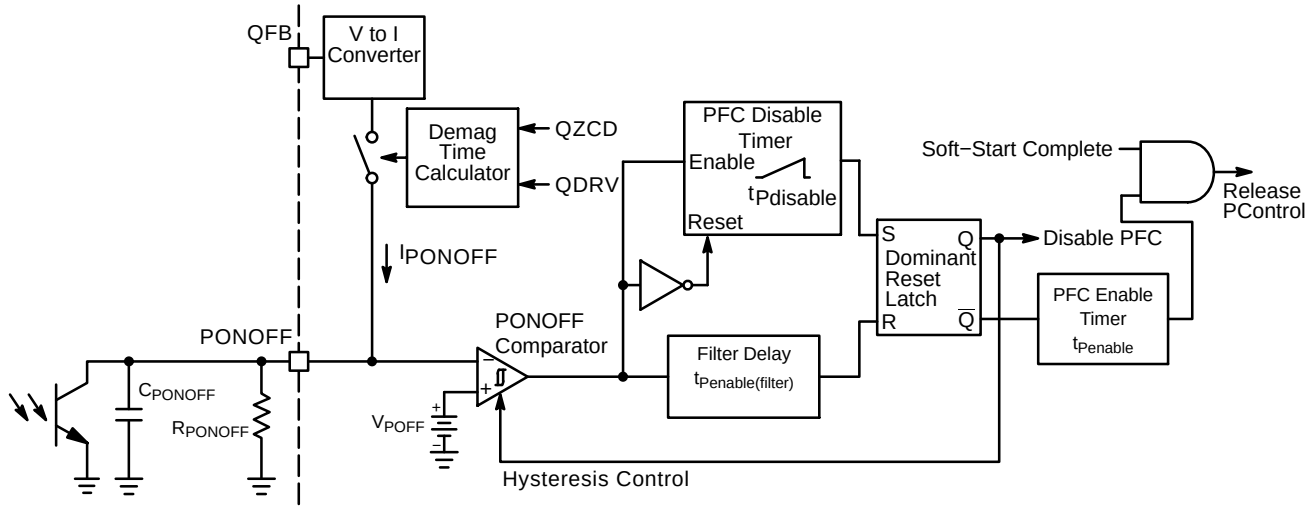


Figure 33. PFC On/Off Control Circuitry

PFC SKIP

The PFC stage incorporates skip cycle operation at light loads to reduce input power. Skip operation disables the PFC stage if the PControl voltage decreases below the skip threshold. The skip threshold voltage is typically 25 mV (ΔV_{PSKIP}) above the PControl minimum voltage clamp, $V_{PControl(MIN)}$. The PFC stage is enabled once $V_{PControl}$ increases above the skip threshold by the skip hysteresis, $V_{PSKIP(HYS)}$. PFC skip is disabled during any initial PFC startup and when the PFC is in a UVP. Skip operation will become active after the PFC has reached regulation.

PFC AND FLYBACK DRIVERS

The NCL30030 maximum supply voltage, $V_{CC(MAX)}$, is 30 V. Typical high voltage MOSFETs have a maximum gate voltage rating of 20 V. Both the PFC and flyback drivers incorporate an active voltage clamp to limit the gate voltage on the external MOSFETs. The PFC and flyback voltage clamps, $V_{PDRV(high2)}$ and $V_{QDRV(high2)}$, are typically 12 V with a maximum limit of 14 V.

AUTO−RECOVERY

The controller is disabled and enters “triple−hiccup” mode if V_{CC} drops below $V_{CC(off)}$. The controller will also enter “triple−hiccup” mode if an overload fault is detected on the non−latching version. A hiccup consists of V_{CC} falling down to $V_{CC(off)}$ and charging up to $V_{CC(on)}$. The controller needs to complete 3 hiccups before restarting.

TEMPERATURE SHUTDOWN

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 150°C. A continuous V_{CC} hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next $V_{CC(on)}$ once the IC temperature drops below below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 40°C.

The thermal shutdown fault is also cleared if V_{CC} drops below $V_{CC(reset)}$, a brown−out fault is detected or if the line voltage is removed. A new power up sequences commences at the next $V_{CC(on)}$ once all the faults are removed.

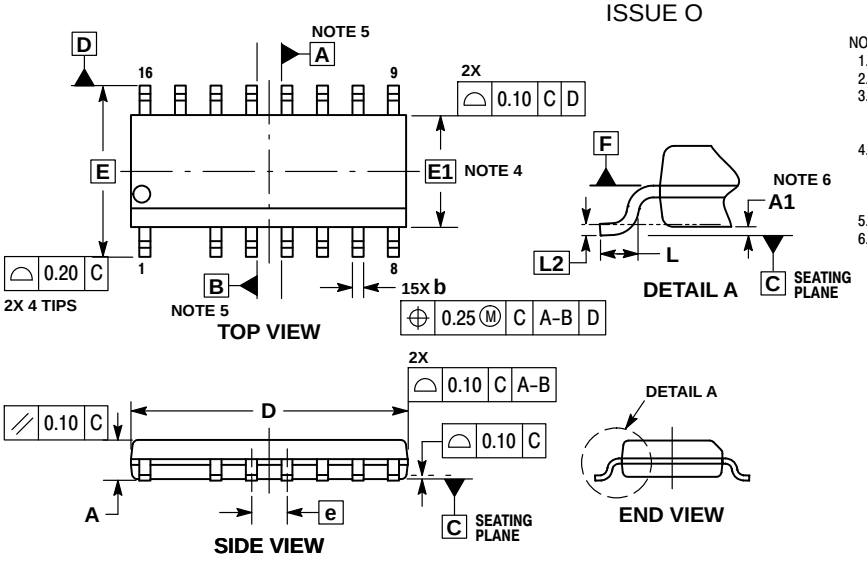
ORDERING INFORMATION

Device	Package	Shipping†
NCL30030B1DR2G	SOIC16 NB LESS PIN 2 (Pb−Free)	2500 / Tape & Reel
NCL30030B2DR2G		
NCL30030B3DR2G		
NCL30030A1DR2G*		
NCL30030A2DR2G*		
NCL30030A3DR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Please contact local sales representative for availability

PACKAGE DIMENSIONS

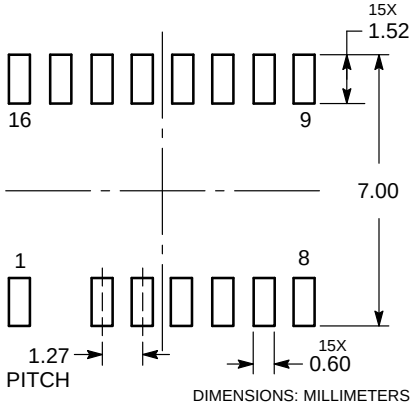
SOIC−16 NB MISSING PIN 2
CASE 751DT
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
c	0.17	0.25
D	9.80	10.00
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.203 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Телефон: 8 (812) 309-75-97 (многоканальный)
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Электронная почта: ocean@oceanchips.ru
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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А