Next Generation OP07 Ultralow Offset Voltage Operational Amplifier

OP77

FEATURES

Outstanding gain linearity
Ultrahigh gain, 5000 V/mV min
Low V_{OS} over temperature, 55 µV max
Excellent TCV_{OS}, 0.3 µV/°C max
High PSRR, 3 µV/V max
Low power consumption, 60 mW max
Fits OP07, 725,108A/308A, 741 sockets
Available in die form

PIN CONNECTIONS

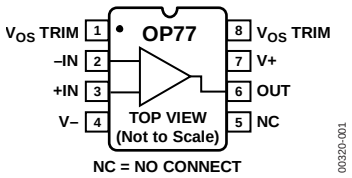


Figure 1. 8-Pin Hermetic DIP_Q-8 (Z Suffix)

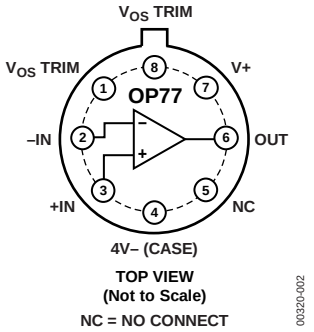


Figure 2. TO-99 (J Suffix)

GENERAL DESCRIPTION

The OP77 significantly advances the state-of-the-art in precision op amps. The outstanding gain of 10,000,000 or more for the OP77 is maintained over the full 10 V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps and provides superior performance in high closed-loop gain applications. Low initial V_{OS} drift and rapid stabilization time, combined with only 50 mW of power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3 µV/°C maximum and the low V_{OS} of 25 µV maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

A PSRR of 3 µV/V (110 dB) and CMRR of 1.0 µV/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP77 ideally suited for high resolution instrumentation and other tight error budget systems.

Rev. E
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REVISION HISTORY

4/10—Rev. D to Rev. E

Removed Figure 33 and Two Subsequent Paragraphs 12

6/09—Rev. C to Rev. D

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10/02—Rev. B to Rev. C

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2/02—Rev. A to Rev. B

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ELECTRICAL SPECIFICATIONS

@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.

Table 1.

			OP77E			OP77F			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE	V_{OS}			10	25		20	60	µV
LONG-TERM STABILITY[1]	V_{OS}/time			0.3			0.4		µV/Mo
INPUT OFFSET CURRENT	I_{OS}			0.3	1.5		0.3	2.8	nA
INPUT BIAS CURRENT	I_B		−0.2	+1.2	+2.0	−0.2	+1.2	+2.8	nA
INPUT NOISE VOLTAGE[2]	e_{np-p}	0.1 Hz to 10 Hz		0.35	0.6		0.38	0.65	μV_{p-p}
INPUT NOISE VOLTAGE DENSITY	e_n	f_O = 10 Hz		10.3	18.0		10.5	20.0	nV/√Hz
		f_O = 100 Hz[2]		10.0	13.0		10.2	13.5	
		f_O = 1000 Hz		9.6	11.0		9.8	11.5	
INPUT NOISE CURRENT[2]	i_{np-p}	0.1 Hz to 10 Hz		14	30		15	35	pA_{p-p}
INPUT NOISE CURRENT DENSITY	i_n	f_O = 10 Hz		0.32	0.80		0.35	0.90	pA√Hz
		f_O = 100 Hz[2]		0.14	0.23		0.15	0.27	
		f_O = 1000 Hz		0.12	0.17		0.13	0.18	
INPUT RESISTANCE									
Differential Mode[3]	R_{IN}		26	45		18.5	45		MΩ
Common Mode	R_{INCM}			200			200		GΩ
INPUT VOLTAGE RANGE	IVR		±13	±14		±13	±14		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V		0.1	1.0		0.1	1.6	µV/V
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±3 V to ±18 V		0.7	3.0		0.7	3.0	µV/V
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	R_L ≥ 2 kΩ	5000	12,000		2000	6000		V/mV
		V_O = ±10 V							
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 10 kΩ	±13.5	±14.0		±13.5	±14.0		V
		R_L ≥ 2 kΩ	±12.5	±13.0		±12.5	±13.0		
		R_L ≥ 1 kΩ	±12.0	±12.5		±12.0	±12.5		
SLEW RATE[2]	SR	R_L ≥ 2 kΩ	0.1	0.3		0.1	0.3		V/µs
CLOSED-LOOP BANDWIDTH[2]	BW	A_{VCL} + 1	0.4	0.6		0.4	0.6		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O			60			60		Ω
POWER CONSUMPTION	P_d	V_S = ±15 V, no load		50	60		50	60	mW
		V_S = ±3 V, no load		3.5	4.5		3.5	4.5	
OFFSET ADJUSTMENT RANGE		Rp = 20 kn		±3			±3		mV

[1] Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
[2] Sample tested.
[3] Guaranteed by design.

@ V_S = ±15 V, −25°C ≤ T_A ≤ +85°C for OP77FJ and OP77E/OP77F, unless otherwise noted.

Table 2.

			OP77E			OP77F			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE	V_{OS}			10	45		20	100	µV
AVERAGE INPUT OFFSET VOLTAGE DRIFT[1]	TCV_{OS}			0.1	0.3		0.2	0.6	µV/°C
INPUT OFFSET CURRENT	I_{OS}			0.5	2.2		0.5	4.5	nA
AVERAGE INPUT OFFSET CURRENT DRIFT[2]	TCI_{OS}			1.5	4.0		1.5	85	pA/°C
INPUT BIAS CURRENT	I_B		−0.2	+2.4	+4.0	−0.2	+2.4	+6.0	nA
AVERAGE INPUT BIAS CURRENT DRIFT[2]	TCI_B			8	40		15	60	pA/°C
INPUT VOLTAGE RANGE	IVR		±13.0	±13.5		±13.0	±13.5		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V		0.1	1.0		0.1	3.0	pV/V
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±3 V to ±18 V		1.0	3.0		1.0	5.0	µV/V
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	R_L ≥ 2 kΩ V_O = ±10 V	2000	6000		1000	4000		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13.0		±12	±13.0		V
POWER CONSUMPTION	P_d	V_S = ±15 V, no load		60	75		60	75	mW

[1] OP77E: TCV_{OS} is 100% tested on J and Z packages.
[2] Guaranteed by end-point limits.

WAFER TEST LIMITS

@ V_S = ±15 V, T_A = 25°C, for OP77NBC devices, unless otherwise noted.

Table 3.

Parameter	**Symbol**	**Conditions**	**OP77NBC Limit**	**Unit**
INPUT OFFSET VOLTAGE	V_{OS}		40	µV max
INPUT OFFSET CURRENT	I_{OS}		2.0	nA max
INPUT BIAS CURRENT	I_B		±2	nA max
INPUT RESISTANCE Differential Mode	R_{IN}		26	MΩ min
INPUT VOLTAGE RANGE	IVR		±13	V min
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V	1	µV/V max
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±3 V to ±18 V	3	µV/V max
OUTPUT VOLTAGE SWING	V_O	R_L = 10 kΩ R_L = 2 kΩ R_L = 1 kΩ	±13.5 ±12.5 ±12.0	V min
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	R_L = 2 kΩ V_O = ±10 V	2000	V/mV min
DIFFERENTIAL INPUT VOLTAGE			±30	V max
POWER CONSUMPTION	P_d	V_O = 0 V	60	mW max

TYPICAL ELECTRICAL CHARACTERISTICS

@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	OP77NBC Limit	Unit
AVERAGE INPUT OFFSET VOLTAGE DRIFT	TCV_{OS}	R_S = 50 Ω	0.1	µV/°C
NULLED INPUT OFFSET VOLTAGE DRIFT	TCV_{OSn}	R_S = 50 Ω, R_P = 20 kΩ	0.1	µV/°C
AVERAGE INPUT OFFSET CURRENT DRIFT	TCI_{OS}		0.5	pA/°C
SLEW RATE	SR	R_L ≥ 2 kΩ	0.3	V/µs
BANDWIDTH	BW	A_{VCL} + 1	0.6	MHz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter[1]	Rating
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[2]	±22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−25°C to +85°C
Junction Temperature (T_J)	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1]Absolute Maximum Ratings apply to both dice and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Pin TO-99 H-08 (J Suffix)	150	18	°C/W
8-Lead Hermetic CERDIP Q-8 (Z Suffix)	148	16	°C/W

[1]θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for a device in socket for the TO-99 and CERDIP packages.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

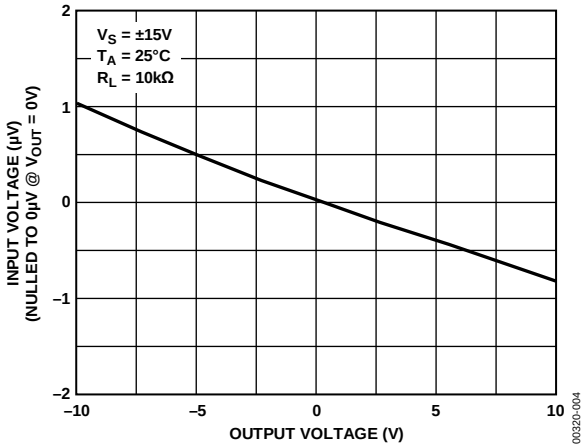


Figure 3. Gain Linearity (Input Voltage vs. Output Voltage)

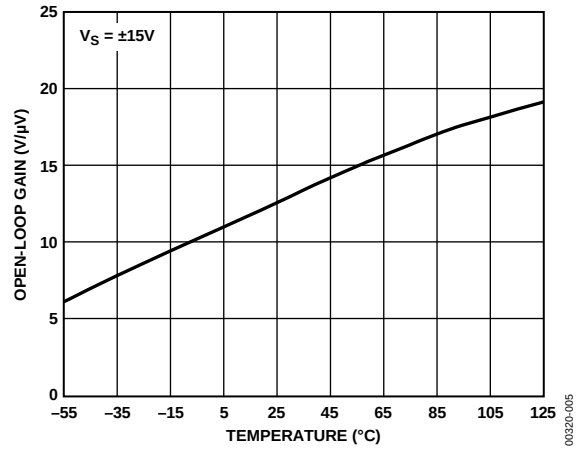


Figure 4. Open-Loop Gain vs. Temperature

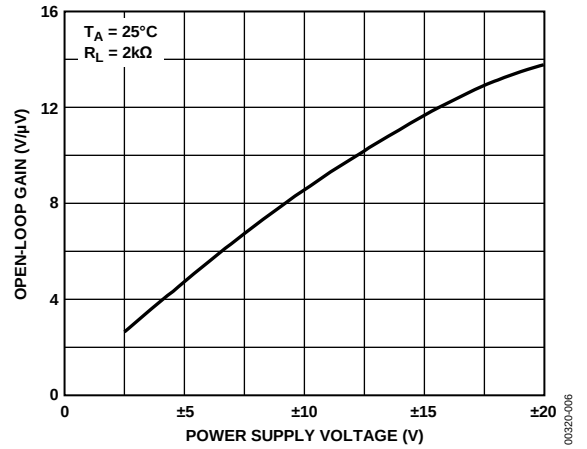


Figure 5. Open-Loop Gain vs. Power Supply Voltage

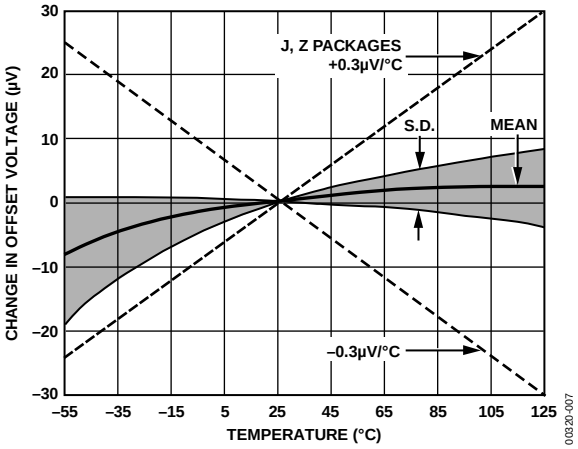


Figure 6. Untrimmed Offset Voltage vs. Temperature

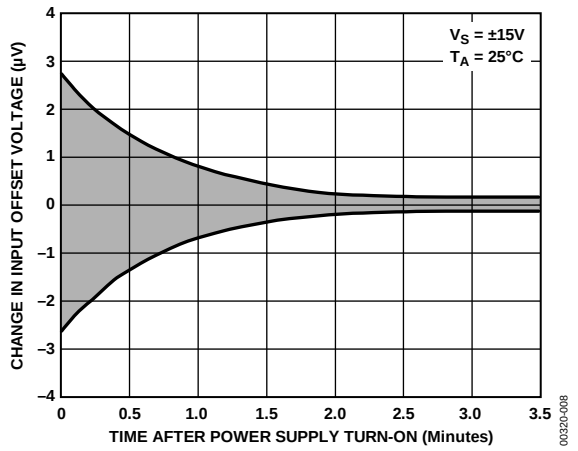


Figure 7. Warm-Up Drift

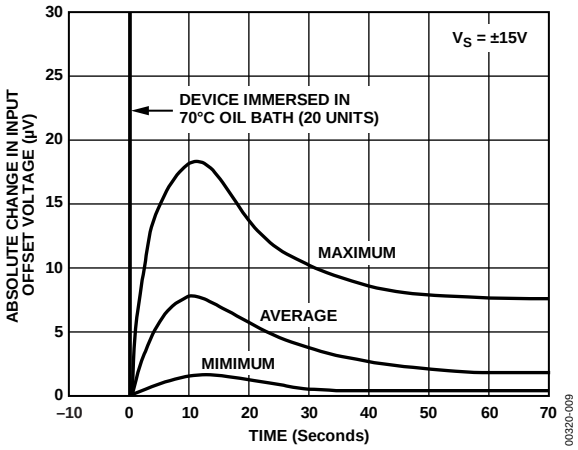


Figure 8. Offset Voltage Change Due to Thermal Shock

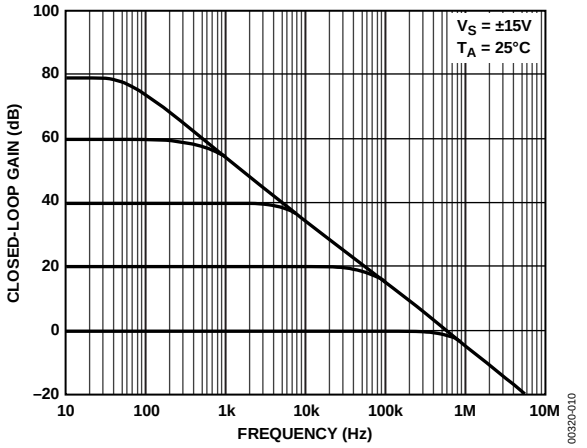


Figure 9. Closed-Loop Response for Various Gain Configurations

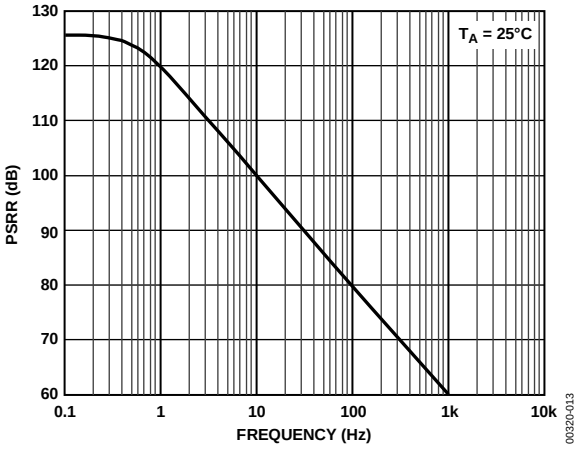


Figure 12. PSRR vs. Frequency

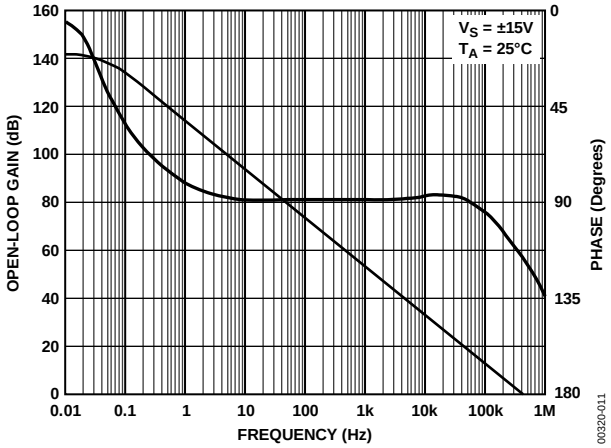


Figure 10. Open-Loop Gain/Phase Response

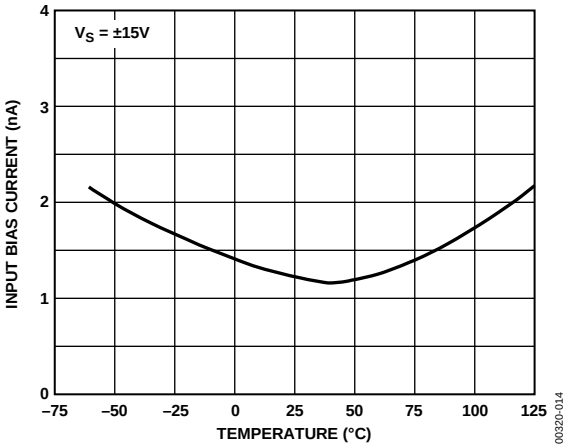


Figure 13. Input Bias Current vs. Temperature

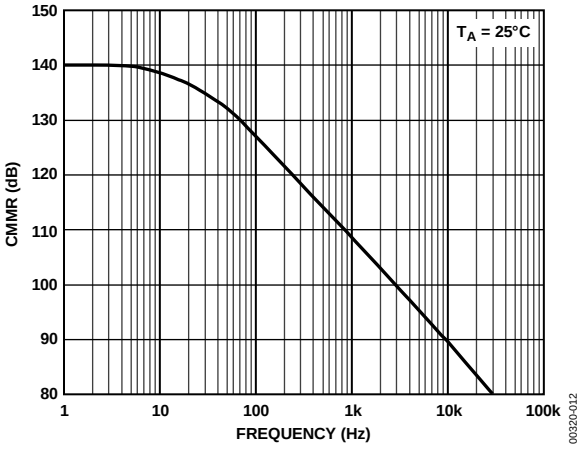


Figure 11. CMRR vs. Frequency

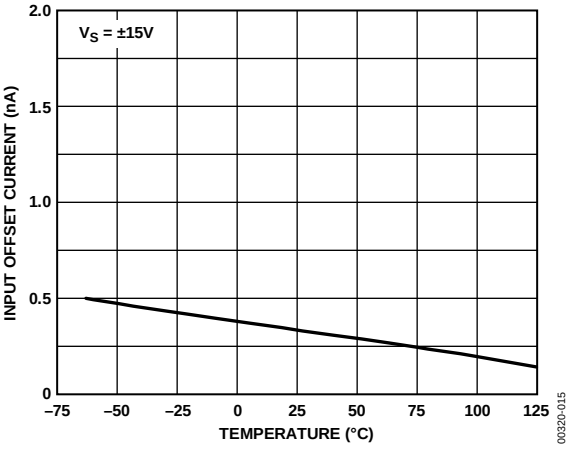


Figure 14. Input Offset Current vs. Temperature

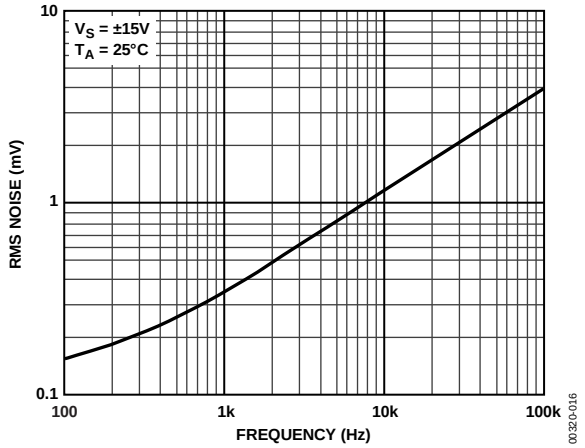


Figure 15. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

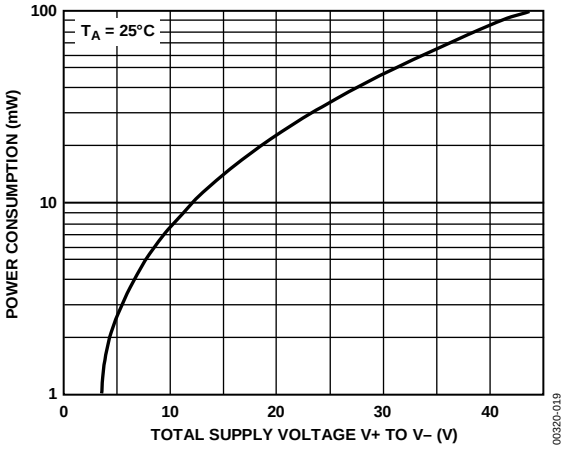


Figure 18. Power Consumption vs. Power Supply

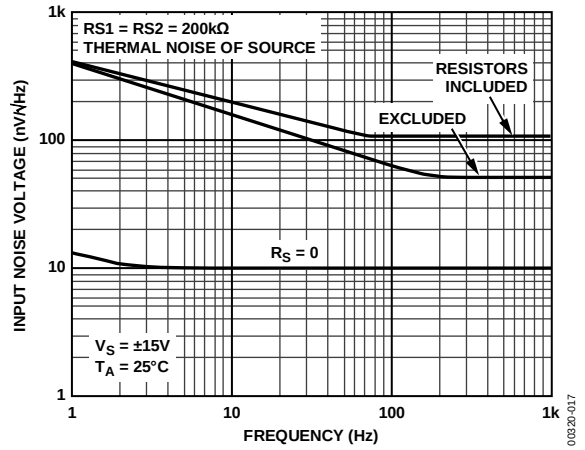


Figure 16. Total Input Noise Voltage vs. Frequency

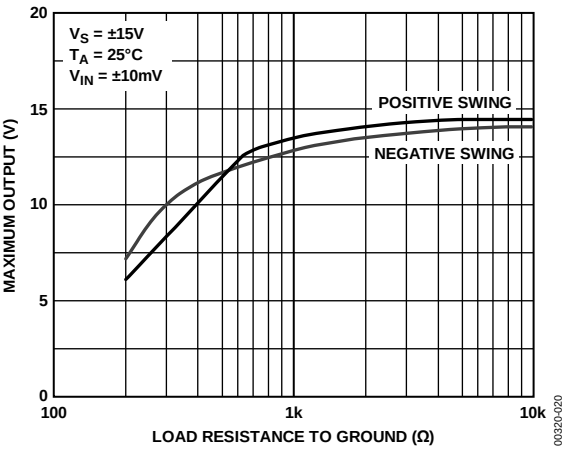


Figure 19. Maximum Output Voltage vs. Load Resistance

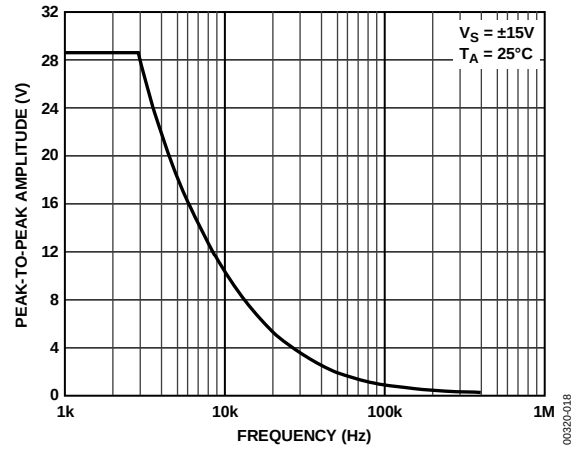


Figure 17. Maximum Output Swing vs. Frequency

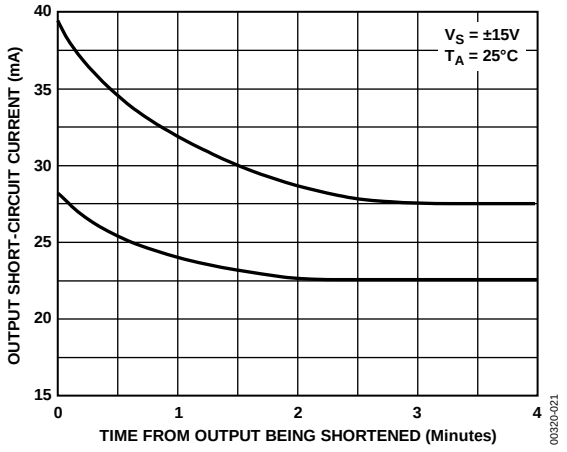


Figure 20. Output Short-Circuit Current vs. Time

TEST CIRCUITS

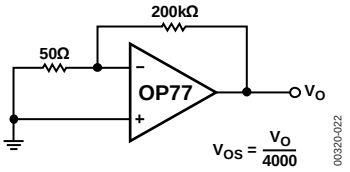


Figure 21. Typical Offset Voltage Test Circuit

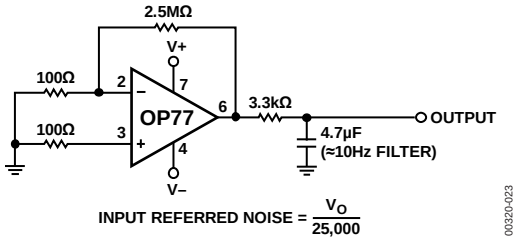


Figure 22. Typical Low-Frequency Noise Test Circuit

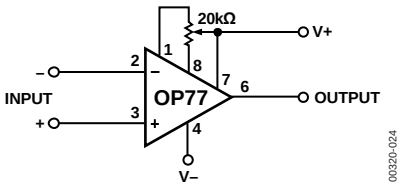


Figure 23. Optional Offset Nulling Circuit

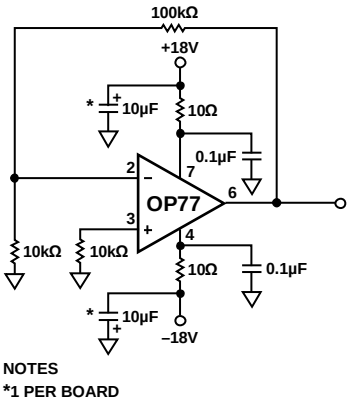


Figure 24. Burn-In Circuit

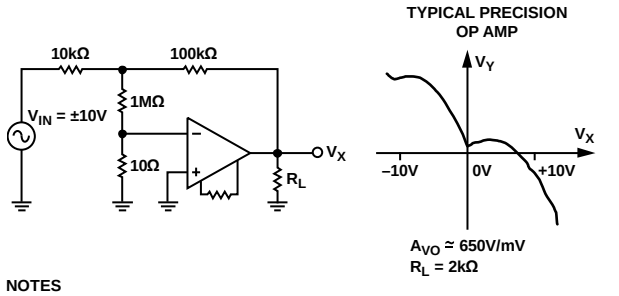


Figure 25. Open-Loop Gain Linearity

Actual open-loop voltage gain can vary greatly at various output voltages. All automated testers use endpoint testing and therefore only show the average gain. This causes errors in high closed-loop gain circuits. Because this is difficult for manufacturers to test, users should make their own evaluations. This simple test circuit makes it easy. An ideal op amp would show a horizontal scope trace.

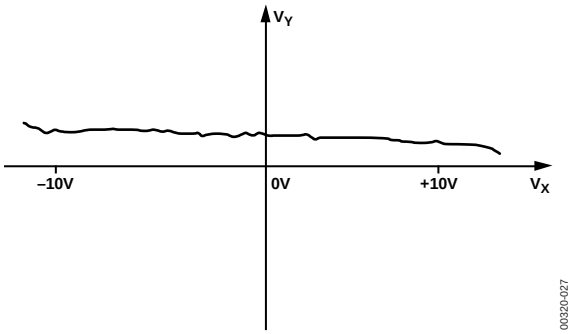


Figure 26. Output Gain Linearity Trace

This is the output gain linearity trace for the new OP77. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. The average open-loop gain is truly impressive—approximately 10,000,000.

APPLICATIONS

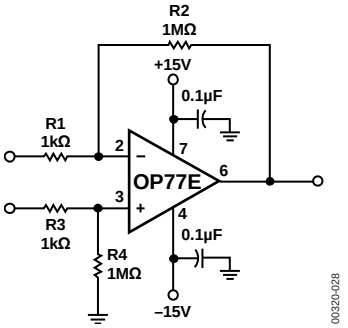


Figure 27. Precision High-Gain Differential Amplifier

The high gain, gain linearity, CMRR, and low TCV_{OS} of the OP77 make it possible to obtain performance not previously available in single-stage, very high-gain amplifier applications.

For best CMR, $\frac{R1}{R2}$ must equal $\frac{R3}{R4}$. In this example, with a 10 mV differential signal, the maximum errors are as listed in Table 7.

Table 7. Maximum Errors

Type	Amount
Common-Mode Voltage	0.01%/V
Gain Linearity, Worst Case	0.02%
TCV_{OS}	0.003%/°C
TCI_{OS}	0.008%/°C

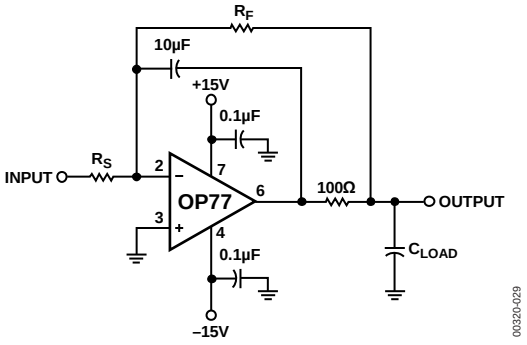


Figure 28. Isolating Large Capacitive Loads

This circuit reduces maximum slew rate but allows driving capacitive loads of any size without instability. Because the boon resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP77.

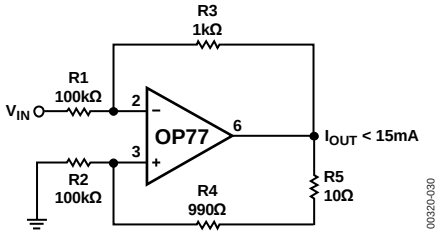


Figure 29. Basic Current Source

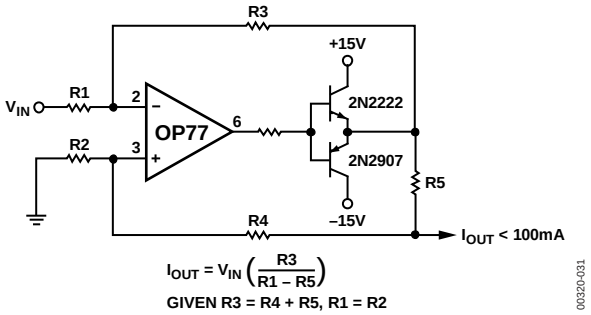


Figure 30. 100 mA Current Source

These current sources can supply both positive and negative current into a grounded load.

Note that

$$Z_O = \frac{R5\left(\frac{R4}{R2}+1\right)}{\frac{R5+R4}{R2}\frac{R3}{R1}}$$

And that for Z_O to be infinite $\frac{R5+R4}{R2}$ must = $\frac{R3}{R1}$

PRECISION CURRENT SINKS

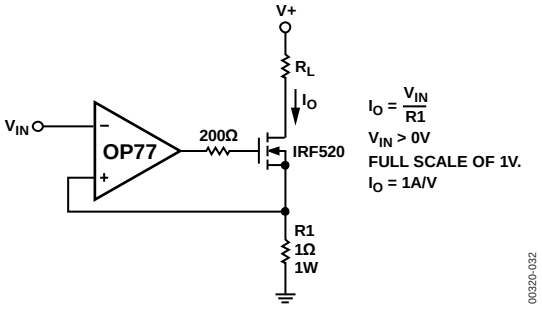


Figure 31. Positive Current Sink

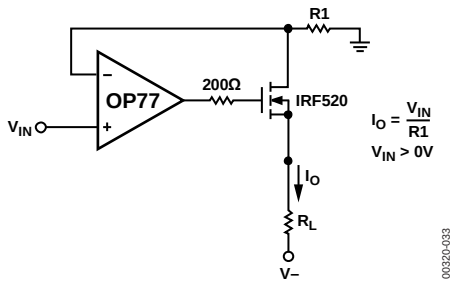


Figure 32. Positive Current Source

The simple high-current sinks, shown Figure 31 and Figure 32, require the load to float between the power supply and the sink.

In these circuits, the high gain, high CMRR, and low TCV_{OS} of the OP77 ensure high accuracy.

The high gain and low TCV_{OS} ensure accurate operation with inputs from microvolts to volts. In Figure 33, the signal always appears as a common-mode signal to the op amps. The OP77EZ CMRR of 1 µV/V ensures errors of less than 2 ppm.

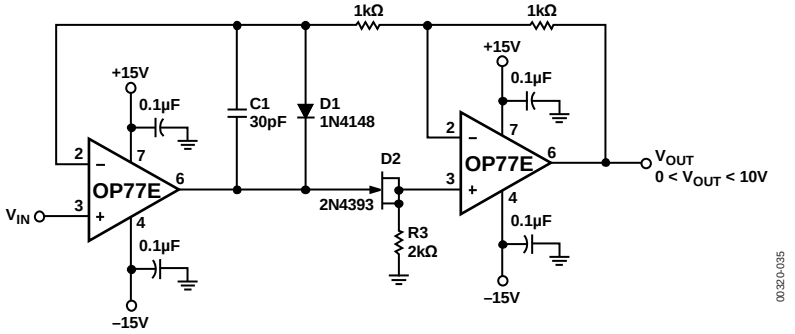


Figure 33. Precision Absolute Value Amplifier

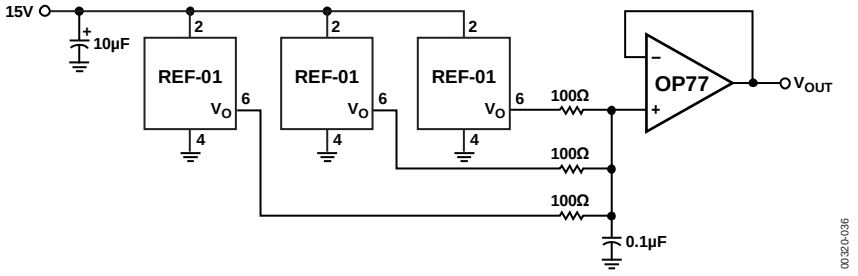


Figure 34. Low Noise Precision Reference

Figure 34 relies upon low TCV_{OS} of the OP77 and noise combined with very high CMRR to provide precision buffering of the averaged REF-01 voltage outputs.

In Figure 35, C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the AD820.

*Teflon is a registered trademark of the Dupont Company

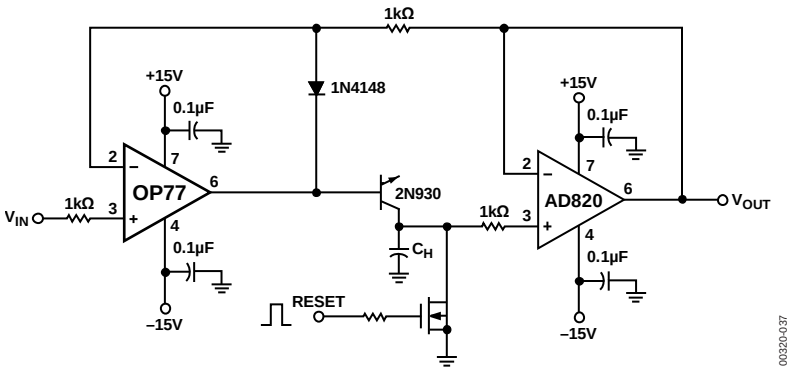


Figure 35. Precision Positive Peak Detector

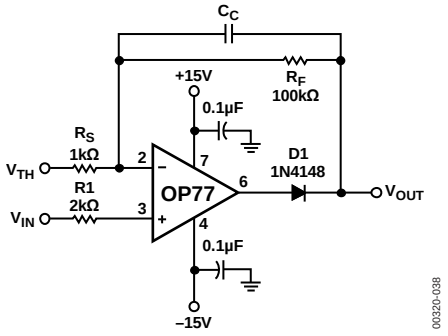


Figure 36. Precision Threshold Detector/Amplifier

When $V_{IN} < V_{TH}$, amplifier output swings negative, reversing the biasing diode D1. $V_O = V_{TH}$ if $R_L = \infty$ when $V_{IN} > V_{TH}$, the loop closes,

$$V_O = V_{TH} + \left(V_{IN} - V_{TH}\right)\left(1 + \frac{R_F}{R_S}\right)$$

C_C is selected to smooth the response of the loop.

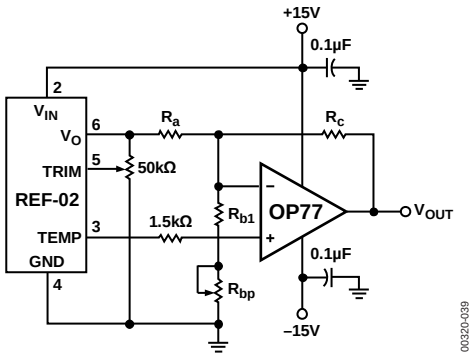
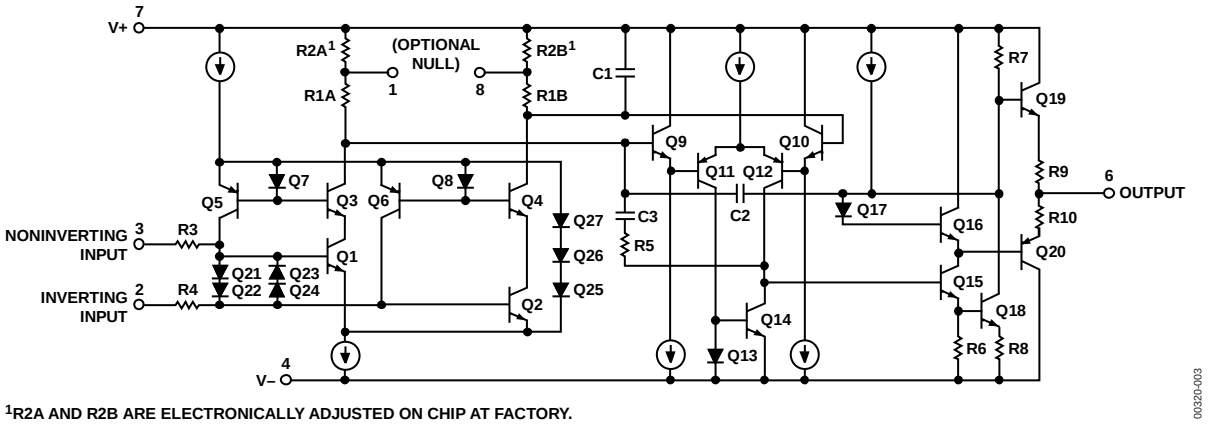


Figure 37. Precision Temperature Sensor

Table 8. Resistor Values

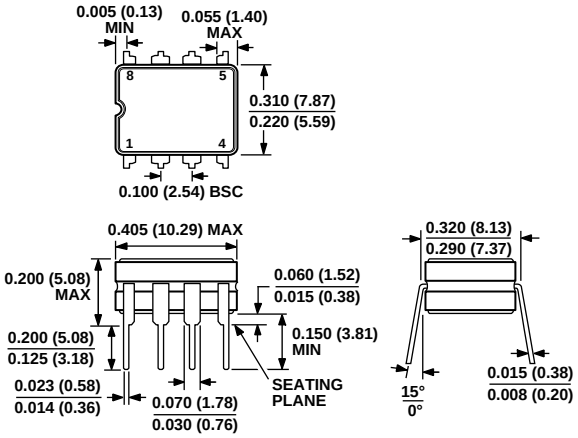
TCV_{OUT} Slope (S)	10 mV/°C	100 mV/°C	10 mV/°F
Temperature Range	−55°C to +125°C	−55°C to +125°C	−67°F to +257°C
Output Voltage Range	−0.55 V to +1.25 V	−5.5 V to +12.5V	−0.67 V to +2.57V
Zero-Scale	0 V @ 0°C	0 V @ 0°C	0 V @ 0°F
R_a (±1% Resistor)	9.09 kΩ	15 kΩ	7.5 kΩ
R_{b1} (±1% Resistor)	1.5 kΩ	1.82 kΩ	1.21 kΩ
R_{bp} (Potentiometer)	200 Ω	500 Ω	200 Ω
R_c (±1% Resistor)	5.11 kΩ	84.5 kΩ	8.25 kΩ



[1]R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY.

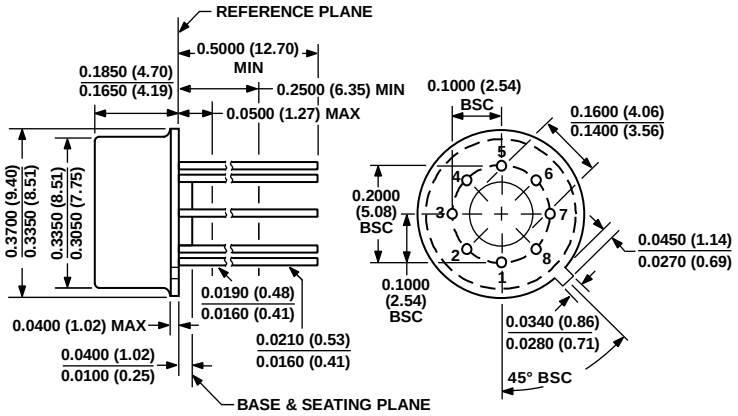
Figure 38. Simplified Schematic

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 39. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-002-AK
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

022306-A

Figure 40. 8-Pin Metal Header [TO-99]
(H-08)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP77FJ	−25°C to +85°C	8-Pin Metal Header [TO-99]	H-08 (J Suffix)
OP77FJZ	−25°C to +85°C	8-Pin Metal Header [TO-99]	H-08 (J Suffix)
OP77EZ	−25°C to +85°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8 (Z Suffix)
OP77FZ	−25°C to +85°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8 (Z Suffix)
OP77NBC		Die	

[1] Z = RoHS Compliant Part.

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D00320-0-4/10(E)

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