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October 2010

# 74AUP1G97 TinyLogic<sup>®</sup> Low Power Universal Configurable Two-Input Logic Gate

#### **Features**

- 0.8V to 3.6V V<sub>CC</sub> Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at V<sub>CC</sub> from 0.8V to 3.6V
- High Speed tpd
  - 3.1ns: Typical at 3.3V
- Power-Off High-Impedance Inputs and Outputs
- Low Static Power Consumption
  - I<sub>CC</sub>=0.9µA Maximum
- Low Dynamic Power Consumption
  - CPD=2.5pF Typical at 3.3V
- Ultra-Small MicroPak™ Packages

#### Description

The 74AUP1G97 is a universal configurable 2-input logic gate that provides a high performance and low power solution ideal for battery-powered portable applications. This product is designed for a wide low voltage operating range (0.8V to 3.6V) and guarantees very low static and dynamic power consumption across the entire voltage range. All inputs are implemented with hysteresis to allow for slower transition input signals and better switching noise immunity.

The 74AUP1G97 provides for multiple functions as determined by various configurations of the three inputs. The potential logic functions provided are MUX, AND, OR, NAND, and NOR, inverter and buffer. Refer to Figures 3 to 9.

## **Ordering Information**

Part Number	Top Mark	Package	Packing Method
74AUP1G97L6X	AD	6-Lead MicroPak™, 1.0mm Wide	5000 Units on Tape & Reel
74AUP1G97FHX	AD	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

## **Logic Diagram**

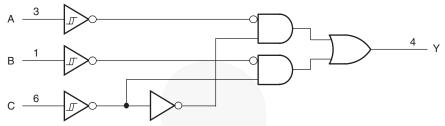


Figure 1. Logic Diagram (Positive Logic)

## **Pin Configurations**

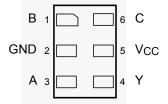


Figure 2. MicroPak™ (Top Through View)

## **Pin Definitions**

Pin #	Name	Description
1	В	Data Input
2	GND	Ground
3	A	Data Input
4	Y	Output
5	V <sub>CC</sub>	Supply Voltage
6	С	Data Input

## **Function Table**

	Inputs		74AUP1G97
С	В	Α	Y=Output
L	L	L	L
L	L	Н	L
L	Н	L	Н
L	Н	Н	Н
Н	L	L	L
Н	L	Н	Н
Н	Н	L	L
Н	Н	Н	Н

H = HIGH Logic Level L = LOW Logic Level

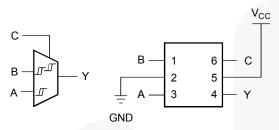
## **Function Selection Table**

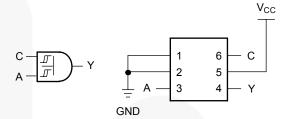
2-Input Logic Function	Connection Configuration		
2-to-1 MUX	Figure 3		
2-Input AND Gate	Figure 4		
2-Input OR Gate with One Inverted Input	Figure 5		
2-Input NAND Gate with One Inverted Input	Figure 5		
2-Input AND Gate with One Inverted Input	Figure 6		
2-Input NOR Gate with One Inverted Input	Figure 6		
2-Input OR Gate	Figure 7		
Inverter	Figure 8		
Buffer	Figure 9		

## 74AUP1G97 Logic Configurations

Figure 3 through Figure 9 show the logical functions that can be implemented using the 74AUP1G97. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical

implementation is next to the board-level physical implementation of how the pins of the function should be connected.



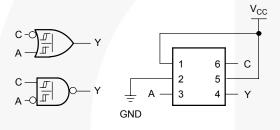


#### Note:

- 1. When C is L, Y=B.
- 2. When C is H, Y=A.

Figure 3. 2-to-1 MUX

Figure 4. 2-Input AND Gate



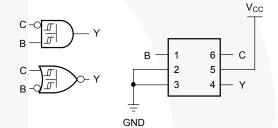


Figure 5. Input OR Gate with One Inverted Input
2-Input NAND Gate with One Inverted Input

Figure 6. 2-Input AND Gate with One Inverted Input 2-Input NOR Gate with One Inverted Input

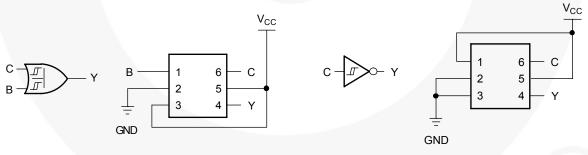


Figure 7. 2-Input OR Gate

Figure 8. Inverter

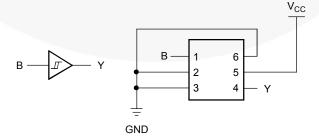


Figure 9. Buffer

## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Para	Parameter			Unit
V <sub>CC</sub>	Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	DC Input Voltage		-0.5	4.6	V
V	DC Output Voltage	HIGH or LOW State <sup>(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	DC Output Voltage	V <sub>CC</sub> =0V	-0.5	4.6	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>IN</sub> < 0V		-50	mA
Lava	DC Output Diodo Current	V <sub>OUT</sub> < 0V		-50	mΛ
I <sub>OK</sub>	DC Output Diode Current	V <sub>OUT</sub> > V <sub>CC</sub>		+50	mA
I <sub>OH</sub> / I <sub>OL</sub>	DC Output Source / Sink Curre		±50	mA	
lo	Continuous Output Current			±20	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current per	Supply Pin		±50	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
$T_J$	Junction Temperature Under B	ias		+150	°C
$T_L$	Junction Lead Temperature, So	oldering 10s		+260	°C
В	Dower Discipation at ±95°C	MicroPak-6		130	mW
$P_D$	Power Dissipation at +85°C	MicroPak2-6		120	IIIVV
ESD	Human Body Model, JEDEC:JESD22-A114			5000+	V
ESD	Charged Device Model, JEDEC	::JESD22-C101		1500	V

#### Note:

3. Io absolute maximum rating must be observed.

## Recommended Operating Conditions<sup>(4)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage		0.8	3.6	V
V <sub>IN</sub>	Input Voltage		0	3.6	V
V	Output Voltage	V <sub>CC</sub> =0V	0	3.6	V
$V_{OUT}$	Output voltage	HIGH or LOW State	0	Vcc	7 °
		V <sub>CC</sub> =3.0V to 3.6V		±4.0	
	Output Current	V <sub>CC</sub> =2.3V to 2.7V		±3.1	
1 /1		V <sub>CC</sub> =1.65V to 1.95V		±1.9	mA
I <sub>OH</sub> /I <sub>OL</sub>		V <sub>CC</sub> =1.4V to 1.6V		±1.7	
		V <sub>CC</sub> =1.1V to 1.3V		±1.1	
		V <sub>CC</sub> =0.8V		±20.0	μΑ
T <sub>A</sub>	Operating Temperature, Free Air		-40	+85	°C
0	The word Decistores	MicroPak-6		500	°C/A/
$ heta_{\sf JA}$	Thermal Resistance	MicroPak2-6		560	°C/W

#### Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

## **DC Electrical Characteristics**

Cumb at	Dorossatas	V	Conditions	T <sub>A</sub> =+	25°C	T <sub>A</sub> =-40 t	-40 to +85°C		
Symbol	Parameter	V <sub>cc</sub>	Conditions	Min.	Max.	Min.	Max.	Uni	
		0.80		0.30	0.60	0.30	0.60		
		1.10		0.53	0.90	0.53	0.90		
	Positive Threshold	1.40		0.74	1.11	0.74	1.11		
$V_P$	Voltage	1.65		0.91	1.29	0.91	1.29	V	
		2.30		1.37	1.77	1.37	1.77		
		3.00		1.88	2.29	1.88	2.29		
		0.80		0.10	0.60	0.10	0.60		
		1.10	1	0.26	0.65	0.26	0.65		
	Negative	1.40	1	0.39	0.75	0.39	0.75		
$V_N$	Threshold Voltage	1.65	-	0.47	0.84	0.47	0.84	V	
		2.30	-	0.69	1.04	0.69	1.04		
		3.00	-	0.88	1.24	0.88	1.24		
		0.80		0.07	0.50	0.07	0.50		
		1.10		0.08	0.46	0.08	0.46		
	5	1.40		0.18	0.56	0.18	0.56		
$V_{H}$	Hysteresis Voltage	1.65	-	0.10	0.66	0.10	0.66	٧	
		2.30	-	0.53	0.92	0.53	0.92		
		3.00	-	0.33	1.31	0.33	1.31		
			L = 20A		1.31		1.31		
		$0.80 \le V_{CC} \le 3.60$	Ι <sub>ΟΗ</sub> =-20μΑ	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1			
			1.10 ≤ V <sub>CC</sub> ≤ 1.30	I <sub>OH</sub> =-1.1mA	0.75 x V <sub>CC</sub>		0.70 x V <sub>CC</sub>		
		$1.40 \le V_{CC} \le 1.60$	I <sub>OH</sub> =-1.7mA	1.11		1.03			
$V_{OH}$	HIGH Level Output	$1.65 \le V_{CC} \le 1.95$	I <sub>OH</sub> =-1.9mA	1.32		1.30		V	
	Voltage	$2.30 \leq V_{CC} \leq 2.70$	I <sub>OH</sub> =-2.3mA	2.05		1.97			
			I <sub>OH</sub> =-3.1mA	1.90		1.85			
		$3.00 \le V_{CC} \le 3.60$	I <sub>OH</sub> =-2.7mA	2.72		2.67			
		3.00 ± V(() ± 3.00	I <sub>OH</sub> =-4.0mA	2.60		2.55			
		$0.80 \leq V_{CC} \leq 3.60$	I <sub>OL</sub> =20μA		0.10		0.10		
		$1.10 \le V_{CC} \le 1.30$	I <sub>OL</sub> =1.1mA		0.30 x V <sub>CC</sub>		0.30 x V <sub>CC</sub>		
		$1.40 \le V_{CC} \le 1.60$	I <sub>OL</sub> =1.7mA		0.31		0.37		
.,	LOW Level Output	$1.65 \leq V_{CC} \leq 1.95$	I <sub>OL</sub> =1.9mA		0.31		0.35	V	
$V_{OL}$	Voltage		I <sub>OL</sub> =2.3mA		0.31		0.33	\ \	
		$2.30 \leq V_{CC} \leq 2.70$	I <sub>OL</sub> =3.1mA		0.44		0.45		
			I <sub>OL</sub> =2.7mA		0.31		0.33		
		$2.70 \leq V_{CC} \leq 3.60$	I <sub>OL</sub> =4.0mA		0.44		0.45		
I <sub>IN</sub>	Input Leakage Current	0V to 3.6V	$0 \le V_{IN} \le 3.6$		±0.1		±0.5	μΑ	
I <sub>OFF</sub>	Power Off Leakage Current	0V	$0 \leq (V_{IN}, V_O) \leq 3.6$		0.2		0.6	μ	
$\Delta l_{OFF}$	Additional Power Off Leakage Current	0V to 0.2V	$V_{IN}$ or $V_{O} = 0V$ to 3.6V		0.2		0.6	μA	
Icc	Quiescent Supply Current	0.8V to 3.6V	V <sub>IN</sub> - V <sub>CC</sub> or GND		0.5		0.9	μA	
	Janon		$V_{CC} \leq V_{IN} \leq 3.6$				±0.9		
$\Delta I_{CC}$	Increase in I <sub>CC</sub> per Input	3.3V	V <sub>IN</sub> = V <sub>CC</sub> -0.6V		40.0		50.0	μA	

## **AC Electrical Characteristics**

Symbol	Parameter	V <sub>cc</sub>	Conditions	1	<sub>A</sub> =+25°	С		40 to 5°C	Units	Figure
				Min.	Тур.	Max	Min	Max		3
		0.80			25.1					
		1.10 ≤ V <sub>CC</sub> ≤ 1.30		2.8	8.6	12.6	2.5	13.0		
		$1.40 \le V_{CC} \le 1.60$		2.3	5.2	7.6	2.5	8.2	]	
		$1.65 \le V_{CC} \le 1.95$	$C_L=5pF, R_L=1M\Omega$	2.1	4.3	6.2	2.0	6.8	]	
		$2.30 \leq V_{CC} \leq 2.70$		1.9	3.3	4.8	1.7	5.3		
		$3.00 \leq V_{CC} \leq 3.60$		1.6	3.1	3.9	1.5	4.1		
		0.80			29.4					
		$1.10 \le V_{CC} \le 1.30$		3.2	9.4	14.3	2.9	14.9		
		$1.40 \le V_{CC} \le 1.60$	C <sub>L</sub> =10pF,	2.6	6.3	8.7	2.8	9.4		
		$1.65 \leq V_{CC} \leq 1.95$	$R_L=1M\Omega$	2.2	4.9	7.0	2.1	7.8		
		$2.30 \leq V_{CC} \leq 2.70$		2.0	4.2	5.2	2.1	5.9		
- 4		$3.00 \leq V_{CC} \leq 3.60$		1.9	3.6	4.6	1.7	4.9		
$t_{\text{PHL}},t_{\text{PLH}}$	Propagation Delay	0.80			31.3				ns	Figure 10 Figure 11
		$1.10 \le V_{CC} \le 1.30$	C <sub>L</sub> =15pF,	3.6	9.6	16.0	3.2	16.7		
		$1.40 \leq V_{CC} \leq 1.60$		2.9	6.3	9.6	3.1	10.4		
		$1.65 \leq V_{CC} \leq 1.95$	$R_L=1M\Omega$	2.4	5.4	7.8	2.3	8.7		
		$2.30 \leq V_{CC} \leq 2.70$		2.3	4.7	5.8	2.1	6.5		
		$3.00 \leq V_{CC} \leq 3.60$		2.0	4.0	5.1	1.8	5.5		
		0.80			32.1					
		1.10 ≤ V <sub>CC</sub> ≤ 1.30		3.4	9.5	18.5	3.4	19.0	1	
		1.40 ≤ V <sub>CC</sub> ≤ 1.60	$C_L$ =30pF, $R_L$ =1M $\Omega$	3.1	5.9	10.5	3.1	11.0		
		$1.65 \le V_{CC} \le 1.95$		1.8	4.8	8.7	1.8	9.5		
		$2.30 \leq V_{CC} \leq 2.70$		1.7	3.7	6.5	1.7	7.1		
		$3.00 \leq V_{CC} \leq 3.60$		1.3	3.1	5.6	1.3	6.3		
C <sub>IN</sub>	Input Capacitance	0			2.1				pF	
C <sub>OUT</sub>	Output Capacitance	0			3,0				pF	
		0.80			1.7					
		$1.10 \le V_{CC} \le 1.30$			1.8					
$C_PD$	Power Dissipation	$1.40 \le V_{CC} \le 1.60$	V <sub>IN</sub> =0V or V <sub>CC</sub> ,		1.81				pF	
<b>⊸</b> FD	Capacitance	$1.65 \leq V_{CC} \leq 1.95$	f=10MHz		1.84					$\mathbb{R}_{1}$
		$2.30 \leq V_{CC} \leq 2.70$			2.1					
		$3.00 \leq V_{CC} \leq 3.60$			2.5		=			

## **AC Loadings and Waveforms**

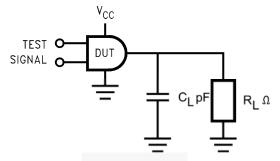


Figure 10. AC Test Circuit

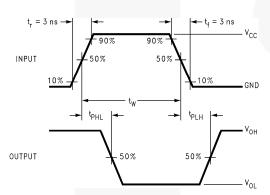
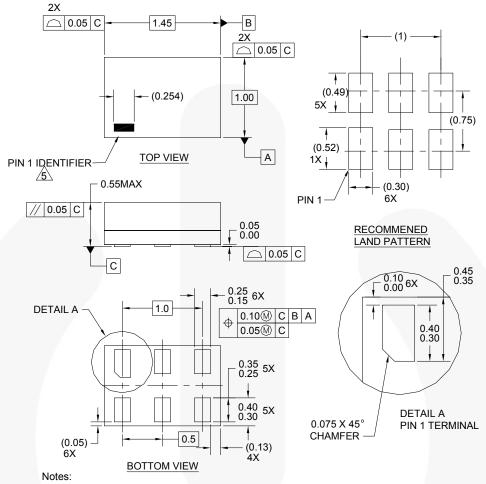


Figure 11. AC Waveforms

Symbol	V <sub>cc</sub>					
Symbol	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.10V	1.2V ± 0.10V	V8.0
V <sub>mi</sub>	V <sub>CC</sub> /2					
$V_{mo}$	V <sub>CC</sub> /2					

### **Physical Dimensions**



- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
  3. DRAWING CONFORMS TO ASME Y14.5M-1994
- FILENAME AND REVISION: MAC06AREV4
- 5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY

OTHER LINE IN THE MARK CODE LAYOUT.

Figure 12. 6-Lead, MicroPak™, 1.0mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

#### **Tape and Reel Specifications**

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/logic/pdf/micropak\_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## **Physical Dimensions**

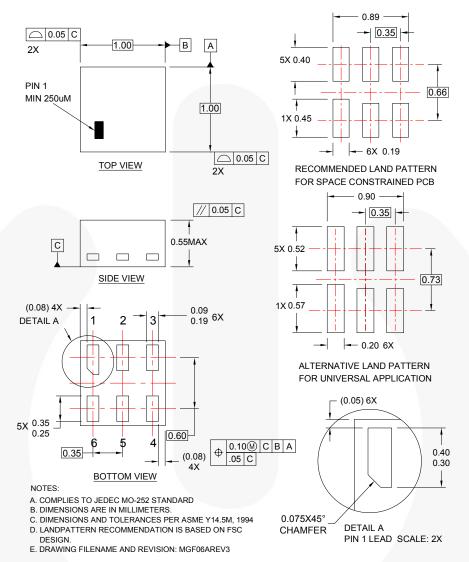


Figure 13. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

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### **Tape and Reel Specifications**

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
FHX	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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FACT Quiet Series™
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FAST<sup>®</sup>
FastvCore™
FETBench™
FlashWriter<sup>®\*</sup>
FPS™

F-PFS™ FRFET®

Global Power Resource<sup>SM</sup>

Green FPS™ Green FPS™ e-Series™

Gmax™ GTO™ IntelliMAX™ ISOPLANAR™

MegaBuck™
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MicroFET™

MicroFe I'M
MicroPak™
MicroPak2™
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SuperSOT™.6

SuperSOT™-8 SupreMOS® SyncFET™ Sync-Lock™ SYSTEM ®\*
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TinyCalc™
TinyCalc™
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TinyPower™
TinyPower™
TinyPower™
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