# Panasonic

**AN32183A**

# 9 x 9 Dots Matrix LED Driver IC

## FEATURES

- 9 × 9 LED Matrix Driver
  (Total LED that can be driven = 81)
- LED Selectable Maximum Current
- LED Music Synchronizing Function
- I²C interface  (Standard Mode, Fast Mode and
  Fast Mode Plus)
  (4 Slave address selectable)
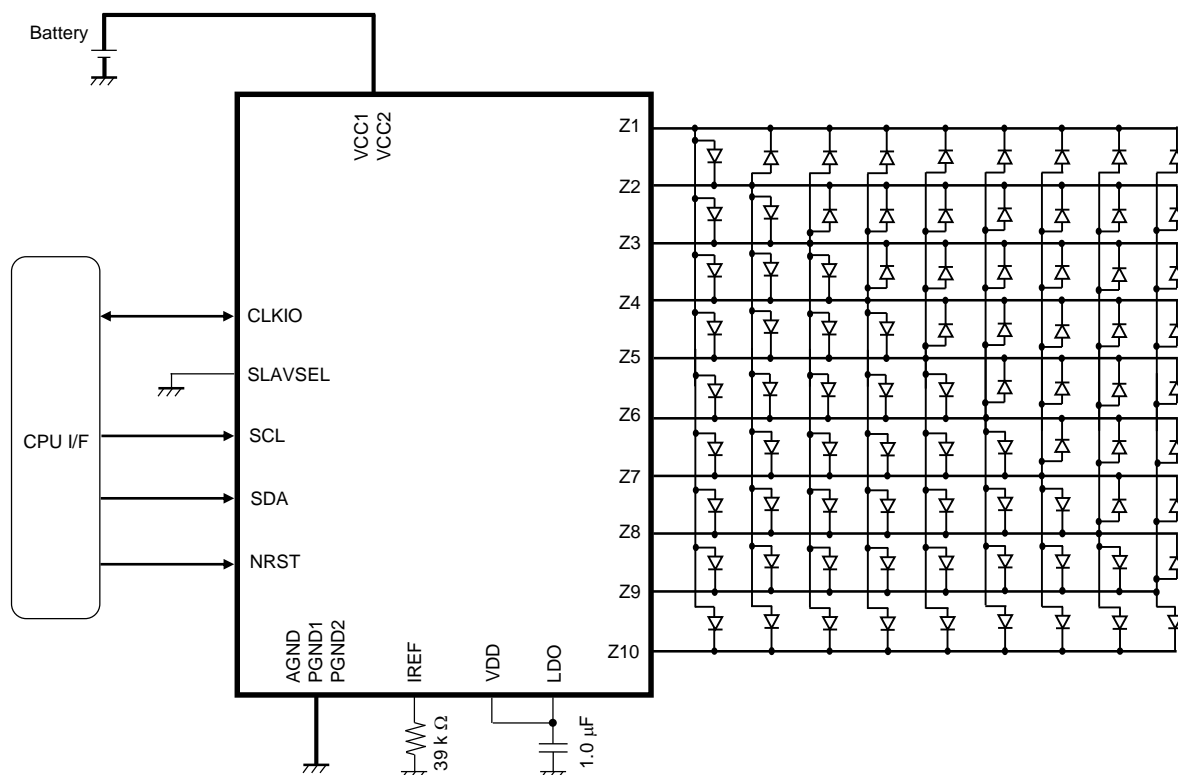- 24 pin Shrink Small Outline Package (SSOP Type)

## DESCRIPTION

AN32183A is a 81 Dots Matrix LED Driver.
It can drive up to 27 RGB LEDs.

## APPLICATIONS

- Mobile, Wearable
- Smart Speaker
- PCs
- Game Consoles
- Home Appliances etc.

## TYPICAL APPLICATION



Note:
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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## ORDERING INFORMATION

| Order Number | Feature | Package | Output Supply |
|---|---|---|---|
| AN32183A-VF | LED Driver for Illumination | 24 pin SSOP | Emboss Taping |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Supply voltage | $VCC_{MAX}$ | 6.0 | V | *1 |
| | $VDD_{MAX}$ | 6.0 | V | *1 |
| Operating ambience temperature | $T_{opr}$ | − 30 to + 85 | °C | *2 |
| Operating junction temperature | $T_j$ | − 30 to + 125 | °C | *2 |
| Storage temperature | $T_{stg}$ | − 55 to + 125 | °C | *2 |
| Input Voltage Range | $V_{SLAVSEL}$, $V_{SCL}$, $V_{SDA}$, $V_{CLKIO}$, $V_{NRST}$ | − 0.3 to 6.0 | V | — |
| Output Voltage Range | $V_{LDO}$, $V_{CLKIO}$, $V_{Z1}$, $V_{Z2}$, $V_{Z3}$, $V_{Z4}$, $V_{Z5}$, $V_{Z6}$, $V_{Z7}$, $V_{Z8}$, $V_{Z9}$, $V_{Z10}$ | − 0.3 to 6.0 | V | — |
| ESD | HBM | 2.0 | kV | — |

Note:  This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum
       rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our
       stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability
       of the product may be affected.
       *1: $VCC_{MAX}$ = VCC1= VCC2, $VDD_{MAX}$ = VDD.
           The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
       *2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for
           Ta = 25°C.

## POWER DISSIPATION RATING

| PACKAGE | $\theta_{JA}$ | $P_D$ (Ta=25 °C) | $P_D$ (Ta=85 °C) |
|---|---|---|---|
| 24 pin Shrink Small Outline Package (SSOP Type) | 135.1 °C /W | 0.740 W | 0.296 W |

Note: For the actual usage, please refer to the $P_D$-Ta characteristics diagram in the package specification, follow the power supply
      voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does
      not exceed the allowable value.

### CAUTION
Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled
properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS
gates.

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## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | 3.1 | 3.6 | 5.5 | V | *1 |
| | $V_{DD}$ | 1.7 | 1.85 | 5.5 | V | *1 |
| Input Voltage Range | $V_{SLAVSEL}$, $V_{SCL}$, $V_{SDA}$, $V_{CLKIO}$ | − 0.3 | — | $V_{DD}$ + 0.3 | V | *2 |
| | $V_{NRST}$ | − 0.3 | — | $V_{CC}$ + 0.3 | V | *2 |
| Output Voltage Range | $V_{LDO}$, $V_{CLKIO}$, $V_{Z1}$, $V_{Z2}$, $V_{Z3}$, $V_{Z4}$, $V_{Z5}$ $V_{Z6}$, $V_{Z7}$, $V_{Z8}$, $V_{Z9}$, $V_{Z10}$ | − 0.3 | — | $V_{CC}$ + 0.3 | V | *2 |

Note: *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

   Do not apply external currents and voltages to any pin not specifically mentioned.

   Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND1 and GND2.

   $V_{CC}$ is voltage for VCC1 and VCC2. $V_{DD}$ is voltage for VDD.

   *2 : ($V_{CC}$ + 0.3 ) V must not exceed 6 V. ($V_{DD}$ + 0.3) V must not exceed 6 V.

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## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 3.6 V, $V_{DD}$ = 1.85 V

Notes:   $T_a$ = 25°C±2°C unless otherwise noted.

| Parameter | | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| **Circuit Current** | | | | | | | | |
| | Circuit Current (1) OFF Mode | $I_{CC1}$ | NRST = 0V | — | 0 | 1 | µA | — |
| | Circuit Current (2) OFF Mode | $I_{CC2}$ | NRST = 3.6V | — | 250 | 500 | µA | — |
| **Internal Oscillator** | | | | | | | | |
| | Oscillation Frequency | FDC1 | $V_{CC}$ = 3.6 V | 1.92 | 2.40 | 2.88 | MHz | — |
| **SCAN Switch** | | | | | | | | |
| | Switch On Resistance | RSCAN | $V_{CC}$ = 3.6 V $I_{Z1~Z9}$ = − 20 mA | — | 1.5 | 3 | Ω | — |
| **Constant Voltage Source (LDO)** | | | | | | | | |
| | Output voltage (1) | $V_{L1}$ | $I_{LDO}$ = − 10 µA | 2.75 | 2.85 | 2.95 | V | — |
| | Output voltage (2) | $V_{L2}$ | $I_{LDO}$ = − 15 mA | 2.75 | 2.85 | 2.95 | V | — |
| **CLKIO** | | | | | | | | |
| | High Level Input Voltage Range | $V_{IH1}$ | High Level Acknowledged Voltage (At External CLK Input Mode) | $0.7 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | — |
| | Low Level Input Voltage Range | $V_{IL1}$ | Low Level Acknowledged Voltage (At External CLK Input Mode) | − 0.3 | — | $0.3 \times V_{DD}$ | V | — |
| | High Level Output Voltage | $V_{OH1}$ | $I_{CLKIO}$ = − 1 mA (At Internal CLK Output Mode) | $0.8 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | — |
| | Low Level Output Voltage | $V_{OL1}$ | $I_{CLKIO}$ = 1 mA (At Internal CLK Output Mode) | − 0.3 | — | $0.2 \times V_{DD}$ | V | — |
| | High Level input Current | $I_{IH1}$ | $V_{CC}$ = 5.5 V $V_{CLKIO}$ = 5.5 V | − 1 | 0 | 1 | µA | — |
| | Low Level input Current | $I_{IL1}$ | $V_{CC}$ = 5.5 V $V_{CLKIO}$ = 0 V | − 1 | 0 | 1 | µA | — |

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## ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}$ = 3.6 V, $V_{DD}$ = 1.85 V

Notes:  $T_a$ = 25°C±2°C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Constant Current Source (Matrix LED)** | | | | | | | |
| Output Current (1) | $I_{MX1}$ | LED Current Setting = 20 mA $I_{MAX}$ = [011], BRTXX = [1010] $V_{Z1~Z10}$ = 1 V | 19 | 20 | 21 | mA | *1 |
| DAC Current Step | DACSTEP | DAC Constant Current Mode LED Current Setting = 20 mA $I_{MAX}$ = [011], BRTXX = [1010] $V_{Z1~Z10}$ = 1V, IDAC1 = $I_{Z1~Z10}$ LED Current Setting = 22 mA $I_{MAX}$ = [011], BRTXX = [1011] $V_{Z1~Z10}$ = 1 V, IDAC2 = $I_{Z1~Z10}$ DACSTEP = IDAC2 − IDAC1 | 0 | 2 | 4 | mA | *2 |
| OFF Mode Leak Current1 | $I_{MXOFF1}$ | $V_{CC}$ = 5.5 V, $V_{DD}$ = 5.5 V MTXON = 0 $V_{Z1~Z10}$ = 5.5V | − 1 | — | 1 | μA | *3 |
| OFF Mode Leak Current2 | $I_{MXOFF2}$ | $V_{CC}$ = 5.5 V, $V_{DD}$ = 5.5 V MTXON = 0 $V_{Z1~Z10}$ = 0 V | − 1 | — | 1 | μA | *3 |
| Channel Difference | $I_{MXCH}$ | LED Current Setting = 20 mA $I_{MAX}$ = [011], BRTXX = [1010] Difference of Z1 to 10 current from the average current value | − 5 | — | 5 | % | — |
| **Voltage at which LED driver can keep constant current value** | | | | | | | |
| LED Driver Voltage | $V_{LD2}$ | LED Current Setting = 20 mA $I_{MAX}$ = [011], BRTXX = [1010] Voltage at which LED Current change within ± 5 % compared with LED Current of pin voltage = 0.5 V. | 0.4 | — | — | V | — |

Note: * 1: This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

* 2: Current step for individual channels (Z1~Z10).

* 3: Please refer to page 23 for more information on the setting.

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## ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC} = 3.6$ V, $V_{DD} = 1.85$ V

Notes: $T_a = 25°C \pm 2°C$ unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **SLAVSEL** | | | | | | | |
| High Level Input Voltage Range | $V_{IH2}$ | High Level Acknowledged Voltage | $0.7 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | — |
| Low Level Input Voltage Range | $V_{IL2}$ | Low Level Acknowledged Voltage | $-0.3$ | — | $0.3 \times V_{DD}$ | V | — |
| High Level Input Current | $I_{IH2}$ | $V_{CC} = 5.5$ V $V_{SLAVSEL} = 3.6$ V | $-1$ | 0 | 1 | µA | — |
| Low Level Input Current | $I_{IL2}$ | $V_{CC} = 5.5$ V $V_{SLAVSEL} = 0$ V | $-1$ | 0 | 1 | µA | — |
| **NRST** | | | | | | | |
| High Level Input Voltage Range | $V_{IH3}$ | High Level Acknowledged Voltage | 1.5 | — | $V_{CC} + 0.3$ | V | — |
| Low Level Input Voltage Range | $V_{IL3}$ | Low Level Acknowledged Voltage | $-0.3$ | — | 0.6 | V | — |
| High Level Input Current | $I_{IH3}$ | $V_{CC} = 5.5$ V $V_{NRST} = 3.6$ V | $-1$ | 0 | 1 | µA | — |
| Low Level Input Current | $I_{IL3}$ | $V_{CC} = 5.5$ V $V_{NRST} = 0$ V | $-1$ | 0 | 1 | µA | — |
| **I²C bus (Internal I/O stage characteristics)** | | | | | | | |
| Low-level input voltage | $V_{IL}$ | Voltage which recognized that SDA and SCL are Low-level | $-0.5$ | — | $0.3 \times V_{DD}$ | V | *4 |
| High-level input voltage | $V_{IH}$ | Voltage which recognized that SDA and SCL are High-level | $0.7 \times V_{DD}$ | — | $VDD_{MAX} + 0.5$ | V | *4 |
| Low-level output voltage 1 | $V_{OL1}$ | $V_{DD} > 2$ V $I_{SDA} = 3$ mA | 0 | — | 0.4 | V | — |
| Low-level output voltage 2 | $V_{OL2}$ | $V_{DD} < 2$ V $I_{SDA} = 3$ mA | 0 | — | $0.2 \times V_{DD}$ | V | — |
| Low-level output current | $I_{OL}$ | $V_{SDA} = 0.4$ V | 20 | — | — | mA | — |
| Input current each I/O pin | $I_i$ | $V_{CC} = 5.5$ V, $V_{DD} = 5.5$ V $V_{SCL}, V_{SDA} =$ $0.1\ VDD_{MAX}$ to $0.9\ VDD_{MAX}$ | $-10$ | 0 | 10 | µA | — |
| SCL clock frequency | $f_{SCL}$ | — | 0 | — | 1 000 | kHz | — |

Note: $VDD_{MAX}$ refers to the maximum operating supply voltage of $V_{DD}$ .

*4 : The input threshold voltage of I²C bus (Vth) is linked to $V_{DD}$ (I²C bus I/O stage supply voltage).

In case the pull-up voltage is not $V_{DD}$, the threshold voltage (Vth) is fixed to (($V_{DD}$ / 2) ± (Schmitt width) / 2 ) and High-level, Low-level of input voltage are not specified. In this case, pay attention to Low-level (max.) value ($V_{ILMAX}$).

It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage ($V_{DD}$).

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## ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}$ = 3.6 V, $V_{DD}$ = 1.85 V

Notes: $T_a$ = 25°C±2°C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **TSD (Thermal shutdown protection circuit)** | | | | | | | |
| Detection temperature | Tdet | Temperature which Constant current circuit, and Matrix SW turn off. | — | 150 | — | °C | *5 *6 |
| **Constant Voltage Source (LDO)** | | | | | | | |
| Ripple rejection ratio (1) | PSL11 | $V_{CC}$ = 3.6 V + 0.3 V[p-p]<br>f = 1 kHz<br>$I_{LDO}$ = −15 mA<br>PSL11 = 20log(ac$V_{LDO}$ / 0.3) | — | − 50 | — | dB | *6 |
| Ripple rejection ratio (2) | PSL12 | $V_{CC}$ = 3.6 V + 0.3 V[p-p]<br>f = 10 kHz<br>$I_{LDO}$ = −15 mA<br>PSL12 = 20log(ac$V_{LDO}$ / 0.3) | — | − 40 | — | dB | *6 |
| Short-circuit protection current | $I_{PT1}$ | $V_{LDO}$ = 0 V | — | 40 | — | mA | *6 |
| **I²C bus (Internal I/O stage characteristics) (Continued)** | | | | | | | |
| Hysteresis of Schmitt trigger input 1 | $V_{hys1}$ | $V_{DD}$ > 2 V,<br>Hysteresis of SDA, SCL | 0.05 × $V_{DD}$ | — | — | V | *7 *8 |
| Hysteresis of Schmitt trigger input 2 | $V_{hys2}$ | $V_{DD}$ < 2 V,<br>Hysteresis of SDA, SCL | 0.1 × $V_{DD}$ | — | — | V | *7 *8 |
| Output fall time from $V_{IHMIN}$ to $V_{ILMAX}$ | $t_{of}$ | Bus capacitance :<br>10pF to 550pF<br>$I_P ≤$ 20 mA ($V_{OLMAX}$ = 0.4 V)<br>$I_P$ : Max. sink current | — | — | 120 | ns | *7 *8 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{SP}$ | — | 0 | — | 50 | ns | *7 *8 |
| Capacitance for each I/O pin | $C_i$ | — | — | — | 10 | pF | *7 *8 |

Note: *5 : Constant current circuit, and Matrix SW turn off and IC reset when TSD operates.

*6 : Typical Design Value

*7 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.10. All values referred to $V_{IHMIN}$ and $V_{ILMAX}$ level.

*8 : These are values checked by design but not production tested.

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## ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}$ = 3.6 V, $V_{DD}$ = 1.85 V

Notes: $T_a$ = 25°C±2°C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **I²C bus (Bus line specifications) (Continue)** | | | | | | | |
| Hold time (repeated) START condition | $t_{HD:STA}$ | The first clock pulse is generated after $t_{HD:STA.}$ | 0.26 | — | — | μs | *7 *8 |
| Low period of the SCL clock | $t_{LOW}$ | — | 0.5 | — | — | μs | *7 *8 |
| High period of the SCL clock | $t_{HIGH}$ | — | 0.26 | — | — | μs | *7 *8 |
| Set-up time for a repeat START condition | $t_{SU:STA}$ | — | 0.26 | — | — | μs | *7 *8 |
| Data hold time | $t_{HD:DAT}$ | — | 0 | — | — | μs | *7 *8 |
| Data set-up time | $t_{SU:DAT}$ | — | 50 | — | — | ns | *7 *8 |
| Rise time of both SDA and SCL signals | $t_r$ | — | — | — | 120 | ns | *7 *8 |
| Fall time of both SDA and SCL signals | $t_f$ | — | — | — | 120 | ns | *7 *8 |
| Set-up time of STOP condition | $t_{SU:STO}$ | — | 0.26 | — | — | μs | *7 *8 |
| Bus free time between STOP and START condition | $t_{BUF}$ | — | 0.5 | — | — | μs | *7 *8 |
| Capacitive load for each bus line | $C_b$ | — | — | — | 550 | pF | *7 *8 |
| Data valid time | $t_{VD:DAT}$ | — | — | — | 0.45 | μs | *7 *8 |
| Data valid acknowledge | $t_{VD:ACK}$ | — | — | — | 0.45 | μs | *7 *8 |
| Noise margin at the Low-level for each connected device | $V_{nL}$ | — | 0.1 × $V_{DD}$ | — | — | V | *7 *8 |
| Noise margin at the High-level for each connected device | $V_{nH}$ | — | 0.2 × $V_{DD}$ | — | — | V | *7 *8 |

Note: *7 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page 10. All values referred to $V_{IHMIN}$ and $V_{ILMAX}$ level.

   *8 : These are values checked by design but not production tested.

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## ELECTRICAL CHARACTERISTICS (Continued)
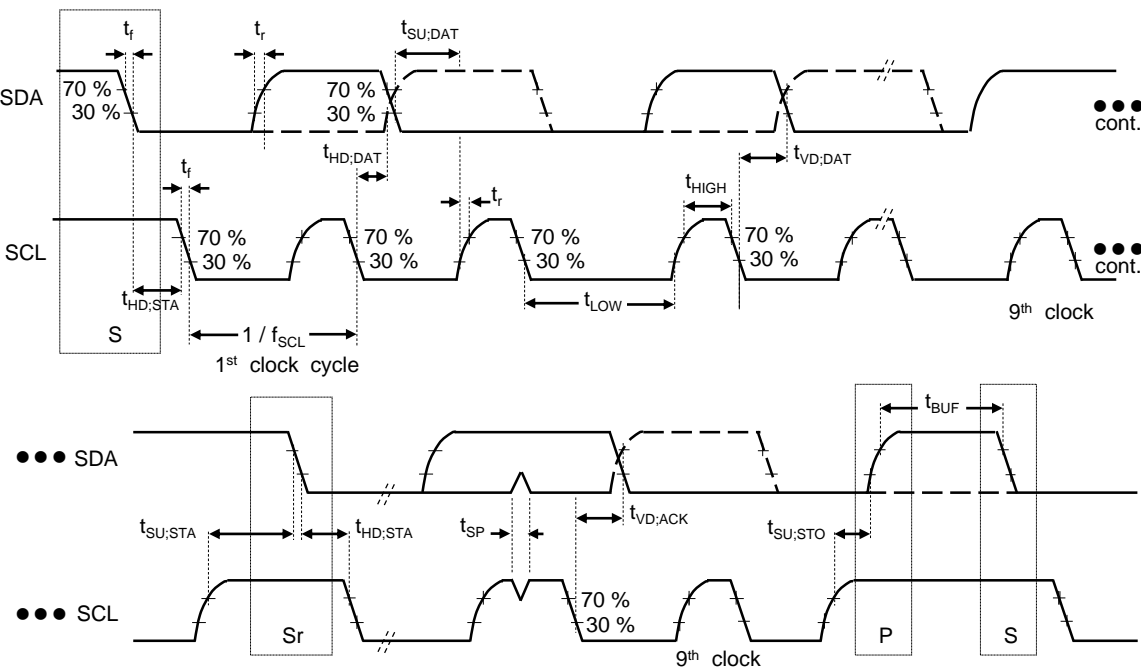


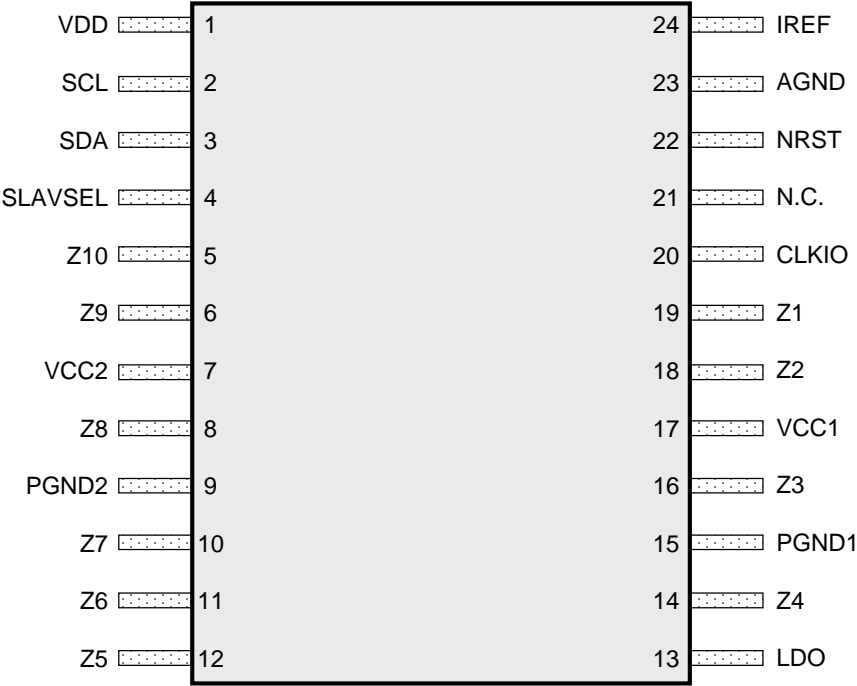$V_{ILMAX} = 0.3\ V_{DD}$

$V_{IHMIN} = 0.7\ V_{DD}$

S : START condition

Sr : Repetitive START condition

P : STOP condition

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## PIN CONFIGURATION

TOP VIEW

| Left pin | No. | | No. | Right pin |
|---|---|---|---|---|
| VDD | 1 | | 24 | IREF |
| SCL | 2 | | 23 | AGND |
| SDA | 3 | | 22 | NRST |
| SLAVSEL | 4 | | 21 | N.C. |
| Z10 | 5 | | 20 | CLKIO |
| Z9 | 6 | | 19 | Z1 |
| VCC2 | 7 | | 18 | Z2 |
| Z8 | 8 | | 17 | VCC1 |
| PGND2 | 9 | | 16 | Z3 |
| Z7 | 10 | | 15 | PGND1 |
| Z6 | 11 | | 14 | Z4 |
| Z5 | 12 | | 13 | LDO |

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## PIN FUNCTIONS

| Pin No. | Pin name | Type | Description | Pin processing at unused |
|---|---|---|---|---|
| 1 | VDD | Power supply | Power supply for I$^2$C interface | (Required pin) |
| 2 | SCL | Input | Clock input pin for I$^2$C interface | (Required pin) |
| 3 | SDA | Input/Output | Data input / output pin for I$^2$C interface | (Required pin) |
| 4 | SLAVSEL | Input | Slave address selection pin for I$^2$C interface | GND or VCC or SCL or SDA |
| 5 | Z10 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 6 | Z9 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 7<br>17 | VCC2<br>VCC1 | Power supply | Power supply for matrix driver, Internal reference circuit | Battery or External power supply |
| 8 | Z8 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 9<br>15 | PGND2<br>PGND1 | Ground | Power Ground pin | (Required pin) |
| 10 | Z7 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 11 | Z6 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 12 | Z5 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 13 | LDO | Output | LDO output pin | (Required pin) |
| 14 | Z4 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 16 | Z3 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 18 | Z2 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 19 | Z1 | Output | Constant current circuit, PWM control output pin, Control switch pin for matrix driver | Open |
| 20 | CLKIO | Input/Output | Reference clock input output / Music Input pin | Open |
| 21 | — | — | N.C | — |
| 22 | NRST | Input | Reset input pin | (Required pin) |
| 23 | AGND | Ground | Ground pin | (Required pin) |
| 24 | IREF | Output | Resistor connection pin for constant current setup | (Required pin) |

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## FUNCTIONAL BLOCK DIAGRAM
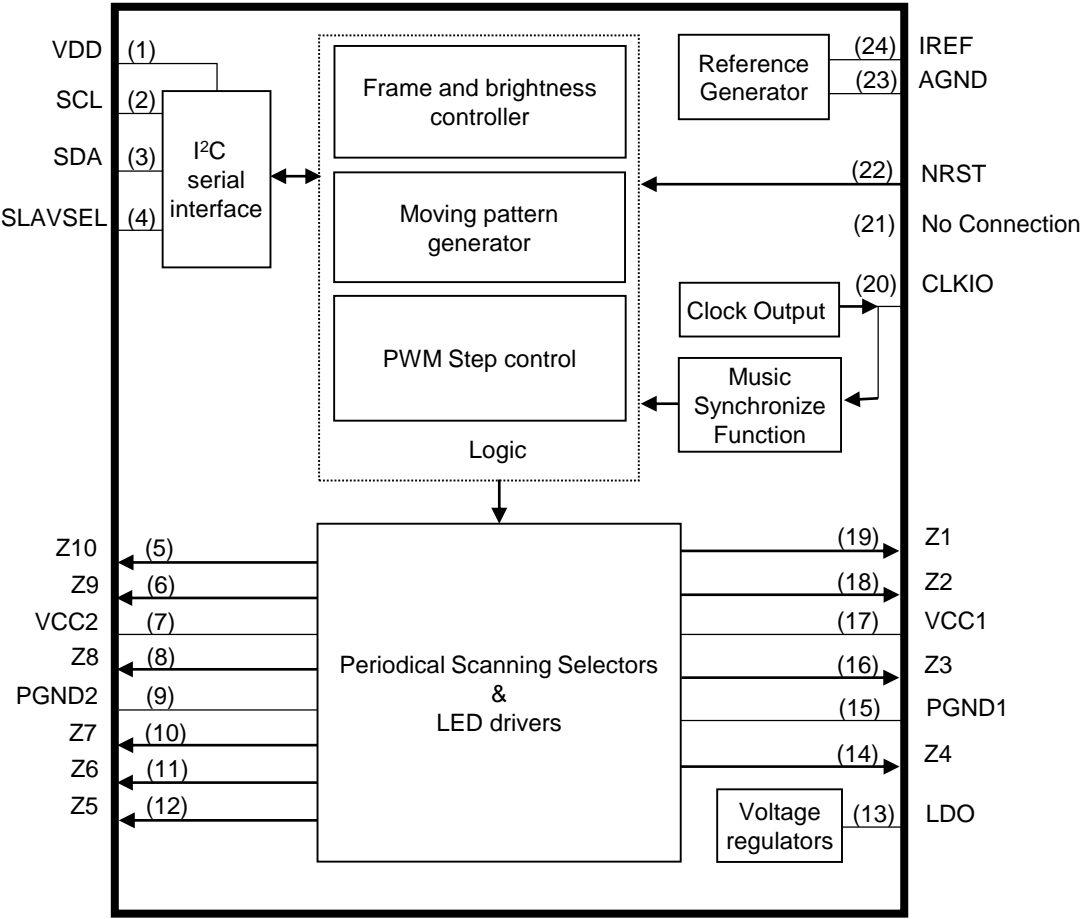

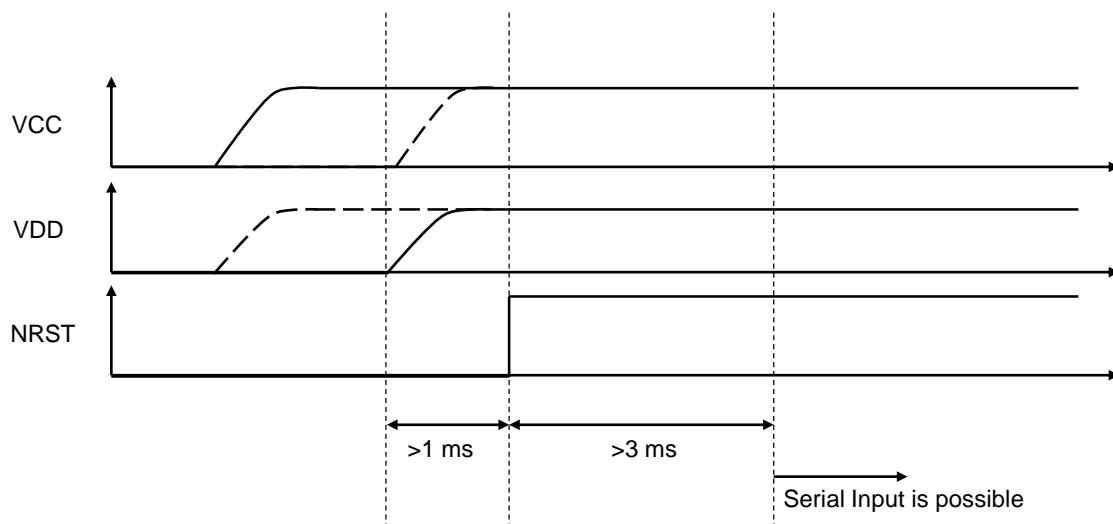
Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.
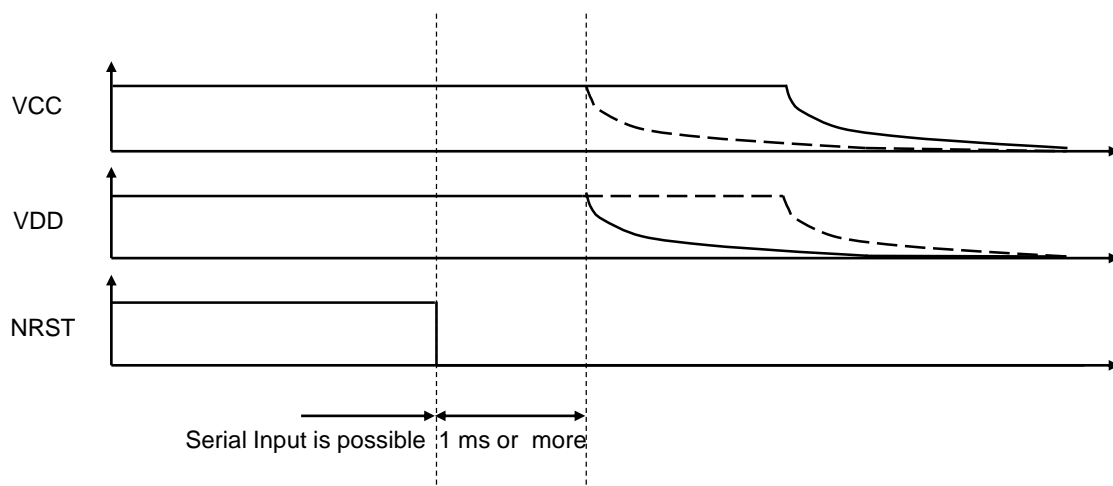
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## OPERATION

### 1. Power Supply Sequence

#### 1.1 Power ON



Note: For the Startup Timing of VCC and VDD, it is possible to be changed.

#### 1.2 Power OFF



Note: For the Shut down Timing of VCC and VDD, it is possible to be changed.

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## OPERATION (Continued)

### 2. Register Map

| ADDR | Register Name | Default | R/W | DATA | | | | | | | |
|------|---------------|---------|-----|------|------|------|------|------|------|------|------|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01h | RST | 00h | W | -- | -- | -- | -- | -- | -- | RAMRST | SRST |
| 02h | POWERCNT | 00h | R/W | | -- | -- | -- | -- | -- | -- | OSCEN |
| 03h | reserved | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 04h | OPTION | 00h | R/W | -- | -- | -- | -- | ZPDEN | MLDACT | CLKOUT | EXTCLK |
| 05h | MTXON | 1Eh | R/W | -- | -- | -- | IMAX Reserved | IMAX[2:0] | | | MTXON |
| 06h | PWMEN1 | 00h | R/W | PWMA8 | PWMA7 | PWMA6 | PWMA5 | PWMA4 | PWMA3 | PWMA2 | PWMA1 |
| 07h | PWMEN2 | 00h | R/W | PWMB7 | PWMB6 | PWMB5 | PWMB4 | PWMB3 | PWMB2 | PWMB1 | PWMA9 |
| 08h | PWMEN3 | 00h | R/W | PWMC6 | PWMC5 | PWMC4 | PWMC3 | PWMC2 | PWMC1 | PWMB9 | PWMB8 |
| 09h | PWMEN4 | 00h | R/W | PWMD5 | PWMD4 | PWMD3 | PWMD2 | PWMD1 | PWMC9 | PWMC8 | PWMC7 |
| 0Ah | PWMEN5 | 00h | R/W | PWME4 | PWME3 | PWME2 | PWME1 | PWMD9 | PWMD8 | PWMD7 | PWMD6 |
| 0Bh | PWMEN6 | 00h | R/W | PWMF3 | PWMF2 | PWMF1 | PWME9 | PWME8 | PWME7 | PWME6 | PWME5 |
| 0Ch | PWMEN7 | 00h | R/W | PWMG2 | PWMG1 | PWMF9 | PWMF8 | PWMF7 | PWMF6 | PWMF5 | PWMF4 |
| 0Dh | PWMEN8 | 00h | R/W | PWMH1 | PWMG9 | PWMG8 | PWMG7 | PWMG6 | PWMG5 | PWMG4 | PWMG3 |
| 0Eh | PWMEN9 | 00h | R/W | PWMH9 | PWMH8 | PWMH7 | PWMH6 | PWMH5 | PWMH4 | PWMH3 | PWMH2 |
| 0Fh | PWMEN10 | 00h | R/W | PWMI8 | PWMI7 | PWMI6 | PWMI5 | PWMI4 | PWMI3 | PWMI2 | PWMI1 |
| 10h | PWMEN11 | 00h | R/W | -- | -- | -- | -- | -- | -- | -- | PWMI9 |
| 11h | MLDEN1 | 00h | R/W | MLDA8 | MLDA7 | MLDA6 | MLDA5 | MLDA4 | MLDA3 | MLDA2 | MLDA1 |
| 12h | MLDEN2 | 00h | R/W | MLDB7 | MLDB6 | MLDB5 | MLDB4 | MLDB3 | MLDB2 | MLDB1 | MLDA9 |
| 13h | MLDEN3 | 00h | R/W | MLDC6 | MLDC5 | MLDC4 | MLDC3 | MLDC2 | MLDC1 | MLDB9 | MLDB8 |
| 14h | MLDEN4 | 00h | R/W | MLDD5 | MLDD4 | MLDD3 | MLDD2 | MLDD1 | MLDC9 | MLDC8 | MLDC7 |
| 15h | MLDEN5 | 00h | R/W | MLDE4 | MLDE3 | MLDE2 | MLDE1 | MLDD9 | MLDD8 | MLDD7 | MLDD6 |
| 16h | MLDEN6 | 00h | R/W | MLDF3 | MLDF2 | MLDF1 | MLDE9 | MLDE8 | MLDE7 | MLDE6 | MLDE5 |
| 17h | MLDEN7 | 00h | R/W | MLDG2 | MLDG1 | MLDF9 | MLDF8 | MLDF7 | MLDF6 | MLDF5 | MLDF4 |
| 18h | MLDEN8 | 00h | R/W | MLDH1 | MLDG9 | MLDG8 | MLDG7 | MLDG6 | MLDG5 | MLDG4 | MLDG3 |
| 19h | MLDEN9 | 00h | R/W | MLDH9 | MLDH8 | MLDH7 | MLDH6 | MLDH5 | MLDH4 | MLDH3 | MLDH2 |
| 1Ah | MLDEN10 | 00h | R/W | MLDI8 | MLDI7 | MLDI6 | MLDI5 | MLDI4 | MLDI3 | MLDI2 | MLDI1 |
| 1Bh | MLDEN11 | 00h | R/W | -- | -- | -- | -- | -- | -- | -- | MLDI9 |
| 2Ah | MLDMODE1 | 00h | R/W | -- | -- | -- | -- | GRP9_9 | GRP9_8 | GRP9_2 | GRP9_1 |
| 2Bh | THOLD | 00h | R/W | THOLD[7:0] | | | | | | | |

Note:  "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read.
Writing to these bits will be ignored. IMAX Reserved will give default value [1].

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# AN32183A

## OPERATION (Continued)

### 2. Register Map (Continued)

| ADDR | Register Name | Default | R/W | DATA | | | | | | | |
|------|--------------|---------|-----|------|------|------|------|------|------|------|------|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2Ch | CONSTX6_1 | 00h | R/W | -- | -- | X6 | X5 | X4 | X3 | X2 | X1 |
| 2Dh | CONSTX10_7 | 00h | R/W | -- | -- | -- | -- | X10 | X9 | X8 | X7 |
| 2Eh | CONSTY6_1 | 00h | R/W | -- | -- | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 2Fh | CONSTY9_7 | 00h | R/W | -- | -- | -- | -- | -- | Y9 | Y8 | Y7 |
| 30h | MASKY6_1 | 00h | R/W | -- | -- | Y6MSK | Y5MSK | Y4MSK | Y3MSK | Y2MSK | Y1MSK |
| 31h | MASKY9_7 | 00h | R/W | -- | -- | -- | -- | -- | Y9MSK | Y8MSK | Y7MSK |
| 32h | SLPTIME | 00h | R/W | -- | -- | -- | FADTIM | SLOPEEXTL[1:0] | | SLOPEEXTH[1:0] | |
| 33h | MLDCOM | 03h | R/W | -- | -- | -- | -- | -- | MLDCOM[2:0] | | |
| 34h | reserved | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 35h | reserved | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 36h | SCANSET | 08h | R/W | -- | -- | -- | -- | SCANSET[3:0] | | | |
| 40h | DTA1 | 00h | R/W | DTA1[7:0] | | | | | | | |
| 41h | DTA2 | 00h | R/W | DTA2[7:0] | | | | | | | |
| 42h | DTA3 | 00h | R/W | DTA3[7:0] | | | | | | | |
| 43h | DTA4 | 00h | R/W | DTA4[7:0] | | | | | | | |
| 44h | DTA5 | 00h | R/W | DTA5[7:0] | | | | | | | |
| 45h | DTA6 | 00h | R/W | DTA6[7:0] | | | | | | | |
| 46h | DTA7 | 00h | R/W | DTA7[7:0] | | | | | | | |
| 47h | DTA8 | 00h | R/W | DTA8[7:0] | | | | | | | |
| 48h | DTA9 | 00h | R/W | DTA9[7:0] | | | | | | | |
| 49h | DTB1 | 00h | R/W | DTB1[7:0] | | | | | | | |
| 4Ah | DTB2 | 00h | R/W | DTB2[7:0] | | | | | | | |
| 4Bh | DTB3 | 00h | R/W | DTB3[7:0] | | | | | | | |
| 4Ch | DTB4 | 00h | R/W | DTB4[7:0] | | | | | | | |
| 4Dh | DTB5 | 00h | R/W | DTB5[7:0] | | | | | | | |
| 4Eh | DTB6 | 00h | R/W | DTB6[7:0] | | | | | | | |
| 4Fh | DTB7 | 00h | R/W | DTB7[7:0] | | | | | | | |
| 50h | DTB8 | 00h | R/W | DTB8[7:0] | | | | | | | |
| 51h | DTB9 | 00h | R/W | DTB9[7:0] | | | | | | | |

Note: "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except from "Reserved" registers, will return "zero" value if these bits are read.
Writing to these bits will be ignored.

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## OPERATION (Continued)

### 2. Register Map (Continued)

| ADDR | Register Name | Default | R/W | DATA | | | | | | | |
|------|---------------|---------|-----|----|----|----|----|----|----|----|----|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 52h | DTC1 | 00h | R/W | DTC1[7:0] | | | | | | | |
| 53h | DTC2 | 00h | R/W | DTC2[7:0] | | | | | | | |
| 54h | DTC3 | 00h | R/W | DTC3[7:0] | | | | | | | |
| 55h | DTC4 | 00h | R/W | DTC4[7:0] | | | | | | | |
| 56h | DTC5 | 00h | R/W | DTC5[7:0] | | | | | | | |
| 57h | DTC6 | 00h | R/W | DTC6[7:0] | | | | | | | |
| 58h | DTC7 | 00h | R/W | DTC7[7:0] | | | | | | | |
| 59h | DTC8 | 00h | R/W | DTC8[7:0] | | | | | | | |
| 5Ah | DTC9 | 00h | R/W | DTC9[7:0] | | | | | | | |
| 5Bh | DTD1 | 00h | R/W | DTD1[7:0] | | | | | | | |
| 5Ch | DTD2 | 00h | R/W | DTD2[7:0] | | | | | | | |
| 5Dh | DTD3 | 00h | R/W | DTD3[7:0] | | | | | | | |
| 5Eh | DTD4 | 00h | R/W | DTD4[7:0] | | | | | | | |
| 5Fh | DTD5 | 00h | R/W | DTD5[7:0] | | | | | | | |
| 60h | DTD6 | 00h | R/W | DTD6[7:0] | | | | | | | |
| 61h | DTD7 | 00h | R/W | DTD7[7:0] | | | | | | | |
| 62h | DTD8 | 00h | R/W | DTD8[7:0] | | | | | | | |
| 63h | DTD9 | 00h | R/W | DTD9[7:0] | | | | | | | |
| 64h | DTE1 | 00h | R/W | DTE1[7:0] | | | | | | | |
| 65h | DTE2 | 00h | R/W | DTE2[7:0] | | | | | | | |
| 66h | DTE3 | 00h | R/W | DTE3[7:0] | | | | | | | |
| 67h | DTE4 | 00h | R/W | DTE4[7:0] | | | | | | | |
| 68h | DTE5 | 00h | R/W | DTE5[7:0] | | | | | | | |
| 69h | DTE6 | 00h | R/W | DTE6[7:0] | | | | | | | |
| 6Ah | DTE7 | 00h | R/W | DTE7[7:0] | | | | | | | |
| 6Bh | DTE8 | 00h | R/W | DTE8[7:0] | | | | | | | |
| 6Ch | DTE9 | 00h | R/W | DTE9[7:0] | | | | | | | |
| 6Dh | DTF1 | 00h | R/W | DTF1[7:0] | | | | | | | |
| 6Eh | DTF2 | 00h | R/W | DTF2[7:0] | | | | | | | |

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## OPERATION (Continued)

### 2. Register Map (Continued)

| ADDR | Register Name | Default | R/W | DATA | | | | | | | |
|------|---------------|---------|-----|------|------|------|------|------|------|------|------|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 6Fh | DTF3 | 00h | R/W | DTF3[7:0] | | | | | | | |
| 70h | DTF4 | 00h | R/W | DTF4[7:0] | | | | | | | |
| 71h | DTF5 | 00h | R/W | DTF5[7:0] | | | | | | | |
| 72h | DTF6 | 00h | R/W | DTF6[7:0] | | | | | | | |
| 73h | DTF7 | 00h | R/W | DTF7[7:0] | | | | | | | |
| 74h | DTF8 | 00h | R/W | DTF8[7:0] | | | | | | | |
| 75h | DTF9 | 00h | R/W | DTF9[7:0] | | | | | | | |
| 76h | DTG1 | 00h | R/W | DTG1[7:0] | | | | | | | |
| 77h | DTG2 | 00h | R/W | DTG2[7:0] | | | | | | | |
| 78h | DTG3 | 00h | R/W | DTG3[7:0] | | | | | | | |
| 79h | DTG4 | 00h | R/W | DTG4[7:0] | | | | | | | |
| 7Ah | DTG5 | 00h | R/W | DTG5[7:0] | | | | | | | |
| 7Bh | DTG6 | 00h | R/W | DTG6[7:0] | | | | | | | |
| 7Ch | DTG7 | 00h | R/W | DTG7[7:0] | | | | | | | |
| 7Dh | DTG8 | 00h | R/W | DTG8[7:0] | | | | | | | |
| 7Eh | DTG9 | 00h | R/W | DTG9[7:0] | | | | | | | |
| 7Fh | DTH1 | 00h | R/W | DTH1[7:0] | | | | | | | |
| 80h | DTH2 | 00h | R/W | DTH2[7:0] | | | | | | | |
| 81h | DTH3 | 00h | R/W | DTH3[7:0] | | | | | | | |
| 82h | DTH4 | 00h | R/W | DTH4[7:0] | | | | | | | |
| 83h | DTH5 | 00h | R/W | DTH5[7:0] | | | | | | | |
| 84h | DTH6 | 00h | R/W | DTH6[7:0] | | | | | | | |
| 85h | DTH7 | 00h | R/W | DTH7[7:0] | | | | | | | |
| 86h | DTH8 | 00h | R/W | DTH8[7:0] | | | | | | | |
| 87h | DTH9 | 00h | R/W | DTH9[7:0] | | | | | | | |
| 88h | DTI1 | 00h | R/W | DTI1[7:0] | | | | | | | |
| 89h | DTI2 | 00h | R/W | DTI2[7:0] | | | | | | | |
| 8Ah | DTI3 | 00h | R/W | DTI3[7:0] | | | | | | | |
| 8Bh | DTI4 | 00h | R/W | DTI4[7:0] | | | | | | | |

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## OPERATION (Continued)

### 2. Register Map (Continued)

| ADDR | Register Name | Default | R/W | DATA | | | | | | | |
|------|---------------|---------|-----|------|------|------|------|------|------|------|------|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 8Ch | DTI5 | 00h | R/W | DTI5[7:0] | | | | | | | |
| 8Dh | DTI6 | 00h | R/W | DTI6[7:0] | | | | | | | |
| 8Eh | DTI7 | 00h | R/W | DTI7[7:0] | | | | | | | |
| 8Fh | DTI8 | 00h | R/W | DTI8[7:0] | | | | | | | |
| 90h | DTI9 | 00h | R/W | DTI9[7:0] | | | | | | | |
| 91h | A1 | 00h | R/W | BRTA1[3:0] | | | | -- | SDTA1[2:0] | | |
| 92h | A2 | 00h | R/W | BRTA2[3:0] | | | | -- | SDTA2[2:0] | | |
| 93h | A3 | 00h | R/W | BRTA3[3:0] | | | | -- | SDTA3[2:0] | | |
| 94h | A4 | 00h | R/W | BRTA4[3:0] | | | | -- | SDTA4[2:0] | | |
| 95h | A5 | 00h | R/W | BRTA5[3:0] | | | | -- | SDTA5[2:0] | | |
| 96h | A6 | 00h | R/W | BRTA6[3:0] | | | | -- | SDTA6[2:0] | | |
| 97h | A7 | 00h | R/W | BRTA7[3:0] | | | | -- | SDTA7[2:0] | | |
| 98h | A8 | 00h | R/W | BRTA8[3:0] | | | | -- | SDTA8[2:0] | | |
| 99h | A9 | 00h | R/W | BRTA9[3:0] | | | | -- | SDTA9[2:0] | | |
| 9Ah | B1 | 00h | R/W | BRTB1[3:0] | | | | -- | SDTB1[2:0] | | |
| 9Bh | B2 | 00h | R/W | BRTB2[3:0] | | | | -- | SDTB2[2:0] | | |
| 9Ch | B3 | 00h | R/W | BRTB3[3:0] | | | | -- | SDTB3[2:0] | | |
| 9Dh | B4 | 00h | R/W | BRTB4[3:0] | | | | -- | SDTB4[2:0] | | |
| 9Eh | B5 | 00h | R/W | BRTB5[3:0] | | | | -- | SDTB5[2:0] | | |
| 9Fh | B6 | 00h | R/W | BRTB6[3:0] | | | | -- | SDTB6[2:0] | | |
| A0h | B7 | 00h | R/W | BRTB7[3:0] | | | | -- | SDTB7[2:0] | | |
| A1h | B8 | 00h | R/W | BRTB8[3:0] | | | | -- | SDTB8[2:0] | | |
| A2h | B9 | 00h | R/W | BRTB9[3:0] | | | | -- | SDTB9[2:0] | | |
| A3h | C1 | 00h | R/W | BRTC1[3:0] | | | | -- | SDTC1[2:0] | | |
| A4h | C2 | 00h | R/W | BRTC2[3:0] | | | | -- | SDTC2[2:0] | | |
| A5h | C3 | 00h | R/W | BRTC3[3:0] | | | | -- | SDTC3[2:0] | | |
| A6h | C4 | 00h | R/W | BRTC4[3:0] | | | | -- | SDTC4[2:0] | | |
| A7h | C5 | 00h | R/W | BRTC5[3:0] | | | | -- | SDTC5[2:0] | | |
| A8h | C6 | 00h | R/W | BRTC6[3:0] | | | | -- | SDTC6[2:0] | | |

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

## Panasonic

**AN32183A**

## OPERATION (Continued)

### 2. Register Map (Continued)

| ADDR | Register Name | Default | R/W | DATA | | | | | | | |
|------|------|------|------|------|------|------|------|------|------|------|------|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| A9h | C7 | 00h | R/W | BRTC7[3:0] | | | | -- | SDTC7[2:0] | | |
| AAh | C8 | 00h | R/W | BRTC8[3:0] | | | | -- | SDTC8[2:0] | | |
| ABh | C9 | 00h | R/W | BRTC9[3:0] | | | | -- | SDTC9[2:0] | | |
| ACh | D1 | 00h | R/W | BRTD1[3:0] | | | | -- | SDTD1[2:0] | | |
| ADh | D2 | 00h | R/W | BRTD2[3:0] | | | | -- | SDTD2[2:0] | | |
| AEh | D3 | 00h | R/W | BRTD3[3:0] | | | | -- | SDTD3[2:0] | | |
| AFh | D4 | 00h | R/W | BRTD4[3:0] | | | | -- | SDTD4[2:0] | | |
| B0h | D5 | 00h | R/W | BRTD5[3:0] | | | | -- | SDTD5[2:0] | | |
| B1h | D6 | 00h | R/W | BRTD6[3:0] | | | | -- | SDTD6[2:0] | | |
| B2h | D7 | 00h | R/W | BRTD7[3:0] | | | | -- | SDTD7[2:0] | | |
| B3h | D8 | 00h | R/W | BRTD8[3:0] | | | | -- | SDTD8[2:0] | | |
| B4h | D9 | 00h | R/W | BRTD9[3:0] | | | | -- | SDTD9[2:0] | | |
| B5h | E1 | 00h | R/W | BRTE1[3:0] | | | | -- | SDTE1[2:0] | | |
| B6h | E2 | 00h | R/W | BRTE2[3:0] | | | | -- | SDTE2[2:0] | | |
| B7h | E3 | 00h | R/W | BRTE3[3:0] | | | | -- | SDTE3[2:0] | | |
| B8h | E4 | 00h | R/W | BRTE4[3:0] | | | | -- | SDTE4[2:0] | | |
| B9h | E5 | 00h | R/W | BRTE5[3:0] | | | | -- | SDTE5[2:0] | | |
| BAh | E6 | 00h | R/W | BRTE6[3:0] | | | | -- | SDTE6[2:0] | | |
| BBh | E7 | 00h | R/W | BRTE7[3:0] | | | | -- | SDTE7[2:0] | | |
| BCh | E8 | 00h | R/W | BRTE8[3:0] | | | | -- | SDTE8[2:0] | | |
| BDh | E9 | 00h | R/W | BRTE9[3:0] | | | | -- | SDTE9[2:0] | | |
| BEh | F1 | 00h | R/W | BRTF1[3:0] | | | | -- | SDTF1[2:0] | | |
| BFh | F2 | 00h | R/W | BRTF2[3:0] | | | | -- | SDTF2[2:0] | | |
| C0h | F3 | 00h | R/W | BRTF3[3:0] | | | | -- | SDTF3[2:0] | | |
| C1h | F4 | 00h | R/W | BRTF4[3:0] | | | | -- | SDTF4[2:0] | | |
| C2h | F5 | 00h | R/W | BRTF5[3:0] | | | | -- | SDTF5[2:0] | | |
| C3h | F6 | 00h | R/W | BRTF6[3:0] | | | | -- | SDTF6[2:0] | | |
| C4h | F7 | 00h | R/W | BRTF7[3:0] | | | | -- | SDTF7[2:0] | | |
| C5h | F8 | 00h | R/W | BRTF8[3:0] | | | | -- | SDTF8[2:0] | | |

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
　　　Writing to these bits will be ignored.

## Panasonic

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## OPERATION (Continued)

### 2. Register Map (Continued)

| ADDR | Register Name | Default | R/W | DATA | | | | | | | |
|------|---------------|---------|-----|------|------|------|------|------|------|------|------|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C6h | F9 | 00h | R/W | BRTF9[3:0] | | | | -- | SDTF9[2:0] | | |
| C7h | G1 | 00h | R/W | BRTG1[3:0] | | | | -- | SDTG1[2:0] | | |
| C8h | G2 | 00h | R/W | BRTG2[3:0] | | | | -- | SDTG2[2:0] | | |
| C9h | G3 | 00h | R/W | BRTG3[3:0] | | | | -- | SDTG3[2:0] | | |
| CAh | G4 | 00h | R/W | BRTG4[3:0] | | | | -- | SDTG4[2:0] | | |
| CBh | G5 | 00h | R/W | BRTG5[3:0] | | | | -- | SDTG5[2:0] | | |
| CCh | G6 | 00h | R/W | BRTG6[3:0] | | | | -- | SDTG6[2:0] | | |
| CDh | G7 | 00h | R/W | BRTG7[3:0] | | | | -- | SDTG7[2:0] | | |
| CEh | G8 | 00h | R/W | BRTG8[3:0] | | | | -- | SDTG8[2:0] | | |
| CFh | G9 | 00h | R/W | BRTG9[3:0] | | | | -- | SDTG9[2:0] | | |
| D0h | H1 | 00h | R/W | BRTH1[3:0] | | | | -- | SDTH1[2:0] | | |
| D1h | H2 | 00h | R/W | BRTH2[3:0] | | | | -- | SDTH2[2:0] | | |
| D2h | H3 | 00h | R/W | BRTH3[3:0] | | | | -- | SDTH3[2:0] | | |
| D3h | H4 | 00h | R/W | BRTH4[3:0] | | | | -- | SDTH4[2:0] | | |
| D4h | H5 | 00h | R/W | BRTH5[3:0] | | | | -- | SDTH5[2:0] | | |
| D5h | H6 | 00h | R/W | BRTH6[3:0] | | | | -- | SDTH6[2:0] | | |
| D6h | H7 | 00h | R/W | BRTH7[3:0] | | | | -- | SDTH7[2:0] | | |
| D7h | H8 | 00h | R/W | BRTH8[3:0] | | | | -- | SDTH8[2:0] | | |
| D8h | H9 | 00h | R/W | BRTH9[3:0] | | | | -- | SDTH9[2:0] | | |
| D9h | I1 | 00h | R/W | BRTI1[3:0] | | | | -- | SDTI1[2:0] | | |
| DAh | I2 | 00h | R/W | BRTI2[3:0] | | | | -- | SDTI2[2:0] | | |
| DBh | I3 | 00h | R/W | BRTI3[3:0] | | | | -- | SDTI3[2:0] | | |
| DCh | I4 | 00h | R/W | BRTI4[3:0] | | | | -- | SDTI4[2:0] | | |
| DDh | I5 | 00h | R/W | BRTI5[3:0] | | | | -- | SDTI5[2:0] | | |
| DEh | I6 | 00h | R/W | BRTI6[3:0] | | | | -- | SDTI6[2:0] | | |
| DFh | I7 | 00h | R/W | BRTI7[3:0] | | | | -- | SDTI7[2:0] | | |
| E0h | I8 | 00h | R/W | BRTI8[3:0] | | | | -- | SDTI8[2:0] | | |
| E1h | I9 | 00h | R/W | BRTI9[3:0] | | | | -- | SDTI9[2:0] | | |

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

# Panasonic

**AN32183A**

## OPERATION (Continued)

### 3. Register map Detailed Explanation

| Register Name | | RST | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 01h | W | -- | -- | -- | -- | -- | -- | RAMRST | SRST |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D1　: RAMRST　　RAM reset
　　　　　　[0] : RAM can be overwrite (default)
　　　　　　[1] : Clear all PWM duty setting and intensity setting

D0　: SRST　　　Soft reset control
　　　　　　[0] : Reset release state (default)
　　　　　　[1] : Reset reset

• This register will auto-return to zero when written with "High" logic value.

| Register Name | | POWERCNT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 02h | R/W | -- | -- | -- | -- | -- | -- | -- | OSCEN |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0　: OSCEN　　Internal oscillator ON/OFF bit
　　　　　　[0] : Internal oscillator OFF (default)
　　　　　　[1] : Internal oscillator ON

• Oscillator will auto turn ON if any of the LED drivers are enabled (MTXON = 1) even if this bit is Low.

## Panasonic

# AN32183A

## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | OPTION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04h | R/W | -- | -- | -- | -- | ZPDEN | MLDACT | CLKOUT | EXTCLK |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D3 : ZPDEN    Ghost Image Prevention Enable
　　　　　　[0] : Turn off ghost image prevention (default)
　　　　　　[1] : Turn on ghost image prevention

D2 : MLDACT    External Melody Input Selection
　　　　　　[0] : Turn off melody mode (default)
　　　　　　[1] : Turn on melody mode

D1 : CLKOUT    Internal clock output enable
　　　　　　[0] : Internal clock is not output from CLKOUT (default)
　　　　　　[1] : Internal clock is output from CLKOUT

D0 : EXTCLK    Internal/external synchronous clock selection
　　　　　　[0] : Internal clock operation (default)
　　　　　　[1] : External clock operation

- Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method. Please refer to page 53 for details.
  Please refer to page 54 for details especially when this IC is used for RGB driver.
- For D2, D1 and D0 cannot be set to High at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

| Register Name | | MTXON | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05h | R/W | -- | -- | -- | IMAX Reserved | | IMAX[2:0] | | MTXON |
| Default | 1Eh | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

D3-1 : IMAX    Maximum current setup selection
　　　　　　[000] : 7.5 mA          [100] : 37.5 mA
　　　　　　[001] : 15 mA           [101] : 45 mA
　　　　　　[010] : 22.5 mA        [110] : 52.5 mA
　　　　　　[011] : 30 mA           [111] : 60 mA (default)

D0 : MTXON    LED Matrix Set up ON/OFF control
　　　　　　[0] : OFF (default)
　　　　　　[1] : ON

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | PWMEN1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06h | R/W | PWMA8 | PWMA7 | PWMA6 | PWMA5 | PWMA4 | PWMA3 | PWMA2 | PWMA1 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7  : PWMA8      A8 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

D6  : PWMA7      A7 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

D5  : PWMA6      A6 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

D4  : PWMA5      A5 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

D3  : PWMA4      A4 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

D2  : PWMA3      A3 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

D1  : PWMA2      A2 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

D0  : PWMA1      A1 PWM mode enable
        [0] : Not PWM mode (default)
        [1] : PWM mode

- Please refer to Page.43 for LED's number A1 to A9.
- The definition for register addresses #07h to #10h is the same as address #06h.

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | MLDEN1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 11h | R/W | MLDA8 | MLDA7 | MLDA6 | MLDA5 | MLDA4 | MLDA3 | MLDA2 | MLDA1 |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7  : MLDA8       A8 Melody  mode enable
  [0] : Not Melody mode (default)
  [1] : Melody mode

D6  : MLDA7       A7 Melody mode enable
  [0] : Not Melody mode (default)
  [1] : Melody mode

D5  : MLDA6       A6 Melody mode enable
  [0] : Not Melody mode (default)
  [1] : Melody mode

D4  : MLDA5       A5 Melody mode enable
  [0] : Not Melody mode (default)
  [1] : Melody mode

D3  : MLDA4       A4 Melody mode enable
  [0] : Not Melody mode (default)
  [1] : Melody mode

D2  : MLDA3       A3 Melody mode enable
  [0] : Not Melody mode (default)
  [1] : Melody mode

D1  : MLDA2       A2 Melody mode enable
  [0] : Not PWM mode (default)
  [1] : Melody mode

D0  : MLDA1       A1 Melody mode enable
  [0] : Not Melody mode (default)
  [1] : Melody mode

- Please refer to Page.43 for LED's number A1 to A9.
- The definition for register addresses #12h to #1Bh is the same as address #11h.

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**AN32183A**

## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | MLDMODE1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2Ah | R/W | -- | -- | -- | -- | GRP9_9 | GRP9_8 | GRP9_2 | GRP9_1 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D3 : GRP9_9     Column 9 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I9 → H9 → G9 → F9 → E9 → D9 → C9 → B9 → A9)

D2 : GRP9_8     Column 8 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I8 → H8 → G8 → F8 → E8 → D8 → C8 → B8 → A8)

D1 : GRP9_2     Column 2 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I2 → H2 → G2 → F2 → E2 → D2 → C2 → B2 → A2)

D0 : GRP9_1     Column 1 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I1 → H1 → G1 → F1 → E1 → D1 → C1 → B1 → A1)
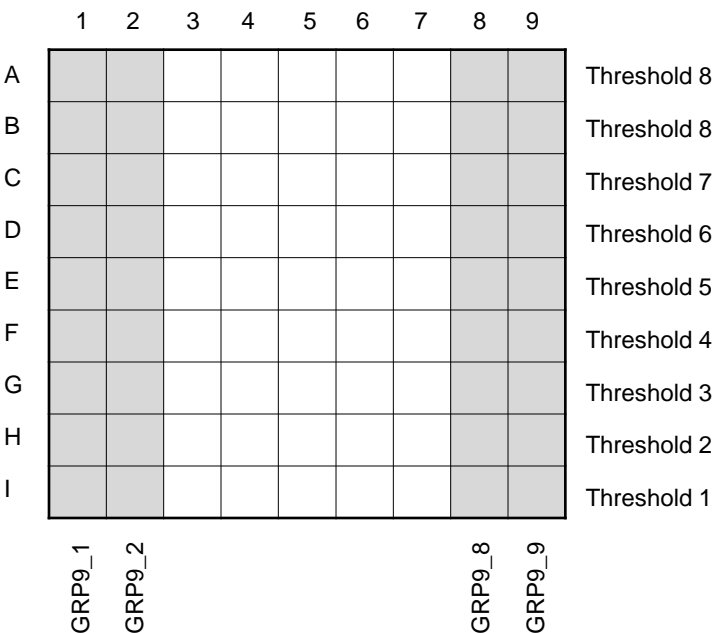
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | | | | | | | | | | Threshold 8 |
| B | | | | | | | | | | Threshold 8 |
| C | | | | | | | | | | Threshold 7 |
| D | | | | | | | | | | Threshold 6 |
| E | | | | | | | | | | Threshold 5 |
| F | | | | | | | | | | Threshold 4 |
| G | | | | | | | | | | Threshold 3 |
| H | | | | | | | | | | Threshold 2 |
| I | | | | | | | | | | Threshold 1 |

GRP9_1, GRP9_2, GRP9_8, GRP9_9

- During Bar Meter Mode, auto threshold detection should be used. This IC does not support Bar Meter Mode with fixed threshold setting.

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**AN32183A**

## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | THOLD | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 2Bh | R/W | | | | THOLD[7:0] | | | | |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7　: THOLD[7]　　Threshold 8 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 8 is used. (Threshold 8 is about 1.93 V)

D6　: THOLD[6]　　Threshold 7 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 7 is used. (Threshold 7 is about 1.80 V)

D5　: THOLD[5]　　Threshold 6 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 6 is used. (Threshold 6 is about 1.67 V)

D4　: THOLD[4]　　Threshold 5 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 5 is used. (Threshold 5 is about 1.55 V)

D3　: THOLD[3]　　Threshold 4 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 4 is used. (Threshold 4 is about 1.42 V)

D2　: THOLD[2]　　Threshold 3 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 3 is used. (Threshold 3 is about 1.30 V)

D1　: THOLD[1]　　Threshold 2 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 2 is used. (Threshold 2 is about 1.17 V)

D0　: THOLD[0]　　Threshold 1 is used as voltage detection.
　　　　　　　　　[0] : Others (default)
　　　　　　　　　[1] : Threshold 1 is used. (Threshold 1 is about 1.04 V)

- When all bits are set zero, threshold is in auto-detection mode (default)
- Do not set more than 1 register bit to logic "High" value at the same time.
- If 2 bits are set to "High" at the same time, system will only recognize the first "High" bit threshold that is set.

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**AN32183A**

## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | CONSTX6_1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2Ch | R/W | -- | -- | X6 | X5 | X4 | X3 | X2 | X1 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D5　: X6　　　　　X6 is fixed as constant current mode.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : X6 is fixed as constant current mode. The LED A6's current setting is used.


D4　: X5　　　　　X5 is fixed as constant current mode.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : X5 is fixed as constant current mode. The LED A5's current setting is used.


D3　: X4　　　　　X4 is fixed as constant current mode.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : X4 is fixed as constant current mode. The LED A4's current setting is used.


D2　: X3　　　　　X3 is fixed as constant current mode.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : X3 is fixed as constant current mode. The LED A3's current setting is used.


D1　: X2　　　　　X2 is fixed as constant current mode.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : X2 is fixed as constant current mode. The LED A2's current setting is used.


D0　: X1　　　　　X1 is fixed as constant current mode.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : X1 is fixed as constant current mode. The LED A1's current setting is used.


• Please refer to page 38 for details.

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | CONSTX10_7 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 2Dh | R/W | -- | -- | -- | -- | X10 | X9 | X8 | X7 |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D3 : X10      X10 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : X10 is fixed as constant current mode. The LED I1's current setting is used.

D2 : X9      X9 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : X9 is fixed as constant current mode. The LED A9's current setting is used.

D1 : X8      X8 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : X8 is fixed as constant current mode. The LED A8's current setting is used.

D0 : X7      X7 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : X7 is fixed as constant current mode. The LED A7's current setting is used.

• Please refer to page 38 for details.

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | CONSTY6_1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2Eh | R/W | -- | -- | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D5 : Y6          Z6 output is fixed to High (VCC level).
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z6 turns on (VCC level).

D4 : Y5          Z5 output is fixed to High (VCC level).
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z5 turns on (VCC level).

D3 : Y4          Z4 output is fixed to High (VCC level).
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z4 turns on (VCC level).

D2 : Y3          Z3 output is fixed to High (VCC level).
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z3 turns on (VCC level).

D1 : Y2          Z2 output is fixed to High (VCC level).
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z2 turns on (VCC level).

D0 : Y1          Z1 output is fixed to High (VCC level).
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z1 turns on (VCC level).

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | CONSTY9_7 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 2Fh | R/W | -- | -- | -- | -- | -- | Y9 | Y8 | Y7 |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D2 : Y9  Z9 output is fixed to High (VCC level).
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z9 turns on (VCC level).

D1 : Y8  Z8 output is fixed to High (VCC level).
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z8 turns on (VCC level).

D0 : Y7  Z7 output is fixed to High (VCC level).
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z7 turns on (VCC level).

• Please refer to page 38 for details.

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | MASKY6_1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 30h | R/W | -- | -- | Y6MSK | Y5MSK | Y4MSK | Y3MSK | Y2MSK | Y1MSK |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

    D5  : Y6MSK        Z6 output is fixed to OFF.
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z6 turns off.

    D4  : Y5MSK        Z5 output is fixed to OFF.
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z5 turns off.

    D3  : Y4MSK        Z4 output is fixed to OFF.
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z4 turns off.

    D2  : Y3MSK        Z3 output is fixed to OFF.
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z3 turns off.

    D1  : Y2MSK        Z2 output is fixed to OFF.
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z2 turns off.

    D0  : Y1MSK        Z1 output is fixed to OFF.
                   [0] : Normal matrix operation (default)
                   [1] : Switch between VCC and Z1 turns off.

• Please refer to page 38 for details.

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | MASKY9_7 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 31h | R/W | -- | -- | -- | -- | -- | Y9MSK | Y8MSK | Y7MSK |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D2 : Y9MSK      Z9 output is fixed to OFF.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : Switch between VCC and Z9 turns off.

D1 : Y8MSK      Z8 output is fixed to OFF.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : Switch between VCC and Z8 turns off.

D0 : Y7MSK      Z7 output is fixed to OFF.
　　　　　　　[0] : Normal matrix operation (default)
　　　　　　　[1] : Switch between VCC and Z7 turns off.


• Please refer to page 38 for details.

## Panasonic

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | SLPTIME | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 32h | R/W | -- | -- | -- | FADTIM | SLOPEEXTL[1:0] | | SLOPEEXTH[1:0] | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D4  : FADTIM        Fade out time control.
            [0] : T3 = T1 (default)
            [1] : T3 = T1 $\times$ 2

• This bit also affect in PWM fade out mode. Fade out time becomes 2 times of fade in time when FADTIM = 1.

D3-2 : SLOPEEXTL   T4 time extent control.
            [00] : T4 = T1 (default)
            [01] : T4 = T1 $\times$ 0.25
            [10] : T4 = T1 $\times$ 0.5
            [11] : T4 = T1 $\times$ 2

D1-0 : SLOPEEXTH   T2 time extent control.
            [00] : T2 = T1 (default)
            [01] : T2 = T1 $\times$ 0.25
            [10] : T2 = T1 $\times$ 0.5
            [11] : T2 = T1 $\times$ 2

• T1 time is controlled by the register #91h to #E1h.

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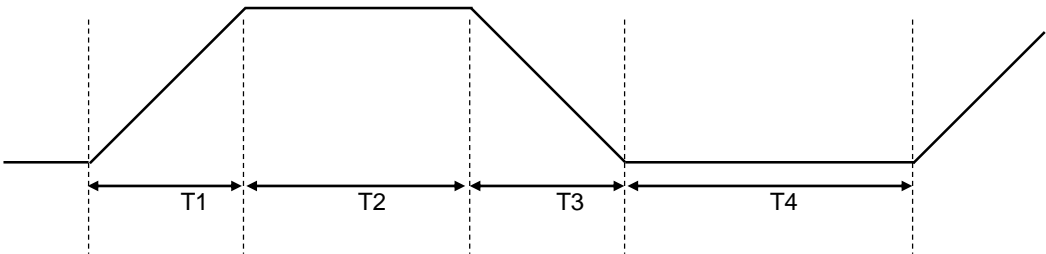
## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | MLDCOM | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 33h | R/W | -- | -- | -- | -- | -- | MLDCOM[2:0] | | |
| Default | 03h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

D2-0 : MLDCOM    LED Turn on time compensation in melody mode

      [000] : 0s

      [001] : 1.94 µs

      [010] : 3.87 µs

      [011] : 5.80 µs (default)

      [100] : 7.74 µs

      [101] : 9.67 µs

      [110] : 11.6 µs

      [111] : 13.5 µs

| Register Name | | SCANSET | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 36h | R/W | -- | -- | -- | -- | SCANSET[3:0] | | | |
| Default | 08h | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

D3-0 : SCANSET    SCAN number control

      [0000] : Only scan the first column.

      [0001] : Only scan the first 2 column.

      [0010] : Only scan the first 3 column.

      [0011] : Only scan the first 4 column.

      [0100] : Only scan the first 5 column.

      [0101] : Only scan the first 6 column.

      [0110] : Only scan the first 7 column.

      [0111] : Only scan the first 8 column.

      [1000] : Scan all column. (default)

• All other values will scan all column.

# Panasonic

## AN32183A

## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | DTA1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 40h | R/W | | | | DTA1[7:0] | | | | |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-0 : DTA1       A1 PWM duty control.
        [0000_0000] : 0%. (default)
        [0000_0001] : 0.39%. (1/256)
        [0000_0010] : 0.78%. (2/256)
        [0000_0011] : 1.17%. (3/256)

        …
        [1111_1100] : 98.8%. (253/256)
        [1111_1110] : 99.2%. (254/256)
        [1111_1111] : 99.6%. (255/256)

- This duty setting is only effective when PWMA1 is High.
- The definition for register addresses #41h to #90h is the same as address #40h.

# Panasonic

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## OPERATION (Continued)

### 3. Register map Detailed Explanation (Continued)

| Register Name | | A1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **R/W** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 91h | R/W | BRTA1[3:0] | | | | -- | SDTA1[2:0] | | |
| **Default** | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-4 : BRTA1　　　　Luminance set up of LED A1 (in case of IMAX [2:0] = [011])
　　　　　　　　[0000] : 0 mA (default)
　　　　　　　　[0001] : 2 mA
　　　　　　　　[0010] : 4 mA
　　　　　　　　[0011] : 6 mA
　　　　　　　　[0100] : 8 mA
　　　　　　　　[0101] : 10 mA
　　　　　　　　…
　　　　　　　　[1010] : 20 mA
　　　　　　　　[1011] : 22 mA
　　　　　　　　[1100] : 24 mA
　　　　　　　　[1101] : 26 mA
　　　　　　　　[1110] : 28 mA
　　　　　　　　[1111] : 30 mA

D2-0 : SDTA1　　　　(SCANSET = [11], default setting)

　　　(1) Firefly Operation (PWMA1 = 0)
　　　　　　　　[000] : Constant current mode (default)
　　　　　　　　[001] : 0.248 s
　　　　　　　　[010] : 0.495 s
　　　　　　　　[011] : 0.99 s
　　　　　　　　[100] : 1.484 s
　　　　　　　　[101] : 1.979 s
　　　　　　　　[110] : 2.473 s
　　　　　　　　[111] : 2.968 s

| T1 | T2 | T3 | T4 |
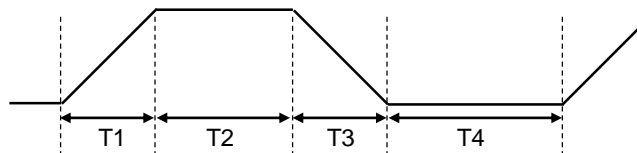
　　　(2) PWM Fade-in/out Operation (PWMA1 = 1)
　　　　　　　　[000] : Instant change mode (default)
　　　　　　　　[001] : 1.939 ms
　　　　　　　　[010] : 3.879 ms
　　　　　　　　[011] : 7.758 ms
　　　　　　　　[100] : 11.636 ms
　　　　　　　　[101] : 15.515 ms
　　　　　　　　[110] : 19.394 ms
　　　　　　　　[111] : 23.273 ms

- In case of PWM duty change from 0 to 255, the longest time is $255 \times 23.273$ ms = 5.957 s.
- T1 time is also controlled by SCANSET in register #36h. The calculation method is as follow:
　　　　SCANSET = 0000 : T1 = $0.111 \times$ T_default
　　　　SCANSET = 0001 : T1 = $0.222 \times$ T_default
　　　　…
　　　　SCANSET = 0111 : T1 = $0.888 \times$ T_default
- The definition for register addresses #92h to #E1h is the same as address #91h.

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## OPERATION (Continued)

### 4. Operation Mode priority

| MTXON | X* | Y*MSK | Y* | PWM* | SDT* | Operation Mode |
|-------|-----|-------|-----|------|------|----------------|
| 0 | x | x | x | x | x | OFF |
| 1 | 1 | x | x | x | x | X*CNT constant mode |
| 1 | 0 | 1 | x | x | x | OFF |
| 1 | 0 | 0 | 1 | x | x | Turn on with all A1, A2, A3, A4 |
| 1 | 0 | 0 | 0 | 1 | x | PWM mode |
| 1 | 0 | 0 | 0 | 0 | !=0 | Blinking mode |
| 1 | 0 | 0 | 0 | 0 | 0 | Constant current mode |

• * for X*, PWM*, SDT* = 1 ~ 10, * for Y*MSK, Y* = 1 ~ 9.

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# AN32183A

## OPERATION (Continued)

### 5. I²C Bus Interface

#### 5.1 Basic Rules

- This IC, I²C-bus, is designed to correspond to the Standard-mode (100 kbps), Fast-mode(400 kbps) and Fast-mode plus (1 000 kbps) devices in the version 03 of NXP's specification. However, it does not correspond to the $H_S$-mode (to 3.4 Mbps).
- This IC will operate as a slave device in the I²C-bus system. This IC will not operate as a master device.
- The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.
- The I²C is the brand of NXP.

#### 5.2 START and STOP conditions

When SDA signal changes from "High" to "Low" while SCL is "High" will trigger START condition. Whereas, STOP condition will be triggered when SDA signal changes from "Low" to "High" while SCL is "High". START condition and STOP condition are always formed by the master. After the START condition occurs, the bus becomes busy state. After STOP condition occurs, the bus becomes free again.
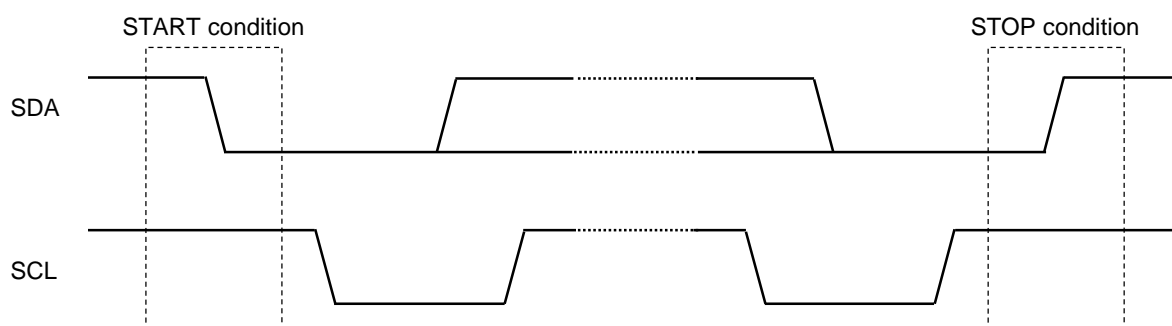
#### 5.3 Data Transfer

Length of each byte output to SDA line is always 8 bits. There is no limitation in the number of bytes that can be transmitted at 1 time. Many bytes can be sent. The acknowledge bit is necessary for each byte. Data is sequentially transmitted from most significant bit (MSB).

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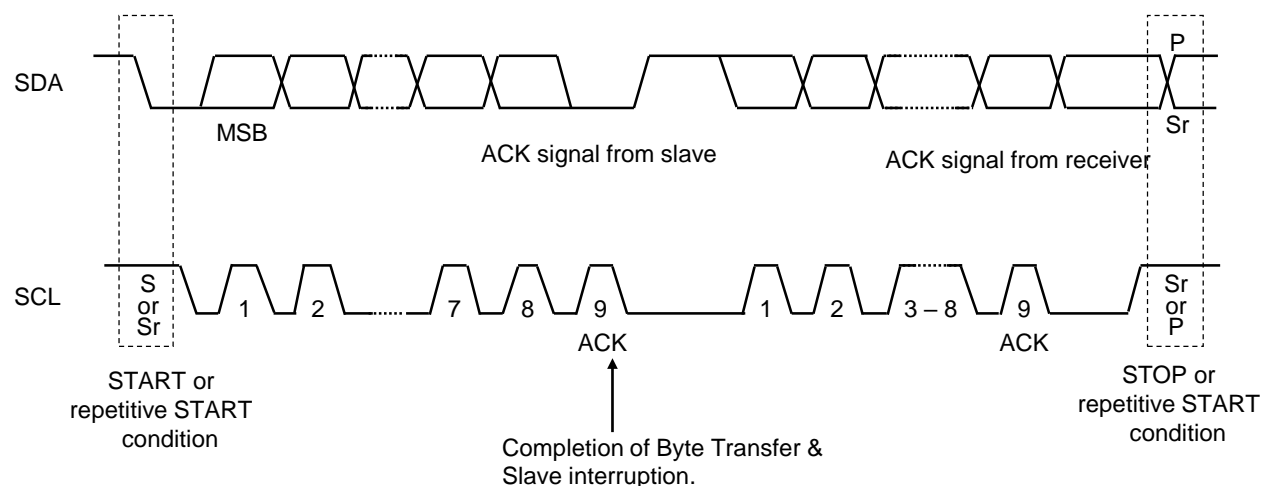
## OPERATION (Continued)

### 5. I²C Bus Interface (Continued)

#### 5.4 I²C Interface - Data Format

In this IC, 4 different Slave addresses can be changed by selecting SLAVSEL ( "Low" or "High" or "SCL" or "SDA").
The slave addresses of this IC are as follow:

| SLAVSEL | Slave address |
|---------|---------------|
| Low | 1011 100X |
| High | 1011 101X |
| SCL | 1011 110X |
| SDA | 1011 111X |

• Write mode

Sub address is not incremented automatically.
The next data byte is written in the same Sub address by transmitting data byte continuously.
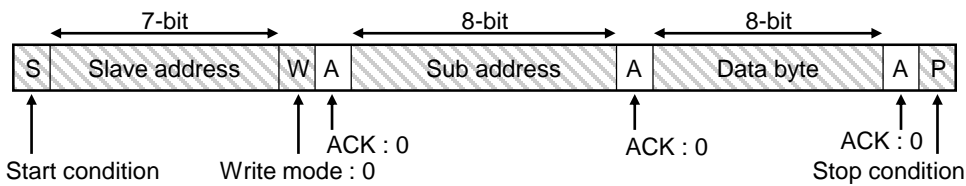


• Write mode (Auto increment mode)

Data byte can be written in Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

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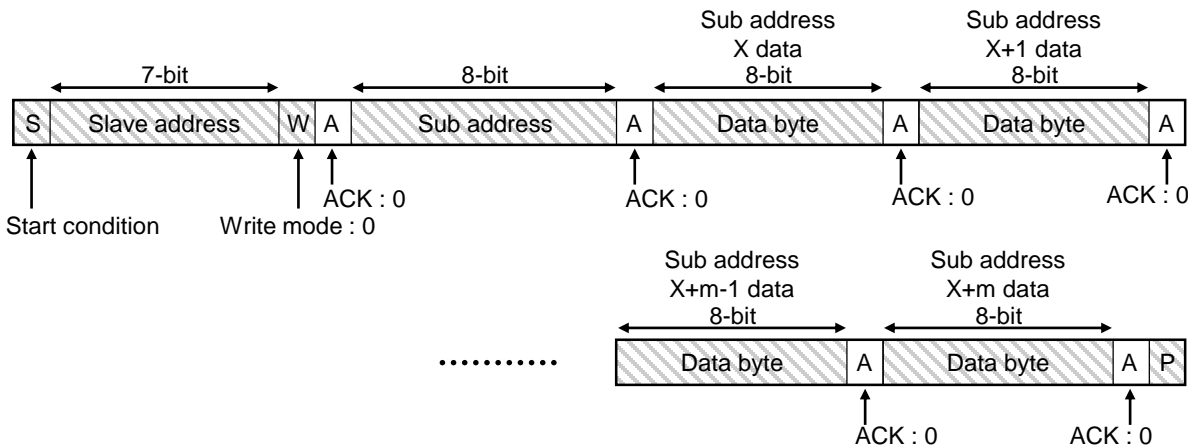
## OPERATION (Continued)

### 5. I²C Bus Interface (Continued)

#### 5.4 I²C Interface - Data Format (Continued)

• Read mode (in case Sub address is not specified)

When Sub address 8 bit is not specified and data is read, this IC allows to read the value of adjacent Sub address specified in the last Write mode.
The next data byte reads the same Sub address by transmitting data byte continuously.

| 7-bit | | | 8-bit | | |
|---|---|---|---|---|---|
| S | Slave address | R | A | Data byte | Ā | P |

ACK : 0    NACK : 1

Start condition    Read mode : 1    Stop condition
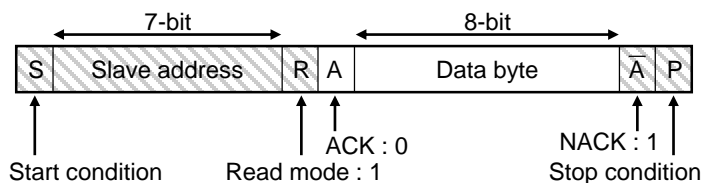
• Read mode (in case Sub address is specified)

Sub address is not incremented automatically.
The next data byte reads the same Sub address by transmitting data byte continuously.

| 7-bit | | 8-bit | | 7-bit | | 8-bit | |
|---|---|---|---|---|---|---|---|
| S | Slave address | W A | Sub address | A Sr | Slave address | R A | Data byte | Ā P |

ACK : 0    ACK : 0    ACK : 0    NACK : 1

Start condition    Write mode : 0    Repeated start condition    Read mode : 1    Stop condition
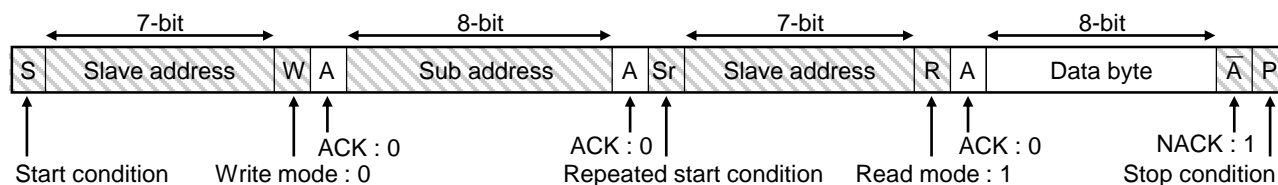
• Read mode (Auto increment mode)

It is possible to read data byte in continuous Sub address by transmitting data byte continuously.
Sub address is incremented automatically.

Sub address
X data
8-bit

| 7-bit | | 8-bit | | 7-bit | | 8-bit | |
|---|---|---|---|---|---|---|---|
| S | Slave address | W A | Sub address | A Sr | Slave address | R A | Data byte | A |

ACK : 0    ACK : 0    ACK : 0    ACK : 0

Start condition    Write mode : 0    Repeated start condition    Read mode : 1

Sub address              Sub address
X+m−1 data               X+m data
8-bit                    8-bit

·········     | Data byte | A | Data byte | Ā P |

ACK : 0    NACK : 1

Stop condition

▨ : Data transmission from Master

☐ : Data transmission from Slave

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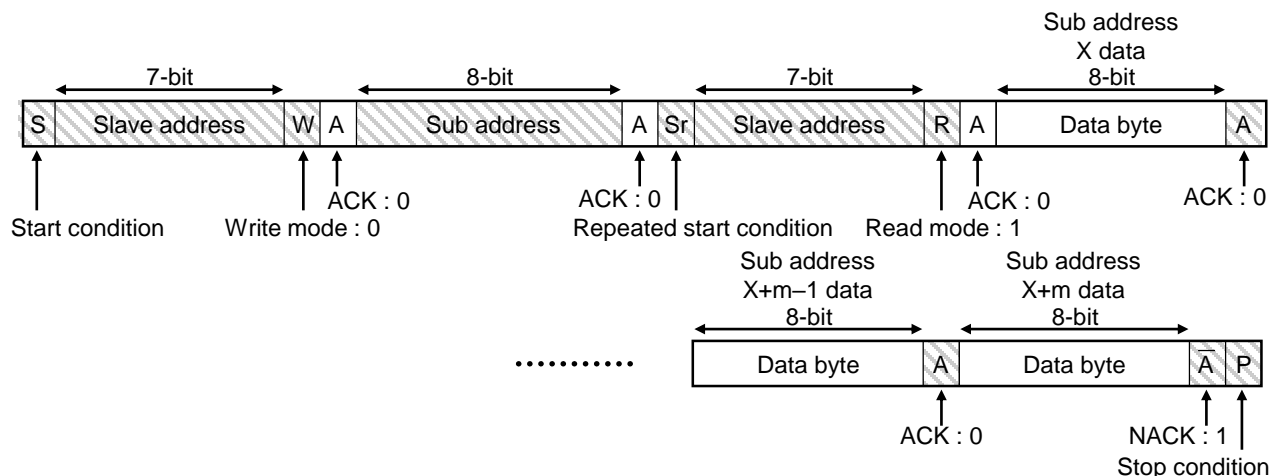
## OPERATION (Continued)

### 6. Signal distribution diagram

#### 6.1 Distribution diagram of power supply
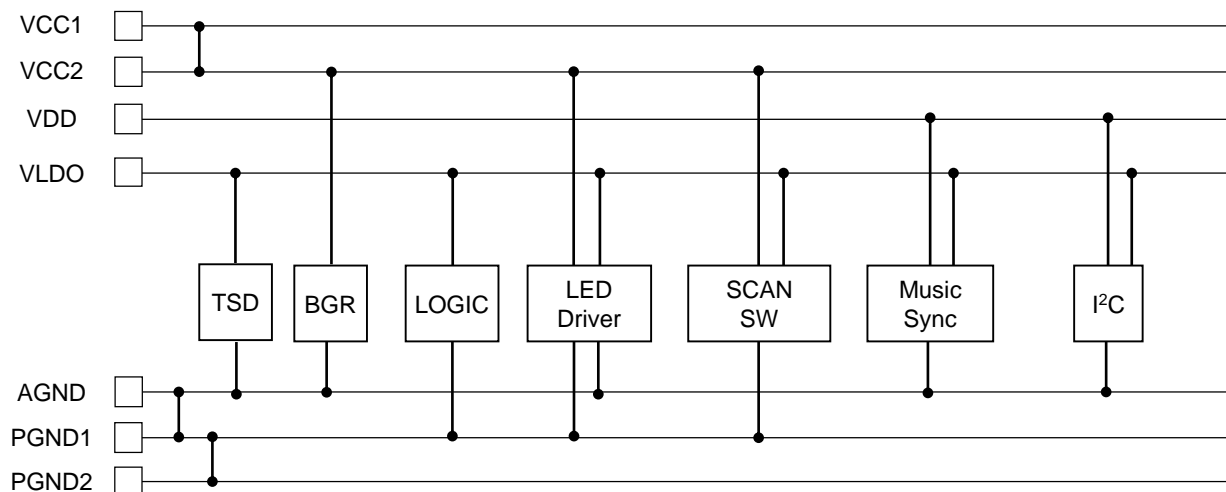


#### 6.2 Distribution diagram of control / clock system

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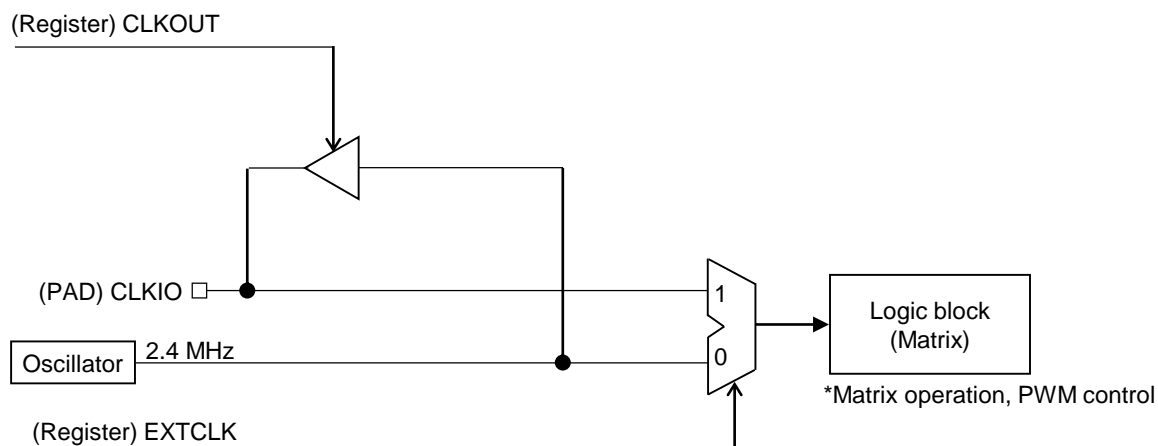
## OPERATION (Continued)

### 7. Block Configuration of Matrix LED

#### 7.1 Matrix LED descriptions, Matrix LED's numbers

LED matrix driver circuit individually drives LED of 9 × 9 matrix. In total, the IC can drive and light up 81 LED.
In this specification, LED's number controlled by each pin corresponds as follows.
The internal logic circuit is operated by using an internal clock or the external clock input to the terminal CLKIO.

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# AN32183A
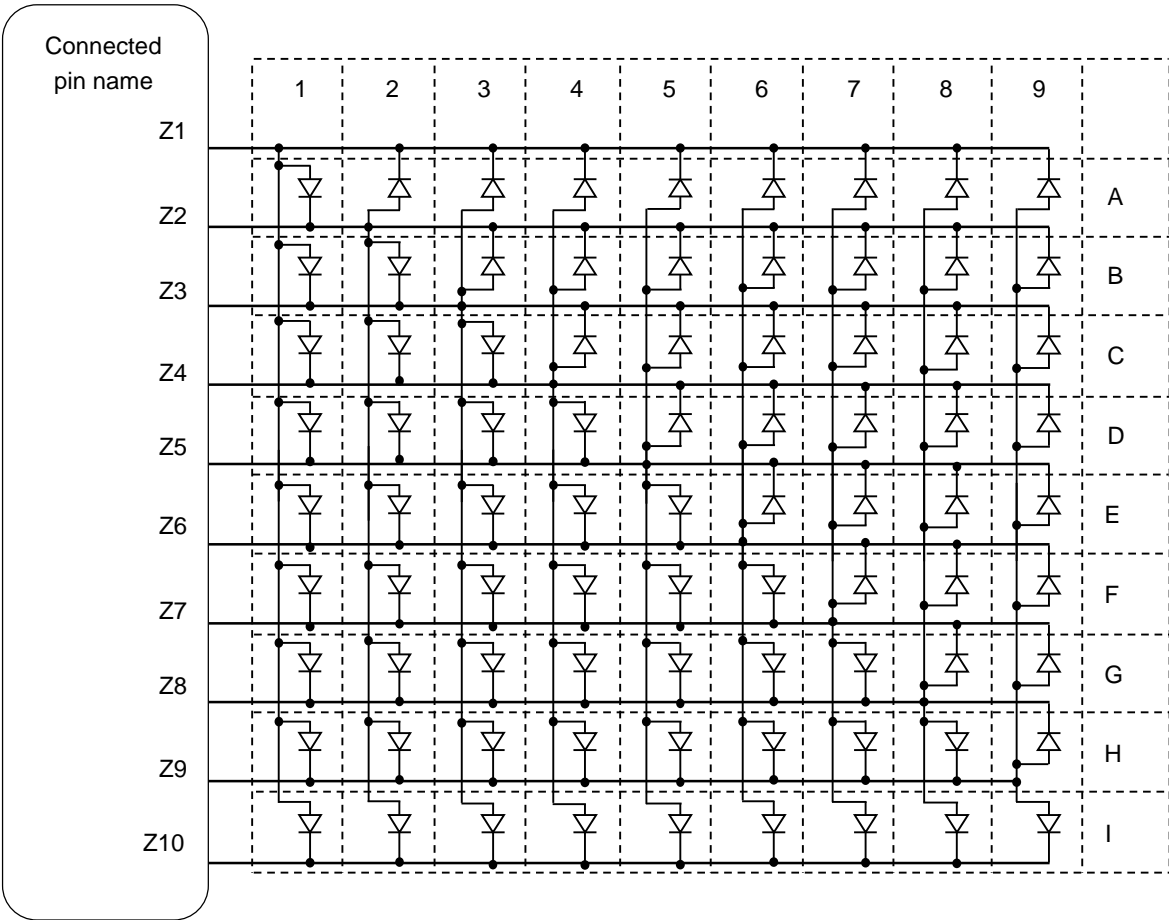
## OPERATION (Continued)

### 7. Block Configuration of Matrix LED (Continued)

#### 7.2 Driver Configuration

- Actual driver configuration is shown in the following figure.
- The anode and cathode of each LED are connected to different Z pin as shown in figure below.
- Z10 pin consists of only Current Sink and Slope control timing driver. Thus, LED anodes are not to be connected to Z10 pin.
- Please do not remove any of the LED inside the matrix if it is not used. If LED are to be removed, it is advised to remove the entire row (e.g: all LED in row A) instead of removing only 1 LED. If only one LED in the row is removed instead of the whole row, user needs to avoid using LED of which reverse breakdown voltage is lower than the operating $V_{CC}$ level.
- Internal control logic according to user register settings is used to control Y1 to Y9CNT(PMOS ON/OFF Scan Switches) as well as X1 to X10CNT (Current sink value as well as PWM/Slope timing for lighting effects)

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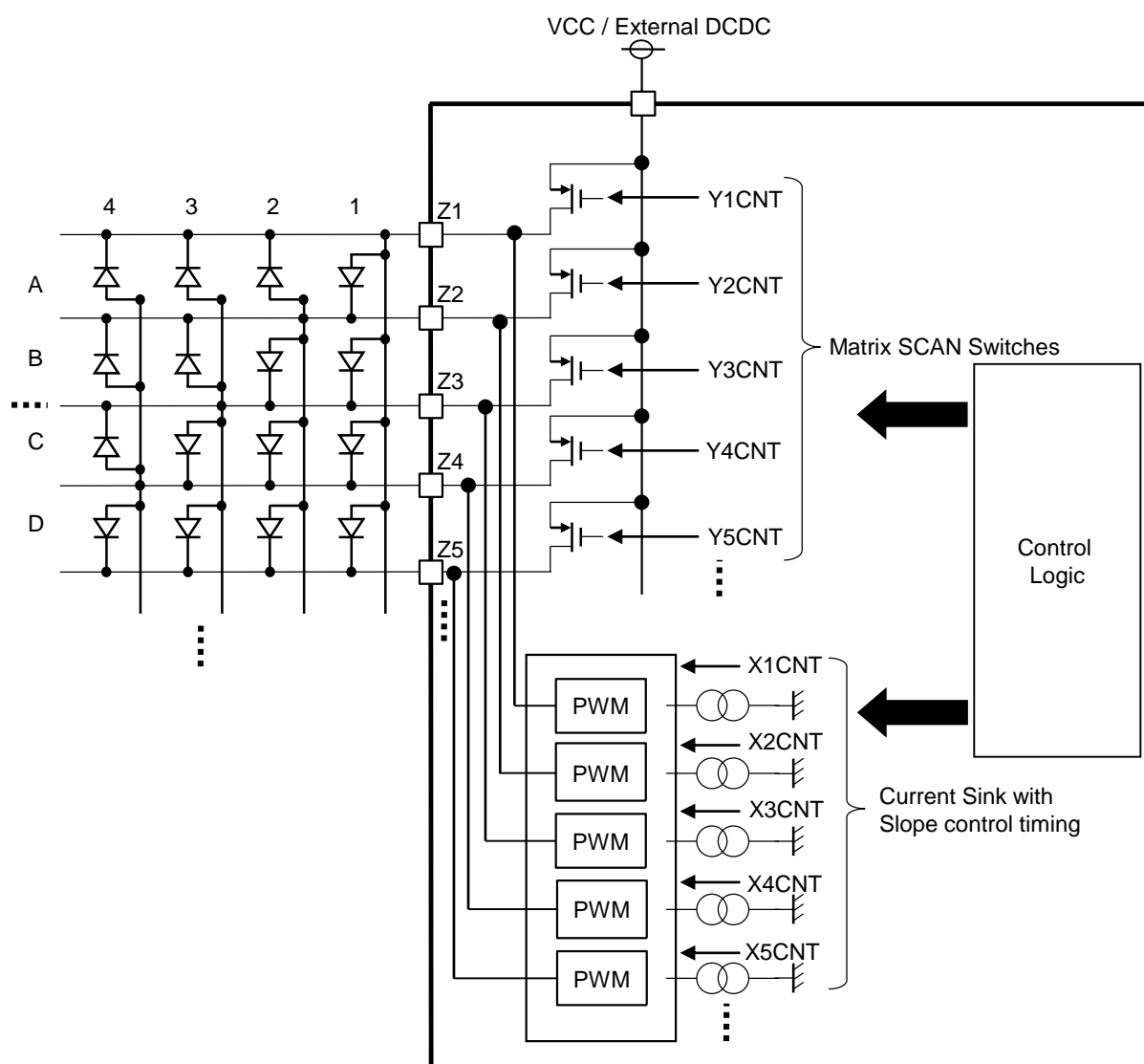
## OPERATION (Continued)

### 7. Block Configuration of Matrix LED (Continued)

#### 7.3 Timing Chart when in operation

- The figure below shows the timing chart when in operation.
- Timing can be controlled according to the external clock frequency input to CLKIO pin.
- In default condition, it is controlled by internal 2.4 MHz clock.
- Y1 to Y9CNT are scan timing which is turned on one at a time. The ON period of each pin is constant 255 clks (106.08 μs) and includes the interval of 4 clks (1.664 μs).
- 81 LED (9 × 9 matrix) are controlled by X1 to X10CNT according to below figure.
- When Y*CNT = "High", X*CNT = "Low", the actual waveform of Z* is set to Hi-Z.
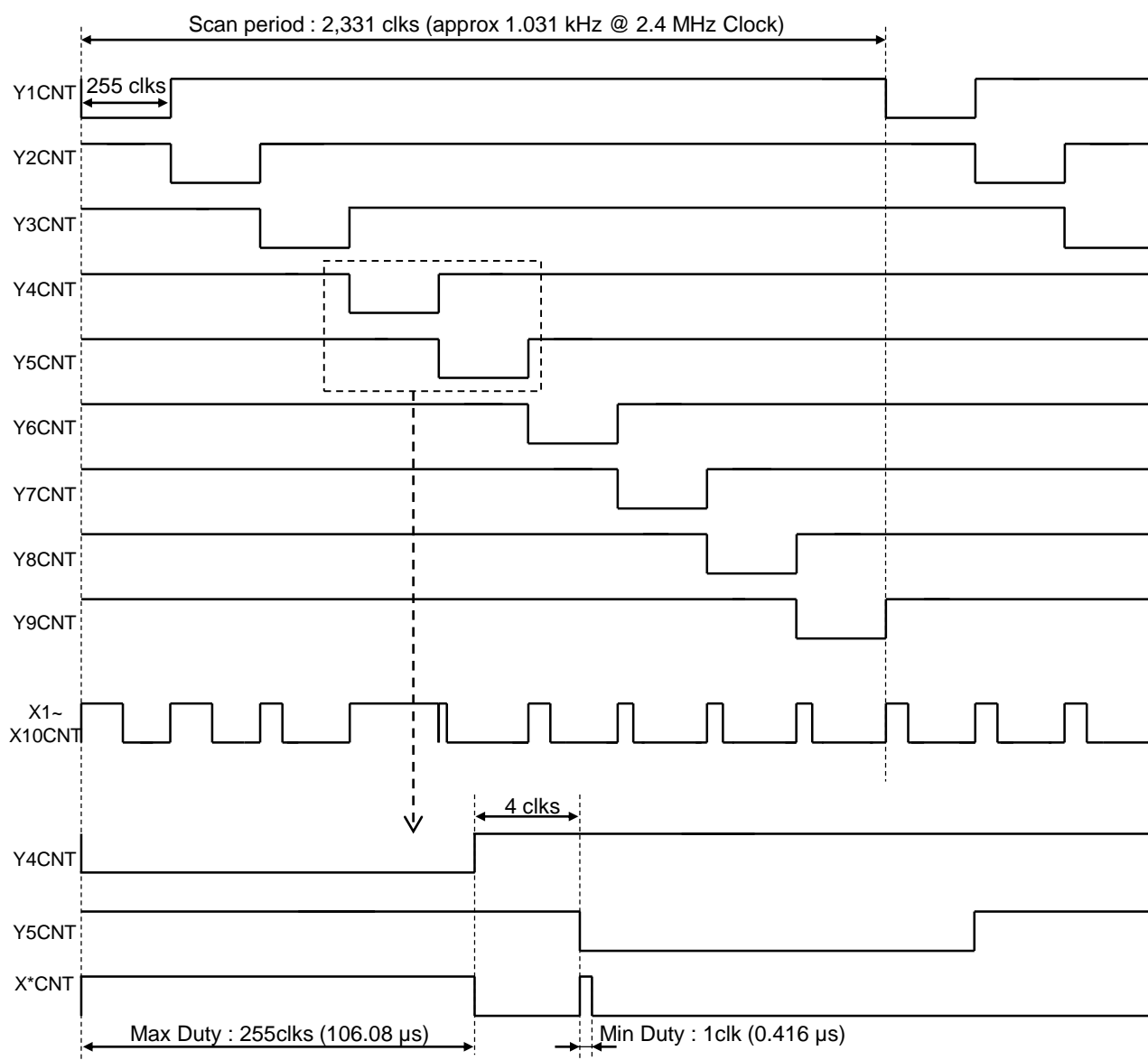


- Duty can be set using register DT*[7:0] from registers #40h to #90h. Additional brightness control is provided through register BRT*[3:0] (registers #91h to #E1h).

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## OPERATION (Continued)

### 8. LED Driver Block Function

• Functions Table for LED Driver

| No. | Features | Setting Range |
|-----|----------|---------------|
| 1 | Constant current mode | IMAX Setting :                                                    7.5 mA to 60 mA (max)<br>DAC Current Step (Brightness) :    0.5 mA to 4 mA (max) step |
| 2 | PWM mode and Fade-in/out mode | IMAX Setting :                           7.5 mA to 60 mA (max)<br>DAC Current Step (Brightness) :    0.5 mA to 4 mA (max) step<br>Adjustable detention Time for each step : (1.939 ms to 23.273 ms / step) |
| 3 | Firefly mode | Fixed Current at 100% Duty IMAX Setting : 7.5 mA to 60 mA (max)<br>DAC Current Step (Brightness) :       0.5 mA to 4 mA (max) step<br>Adjustable detention Time for each step :   (0.248 s to 2.968 s / step) |
| 4 | Melody mode | IMAX Setting :                           7.5 mA to 60 mA (max)<br>DAC Current Step (Brightness) :    0.5 mA to 4 mA (max) step<br>Each LED can synchronize with Music Input from CLKIO pin |
| 5 | Bar Meter Mode | IMAX Setting :                           7.5 mA to 60 mA (max)<br>DAC Current Step (Brightness) :    0.5 mA to 4 mA (max) step<br>Group LED can synchronize with Music Input from CLKIO pin<br>Bar Meter Mode has more priority than Melody mode. |

### 8.1  Constant Current Mode

Maximum current setting value can be set up as 60mA using register IMAX[2:0] (register 05h). Brightness can be set through the register BRT*[3:0] (register #91h to #E1h) for individual LED.

Example)

E.g. If user sets register IMAX[2:0](#05h) = 011 and BRT*[3:0](#91h to #E1h) = 1111, the current will be 30 mA.
E.g. If user sets register IMAX[2:0](#05h) = 111 and BRT*[3:0](#91h to #E1h) = 1111, the current will be 60 mA.
E.g. If user sets register IMAX[2:0](#05h) = 111 and BRT*[3:0](#91h to #E1h) = 0111, the current will be 28 mA.

Current value

60 mA (max)

t

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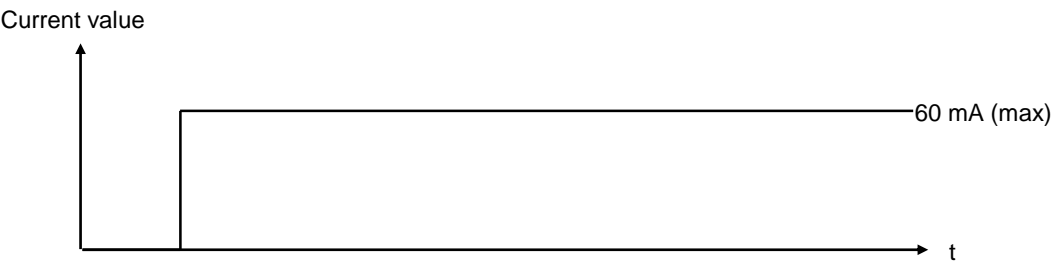
## OPERATION (Continued)

### 8. LED Driver Block Function (Continued)

#### 8.2  PWM Mode and Fade-in/out Mode

This operation is characterized by PWM signal having variable duty depending on register DT*[7:0] (registers #40h to #90h). However, any changes in duty are not instantaneous, but rather it will step to the new duty at time determined by register SDT*[2:0].

Example)

Case 1 :  LED*DT(new) > LED*DT(old) (PWM Mode without Fade in/out control)
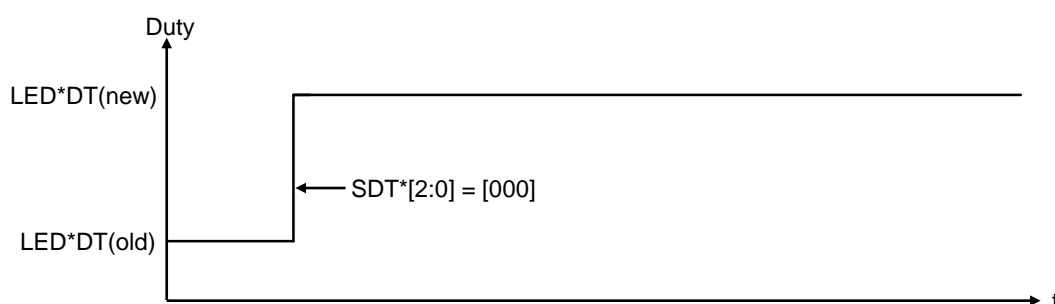


In Case 1, PWM duty has been changed from low to high duty. But the register SDT*[2:0] setting is [000] indicating that there is no Fade in/out control. Therefore, PWM duty changes instantaneously. Users can see that LED becomes brighter instantaneously once PWM duty has been changed.

Case 2 :  LED*DT(new) > LED*DT(old) (PWM Mode with Fade in control)
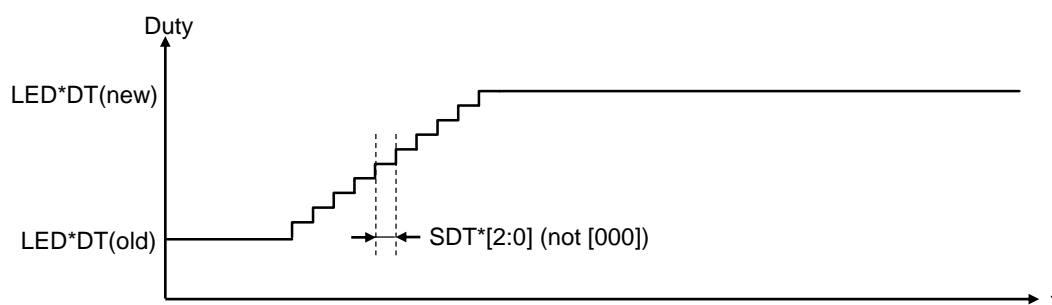


In Case 2, PWM duty has also been changed from low to high duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 2. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade in control. Users can see that LED becomes brighter slowly according to the timing set in register SDT*[2:0].

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## OPERATION (Continued)

### 8. LED Driver Block Function (Continued)

#### 8.2 PWM Mode and Fade-in/out Mode (Continued)

Example) (continued)

Case 3 :  LED*DT (new) < LED*DT (old) (PWM Mode with Fade out control), FADTIM = [0]
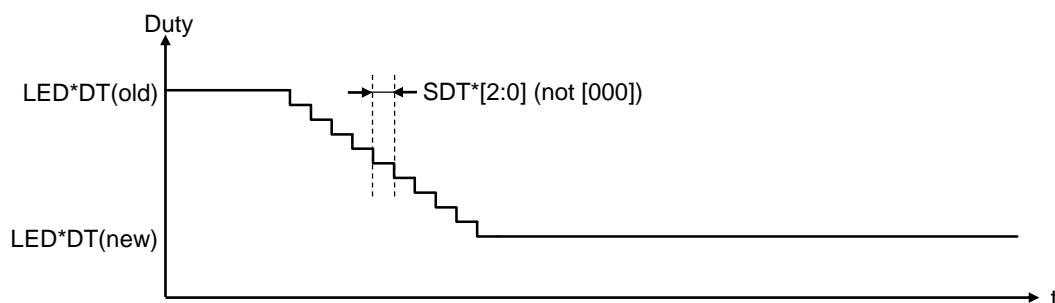


In Case 3, PWM duty has been changed from high to low duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 3. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade out control. Users can see that LED becomes dimmer slowly according to the timing set in register SDT*[2:0].

Case 4 :  LED*DT (new) < LED*DT (old) (PWM Mode with Fade out control), FADTIM = [1]
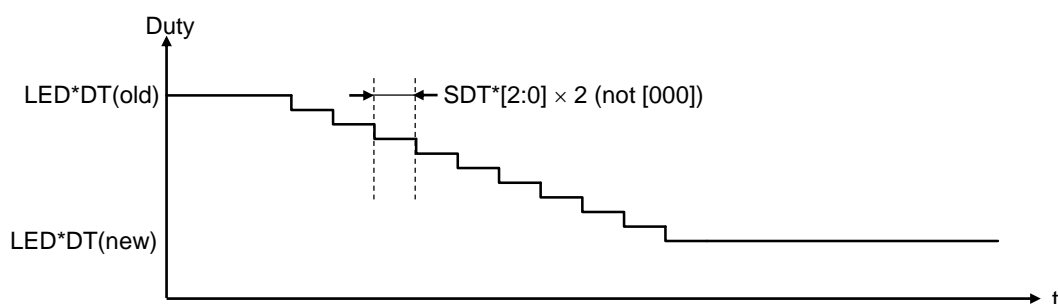


In Case 4, PWM duty has also been changed from high to low duty. Unlike in case 3, the register FADTIM is not [0]. Again, the register SDT*[2:0] setting is also not [000] in case 4. PWM duty has changed according to the register SDT*[2:0] setting. Users can see that LED becomes dimmer slowly. It is slower than Case3 as FADTIM register is high (2 times slower than Case 3 Fade out control).

DT*[7:0] is set through register #40h to #90h. FADTIM is set through register #32h. SDT*[2:0] is set through register #91h to #E1h.

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## OPERATION (Continued)

### 8. LED Driver Block Function (Continued)

#### 8.3 Firefly Control

This operation is characterized by PWM signal cycling from minimum to maximum duty and vice versa with auto repeat function at time step determined by register SDT*[2:0]. Unlike PWM Fade in/out mode, firefly is auto repetition of the sequence and thus creating LED blinking function effect.
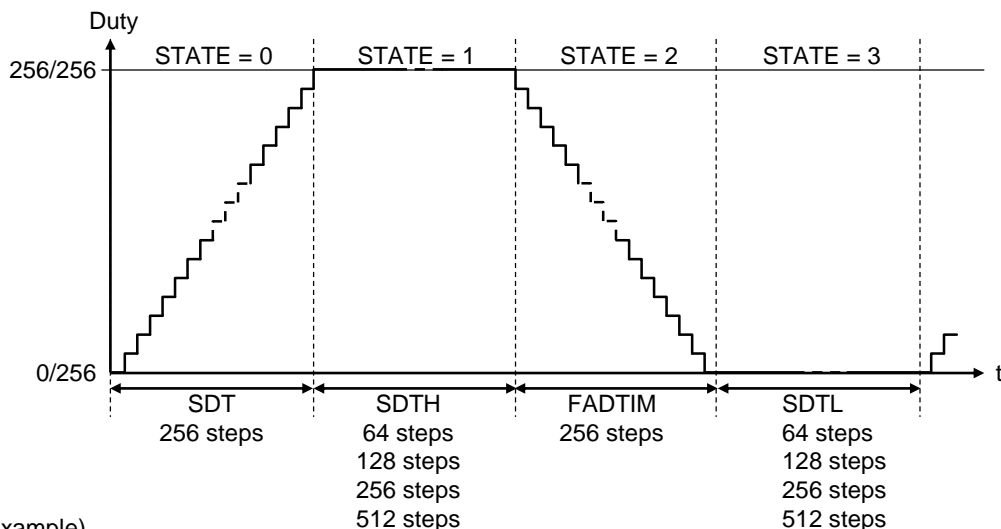
Example)

Example 1 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 0
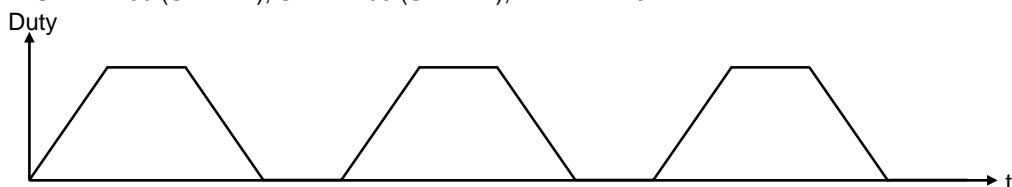
Example 2 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 1 (SDT × 2)
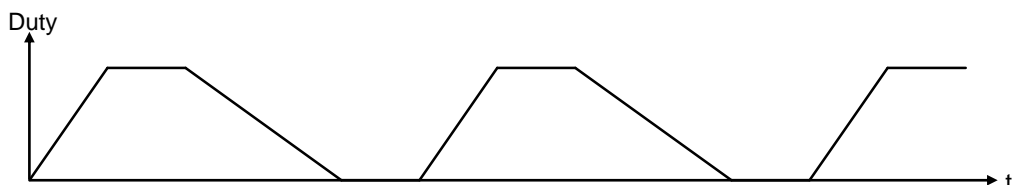
Example 3 : SDTH = 01 (SDT × 0.25), SDTL = 11 (SDT × 2), FADTIM = 0
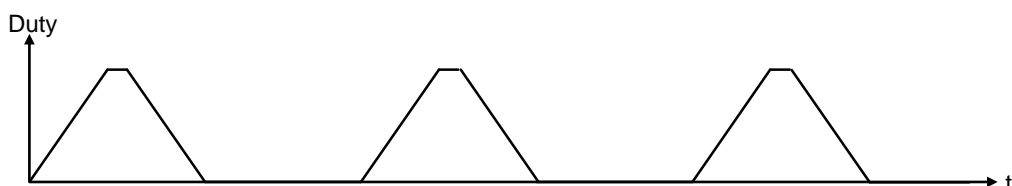
The SDTH is controlled by SLOPEEXTH[1:0] register, SDTL is controlled by SLOPEEXTL[1:0] register. All these register, SLOPEEXTH[1:0], SLOPEEXTL[1:0] and FADTIM can be set through register #32h.
SDT*[2:0] registers are set individually through register #91h to #E1h. All other combinations of SDTH, SDTL and FADTIM is possible.

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## OPERATION (Continued)

### 8. LED Driver Block Function (Continued)

#### 8.4 Melody Mode Explanation

Melody mode is to synchronize LED to external music signal. Melody mode can be set through register MLDACT from register 04h. Each of the 16 LED matrix can be individually enabled for external music synchronization through register data (address #08h to #09h when register address 04h is set as data 04h).

External Music Signal can be injected from CLKIO pin. CLKIO pin serve as both input and output. CLKIO pin can output internal oscillator frequency by using CLKOUT register (register 04h).

CLKIO pin can be used as input for external signal by using EXTCLK register (register 04h). External clock frequency is typically 2.4 MHz. It is advisable to use external clock frequency from 1.2 MHz to 4.8 MHz.

Please do not set MLDACT, EXTCLK and CLKOUT register to "High" at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Case 1 : CLKIO as output pin
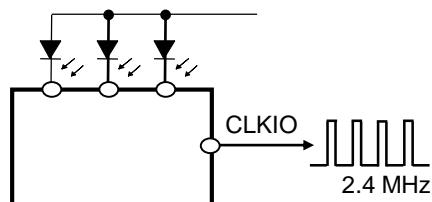
CLKIO output internal frequency by using CLKOUT register

2.4 MHz

Case 2 : CLKIO as input for external clock
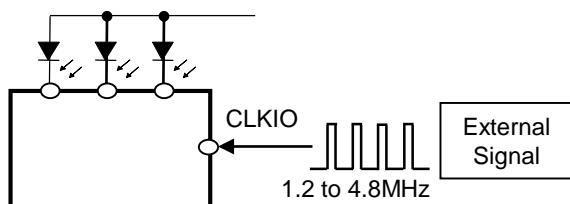
CLKIO uses as external input by using EXTCLK register

1.2 to 4.8MHz    External Signal

Case 3 : CLKIO as input for music signal during melody mode
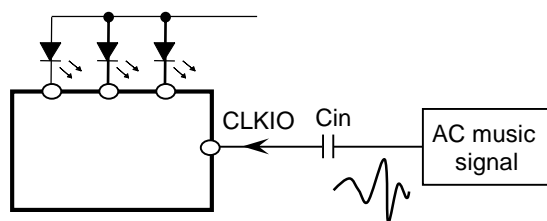
CLKIO uses as music input when melody mode is enabled by register MLDACT from register 04h.

CLKIO Cin    AC music signal

Note : If input CLKIO voltage is higher than VDD, there will be back flow current to VDD. It can be calculated as below :

$$I_{BackFlow} = \frac{(V_{CLKIO} - 0.7\ V - VDD)}{393\ k\Omega}$$

Note : Cin can be calculated as below : In case of that the applicable music frequency is 20 Hz.

$$Cin \geq \frac{1}{(20\ Hz) \times 2 \times 3.14 \times 175\ k\Omega} = 45.5\ nF$$

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## OPERATION (Continued)

### 8. LED Driver Block Function (Continued)

#### 8.4  Melody Mode Explanation (Continued)

AC music signal input from CLKIO pin will be compared with internal threshold setting. Based on the comparison of music signal and threshold voltage, PWM driver control will change and control the LED ON/OFF. Therefore, LED light ON/OFF control will synchronize with music tempo while LED brightness will synchronize with music loudness. There are two threshold modes, one is auto threshold and the other is fixed threshold mode.

There are 8 threshold voltage levels in this IC as defined in the register 2Bh (THOLD[7:0]). Auto threshold mode means that the 8 threshold voltages will be scanned automatically from the lowest to highest threshold voltages at a fixed frequency higher than audio frequency. Input music signal will be compared with these scanning threshold voltages to control PWM Driver in order to have music synchronization effects. This mode allows user to easily use music synchronize function without having the trouble of manually setting the detection threshold. When melody mode is enabled, auto threshold mode will be the default mode.

Fixed threshold mode means that the threshold voltage is fixed at one threshold level. It can be set using register 2Bh (THOLD[7:0]). Input music signal will be compared with this fixed threshold voltage set by the user. During fixed threshold mode, do not set more than 1 register bit to logic "High" value at the same time. If user set more register bits to logic "High" after setting 1 register bit to "High", system will only recognise the first "High" bit threshold that is set. In this mode, user can have the flexibility to configure different threshold voltage levels to achieve the desired LED music synchronizing visual effect according to the system music input level.

It is also advised that AC music signal peak to peak voltage to be at least 0.35 V and not more than 2.8 V.
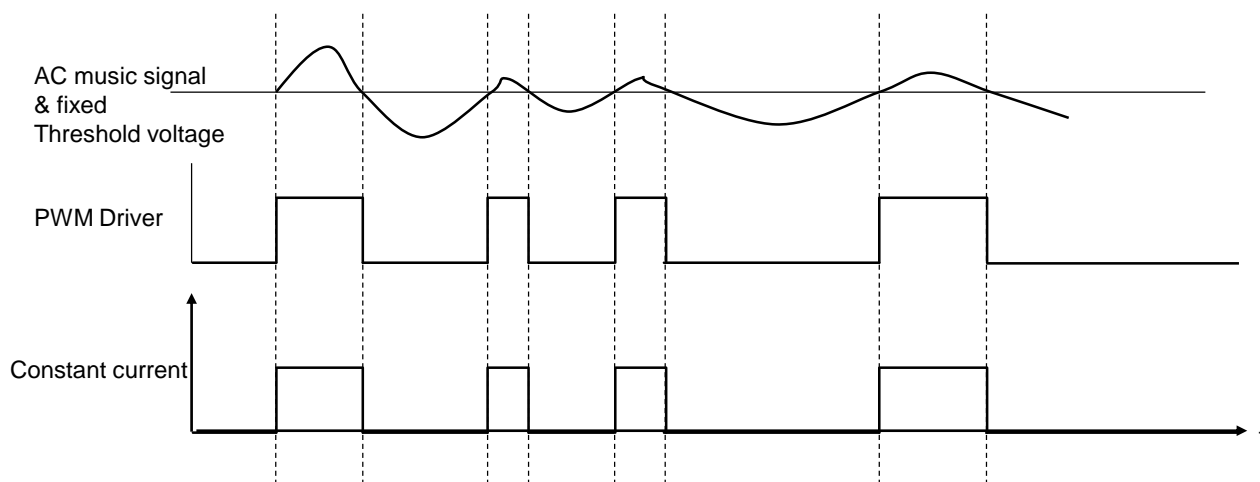


Example of Fixed threshold mode

- Brightness Compensation in Melody Mode

  Additional brightness compensation in melody mode can be achieved by increasing or decreasing the turning on period of LED.  Using brightness compensation register MLDCOM[2:0] (#33h), LED turning on period can be controlled and LED can become brighter or dimmer.

  This additional brightness compensation will be effective only in auto threshold mode. If fixed threshold mode is used, this register will not be able to control LED brightness.

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## OPERATION (Continued)

### 8. LED Driver Block Function (Continued)

#### 8.5 Bar Meter Mode Explanation

Bar Meter Mode operation is another method of external melody mode wherein a group of LEDs are used instead of individual LED. Bar Meter Mode has higher priority than individual LED melody mode.
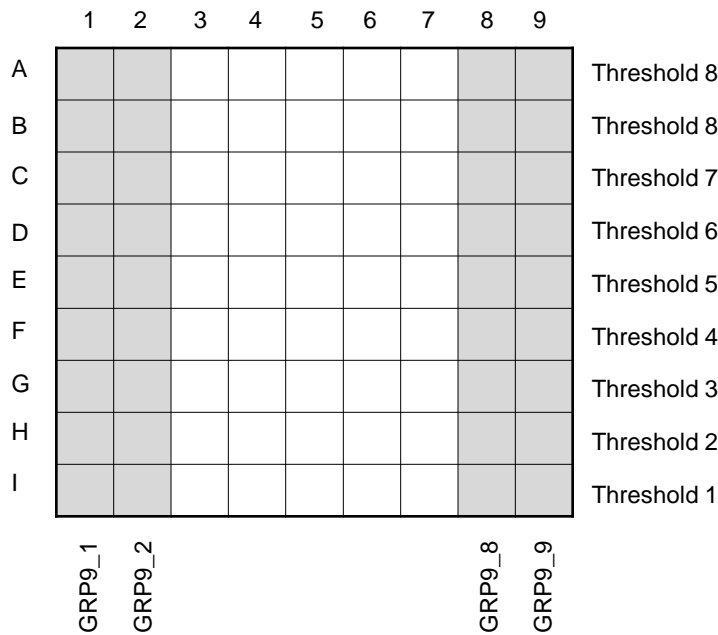


In the above diagram, column 1 = group1, column 2 = group2, column 8 = group8 and column 9 = group9. Each group can be enabled through register GRP9_1, 9_2, 9_8, 9_9 (address #2Ah). The LED in the all groups will be synchronized to threshold signals as follow:

| Threshold Signal | Bar Meter Mode Group LED ON |
|---|---|
| Threshold 1 | Row's                          I |
| Threshold 2 | Row's                       H, I |
| Threshold 3 | Row's                    G, H, I |
| Threshold 4 | Row's                 F, G, H, I |
| Threshold 5 | Row's              E, F, G, H, I |
| Threshold 6 | Row's           D, E, F, G, H, I |
| Threshold 7 | Row's        C, D, E, F, G, H, I |
| Threshold 8 | Row's  A, B, C, D, E, F, G, H, I |

All other LEDs not in Bar Meter Mode can operate in individual external melody mode or other modes.

During Bar Meter Mode, auto threshold detection should be used. This IC does not support Bar Meter Mode with fixed threshold setting. It is also recommended not to use other modes together with Bar Meter Mode of LED in group 1, 2, 8 & 9 (i.e. LED A to I1, 2, 8, 9)

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## OPERATION (Continued)

### 9. Ghost Image Prevention Function

Ghost images sometimes appear during LED matrix mode operation. Very dim light can appear in some LED even during OFF condition. This is called Ghost Image. In this IC, Ghost Image Prevention Function is included to reduce Ghost Image effect. Ghost Image Prevention Function can be enabled through register ZPDEN (register 04h).
• Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method.
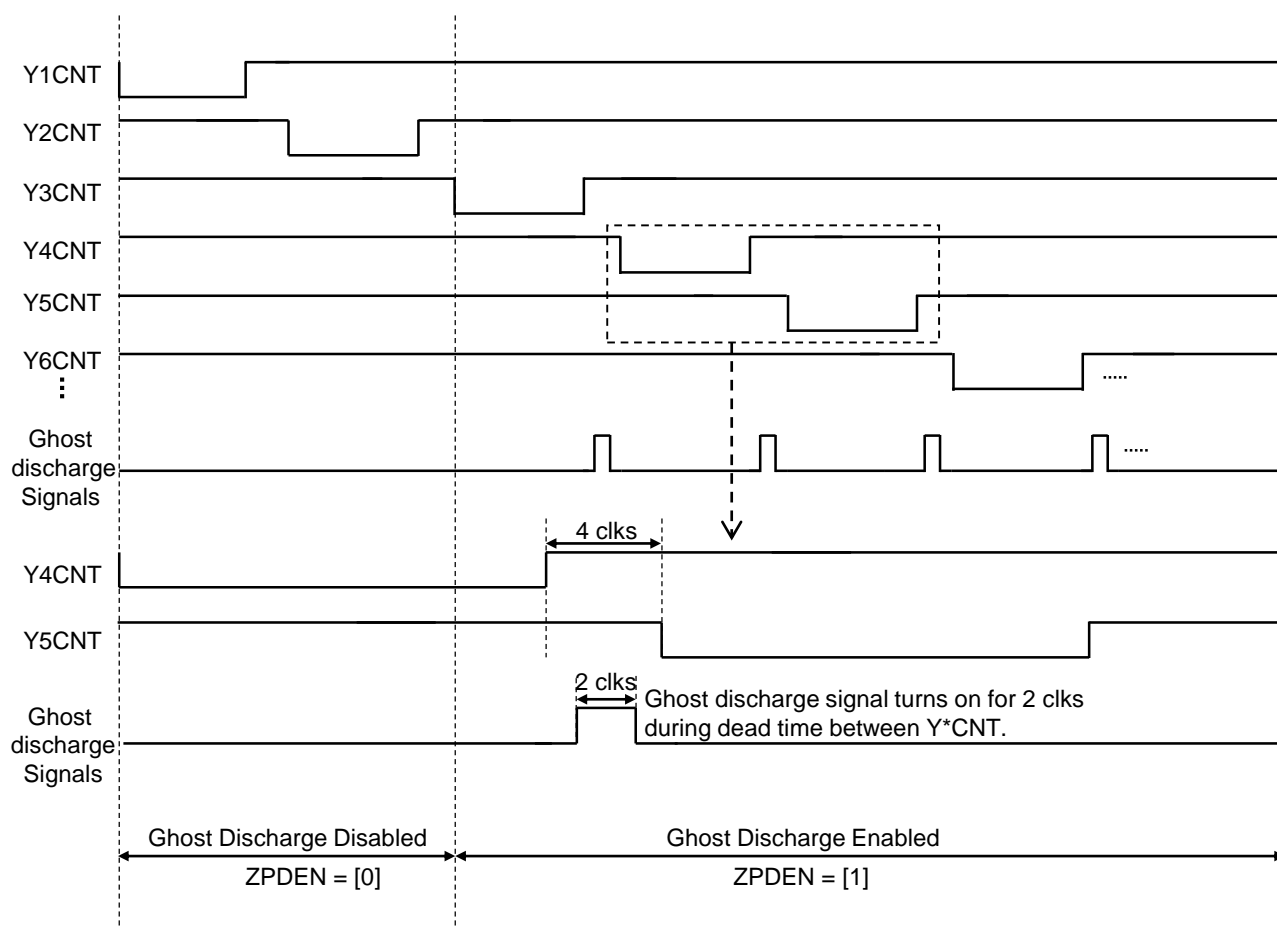


During normal operation, ghost discharge signal will be always low. When ghost image prevention function is enabled through register 04h, ghost discharge signal will turn on for 2 clks cycle during 4 clks dead time between each YCNT. During on period of 2 clks cycle, output Z pin will be forced to half of $V_{CC}$.

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## OPERATION (Continued)

### 9. Ghost Image Prevention Function (Continued)

To minimize ghost image, it is recommended to use LED with same forward voltage drop in LED panel. If user wants to use LED with different forward voltage drop in LED panel (e.g. RGB LED in LED panel), it is recommended that all the cathodes of LED connected to the same pin must have same forward voltage drop. (i.e. same colour LED sharing the same cathode). A recommended RGB LED connection to minimize ghost image is shown in diagram below.
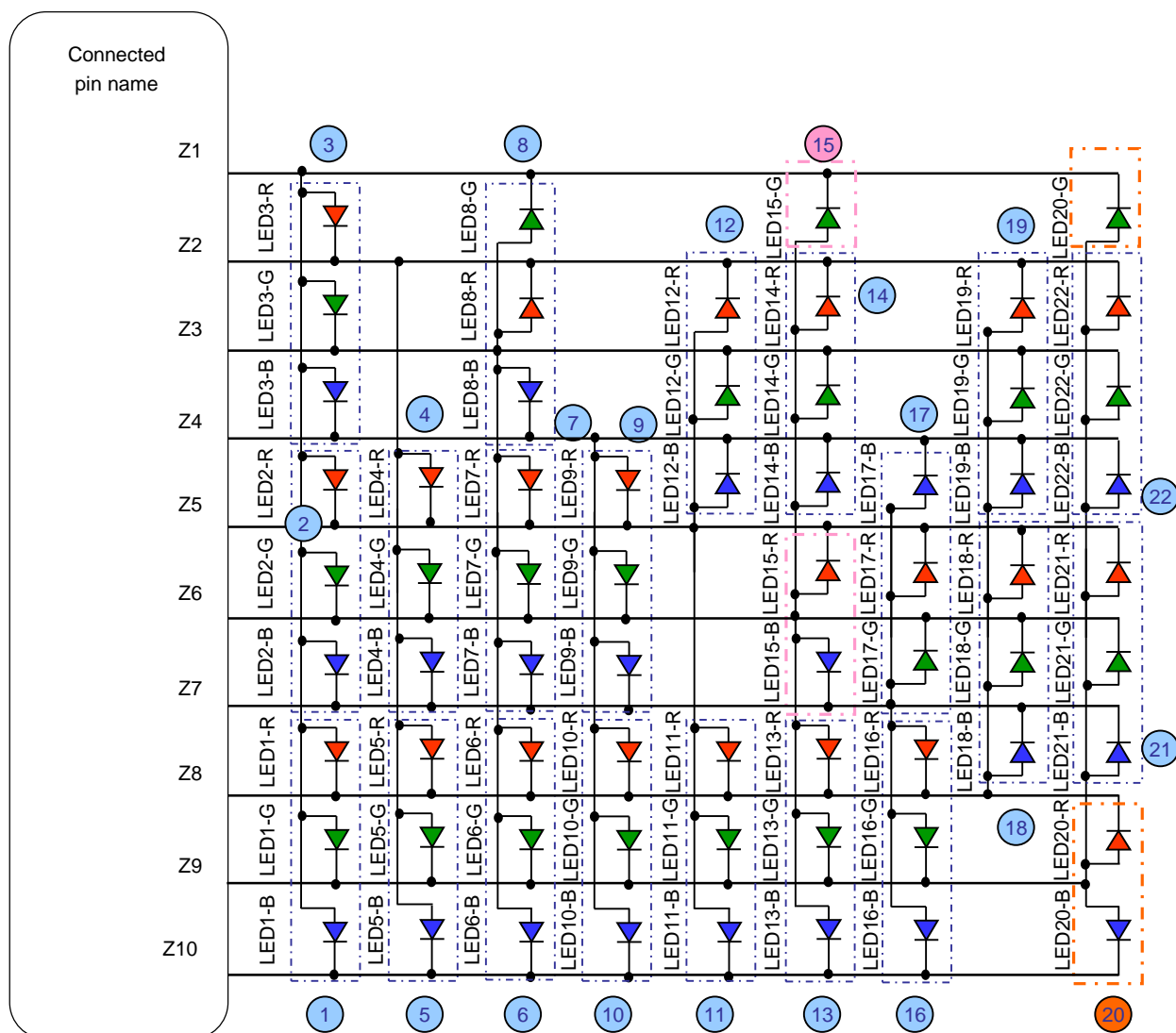


Example of RGB LED connection

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## PACKAGE INFORMATION (Reference Data)

**Unit:mm**

| Body Material  : | Br/Sb Free Epoxy resin |
|---|---|
| Lead Material  : | Cu Alloy |
| Lead Finish Method  : | SnBi Plating |

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## IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.

2. When the application system is designed by using this IC, please confirm the notes in this book.
Please read the notes to descriptions and the usage notes in the book.

3. This IC is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.

4. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.

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## USAGE NOTES

1. Pay attention to the direction of IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.

2. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

3. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.

4. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

5. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.

6. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

7. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.

8. Verify the risks which might be caused by the malfunctions of external components.

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- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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