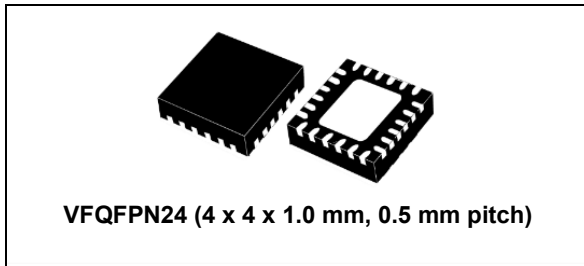


Miniature KNX transceiver with voltage regulators and microcontroller support

Datasheet - production data



Features

- Very thin fine pitch 4 x 4 mm VQFNPN24 package
- KNX certified, KNX TP1-256 supported
- Easy interface to μC
- Very small system solution
- Two integrated voltage regulators for external use in application
 - Selectable 3.3 V / 5 V - 20 mA linear regulator
 - Adjustable 1 V to 12 V - 150 mA high-efficiency DC/DC step down switching converter
- KNX bus power extractor supporting bus current up to 30 mA
- Adjustable KNX bus current slew rate dI/dt
- No crystal required
- Operating temperature range -40 °C to +85 °C

Applications

- KNX twisted pair network (KNX TP1-256)

Description

The STKNX is a transceiver device for KNX TP communication. The small package and few external components enable the very compact KNX nodes design.

The simple interface to the μC allows easy replacement of physical layer discrete components implementations.

The STKNX device features two integrated voltage regulators for external use in the application: the selectable 3.3 V / 5 V - 20 mA linear regulator and the adjustable 1 V to 12 V - 150 mA high-efficiency DC/DC step down switching converter.

The integrated KNX bus power extractor supports bus current up to 30 mA to power external devices and the STKNX transceiver's own power needs, while limiting the bus current slew rate according to KNX specifications.

The STKNX assures the safe coupling to the bus and provides the bus monitoring warning for the loss of bus power.

Table 1. Device summary

Order code	Package	Packaging
STKNX	VFQFPN24	Tray
STKNXTR	VFQFPN24	Tape and reel

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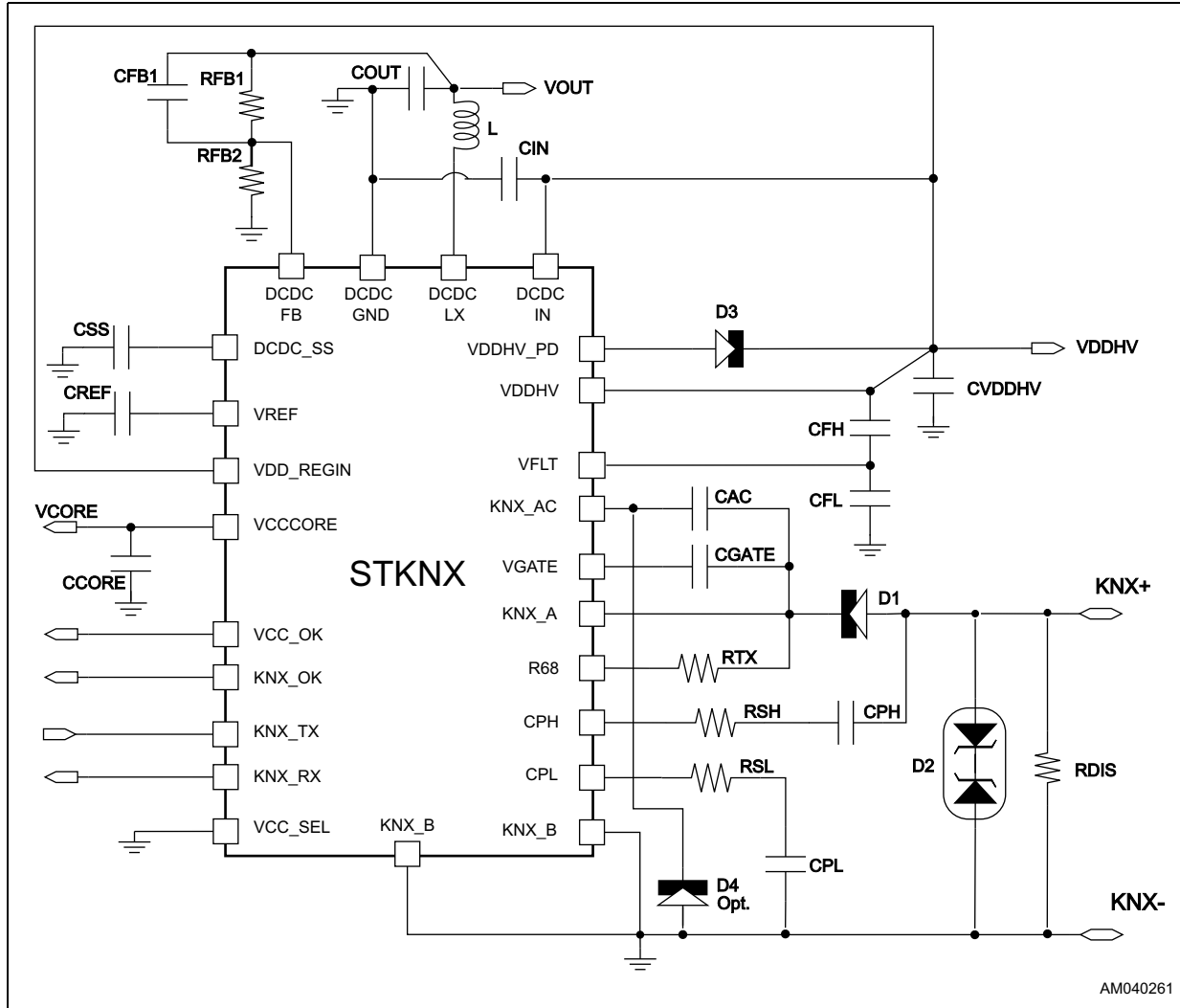
- 6 Package information 20**
 - 6.1 VFQFPN 4 x 4 x 1.0 24 pitch 0.5 package information 21

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1 Typical application circuit and block diagram

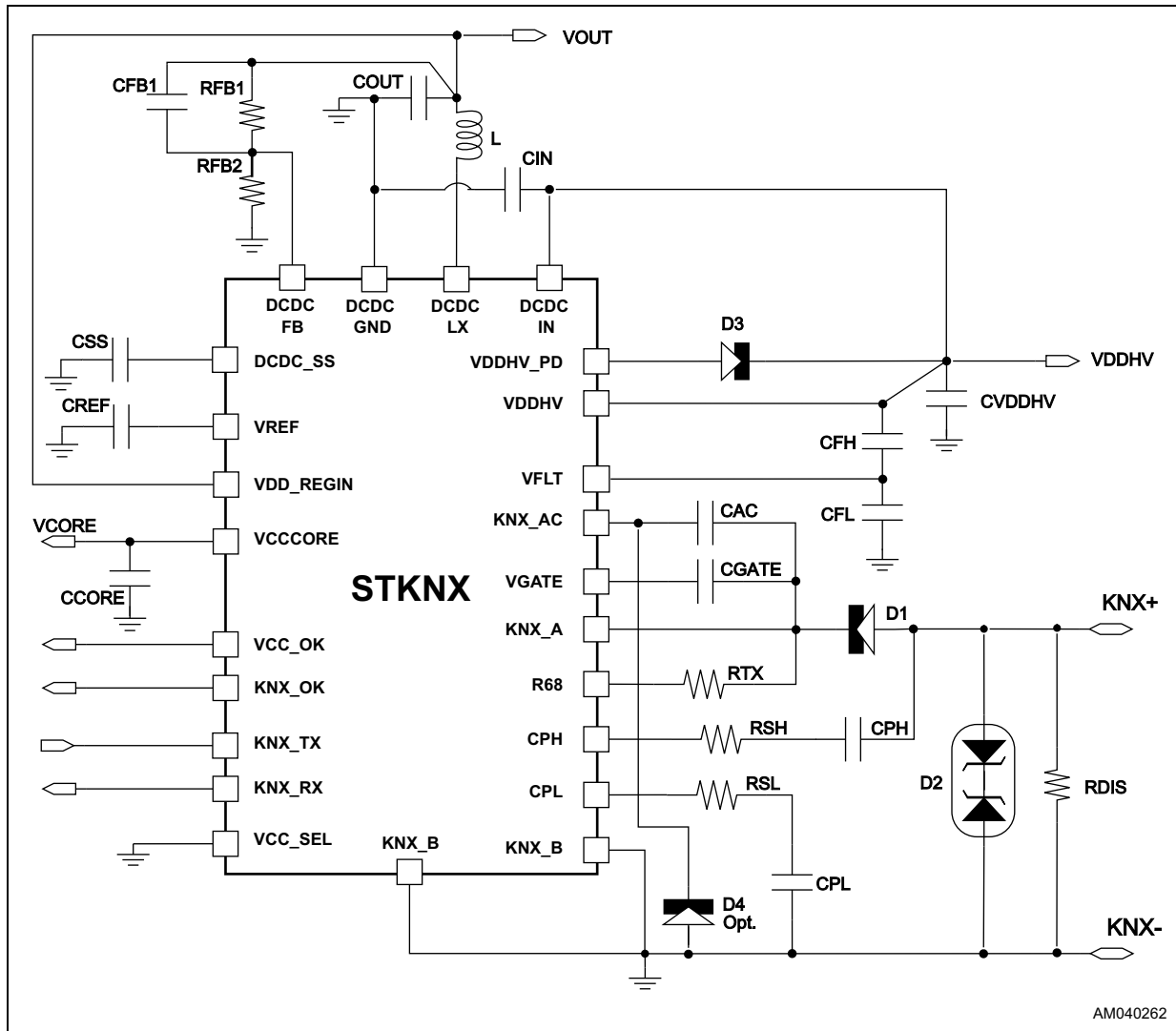
1.1 Typical application circuit

Figure 1. Typical application circuit, buck converter enabled, linear regulator supplied by impedance modulator



Note: *VOUT* range 1 V ÷ 12 V.
VCORE selectable to 3.3 V / 5 V through *VCC_SEL* (3.3 V in the example).

Figure 2. Typical application circuit, buck converter enabled, linear regulator supplied by buck converter

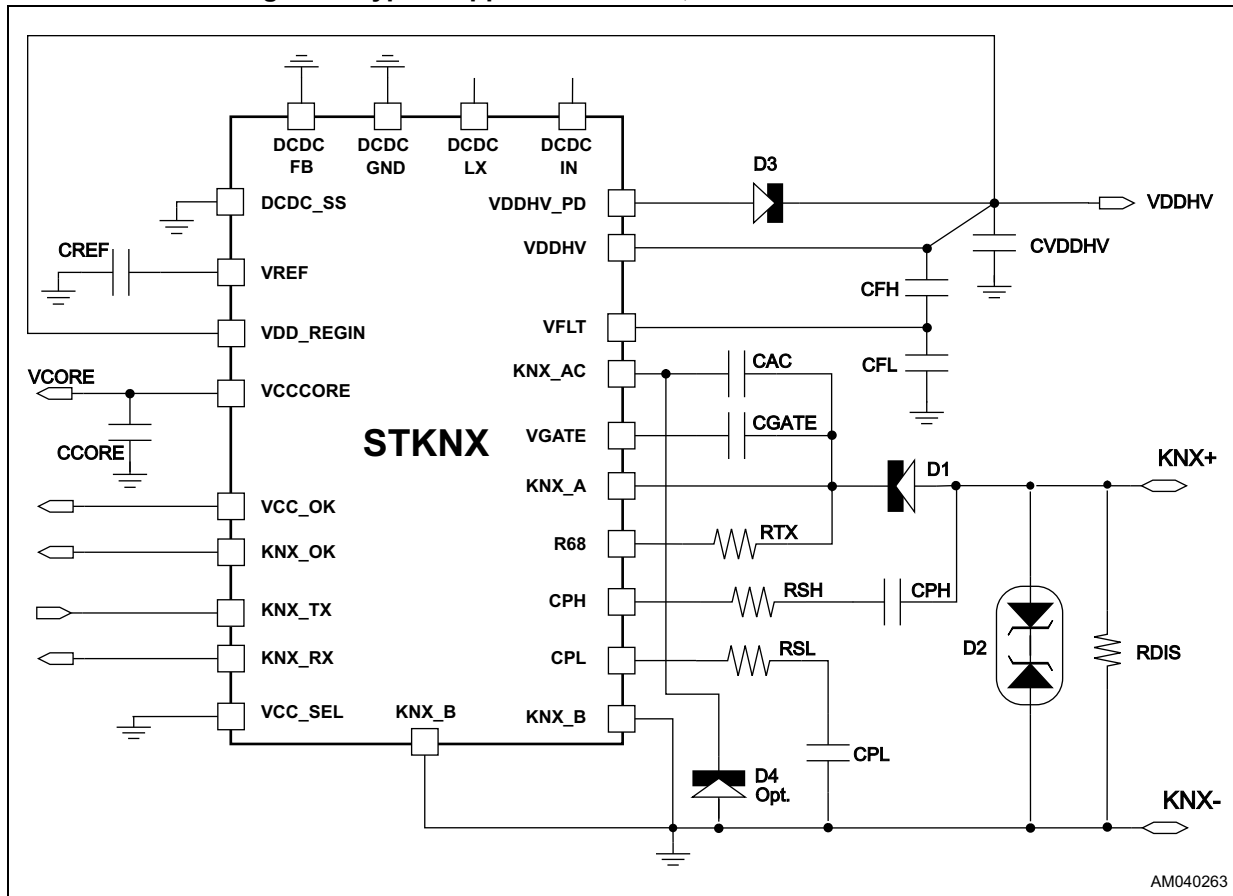


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Note: The VOUT level needs to be compliant with VDD_REGIN recommended operating conditions.

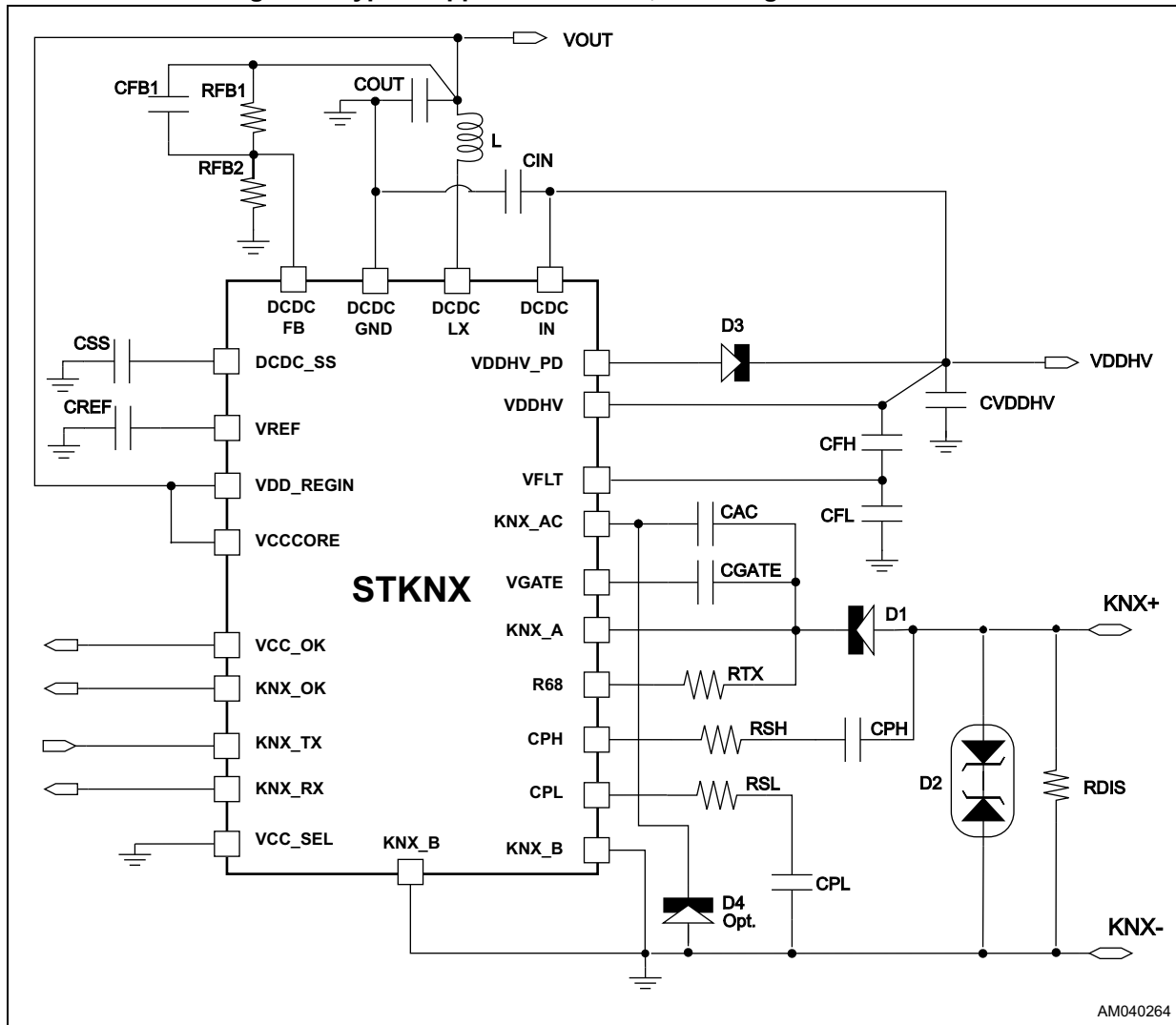
VCORE selectable to 3.3 V / 5 V through VCC_SEL (3.3 V in the example).

Figure 3. Typical application circuit, buck converter disabled



Note: VCORE selectable to 3.3 V / 5 V through VCC_SEL (3.3 V in the example).

Figure 4. Typical application circuit, linear regulator disabled



Note: The VOUT level needs to be compliant with VCCCORE recommended operating conditions. VCC_SEL needs to be set according to the VCCCORE level (3.3 V in the example).

Table 2. External components typical value

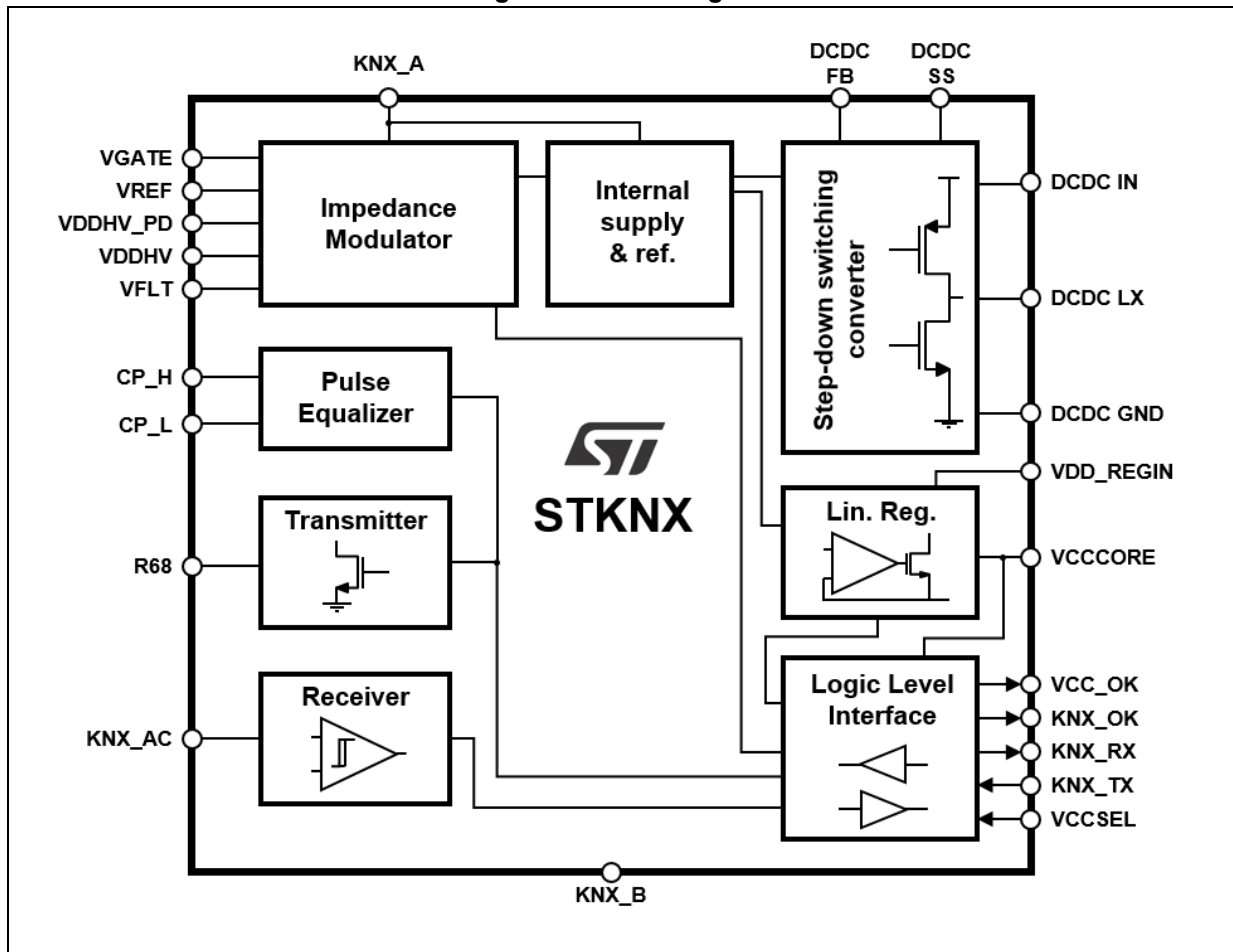
Reference	Type	Typ. value	Rating	Description
Capacitors				
CPH	MLCC	100 nF	$V_{RATED} \geq 50 \text{ V}$	Equalizer storage capacitor
CPL	MLCC	100 nF	$V_{RATED} \geq 50 \text{ V}$	Equalizer storage capacitor
CGATE	MLCC or electrolytic	$10 \mu\text{F} \div 47 \mu\text{F}$	$V_{RATED} \geq 10 \text{ V}$	Impedance modulator storage capacitor - see Table 8 on page 18
CAC	MLCC	10 nF	$V_{RATED} \geq 50 \text{ V}$	Bus AC coupling capacitor
CVDDHV	Electrolytic	$\geq 100 \mu\text{F}$	$V_{RATED} \geq 35 \text{ V}$	Impedance modulator output bulk capacitor - see Table 8 on page 18
CFH	MLCC	47 nF	$V_{RATED} \geq 35 \text{ V}$	Impedance modulator compensation capacitor
CFL	MLCC	47 nF	$V_{RATED} \geq 35 \text{ V}$	Impedance modulator compensation capacitor
CIN	MLCC	10 μF	$V_{RATED} \geq 35 \text{ V}$	Buck converter input decoupling capacitor
COUT	MLCC	22 μF	$V_{RATED} > V_{OUT}$	Buck converter output capacitor
CSS	MLCC	10 nF \div 470 nF	$V_{RATED} \geq 6.3 \text{ V}$	Buck converter soft-start time programming capacitor - see Equation 3 on page 19
CREF	MLCC	470 nF	$V_{RATED} \geq 35 \text{ V}$	VREF decoupling capacitor
CCORE	MLCC	4.7 μF	$V_{RATED} \geq 6.3 \text{ V}$	Linear regulator output capacitor
CFB1	MLCC	$1/(2\pi * R_{FB1} * 28 \text{ kHz})$, NM if $R_{FB1} = 0 \Omega$	$V_{RATED} \geq 16 \text{ V}$	Buck converter compensation capacitor
Resistors				
RDIS	Resistor	4.7 M Ω	-	Reverse polarity discharging resistor
RSH	Resistor	1 k Ω	-	Series resistor to CPH
RSL	Resistor	1 k Ω	-	Series resistor to CPL
RTX	Resistor	68 Ω	$P_{DISS} \geq 1 \text{ W}$	Tx current limiting resistor
RFB1	Resistor	$(V_{OUT} / 1 \text{ V} - 1) * R_{FB2}$, 0 Ω for $V_{OUT} = 1 \text{ V}$	-	Buck converter output voltage adjusting resistor
RFB2	Resistor	10 k Ω typ. (< 100 k Ω), NM for $V_{OUT} = 1 \text{ V}$	-	Buck converter output voltage adjusting resistor
Inductors				
L	Power inductor	33 μH	$I_R > 150 \text{ mA}$, $I_{SAT} > 550 \text{ mA}$	Buck converter output inductor
Diodes				
D1	Diode	LL4148 or equivalent	$V_{BR} > 50 \text{ V}$, $V_F (50 \text{ mA}) < 1 \text{ V}$	Input diode (protection from reverse polarity connection)
D2	TVS	SMAJ40CA or equivalent	-	Transient voltage suppressor diode

Table 2. External components typical value (continued)

Reference	Type	Typ. value	Rating	Description
D3	Diode	LL4148 or equivalent	$V_{BR} > 50\text{ V}$, $V_F(50\text{ mA}) < 1\text{ V}$	Output diode
D4	Diode	LL4148 or equivalent	$V_{BR} > 50\text{ V}$, $V_F(50\text{ mA}) < 1\text{ V}$	Optional KNX_AC clamping diode. Recommended for noise immunity improvement in noisy environment.

1.2 Block diagram

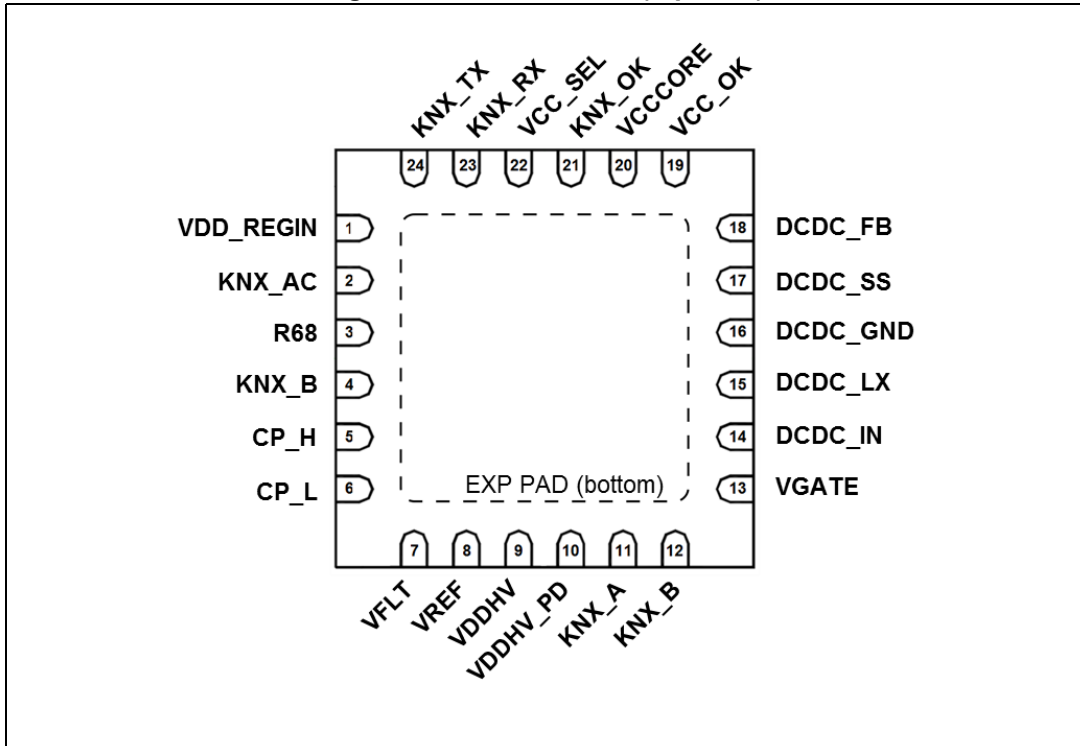
Figure 5. Block diagram



2 Pin connection and pin description

2.1 Pin connection

Figure 6. Pin connection (top view)



2.2 Pin description

Table 3. Pin description

Pin	Pin name	Function
1	VDD_REGIN	Linear regulator supply input. Short to VCCCORE to disable the linear regulator and supply VCCCORE externally.
2	KNX_AC	BUS AC-coupled sense for the Rx input and Tx feedback. DC biased to 9.7 V typ.
3	R68	KNX transmitter output
4	KNX_B	Analog ground
5	CP_H	Equalization cap connection to KNX supply (KNX+)
6	CP_L	Equalization cap connection to KNX ground (KNX-)
7	VFLT	Impedance modulator compensation
8	VREF	Impedance modulator reference
9	VDDHV	VDDHV supply input and impedance modulator feedback
10	VDDHV_PD	Impedance modulator power output
11	KNX_A	KNX power supply input (KNX+)
12	KNX_B	Analog ground
13	VGATE	Impedance modulator storage capacitor connection
14	DCDC_IN	Step down converter supply input. Short to ground or leave floating to disable the switching converter.
15	DCDC_LX	Step down converter switching output
16	DCDC_GND	Step down converter power ground
17	DCDC_SS	Step down converter soft-start programming pin
18	DCDC_FB	Step down converter feedback input. Sets output voltage (1 V ÷ 12 V range) through the resistor divider.
19	VCC_OK	VCCCORE power good CMOS digital output
20	VCCCORE	Linear regulator output (3.3 V / 5 V selectable). Supply voltage for digital I/O.
21	KNX_OK	KNX bus power good CMOS digital output
22	VCC_SEL	Selects linear regulator output voltage. Internally pulled-down (6 μ A typ.). Tie to VCCCORE to select 5 V. Short to ground or leave floating to select 3.3 V.
23	KNX_RX	Receiver CMOS digital output
24	KNX_TX	Transmitter digital input. Internally pulled-down (6 μ A typ.).
-	Exposed pad	Connect to analog ground. For thermal optimization, maximize the area of the ground layer on which the exposed pad is soldered and provide good thermal connection with the bottom ground layer through vias.

3 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Test condition	Value	Unit
T_J	Maximum operating junction temperature	-	110	°C
T_{AMB}	Operating ambient temperature	-	-40 to 85	°C
T_{STG}	Storage temperature	-	-50 to 150	°C
R_{thJA}	Thermal resistance junction to ambient, steady state	Mounted on a 2s2p PCB, with a dissipating surface connected through vias on the bottom side of the PCB.	35	°C/W

4 Electrical specifications

4.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
KNX_A	KNX supply input	-0.3	45	V
VDD_REGIN	Linear regulator supply input	-0.3	40	V
VDDHV	VDDHV supply input and impedance modulator feedback	-0.3	40	V
VREF	Impedance modulator reference	-0.3	40	V
KNX_B, DCDC_GND	Variation between different ground pins	-0.3	0.3	V
CP_H	Equalizing cap. high	-0.3	KNX_A + 0.3	V
CP_L	Equalizing cap. low	-0.3	KNX_A + 0.3	V
R68	KNX transmitter output	-0.3	KNX_A + 0.3	V
KNX_AC	BUS AC-coupled sense	-0.3	KNX_A + 0.3	V
VDDHV_PD	Impedance modulator power output	-0.3	KNX_A + 0.3	V
VGATE	Impedance modulator coupling cap.	Max. (-0.3, KNX_A - 7.2)	KNX_A + 0.3	V
VCCCORE	Linear reg. output. I/O supply.	-0.3	5.5	V
KNX_TX	Transmitter digital input	-0.3	Min. (5.5, VCCCORE + 0.3)	V
KNX_RX	Transmitter digital output	-0.3	Min. (5.5, VCCCORE + 0.3)	V
KNX_OK	KNX bus power good	-0.3	Min. (5.5, VCCCORE + 0.3)	V
VCC_SEL	3.3 V / 5 V selection for linear reg.	-0.3	Min. (5.5, VCCCORE + 0.3)	V
VCC_OK	VCCCORE power good	-0.3	Min. (5.5, VCCCORE + 0.3)	V
VFLT	Impedance modulator compensation	-0.3	5.5	V
DCDC_IN	Step down converter input	-0.3	40	V
DCDC_LX	Step down converter switching node	-0.3	Min. (40, DCDC_IN + 0.3)	V
DCDC_FB	Step down converter feedback	-0.3	3.6	V
DCDC_SS	Step down converter soft-start programming pin	-0.3	3.6	V

4.2 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Max.	Unit
KNX_A	KNX supply input ⁽¹⁾	-	20	32	V
VCCCORE	I/O supply and linear reg. output	-	3	5.5	V
DCDC_IN	Step down converter input	-	13	32	V
VDD_REGIN	Linear regulator supply input ⁽²⁾	VCC_SEL shorted to GND	6.8	32	V
		VCC_SEL shorted to VCCCORE	8.5	32	V
I _{VDDHV_PD}	Continuous output current from VDDHV pin ⁽³⁾	-	-	30	mA
I _{REG}	Continuous output current from VCCCORE pin ⁽³⁾	-	-	20	mA
I _{DCDC}	Continuous output current from DCDC switching converter ⁽³⁾	-	-	150	mA

1. Indicates DC value. With the active and equalization pulse bus voltage must be between 11 V and 45 V.
2. Short VDD_REGIN to VCCCORE to disable the internal linear regulator and provide VCCCORE voltage externally.
3. The maximum current capability refers to the voltage regulator only. The usable current capability can be limited by the KNX bus current consumption specification.

4.3 Electrical characteristics

Parameters given for a device operating within the recommended operating conditions, unless otherwise specified. Typical values are referred to T_J = 27 °C.

Table 7. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
V(KNX_A)	DC supply voltage on KNX_A pin	Excluding active and equalization pulse	20	-	32	V
I(KNX_A)	Bus current consumption, no load	V(KNX_A) = 32 V, no activity on bus, no transmission, no external load	-	1	-	mA
	Bus current consumption, 30 mA load	V(KNX_A) = 32 V, no activity on bus, no transmission, 30 mA load on VDDHV rail (including linear regulator and switching converter)	-	31	-	mA
KNX_OK _{RIS} (VREF)	KNX_OK rising threshold referred to VREF voltage	VREF rising	-	-	13.5	V
KNX_OK _{FALL} (VREF)	KNX_OK falling threshold referred to VREF voltage	VREF falling	9.7	-	-	V

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
KNX_OK _{HYST} (VREF)	KNX_OK hysteresis referred to VREF voltage	-	-	1.4	-	V
KNX_OK _{RIS} (KNX_A)	KNX_OK rising threshold referred to KNX_A DC voltage	KNX_A rising slowly, VREF settled	-	-	18.5	V
Impedance modulator						
VDDHV drop	V(KNX_A) - V(VDDHV) voltage drop	V(KNX_A) = 20 V DC, I _{LOAD} = 5 mA, D3 = LL4148 or equivalent	-	-	6.5	V
VDDHV drop	V(KNX_A) - V(VDDHV) voltage drop	V(KNX_A) = 20 V DC, I _{LOAD} = 30 mA, D3 = LL4148 or equivalent	-	-	7.2	V
VREF drop	V(KNX_A) - V(REF) voltage drop	V(KNX_A) = 20 V DC, VREF settled	3	4.3	5	V
VCCCORE voltage and linear regulator						
VCCCORE	Regulated voltage	VCC_SEL shorted to GND	3	3.3	3.6	V
		VCC_SEL shorted to VCCCORE	4.5	5	5.5	V
VCC_OK _{RIS}	VCC_OK rising threshold	VCC_SEL shorted to GND	2.3	-	2.8	V
		VCC_SEL shorted to VCCCORE	3.3	-	4	V
VCC_OK _{FALL}	VCC_OK falling threshold	VCC_SEL shorted to GND	2.0	-	2.5	V
		VCC_SEL shorted to VCCCORE	2.9	-	3.6	V
VCC_OK _{HYST}	VCC_OK hysteresis	VCC_SEL shorted to GND	-	0.3	-	V
		VCC_SEL shorted to VCCCORE	-	0.4	-	V
I _{VCCSEL}	VCCSEL internal pull-down current	-	-	6	-	μA
Programmable DC-DC switching converter						
V _{IN}	Input voltage at DCDC_IN pin	-	13	-	32	V
V _{OUT}	Output voltage adjusting range	-	1	-	12	V
V _{FB}	Feedback voltage reference	-	0.9	1	1.1	V
UVLO _{RIS}	Undervoltage lockout rising threshold on VIN voltage	V _{IN} rising	9	10	11	V
UVLO _{FALL}	Undervoltage lockout falling threshold on VIN voltage	V _{IN} falling	5.4	6	6.6	V
UVLO _{HYST}	Undervoltage lockout hysteresis on VIN voltage	-	-	4	-	V

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{LIM}	High side MOSFET current limit	-	325	650	975	mA
V_{OUT_RIP}	Output voltage ripple	13 V < V_{IN} < 32 V, 3.3 V < V_{OUT} < 12 V $I_{OUT} = 5 \text{ mA} \sim 150 \text{ mA}$, $C_{OUT} = 22 \mu\text{F MLCC}^{(1)}$	-	50	-	mV
$R_{DS(ON)}$	High side MOSFET on resistance	-	-	1.9	-	Ω
	Low side MOSFET on resistance	-	-	1.2	-	
OTP	Overtemperature protection	Junction temperature ⁽²⁾	110	140	-	$^{\circ}\text{C}$
OVP_{RIS}	Overvoltage protection rising threshold on FB	FB voltage rising	1.1	1.25	1.4	V
OVP_{FALL}	Overvoltage protection falling threshold on FB	FB voltage falling	0.95	1.1	1.25	V
I_{SS}	Current sourced from SS pin	During soft-start	-	2.5	-	μA
Transmitter						
$R_{DS(ON)}$	Tx MOSFET on resistance	-	-	5	-	Ω
I_{KNX_TX}	KNX_TX internal pull-down current	-	-	6	-	μA
Digital I/Os						
V_{IL}	Maximum voltage level that will be interpreted as a logic 0	$V_{CCCORE} = 3.3 \text{ V}$	0.7	-	-	V
		$V_{CCCORE} = 5 \text{ V}$	1.2	-	-	
V_{IH}	Minimum voltage level that will be interpreted as a logic 1	$V_{CCCORE} = 3.3 \text{ V}$	-	-	2.2	V
		$V_{CCCORE} = 5 \text{ V}$	-	-	3	
V_{OL}	Logic low output level	$V_{CCCORE} = 3.3 \text{ V}$, $I_{SUNK} = 300 \mu\text{A}$	0	-	0.4	V
		$V_{CCCORE} = 5 \text{ V}$, $I_{SUNK} = 400 \mu\text{A}$	0	-	0.4	V
V_{OH}	Logic high output level	$V_{CCCORE} = 3.3 \text{ V}$, $I_{SOURCED} = 300 \mu\text{A}$	$V_{CCCORE} - 0.5$	-	V_{CCCORE}	V
		$V_{CCCORE} = 5 \text{ V}$, $I_{SOURCED} = 400 \mu\text{A}$	$V_{CCCORE} - 0.5$	-	V_{CCCORE}	V

1. Not tested in production. Guaranteed by design.

2. Not tested in production. Based on characterization.

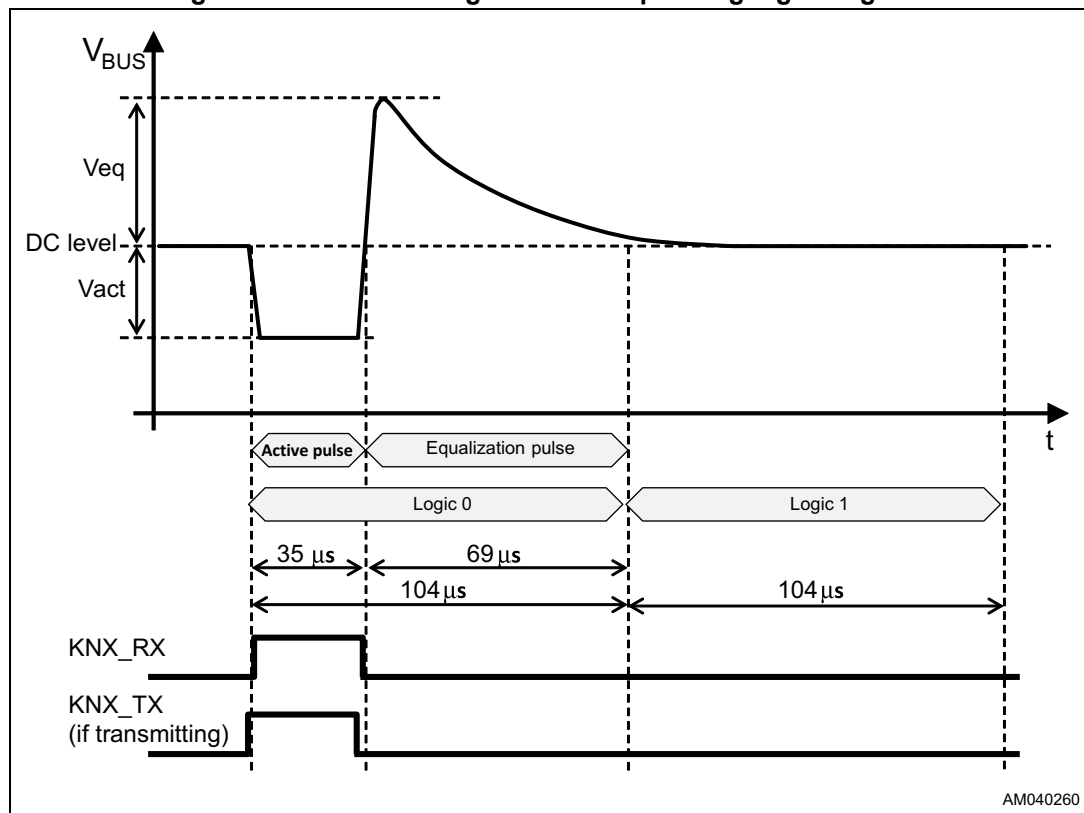
5 Device description

The STKNX is a transceiver device for twisted pair communication, following the KNX twisted pair standard (KNX TP1-256). Detailed information on the KNX bus can be found in the KNX standards and on the KNX website (www.knx.org).

The STKNX is composed of two main functional blocks: the bus interface and the voltage regulators.

- The bus interface consists of the transmitter, receiver and impedance modulator
- The voltage regulators block consists of an adjustable output voltage step down switching converter with integrated power MOSFETs and a 3.3 V / 5 V programmable linear regulator

Figure 7. KNX bus voltage and corresponding digital signals



5.1 Bus interface

The bus interface connects the STKNX to the KNX bus for transmitting, receiving and extracting power.

Through the bus interface, the STKNX supports

- Interfacing a microcontroller with the KNX bus, translating signals between the logic level domain and KNX bus domain
- Extracting power from the bus to supply the STKNX itself, the microcontroller and application devices

The KNX standard specifies a bit period of 104 μs . It defines the logic 1 as the idle state of the bus (DC voltage level between 21 V and 32 V), the logic 0 (also called active pulse) as a voltage drop of the bus.

The active pulse is generated by the transmitter. Ideally, the drop has a rectangular shape, a depth between 6 V and 9 V and a duration of 35 μs . Each active pulse is followed by an equalization phase of 69 μs typical duration, which consists in an overshoot of the bus voltage above the DC level, followed by an exponential decay.

See the KNX Twisted Pair Standard (KNX TP1-256) for more detailed information.

5.1.1 Transmitter

The transmitter converts logic level signals received at the KNX_TX pin to analog signals on the KNX bus. To transmit a logic 1 (equivalent to transmitter in idle state), the KNX_TX pin has to be kept low for 104 μs . To transmit a logic 0, the KNX_TX has to be forced high for 35 μs (active pulse) and then low for 69 μs .

During the active pulse, the transmitter forces a voltage drop of 7.5 V typ. on the KNX bus, by sinking current through the R68 pin.

5.1.2 Receiver

The receiver detects the beginning and the end of the active pulse and provides a logic level output on the KNX_RX pin. The KNX_RX pin is high during the active pulse, low during the equalization phase and idle state.

The detection threshold for the start of the active pulse is 0.6 V typ. below the bus DC voltage.

5.1.3 Impedance modulator

The KNX standard allows a bus voltage ranging from 21 V to 32 V (DC component). The bus provides supply for the STKNX and is the communication medium. During transmission, a -10.5 V / +13 V AC component can be superimposed to the DC component mentioned above.

Moreover, the KNX standard specifies that each module connected to the bus has to show a controlled impedance and to limit the bus load current slope di/dt , while not transmitting.

The impedance modulator purpose is to extract power from the KNX bus in order to supply STKNX integrated voltage converters and the application on the KNX module, while ensuring compliance to KNX impedance specifications.

In particular, impedance modulator

- Extracts a stable power rail (VDDHV) from the KNX bus DC level
- Smooths any load change applied at its output, limiting di/dt on the bus current
- Controls the impedance of the bus device during the active pulse and the equalization pulse according to KNX standard requirements

Since the current drawn from the bus must change very slowly, abrupt load current steps from the load applied to the STKNX have to be absorbed by the large filter capacitor on VDDHV rail (CVDDHV on [Figure 1 on page 3](#)), which should be sized accordingly.

The bus current slope limit is controlled through CGATE ([Figure 1](#)).

CGATE = 47 μ F sets a slope lower than 0.5 mA/ms, compliant to the KNX requirement for fan in model up to the 10 mA bus load.

For a higher fan in, it can be useful to set a higher current slope limit, in order to manage wider load changes minimizing the CVDDHV value. That can be done by reducing the CGATE value proportionally to the desired slope limit increase.

[Table 8](#) shows recommended CGATE and CVDDHV values for the minimum and maximum fan in.

Table 8. Recommended CGATE and CVDDHV vs. fan-in

Fan in	Recommended CGATE	Recommended minimum CVDDHV
10 mA	47 μ F	100 μ F
30 mA	10 μ F ÷ 47 μ F	220 μ F

5.2 Voltage regulators

The STKNX features two integrated voltage regulators for external use in the application: a linear regulator with 3.3 V or 5 V selectable output voltage, 20 mA current capability, and a step down switching converter with 1 V ÷ 12 V adjustable output voltage, 150 mA current capability.

5.2.1 3.3 V / 5 V linear regulator

The linear regulator converts the input voltage on the VDD_REGIN pin to 3.3 V or 5 V output on the VCCCORE pin. The output voltage level is selectable by the VCCSEL pin.

- VCCSEL tied to GND → VCCCORE = 3.3 V
- VCCSEL tied to VCCCORE → VCCCORE = 5 V

VCCSEL should not be changed when STKNX is operational.

The output current capability is 20 mA. A 4.7 μ F capacitor or higher is required between VCCCORE and KNX_B for stability.

VCCCORE is also the supply input for STKNX digital I/Os. The linear regulator can be disabled by shorting VCCCORE to VDD_REGIN; in that case VCCCORE voltage to supply I/Os has to be provided externally and VCCSEL has to be configured according to the voltage level (3.3 V or 5 V).

5.2.2 Buck converter

The STKNX integrates a high-efficiency low-consumption buck switching converter.

The switching converter is supplied from the DCDC_IN pin, connected to VDDHV rail in the typical application. When voltage at the DCDC_IN pin is lower than UVLO, the switching converter is disabled.

Buck converter output voltage is adjustable between 1 V and 12 V by means of an external resistor divider on the DCDC_FB pin, according to the following expression:

Equation 1

$$V_{out} = 1 \text{ V} \cdot (1 + R_{FB1} / R_{FB2})$$

where R_{FB1} and R_{FB2} are the upper and lower resistor of the divider respectively (see [Figure 1 on page 3](#)). The R_{FB2} typical value is 10 k Ω (R_{FB2} values higher than 100 k Ω should be avoided).

To set $V_{OUT} = 1 \text{ V}$, R_{FB1} should be 0 Ω and R_{FB2} not mounted.

In the usual case of the low ESR ceramic capacitor as the output capacitor for the converter, it is recommended to add an external feedforward compensation capacitor CFB1 in parallel to R_{FB1} , for $V_{OUT} > 1 \text{ V}$.

The CFB1 default value can be calculated according to the following expression:

Equation 2

$$CFB1 = 1 / (2\pi \cdot R_{FB1} \cdot 28 \text{ kHz})$$

The buck converter can deliver a continuous output current up to 150 mA, however the maximum current capability will not always be usable. In fact, at the application level, the KNX bus current consumption must stay within the KNX specification.

The buck converter implements the soft-start to prevent a high inrush current at the start-up. Soft-start time T_{SS} is programmable through the external capacitor C_{SS} between the DCDC_SS pin and GND, according to the following expression:

Equation 3

$$T_{SS} = 1 \text{ V} \cdot C_{SS} / I_{SS}$$

where I_{SS} is 2.5 μA typ.

The buck converter features a full set of protections, which includes overtemperature protection (OTP), overcurrent protection (OCP) and overvoltage protection (OVP).

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

6.1 VFQFPN 4 x 4 x 1.0 24 pitch 0.5 package information

Figure 8. VFQFPN 4 x 4 x 1.0 24 pitch 0.5 package outline

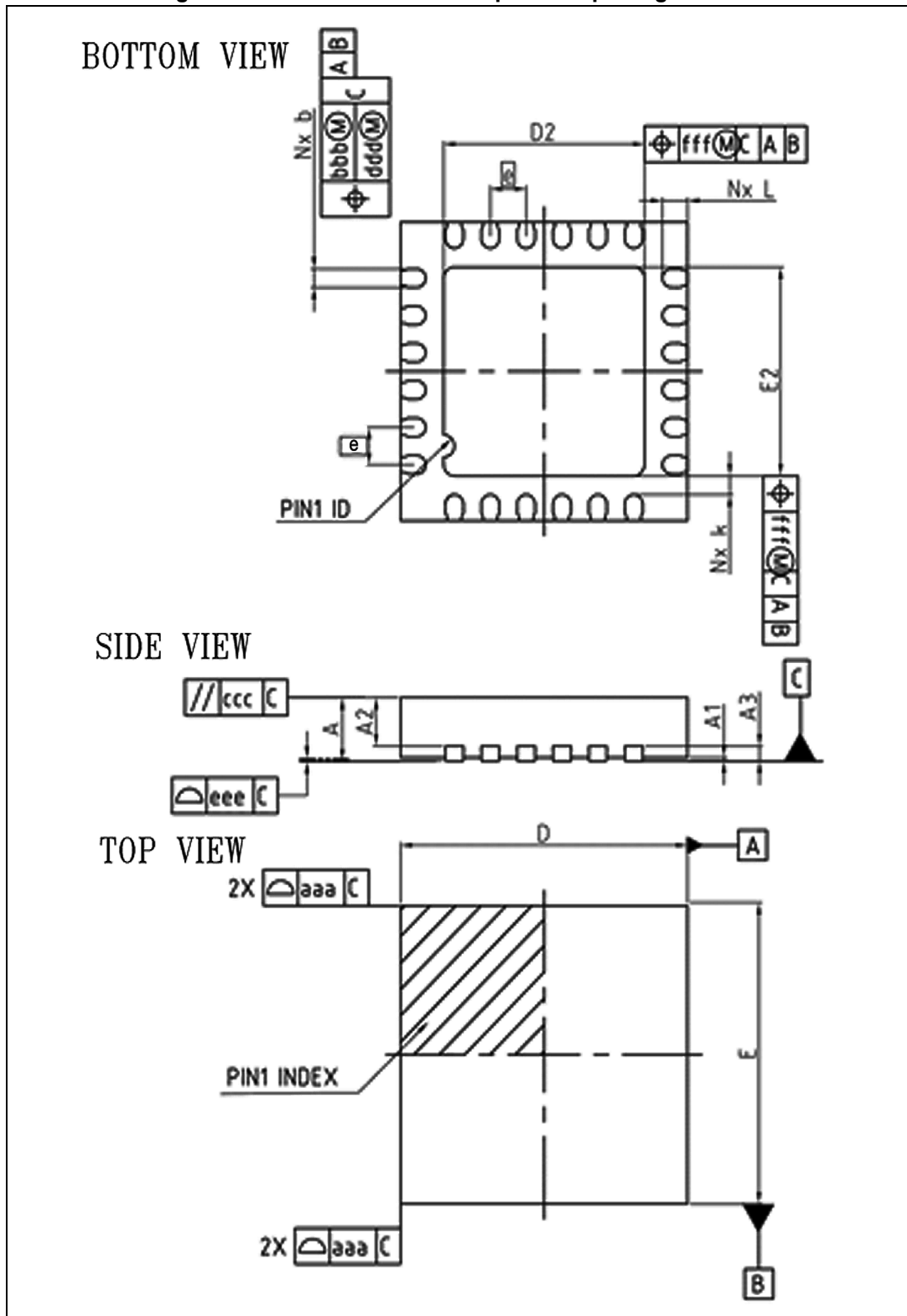
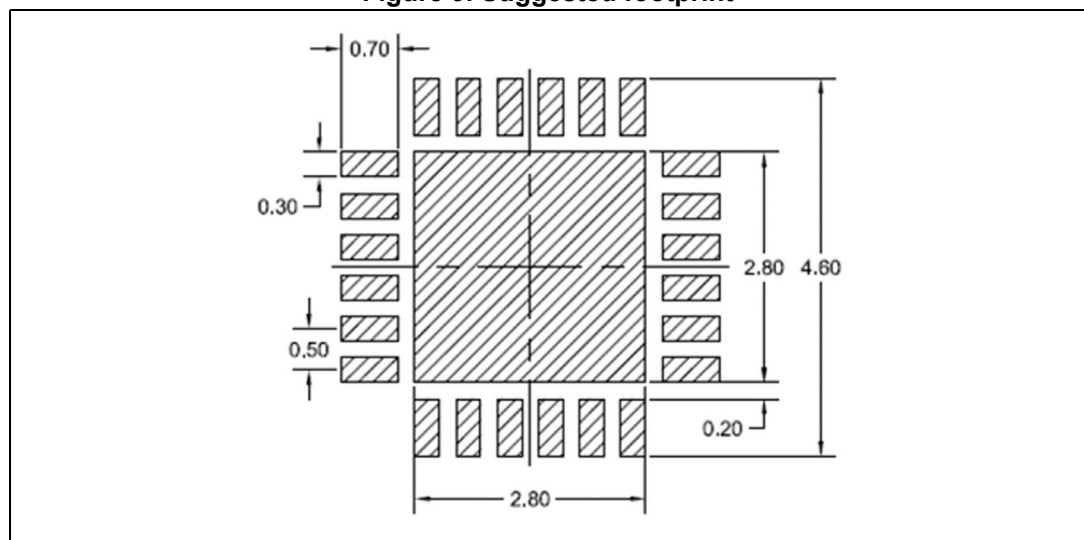


Table 9. VFQFPN 4 x 4 x 1.0 24 pitch 0.5 package mechanical data

Symbol	Dimensions [mm]		
	Min.	Nom.	Max.
A	0.80	-	1.00
A1	0.00	-	0.05
A2	-	0.65	-
A3	-	0.20	-
b	0.20	0.25	0.30
D	3.9	4.0	4.1
D2	2.7	2.8	2.9
e	-	0.5	-
E	3.9	4.0	4.1
E2	2.7	2.8	2.9
L	0.30	0.35	0.40
k	0.20	-	-
N	-	24	-
Symbol	Tolerance of form and position [mm]		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 9. Suggested footprint



7 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-Feb-2018	1	Initial release.

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