Integrated Device Technology

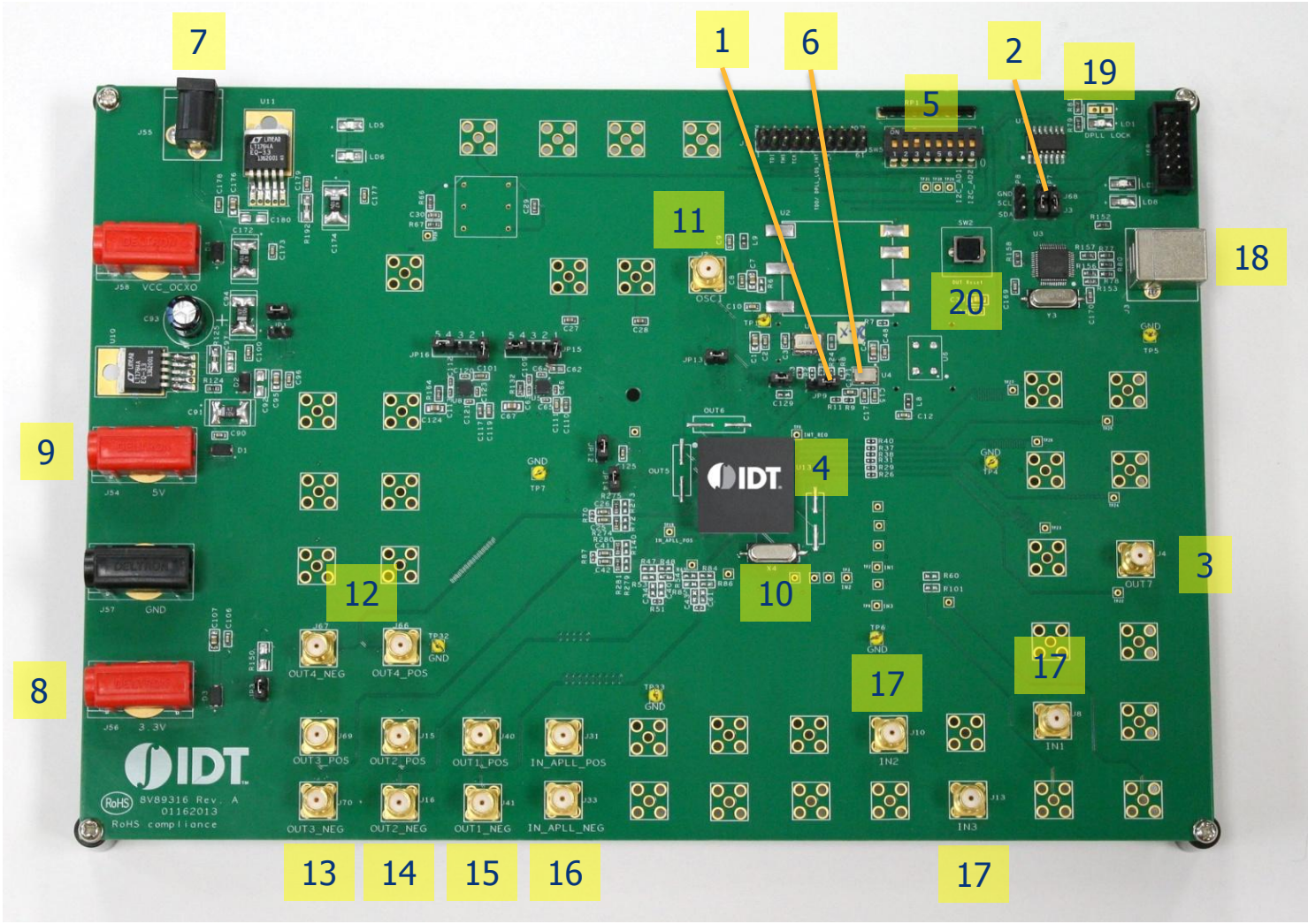
The Analog and Digital Company™

8EBV89316 Installation Guide - Windows®

Prepare Hardware

1. Choose suitable power adapter from selection provided in the evaluation kit
2. Attach adapter to power supply and plug in to mains supply but do not plug into the board yet
3. Plug USB cable into computer but do not plug into board yet
4. Check jumper and DIP switch settings match the 8EBV89316 hardware configuration shown on the next page

8EBV89316 Hardware Configuration



8EBV89316 Hardware Configuration

[1] JP9 jumper. Leave at factory set position for normal operation (linking center and right pins)

[2] JP6 and JP7 jumpers. Leave at factory set position for normal operation (linking center and lower pins)

[3] LVCMOS Output clock

[4] IDT8V89316 chip

[5] Switch SW5: The function of this switch is described in Table 1

[6] Crystal oscillator Master Clock

[7] +5 V DC power supply

[8] +3.3 V power supply for test purpose

[9] +5 V power supply for test purpose

[10] Crystal oscillator for APLL

[11] OSCI: master clock input

[12] Output clock 4 (differential)

[13] Output clock 3 (differential)

[14] Output clock 2 (differential)

[15] Output clock 1 (differential)

[16] Input clock to APLL (differential)

[17] Input clock 1, 2 and 3

[18] USB communication port

[19] DPLL lock indicator

[20] Reset button: Press to reset all devices on the board. Restart the management API following a reset to reconnect the host computer to the board.

Table 1: Switch SW5 Functions

Switch	Function	
SW5-1	Not used	
SW5-2	Not used	
SW5-3	Must be set on for normal operation	Off: “0” On: “1”
SW5-4	Not used	
SW5-5	Not used	
SW5-6	Not used	
SW5-7	I2C_AD1 Set off for normal operation	Off: “0” On: “1”
SW5-8	I2C_AD2 Set off for normal operation	Off: “0” On: “1”

Note: Evaluation board GUI expects a fixed I2C address of 0x51. SW5-7 and SW5-8 should be set to 0 (off) for normal operation.

Install 8EBV89316 Software

1. Unzip the 8EBV89316 and 8EBV89317 combined GUI zip file and copy contents to a new folder on the Windows®-based computer (for example C:\Users\...\Desktop\PLL _GUI_Files)
2. If Java® is not already installed on the computer, install it from http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html
3. If Visual Studio® C++ Redistributable Package is not already installed on the computer, install it from

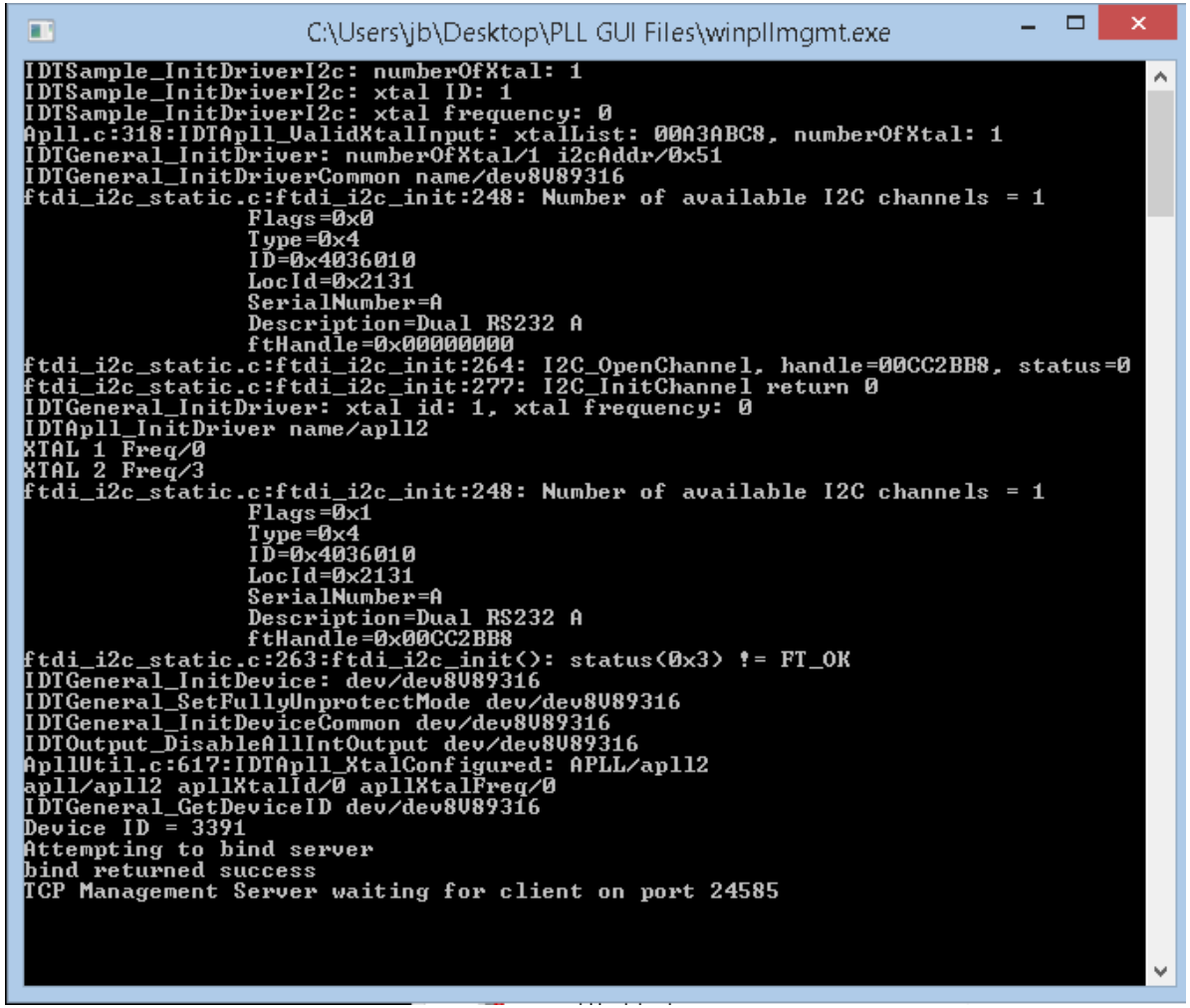
   http://www.microsoft.com/en-ca/download/details.aspx?id=5555
4. Click on http://www.ftdichip.com/Drivers/D2XX.htm
5. Click on “set executable” in table, this launches the following executable:

   http://www.ftdichip.com/Drivers/CDM/CDM%20v2.10.00%20WHQL%20Certified.exe
6. For manual installation using Windows® device manager, follow procedure in [1] on the “Useful Information and Links” page at the end of this guide

Start Hardware and Connect to Management API

1. Plug USB cable into board
   - Red LED LD8 lights next to USB socket on board
   - Windows® drivers load for new hardware
2. Plug power supply into socket marked J55
   - Red LEDs LD5 and LD6 light
3. Run winpllmgmt.exe from the folder created in step 1 – either from a DOS window or by double-clicking the file in Explorer
4. A DOS window appears a shown on the next page. Leave this window open. CTRL-C stops the process and returns to the command prompt.
5. To reconnect the board to the Management API after a manual board reset, run winpllmgmt.exe again as in step 3 above.

Connect to Management API



GUI Start Screen

- Run PllGui.jar from the folder created in step 1 – either from a DOS window or by clicking the file in Explorer. The window below appears.

Useful information and links

- The computer is now connected to the Evaluation board and the GUI is ready for use. Details of the GUI operation are found in the “Ethernet PLL Configuration GUI User Manual” included with the GUI zip file
- FTDI chip Windows® 7 application note an-119:

  http://www.ftdichip.com/Support/Documents/AppNotes/AN_119_FTDI_Drivers_Installation_Guide_for_Windows7.pdf

  Note that USB 2.0 connection using USB 3.0 ports in Windows 7 is not currently supported
- USB view (for verifying the FTDI USB port location)
  - http://www.ftdichip.com/Support/Utilities/usbview.zip

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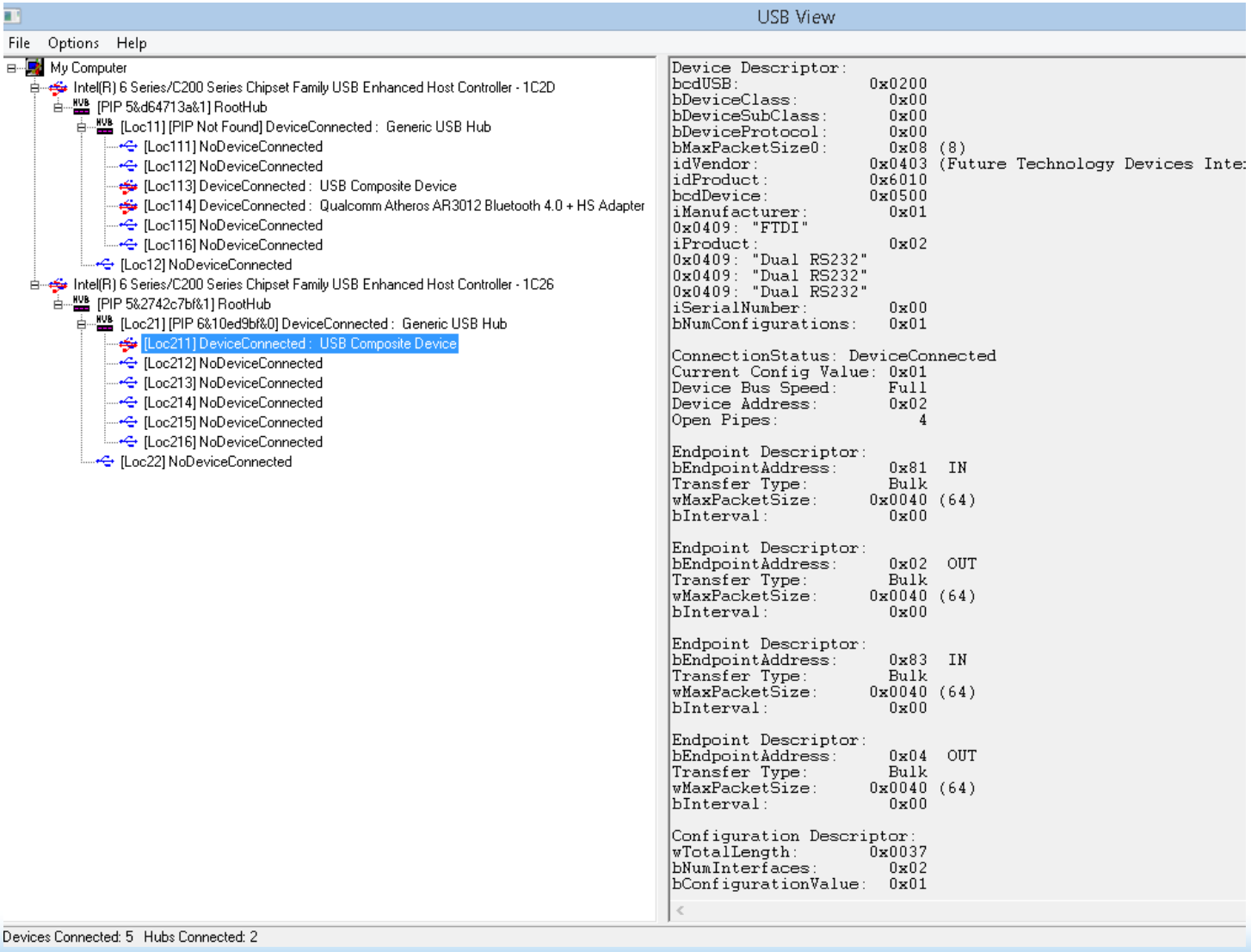
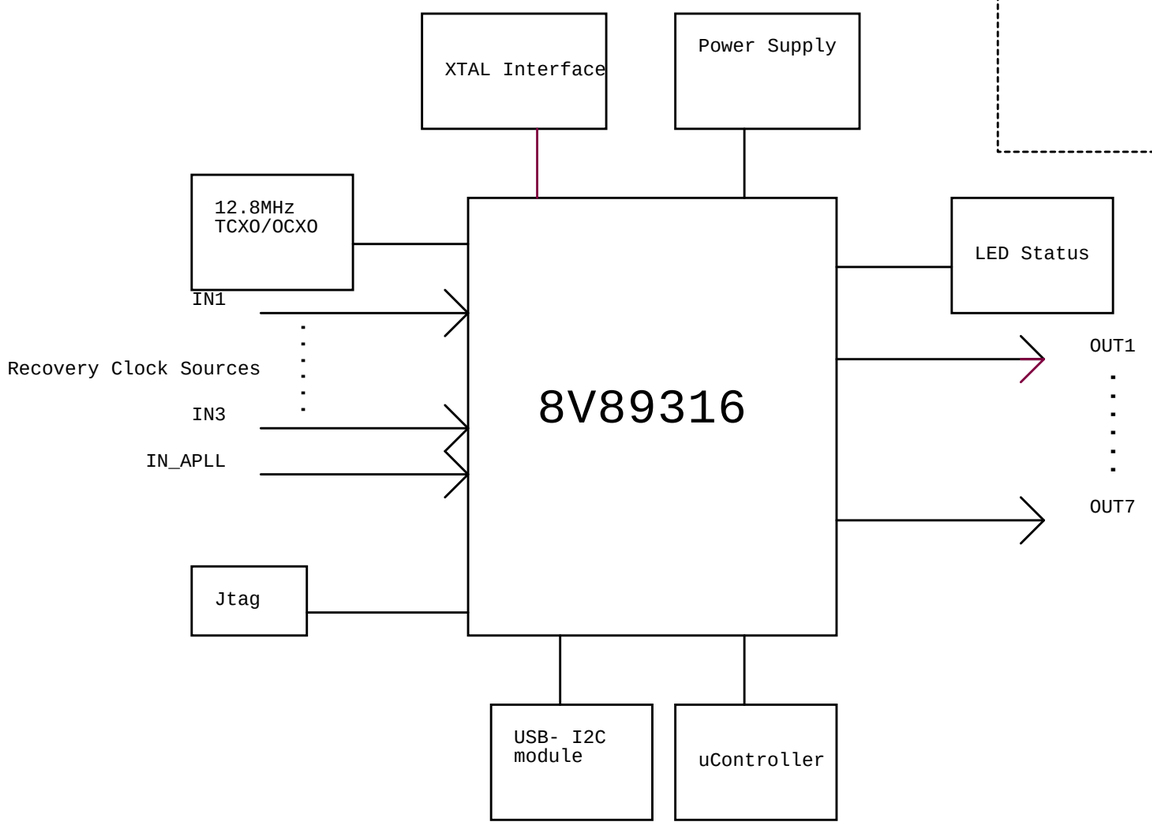
USB View for Typical USB Tree



Schematics

Disclaimer: IDT is providing this schematic for reference purposes only. Although the schematic was taken from a known working design, it is being provided "as is" without any express or implied warranty of any kind.



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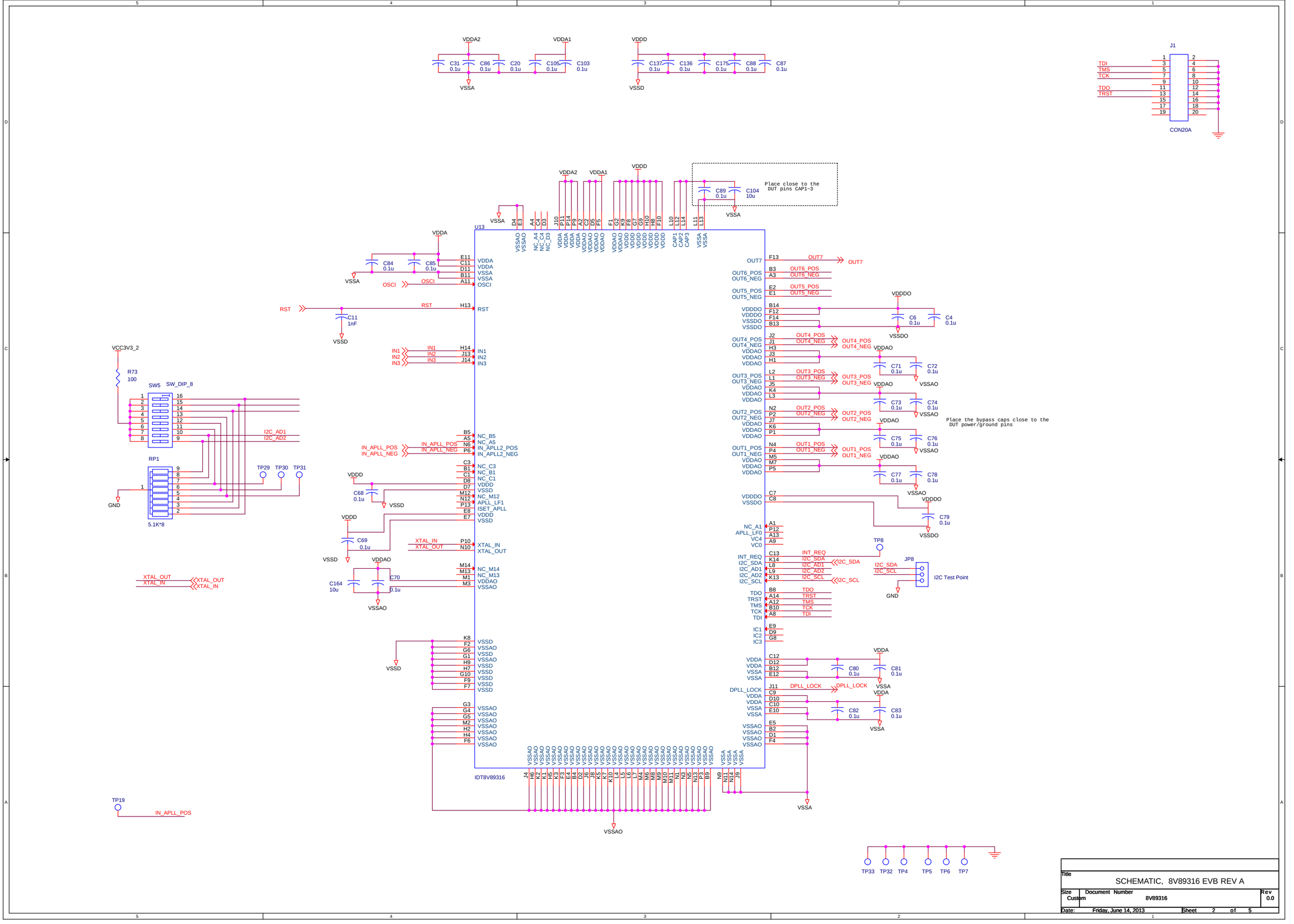

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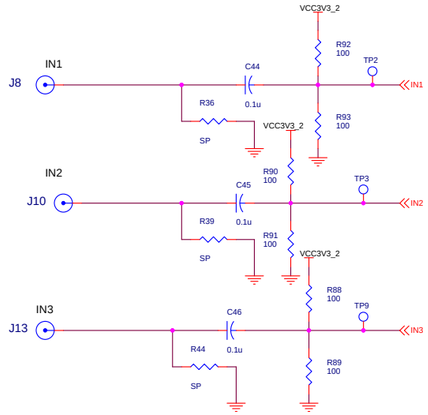
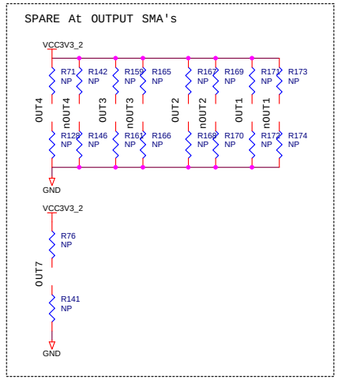
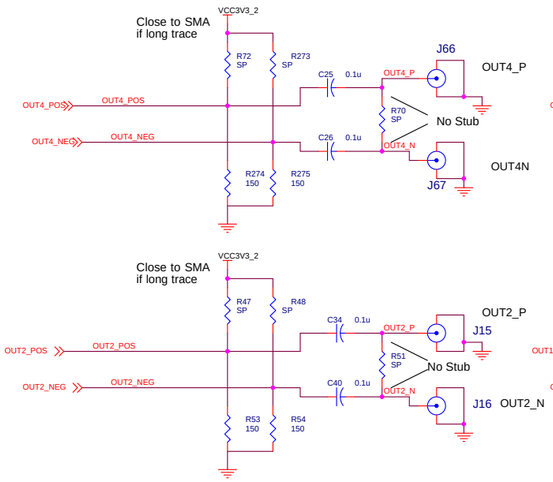
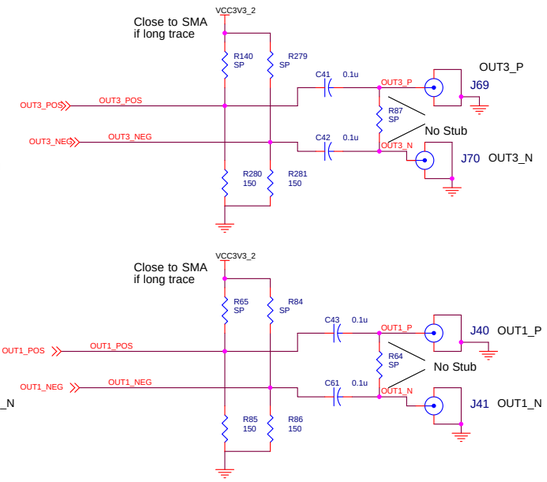


Series termination resistors close to output driver



Close to IC pins





SMA's for input can be either END LAUNCH
or STRAIGHT depends on which way save
space. TBD during layout

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12.8MHz, TCXO or OCXO (Place close to the DUT)

U6 M5626LF 12.8MHz
DNC GND
VCC OUT
OCXO_Power
C47 10u
C48 0.1u
U1 12M8_ TCXO
Tri-state_Enable NC7 NC6
DNC1 NC2 DNC3
VCC DNC10
OUT GND
C1 10u
C2 0.1u
C3 0.1u
R1 SP
TCXO
R24 SP
R3 0
J2
JP9
XO/SMA option
OSCI
R2 SP
R8 0
R5 SP
U4 RTX5032
NC1 NC2 NC3 GND
VC FILTER
VCC NC8 RF OUT
NC10 NC5
C15 0.1u
C17 0.1u
C171 0.1u
R9 100
R11 100
VCC3V2_2
L8 BLM18BB221SN1
C12 0.1u
VCC_OCXO
L9 BLM18BB221SN1
C9 0.1u
C7 10u
C8 0.1u
R6 SP
TP1
U2
INPUT_SUPPLY RF_OUTPUT
NC2 NC1 NC5 NC6 GND
2910 Stratum 3E OCXO
C10 0.1u
R7 SP
OCXO

25MHz XTAL Interface (Place close to the DUT and Put xtals on same layer as BGA pads, shorter trace length, no stubs)

1) Clocks and frequently switched signals should not be routed close to the crystals.
2) Digital signals should not be routed directly under the crystal or XTALn_IN/OUT pins.
3) Keep the crystal bond pads and trace width to the XTALn_IN/OUT pins as small as possible.
4) All metal layers in the PCB are recommended to be removed under the XTALn_OUT ball, crystal pad and associated trace.
5) It is recommended to protect crystal traces with ground traces and guard rings.

XTAL_OUT
XTAL_IN
0025.000000 MHz
X4

XTAL_OUT
XTAL_IN

VCC3V2_2
C39 1u
SW2
R74 10K
SW_PUSHBUTTON
RST
U7C 74HC14/SO

Indicator
C13 0.1u
U7D 74HC14/SO
T0_LOCK
R79 1K
LD1

LD8 RED LED
R152 1K
R189 0
VCC2232
R153 470
C168 0.1u
C167 0.1u
C165 10u
C138 0.1u
C166 0.01u
J3 USB PORT
VBUS D- D+ GND
R77 27
R78 27
VCC2232_3V
3V3_USB
C147 0.1u
U3
3V3OUT AVCC VCC VCC VCCIOA VCCIOB
USBDM USBDP RSTOUT# XTIN XTOUT RESET# EECS EESK EEDATA TEST
TCK/SK TDI/DO TDO/DI TMS/CS GPIOL0 GPIOL1 GPIOL2 GPIOL3
GPIOH0 GPIOH1 GPIOH2 GPIOH3
SI/WUA SI/WUB PWREN#
UNUSED0 UNUSED1 UNUSED2 UNUSED3 UNUSED4 UNUSED5 UNUSED6 UNUSED7
UNUSED8 UNUSED9 UNUSED10 UNUSED11
AGND GND GND GND GND
ft2232_chip
R80 1.5K
XTIN
Y3 6MHz
XTOUT
C169 33PF
C170 33PF
R156 10K
R157 10K
R158 10K
R10 0
SCL1
SDA1
R188 4.7K
R187 4.7K
R190
R191
SP
I2C_SCL
I2C_SDA
R154 470
LD9 Green LED
R13 SP
R14 0
USB to I2C
JP6
JP7
Header_3Pin
J68
SCL2
SDA2
Aardvark I2C/SPI Host Adapter

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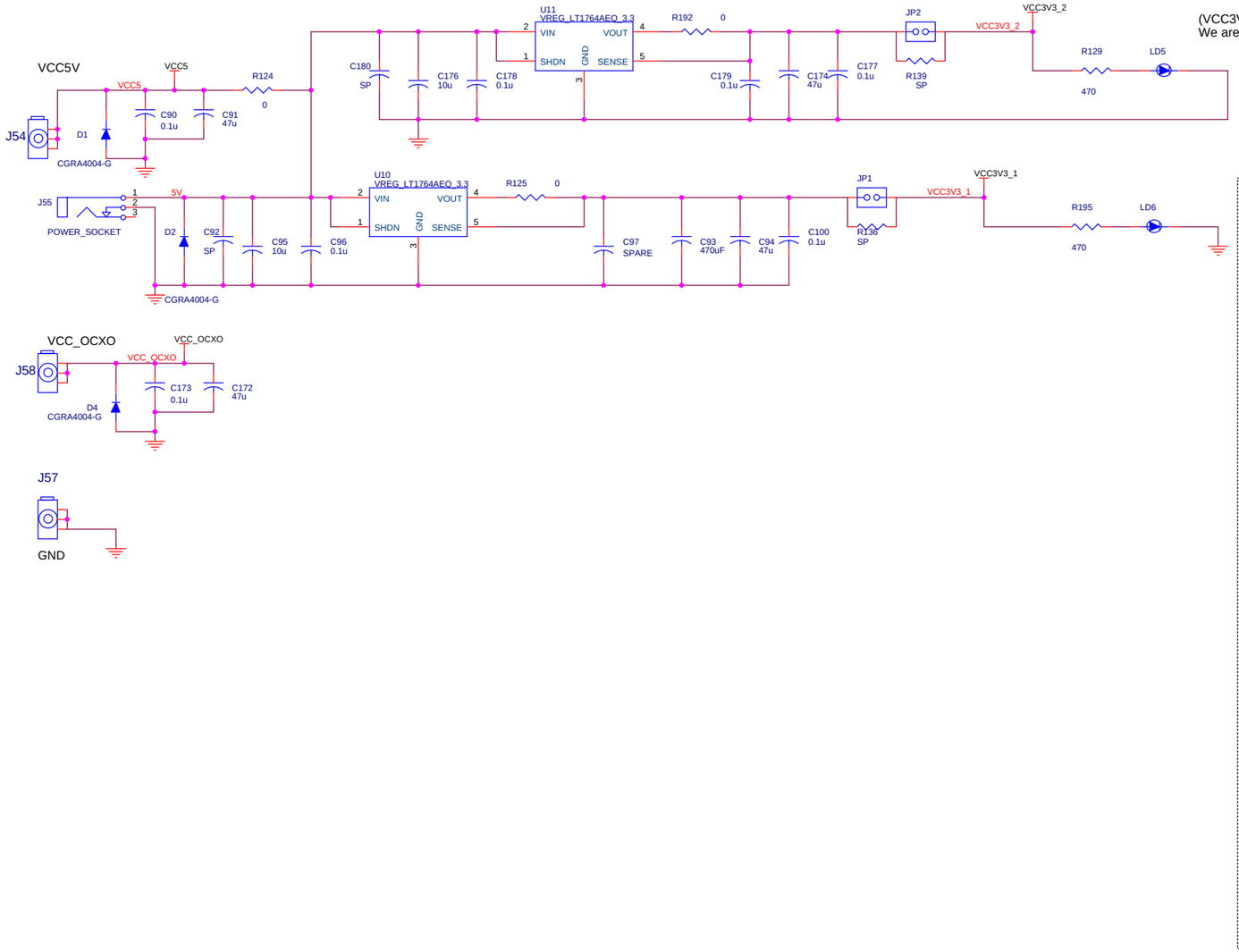
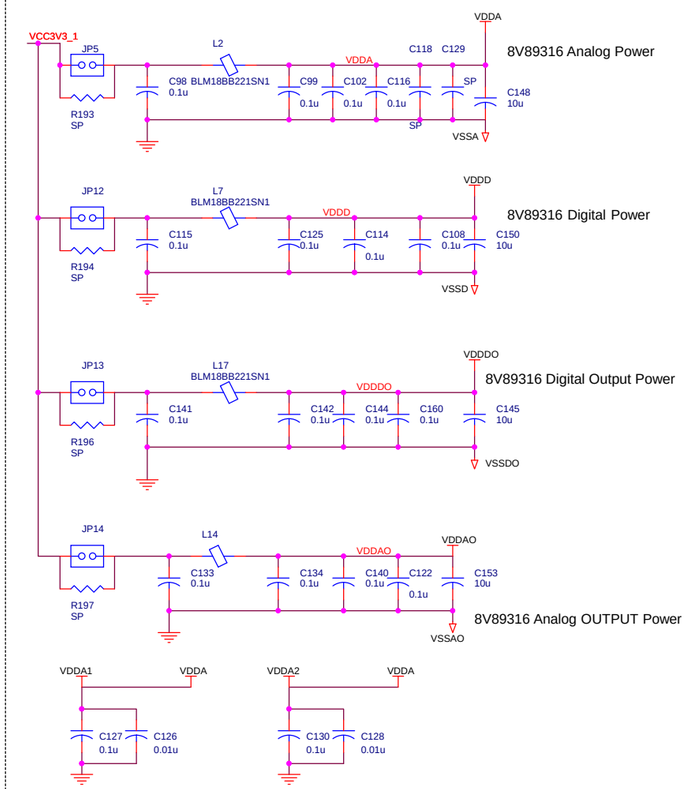
(VCC3V3_1 is used for the 8V89316 DUT and VCC3V3_2 is for the rest of the board circuits.
We are not suggesting a dedicated LDO for the 8V89316 with this reference design, this is just convenient for the test.)



(Place caps close to and accross power and ground pins)



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