SL28610

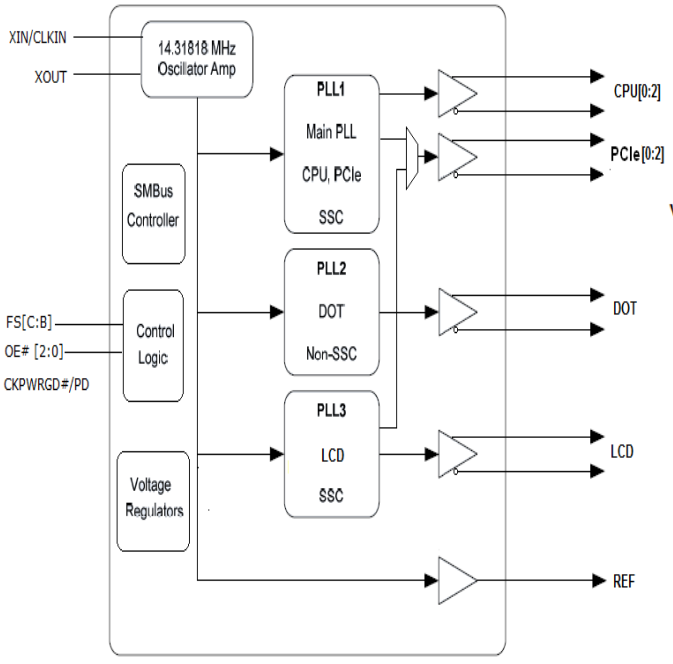
Low Power Clock Generator for Intel® Ultra Mobile Platform

Features

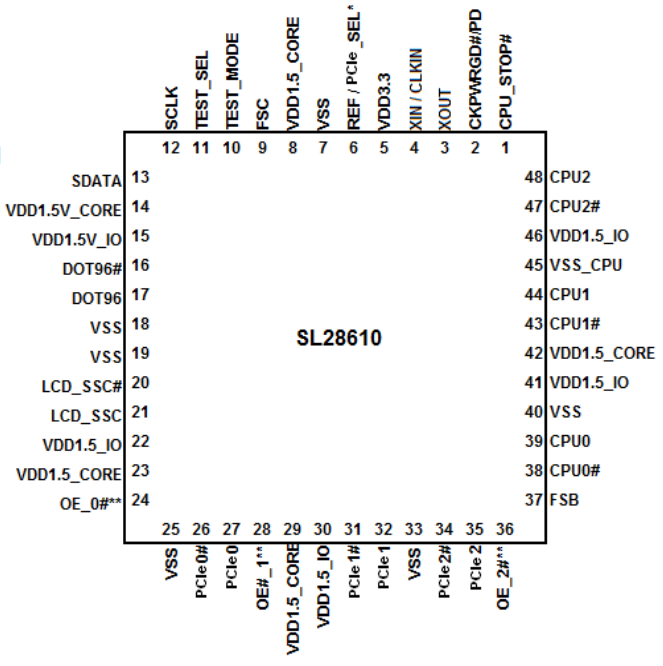
- **Supports intel's Moorestown and Menlow clocking requirements**
- **Compliant to Intel® CK610**
- **Low power push-pull type differential output buffers**
- **Integrated voltage regulator**
- **Integrated resistors on differential clocks**
- **Differential CPU clocks with selectable frequency**
- **100MHz Differential PCIe clocks**
- **100MHz LCD Video Clock**
- **96MHz Differential DOT clock**
- **Buffered Reference Clock 14.318MHz**
- **14.318 MHz Crystal Input or Clock Input**
- **Low-voltage frequency select input**
- **I^2C support with readback capabilities**
- **Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **Industrial Temperature -40°C to 85°C**
- **48-pin QFN package**

CPU	PCIe	DOT96	LCD	REF
x3	x3	x 1	x1	x 1

Block Diagram



Pin Configuration



* 100K-ohm Internal pull down
** 10K-ohm Internal pull-up

400 West Cesar Chavez, Austin, TX 78701 1+(512) 416-8500 1+(512) 416-9669 www.silabs.com

Pin Definitions

Pin No.	Name	Type	Description
1	CPU_STP#	I, SE	3.3V input for CPU_STP# (active low) functionality
2	CKPWRGD#/PD	I, SE	3.3V LVTTL input (active low)
3	XOUT	O, SE	3.3V, 14.31818MHz crystal output *(When used a clock input, float XOUT)*
4	XIN/CLKIN	I, SE	3.3V, 14.31818MHz crystal input, 3.3V Clock Input.
5	VDD3.3V	PWR	3.3V power supply for single-ended clock
6	REF / PCIe_SEL	IO, PD, SE	3.3V, 14.31818MHz output / 1.5V input active high signal latched on CKPWRGD# signal to select PCIe from PLL3 *(share with LCD PLL; 100K-ohm internal pull-down)*
7	VSS	GND	Ground
8	VDD1.5_CORE	PWR	1.5V power supply for core
9	FSC	I, SE	1.05V Frequency Select C
10	TEST_MODE	I, SE	3.3V-tolerant input to selects Ref/N or Tri-state when in test mode. 0 = Tri-state, 1 = Ref/N
11	TEST_SEL	I, SE	3.3V-tolerant input to selects TEST_SEL 0 = Normal, 1 = Test Entry
12	SCLK	I, SE	3.3V SMBus Clock Line
13	SDATA	I/O, SE	3.3V SMBus Data Line
14	VDD1.5_CORE	PWR	1.5V power supply for core
15	VDD1.5_IO	PWR	1.5V power supply for differential outputs
16	DOT96#	O, DIFF	Fixed complimentary 96MHz clock output
17	DOT96	O, DIFF	Fixed true 96MHz clock output
18	VSS	GND	Ground
19	VSS	GND	Ground
20	LCD_SSC#	O, DIF	Complementary 100MHz Differential clock
21	LCD_SSC	O, DIF	True 100MHz Differential clock
22	VDD1.5_IO	PWR	1.5V power supply for differential outputs
23	VDD1.5_CORE	PWR	1.5V power supply for core
24	OE_0#	I, SE	Output enable for PCIe0, *(10K-ohm internal pull-up)* 0 =enable, 1=disable
25	VSS	GND	Ground
26	PCIe0#	O, DIF	Complementary 100MHz Differential clock
27	PCIe0	O, DIF	True 100MHz Differential clock
28	OE_1#	I, SE	Output enable for PCIe1, *(10K-ohm internal pull-up)* 0 =enable, 1=disable
29	VDD1.5_CORE	PWR	1.5V Power Supply for core
30	VDD1.5_IO	PWR	1.5V Power Supply for differential output
31	PCIe1#	O, DIF	Complementary 100MHz Differential clock
32	PCIe1	O, DIF	True 100MHz Differential clock
33	VSS	GND	Ground
34	PCIe2#	O, DIF	Complementary 100MHz Differential clock
35	PCIe2	O, DIF	True 100MHz Differential clock
36	OE_2#	I, SE	Output enable for PCIe2, *(10K-ohm internal pull-up)* 0 =enable, 1=disable
37	FSB	I, SE	1.05V Frequency Select B
38	CPU0#	O, DIF	Complementary Host Differential clock
39	CPU0	O, DIF	True Host Differential clock

Pin Definitions (continued)

Pin No.	Name	Type	Description
40	VSS	GND	Ground
41	VDD1.5_IO	PWR	1.5V Power Supply for differential output
42	VDD1.5_CORE	PWR	1.5V Power Supply for core
43	CPU1#	O, DIF	Complementary Host Differential clock
44	CPU1	O, DIF	True Host Differential clock
45	VSS_CPU	GND	Ground
46	VDD1.5_IO	PWR	1.5V Power Supply for differential output
47	CPU2#	O, DIF	Complementary Host Differential clock
48	CPU2	O, DIF	True Host Differential clock

Table 1. Frequency Select Pin (FSB and FSC)

FSC	FSB	CPU	PCIe	LCD	DOT96	REF
1	0	100 MHz	100 MHz	100 MHz	96 MHz	14.318 MHz
0	0	133 MHz	100 MHz	100 MHz	96 MHz	14.318 MHz
0	1	166 MHz	100 MHz	100 MHz	96 MHz	14.318 MHz
1	1	200 MHz	100 MHz	100 MHz	96 MHz	14.318 MHz

Frequency Select Pin (FSB and FSC)

Apply the appropriate logic levels to FSB and FSC inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled LOW on CKPWRGD and indicates that VTT voltage is stable then FSB and FSC input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid LOW, all other FSB, FSC, and CKPWRGD transitions are ignored except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave

Table 3. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
27:20	Byte Count–8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	PLL1_EN	PLL1 Enable 0 = Disabled, 1 = Enabled
6	1	PLL2_EN	PLL2 Enable 0 = Disabled, 1 = Enabled
5	1	PLL3_EN	PLL3 Enable 0 = Disabled, 1 = Enabled
4	0	RESERVED	RESERVED
3	1	CPU_DIV	CPU Output Divider Enable 0 = Disabled, 1 = Enabled
2	1	PCIe_DIV	PCIe Output Divider Enable 0 = Disabled, 1 = Enabled
1	1	LCD_DIV	LCD Output Divider Enable 0 = Disabled, 1 = Enabled
0	1	DOT96_DIV	DOT96 Output Divider Enable 0 = Disabled, 1 = Enabled

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	PLL1_Spread _EN	PLL1 Spread Enable 0 = Disabled, 1 = Enabled
6	1	PLL3_Spread _EN	PLL3 Spread Enable 0 = Disabled, 1 = Enabled
5	0	PLL3_CFB2	PLL3 Spread Spectrum Select PLL3_CFB[2:0] 000 = -%0.5 (Down Spread) - Default 001 = -%1.0, DS 010 = -%1.5, DS 011 = -% 2.0, DS 100 = %±0.30 (Center Spread) 101 = %±0.50, CS 110 = %±1.00, CS 111 = %±1.25, CS
4	0	PLL3_CFB1	
3	0	PLL3_CFB0	
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	CPU0_OE	Output enable for CPU0 0 = Output Disabled, 1 = Output Enabled
6	1	CPU1_OE	Output enable for CPU1 0 = Output Disabled, 1 = Output Enabled
5	1	CPU2_OE	Output enable for CPU2 0 = Output Disabled, 1 = Output Enabled
4	1	PCIe0_OE	Output enable for PCIe0 0 = Output Disabled, 1 = Output Enabled
3	1	PCIe1_OE	Output enable for PCIe1 0 = Output Disabled, 1 = Output Enabled

Byte 2: Control Register 2 (continued)

Bit	@Pup	Name	Description
2	1	PCIe2_OE	Output enable for SCR2 0 = Output Disabled, 1 = Output Enabled
1	1	DOT96_OE	Output enable for DOT96 0 = Output Disabled, 1 = Output Enabled
0	1	LCD_OE	Output enable for LCD 0 = Output Disabled, 1 = Output Enabled

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	REF_OE	Output enable for REF 0 = Output Disabled, 1 = Output Enabled
4	1	REF_Bit1	REF Slew Rate Control Bit2*(see Byte 16 Bit [7:6] for Slew Rate REF_Bit0 & REF_Bit2)* 0 = 1 load, 1 = 2 loads
3	0	RESERVED	RESERVED
2	0	CPU0_STP#	CPU0 CPU_STP# Control 0 = Free Running, 1 = Stopped with CPU_STP#
1	0	CPU1_STP#	CPU1 CPU_STP# Control 0 = Free Running, 1 = Stopped with CPU_STP#
0	0	CPU2_STP#	CPU2 CPU_STP# Control 0 = Free Running, 1 = Stopped with CPU_STP#

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	HW	PLL1 M DIV 7	This is a read only register of the multiplier used for PLL1 M Divider HW= Read Only
6	HW	PLL1 M DIV 6	
5	HW	PLL1 M DIV 5	
4	HW	PLL1 M DIV 4	
3	HW	PLL1 M DIV 3	
2	HW	PLL1 M DIV 2	
1	HW	PLL1 M DIV 1	
0	HW	PLL1 M DIV 0	

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	HW	PLL1 N DIV 7	This is a read only register of the multiplier used for PLL1 N Divider HW= Read Only
6	HW	PLL1 N DIV 6	
5	HW	PLL1 N DIV 5	
4	HW	PLL1 N DIV 4	
3	HW	PLL1 N DIV 3	
2	HW	PLL1 N DIV 2	
1	HW	PLL1 N DIV 1	
0	HW	PLL1 N DIV 0	

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	HW	PLL2 N DIV 8	This is a read only register of the multiplier used for PLL2 M and N Dividers HW= Read Only
6	HW	PLL2 N DIV 9	
5	HW	PLL2 M DIV 5	
4	HW	PLL2 M DIV 4	
3	HW	PLL2 M DIV 3	
2	HW	PLL2 M DIV 2	
1	HW	PLL2 M DIV 1	
0	HW	PLL2 M DIV 0	

Byte 7: Control Register 7

Bit	@Pup	Name	Description
7	HW	PLL2 N DIV 7	This is a read only register of the multiplier used for PLL2 N Divider HW= Read Only
6	HW	PLL2 N DIV 6	
5	HW	PLL2 N DIV 5	
4	HW	PLL2 N DIV 4	
3	HW	PLL2 N DIV 3	
2	HW	PLL2 N DIV 2	
1	HW	PLL2 N DIV 1	
0	HW	PLL2 N DIV 0	

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	HW	PLL3 M DIV 7	This is a read only register of the multiplier used for PLL3 M Divider HW= Read Only
6	HW	PLL3 M DIV 6	
5	HW	PLL3 M DIV 5	
4	HW	PLL3 M DIV 4	
3	HW	PLL3 M DIV 3	
2	HW	PLL3 M DIV 2	
1	HW	PLL3 M DIV 1	
0	HW	PLL3 M DIV 0	

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	HW	PLL3 N DIV 7	This is a read only register of the multiplier used for PLL3 N Divider HW= Read Only
6	HW	PLL3 N DIV 6	
5	HW	PLL3 N DIV 5	
4	HW	PLL3 N DIV 4	
3	HW	PLL3 N DIV 3	
2	HW	PLL3 N DIV 2	
1	HW	PLL3 N DIV 1	
0	HW	PLL3 N DIV 0	

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	HW	FSB	FSB status bit, CPU Frequency Select Bit, read only
6	HW	FSC	FSC status bit, CPU Frequency Select Bit, read only
5	HW	OE#_0	OE#_0 status bit, PCIe0 enable status, read only 0 = PCIe0 disabled, 1 = PCIe0 enabled
4	HW	OE#_1	OE#_0 status bit, PCIe1 enable status, read only 0 = PCIe1 disabled, 1 = PCIe1 enabled
3	HW	OE#_2	OE#_0 status bit, PCIe2 enable status, read only 0 = PCIe2 disabled, 1 = PCIe2 enabled
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	1	Vendor ID bit 3	Vendor ID Bit 3
6	0	Vendor ID bit 2	Vendor ID Bit 2
5	0	Vendor ID bit 1	Vendor ID Bit 1
4	0	Vendor ID bit 0	Vendor ID Bit 0
3	0	Rev Code Bit 3	Revision Code Bit 3
2	0	Rev Code Bit 2	Revision Code Bit 2
1	0	Rev Code Bit 1	Revision Code Bit 1
0	1	Rev Code Bit 0	Revision Code Bit 0

Byte 12: Byte Count 12

Bit	@Pup	Name	Description
7	1	Device_ID3	0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = CK610 Yellow Cover Device, 48-pin QFN 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
6	0	Device_ID2	
5	1	Device_ID1	
4	0	Device_ID0	
7	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 14: Control Register 14

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
7	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 15: Control Register 15

Bit	@Pup	Name	Description
7	0	BC7	Byte count 7
6	0	BC6	Byte count 6
5	0	BC5	Byte count 5
4	1	BC4	Byte count 4
3	0	BC3	Byte count 3
2	1	BC2	Byte count 2
1	1	BC1	Byte count 1
0	0	BC0	Byte count 0

Byte 16: Control Register 16

<table>
<tr><th>Bit</th><th>@Pup</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>0</td><td>REF_Bit2</td><td rowspan="2">REF Slew Rate Control Bit2 & Bit0 (see Byte 3 Bit 4 for Slew Rate REF_Bit1)
<table>
<tr><th>Mode</th><th>Bit2</th><th>Bit1</th><th>Bit0</th><th>Buffer Strength</th></tr>
<tr><td></td><td>1</td><td>1</td><td>1</td><td rowspan="9">Strong
↓
Weak</td></tr>
<tr><td></td><td>1</td><td>1</td><td>0</td></tr>
<tr><td></td><td>1</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Default</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td></td><td>0</td><td>1</td><td>0</td></tr>
<tr><td></td><td>0</td><td>0</td><td>1</td></tr>
<tr><td></td><td>0</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>6</td><td>1</td><td>REF_Bit0</td></tr>
<tr><td>5:0</td><td>0</td><td>RESERVED</td><td>RESERVED</td></tr>
</table>

Byte 17: Control Register 17

Bit	@Pup	Name	Description
7	0	PLL1_DAF_N7	If Prog_PLL1_EN is set, the values programmed in PLL1_DAF_N[7:0] and PLL1_DAF_M[7:0] are used to determine the PLL1 output frequency.
6	0	PLL1_DAF_N6	
5	0	PLL1_DAF_N5	
4	0	PLL1_DAF_N4	
7	0	PLL1_DAF_N3	
2	0	PLL1_DAF_N2	
1	0	PLL1_DAF_N1	
0	0	PLL1_DAF_N0	

Byte 18: Control Register 18

Bit	@Pup	Name	Description
7	0	PLL1_DAF_M7	If Prog_PLL1_EN is set, the values programmed in PLL1_DAF_N[7:0] and PLL1_DAF_M[7:0] are used to determine the PLL1 output frequency.
6	0	PLL1_DAF_M6	
5	0	PLL1_DAF_M5	
4	0	PLL1_DAF_M4	
7	0	PLL1_DAF_M3	
2	0	PLL1_DAF_M2	
1	0	PLL1_DAF_M1	
0	0	PLL1_DAF_M0	

Byte 19: Control Register 19

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	Prog_PLL1_EN	Programmable PLL1 frequency enable 0 = Disabled, 1= Enabled
4	0	Prog_PLL3_EN	Programmable PLL3 frequency enable 0 = Disabled, 1= Enabled
3	0	CPU_OEB_DRIVE _Mode	Controls CPU Output Drive States 1 = OUT=LOW and OUT#=LOW 0= OUT=HIGH and OUT#=LOW
2	0	PCIe_OEB_DRIVE _Mode	Controls PCIe Output Drive States 1 = OUT=LOW and OUT#=LOW 0= OUT=HIGH and OUT#=LOW
1	0	LVDS_OEB_DRIVE _Mode	Controls LVDS Output Drive States 1 = OUT=LOW and OUT#=LOW 0= OUT=HIGH and OUT#=LOW
0	0	DOT_OEB_DRIVE _Mode	Controls DOT Output Drive States 1 = OUT=LOW and OUT#=LOW 0= OUT=HIGH and OUT#=LOW

Byte 20: Control Register 20

Bit	@Pup	Name	Description
7	0	PLL3_DAF_N7	If Prog_PLL3_EN is set, the values programmed in PLL3_DAF_N[7:0] and PLL3_DAF_M[7:0] are used to determine the PLL3 output frequency.
6	0	PLL3_DAF_N6	
5	0	PLL3_DAF_N5	
4	0	PLL3_DAF_N4	
7	0	PLL3_DAF_N3	
2	0	PLL3_DAF_N2	
1	0	PLL3_DAF_N1	
0	0	PLL3_DAF_N0	

Byte 21: Control Register 21

Bit	@Pup	Name	Description
7	0	PLL3_DAF_M7	If Prog_PLL3_EN is set, the values programmed in PLL3_DAF_N[7:0] and PLL3_DAF_M[7:0] are used to determine the PLL3 output frequency.
6	0	PLL3_DAF_M6	
5	0	PLL3_DAF_M5	
4	0	PLL3_DAF_M4	
7	0	PLL3_DAF_M3	
2	0	PLL3_DAF_M2	
1	0	PLL3_DAF_M1	
0	0	PLL3_DAF_M0	

CKPWRGD#/PD (Power down) Clarification

The CKPWRGD#/PD pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD#. Once CKPWRGD# has been sampled HIGH by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

CKPWRGD#/PD (Power down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held HIGH on their next HIGH-to-LOW transition and differential clocks must held HIGH. When PD mode is desired as the initial power on state, PD must be asserted HIGH in less than 10 μs after asserting CKPWRGD.

CKPWRGD#/PD (Power Down) Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from power down are driven high in less than 300 μs of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. *Figure 2* is an example showing the relationship of clocks coming up.

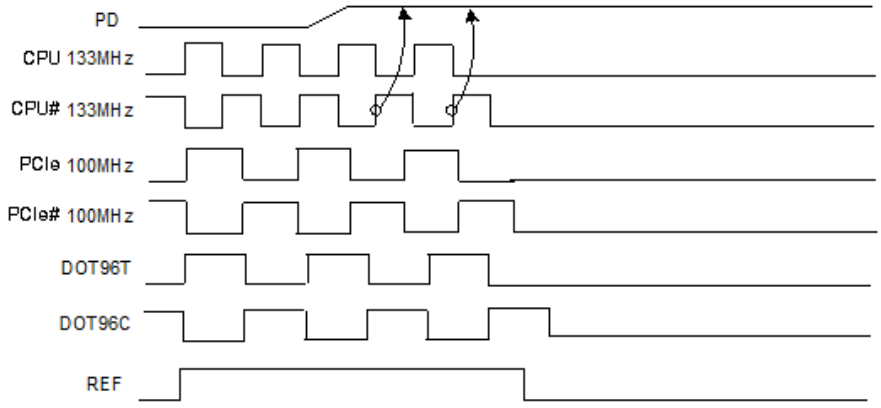


Figure 1. Power down Assertion Timing Waveform

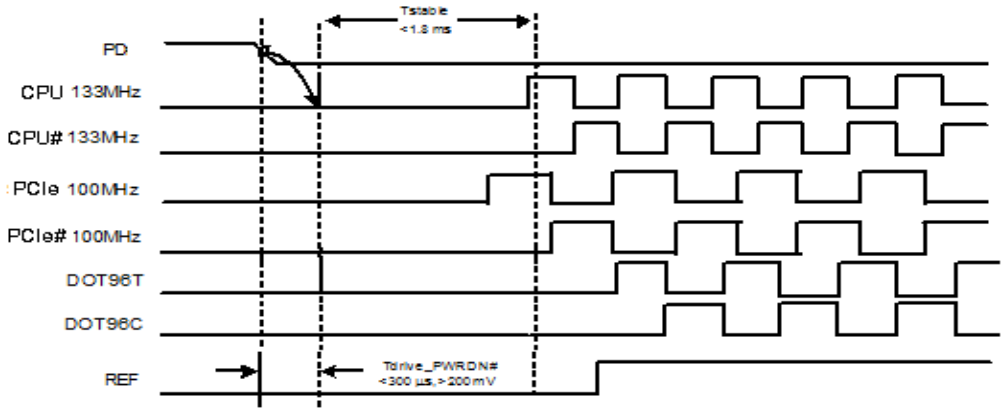


Figure 2. Power down Deassertion Timing Waveform

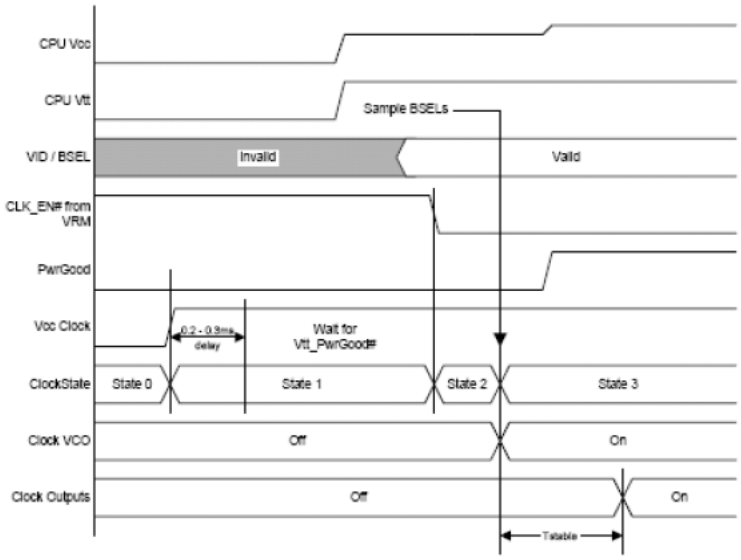


Figure 3. CKPWRGD# Timing Diagram

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable are stopped within two to six CPU clock periods after sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

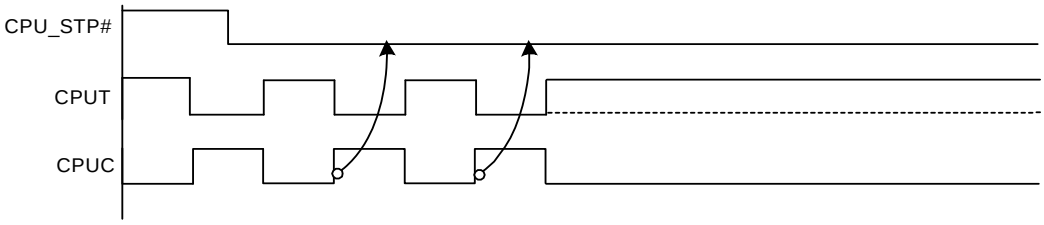


Figure 4. CPU_STP# Assertion Waveform

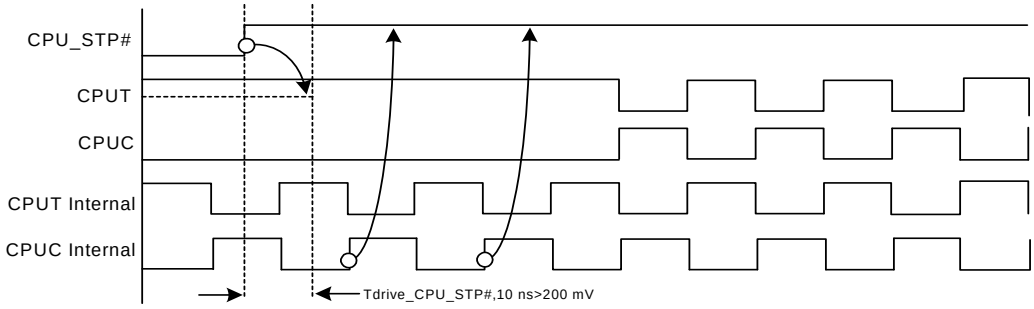


Figure 5. CPU_STP# Deassertion Waveform

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Table 1. Output Driver Status during PCI_STPPCI_STP# and CPU_STP#

		CPU_STP# Asserted	SMBus Disabled	OE# Pins Disabled
Single-ended Clocks	Stoppable	Running	Driven low	Driven low
	Non stoppable	Running		
Differential Clocks	Stoppable	Clock driven high	Driven Low	Clock driven high*
		Clock# driven low		Clock# driven low*
	Non stoppable	Running		

Note: *Differential clocks output state can be configured through Byte 19 bits 3:.0

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
3.3V_V_{DD}	3.3V Supply Voltage	Functional	–0.5	4.6	V
1.5V_V_{DD_CORE}	1.5V Supply Voltage	Functional	–0.5	2.1	V
1.5V_V_{DD_IO}	DIFF I/O Supply Voltage	Functional	–0.5	2.1	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Commercial Temperature, Operating Ambient	Functional	0	85	°C
	Industrial Temperature, Operating Ambient		-40	+85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22-A114)	2000	–	V
UL-94	Flammability Rating	UL (CLASS)	V–0		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
1.5V_V_{DD_CORE}	1.5V Operating Voltage	1.5V ± 5%	1.425	1.575	V
1.5V_V_{DD_IO}	1.5V Differential I/O Supply Voltage	1.5V ± 5%	1.425	1.575	V
3.3V_V_{DD}	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
3.3V_V_{IH}	3.3V Input High Voltage (SE)	3.3V_V_{DD}	2	3.3V_CORE+ 0.3	V
3.3V_V_{IL}	3.3V Input Low Voltage (SE)		V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IH_FS}	FS_[C,B] Input High Voltage	1.05V_CORE	0.9	1.5V_CORE + 0.3	V
V_{IL_FS}	FS_[C,B] Input Low Voltage		GND-0.3	0.25	V
V_{IH}	OE# Input High Voltage	1.5V_CORE	1.2	1.5V_CORE + 0.3	V
V_{IL}	OE# Input Low Voltage		GND-0.3	0.3	V
V_{IH}	PCIe_SEL Input High Voltage	3.3V_CORE	2.0	VDD+0.3	V
V_{IL}	PCIe_SEL Input Low Voltage		GND-0.3	0.8	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
$V_{DD\ IO}$	Low Voltage IO Supply Voltage		0.72	0.88	
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF

DC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
Power	Power Consumption		–	100	mW

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device operates reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R/T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-µs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
Clock Input					
T_{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T_R/T_F	CLKIN Rise and Fall Times	Measured between $0.2V_{DD}$ and $0.8V_{DD}$	0.5	4.0	V/ns
T_{CCJ}	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T_{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V_{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
V_{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
I_{IL}	Input LowCurrent	XIN / CLKIN pin, 0 < VIN <0.8	–	20	uA
I_{IH}	Input HighCurrent	XIN / CLKIN pin, VIN = VDD	–	35	uA
CPU at 0.7V					
T_{DC}	CPU Clock Duty Cycle	Measured at 0V differential at 0.1s	45	55	%
T_{PERIOD}	100 MHz CPU Clock Period	Measured at 0V differential at 0.1s	9.997001	10.00300	ns
T_{PERIOD}	133 MHz CPU Clock Period	Measured at 0V differential at 0.1s	7.497751	7.587251	ns
T_{PERIOD}	166 MHz CPU Clock Period	Measured at 0V differential at 0.1s	5.998201	6.001801	ns
T_{PERIOD}	200 MHz CPU Clock Period	Measured at 0V differential at0.1s	4.99950	5.00050	ns
$T_{PERIODSS}$	100 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	9.997001	10.05327	ns
$T_{PERIODSS}$	133 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	7.412751	7.624950	ns
$T_{PERIODSS}$	166 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	5.998201	6.031960	ns
$T_{PERIODSS}$	200 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	5.01203	5.01303	ns
$T_{PERIODAbs}$	100 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	9.912001	10.08800	ns
$T_{PERIODAbs}$	133 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	7.412751	7.587251	ns
$T_{PERIODAbs}$	166 MHz CPU Clock Absolute period	Measured at 0V differential at1 clock	5.913201	6.086801	ns
$T_{PERIODAbs}$	200 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	4.91450	5.08550	ns
$T_{PERIODSSAbs}$	100 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at1 clock	9.912001	10.13827	ns
$T_{PERIODSSAbs}$	133 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	7.412751	7.624950	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERIODSSAbs}$	166 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	5.913201	6.116960	ns
$T_{PERIODSSAbs}$	200 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	4.91453	5.11060	ns
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at 0V differential	–	85	ps
$L_{ACC_non\text{-}SSC}$	Long-term Accuracy	Measured at 0V differential	–	300	ppm
L_{ACC_SSC}	Long-term Accuracy	Measured at 0V differential	–	2800	ppm
T_{SKEW}	Pin-to-pin Skew	Measured at 0V differential	–	100	ps
T_R / T_F	CPU Clock Rise and Fall Time	Measured differentially from ±150 mV	0.6	4	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{abs}	Absolute Min and Max V_{SWING}	Measured single-endedly	–0.3	1.15V	V
V_{OX}	Crossing Point Voltage at 0.7V Swing	Measured single-endedly	300	550	mV
Vox_variation	Crossing Point Variation	Measured single-endedly		140	mV
V_{OVS}	Maximum Voltage (Overshoot)	Measured single-endedly		V_{HIGH}+ 0.3V	V
V_{UDS}	Maximum Voltage (Undershoot)	Measured single-endedly	0.3		V
V_{RB}	Ring back voltage	Measured single-endedly	-100	100	mV
T_{STABLE}	Time before V_{RB}	Measured single-endedly	500		ps
PCIe at 0.7V					
T_{DC}	PCIe Clock Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz PCIe Clock Period	Measured at 0V differential at 0.1s	9.997001	10.0030	ns
$T_{PERIODSS}$	100 MHz PCIe Clock Period, SSC	Measured at 0V differential at 0.1s	9.997001	10.05327	ns
$T_{PERIODAbs}$	100 MHz PCIe Clock Absolute Period	Measured at 0V differential at 1 clock	9.912001	10.08800	ns
$T_{PERIODSSAbs}$	100 MHz PCIePCIe Clock Absolute Period, SSC	Measured at 0V differential at 1 clock	9.912001	10.13827	ns
T_{CCJ}	PCIe Clock Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
$L_{ACC_non\text{-}SSC}$	Long-term Accuracy	Measured at 0V differential	–	300	ppm
L_{ACC_SSC}	Long-term Accuracy	Measured at 0V differential	–	2800	ppm
T_{SKEW}	Pin-to-pin Skew	Measured at 0V differential	–	100	ps
T_R / T_F	PCIe Clock Rise and Fall Time	Measured differentially from ±150 mV	0.6	4	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{abs}	Absolute Min and Max V_{SWING}	Measured single-endedly	–0.3	1.15V	V
V_{OX}	Crossing Point Voltage at 0.7V Swing	Measured single-endedly	300	550	mV
Vox_variation	Crossing Point Variation	Measured single-endedly		140	mV
V_{OVS}	Maximum Voltage (Overshoot)	Measured single-endedly		V_{HIGH}+ 0.3V	V
V_{UDS}	Maximum Voltage (Undershoot)	Measured single-endedly	0.3		V
V_{RB}	Ring back voltage	Measured single-endedly	-100	100	mV
T_{STABLE}	Time before V_{RB}	Measured single-endedly	500		ps
DOT96 at 0.7V					
T_{DC}	DOT96 Clock Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	DOT96 Clock Period	Measured at 0V differential at 0.1s	10.41354	10.41979	ns
$T_{PERIODAbs}$	DOT96 Clock Absolute Period	Measured at 0V differential at 0.1s	10.16354	10.66979	ns
T_{CCJ}	DOT96 Clock Cycle to Cycle Jitter	Measured at 0V differential at 1 clock	–	250	ps
L_{ACC}	DOT96 Clock Long Term Accuracy	Measured at 0V differential at 1 clock	–	300	ppm

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{SKEW}	Pin-to-pin Skew	Measured at 0V differential	–	100	ps
T_R / T_F	DOT96 Clock Rise and Fall Time	Measured differentially from ±150 mV	0.6	4	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{abs}	Absolute Min and Max V_{SWING}	Measured single-endedly	–0.3	1.15V	V
V_{OX}	Crossing Point Voltage at 0.7V Swing	Measured single-endedly	300	550	mV
Vox_variation	Crossing Point Variation	Measured single-endedly		140	mV
VOVS	Maximum Voltage (Overshoot)	Measured single-endedly		VHIGH+ 0.3V	V
VUDS	Maximum Voltage (Undershoot)	Measured single-endedly	0.3		V
V_{RB}	Ring back voltage	Measured single-endedly	-100	100	mV
T_{STABLE}	Time before V_{RB}	Measured single-endedly	500		ps
LCD_100_SSC at 0.7V					
T_{DC}	SSC Clock Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SSC Clock Period	Measured at 0V differential at 0.1s	9.997001	10.0030	ns
$T_{PERIODSS}$	100 MHz SSC Clock Period, SSC	Measured at 0V differential at 0.1s	9.997001	10.05327	ns
$T_{PERIODAbs}$	100 MHz SSC Clock Absolute Period	Measured at 0V differential at 1 clock	9.912001	10.08800	ns
$T_{PERIODSSAbs}$	100 MHz SSC Clock Absolute Period, SSC	Measured at 0V differential at 1 clock	9.912001	10.13827	ns
T_{CCJ}	SSC Clock Cycle to Cycle Jitter	Measured at 0V differential	–	250	ps
L_{ACC}	SSC Clock Long Term Accuracy	Measured at 0V differential	–	300	ppm
T_{SKEW}	Pin-to-pin Skew	Measured at 0V differential	–	100	ps
T_R / T_F	SSC Clock Rise and Fall Time	Measured differentially from ±150 mV	0.6	4	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{abs}	Absolute Min and Max V_{SWING}	Measured single-endedly	–0.3	1.15V	V
V_{OX}	Crossing Point Voltage at 0.7V Swing	Measured single-endedly	300	550	mV
Vox_variation	Crossing Point Variation	Measured single-endedly		140	mV
VOVS	Maximum Voltage (Overshoot)	Measured single-endedly		VHIGH+ 0.3V	V
VUDS	Maximum Voltage (Undershoot)	Measured single-endedly	0.3		V
V_{RB}	Ring back voltage	Measured single-endedly	-100	100	mV
T_{STABLE}	Time before V_{RB}	Measured single-endedly	500		ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.82033	69.86224	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T_R / T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
$T_{HIGH/LOSW}$	Clock High /Low Time	Measured single-endedly	32	39	
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	95	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

1

Test and Measurement Set-up

For Single-ended Reference Clock

The following diagram shows the load configurations for the single-ended REF output signals.

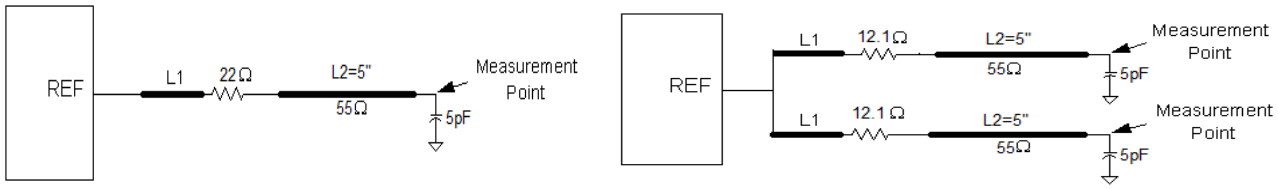


Figure 6. Single-ended REF Load Configuration

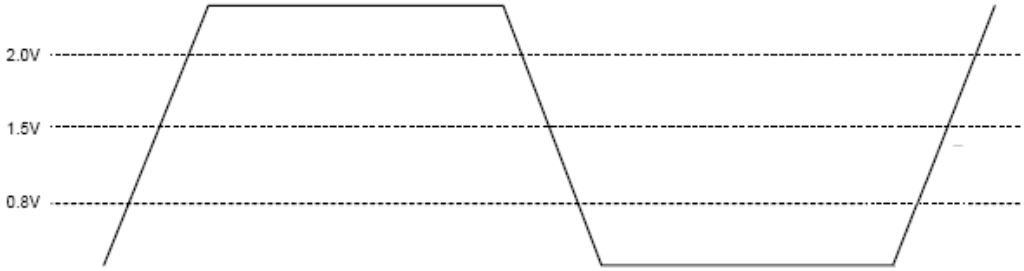


Figure 7. Single-ended Output Signals (for AC Parameters Measurement)

For CPU, PCIe, and DOT96 Signals and Reference

This diagram shows the test load configuration for the differential CPU and PCIe outputs

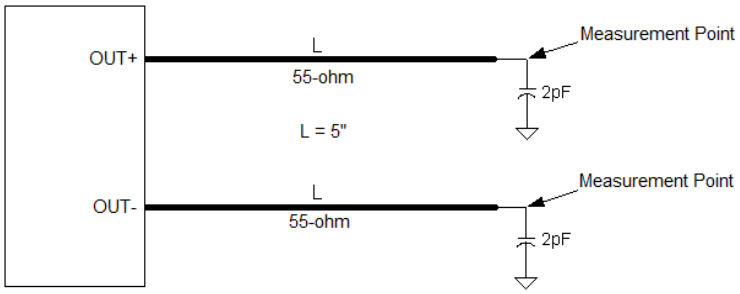


Figure 8. 0.7V Differential Load Configuration

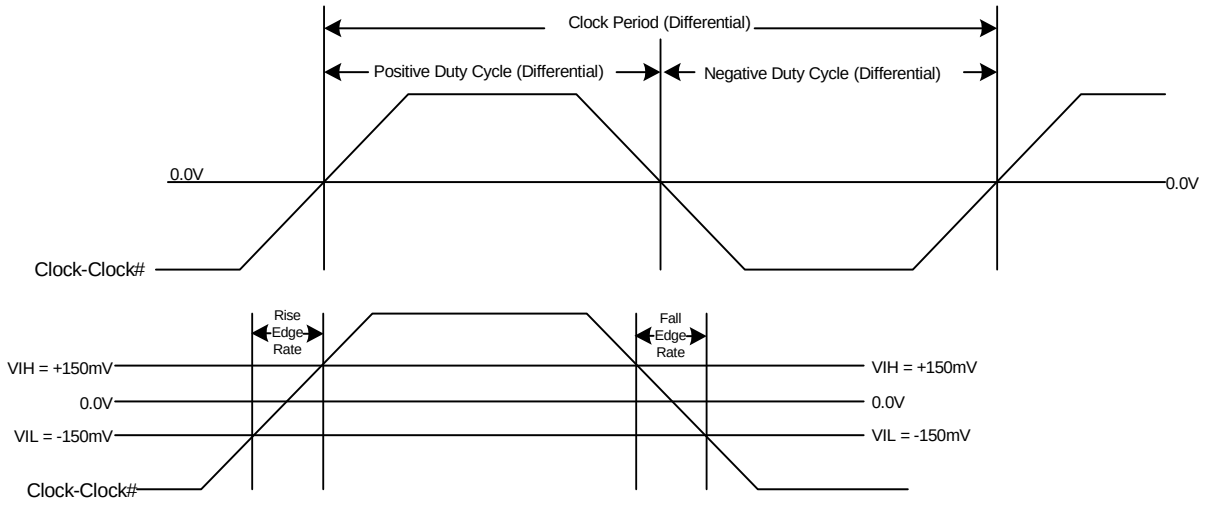


Figure 9. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

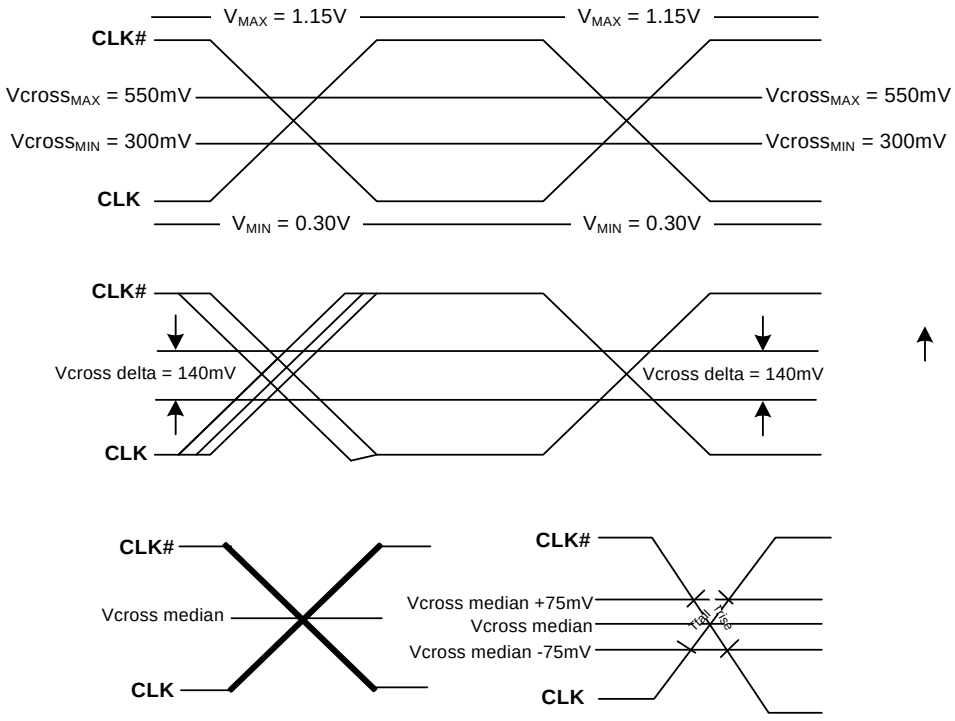
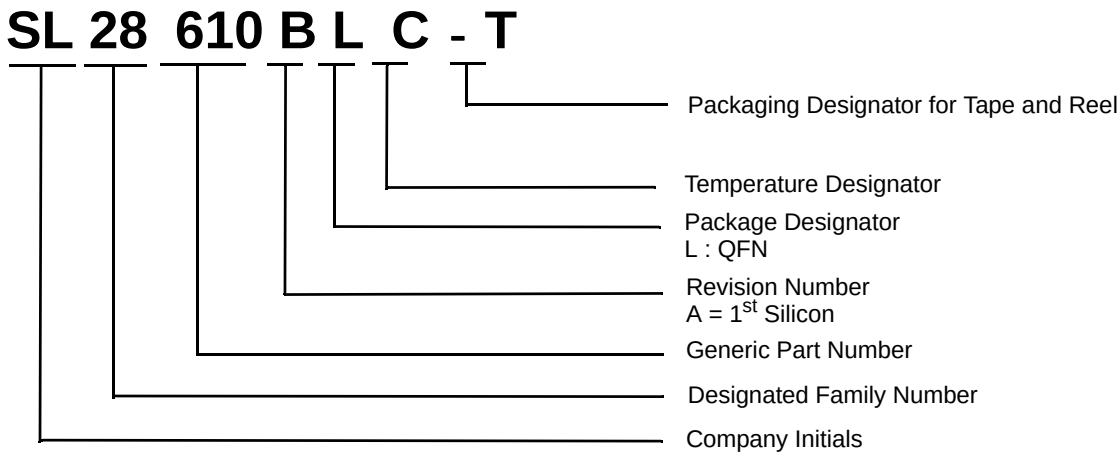


Figure 10. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

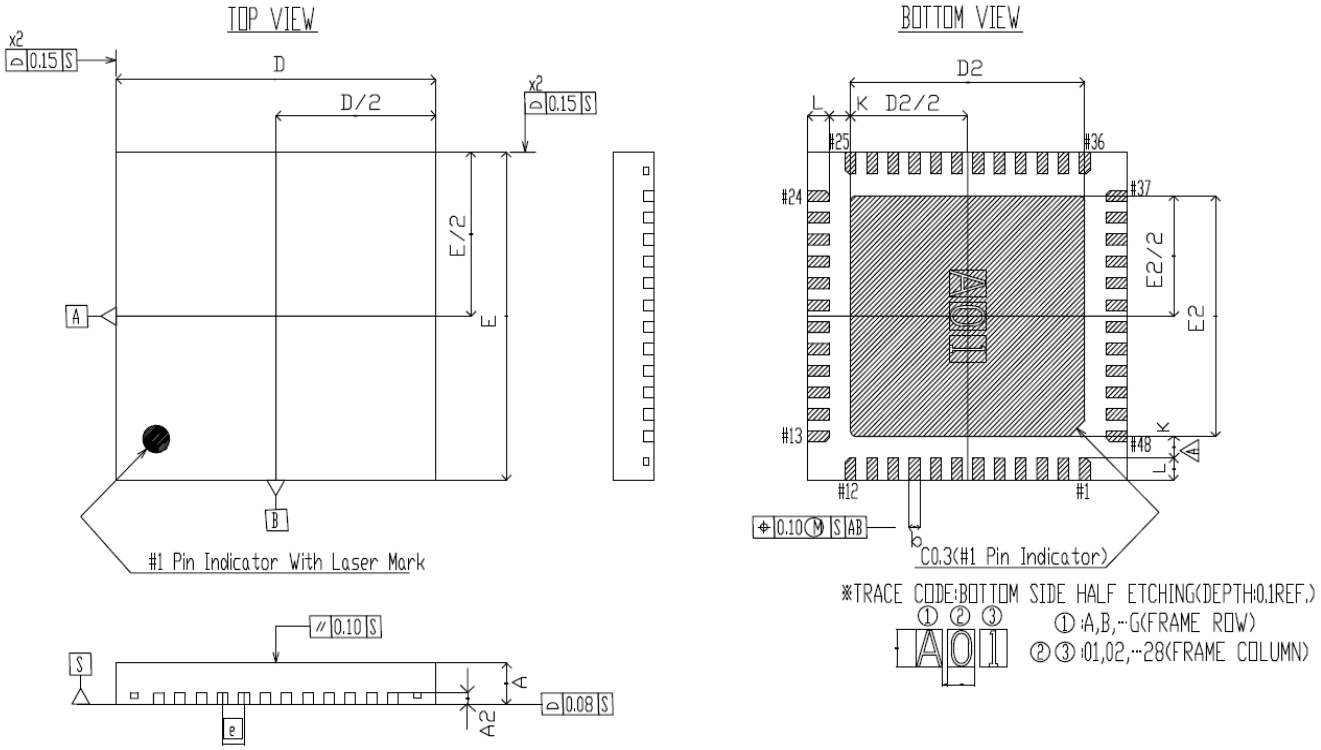
Part Number	Package Type	Product Flow
Lead-free		
SL28610BLC	48-pin QFN	Commerial, 0° to 85°C
SL28610BLI	48-pin QFN	Industrial, -40° to 85°C

This device is Pb free and RoHS compliant.



Package Diagrams

48-Lead QFN 6 x 6mm LF48A



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	4.25	4.40	4.55
E	5.90	6.00	6.10
E2	4.25	4.40	4.55
e		0.40 BSC.	
k	0.36	—	—
L	0.30	0.40	0.50

NOTES)
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.10.
3.THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8μm.
4.PROTRUSIONS AT PKG.OUTLINE SHALL NOT EXCEED 0.10.

Document History Page

Document Title: SL28610 PC Low Power Clock Generator for Intel® Ultra Mobile Platform DOC #: SP-AP-0078 (Rev. 1.0)				
REV.	**ECR#**	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0		09/15/08	JMA	New Datasheet
1.1		10/12/09	JMA	1. Renamed PWRGD# to CKPWRGD# 2. Updated block diagram to show differential outputs 3. Updated miscellaneous text contents
AA	1633	05/27/10	JMA	1. Updated to be ISO compliant 2. Added Clock input feature 3. Updated MIL-STD to JEDEC
AA	1801	09/23/10	TRP	1. Updates VIL_FS 2. Updated miscellaneous text and format contents 3. Removed crystal recommendations
AA	1801	10/1/10	TRP	1. Added clock feature 2. Updated block diagram 3. Updated SRC clock as PCIe

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- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

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