NCN51205GEVB

KNX Evaluation Board User's Manual

ON Semiconductor®

EVAL BOARD USER'S MANUAL

Introduction

The NCN5120 Development Board is the ideal solution for developing your KNX application with the ON Semiconductor KNX transceiver NCN5120. The development board contains the NCN5120 KNX Transceiver which handles the transmission and reception of data on the bus. It will also generate all necessary voltages to power the board and external loads.

It also contains a microcontroller with debug interface for custom firmware development. Up to 8 external switches can be monitored and up to 4 external loads can be controlled. A voltage between 3.3 V and 21 V is available to drive the external loads.

The NCN5120 Development Board assures safe coupling to and decoupling from the KNX bus. Bus monitoring warns the external microcontroller for loss of power so that critical data can be stored in time.

Key Features

- 9,600 baud KNX Communication Speed
- Supervision of KNX Bus Voltage
- High Efficient 3.3 V to 21 V Selectable DC−DC Converter to Drive External Loads
- Monitoring of Power Regulators
- No Additional Power Supply Required
- Buffering of Sent Data Frames (Extended Frames Supported)
- Selectable UART or SPI Interface to Host Controller
- Selectable UART and SPI Baud Rate to Host Controller
- Optional CRC on UART to the Host
- Optional MARKER Character to the Host
- Optional Direct Coupling of RxD and TxD to Host (Analog Mode)
- Auto Polling (Optional)
- Temperature Monitoring
- Contains Freely Programmable Microcontroller for Custom Applications
- Monitoring of 8 External Switches
- Controlling of 4 External (High Voltage) Loads (e.g. LED's)
- One Freely Usable Push Button
- 3 Freely Usable LED's
- Operating Temperature Range −25°C to +85°C

Figure 1. NCN5120 Development Board

May, 2013 – Rev. 0
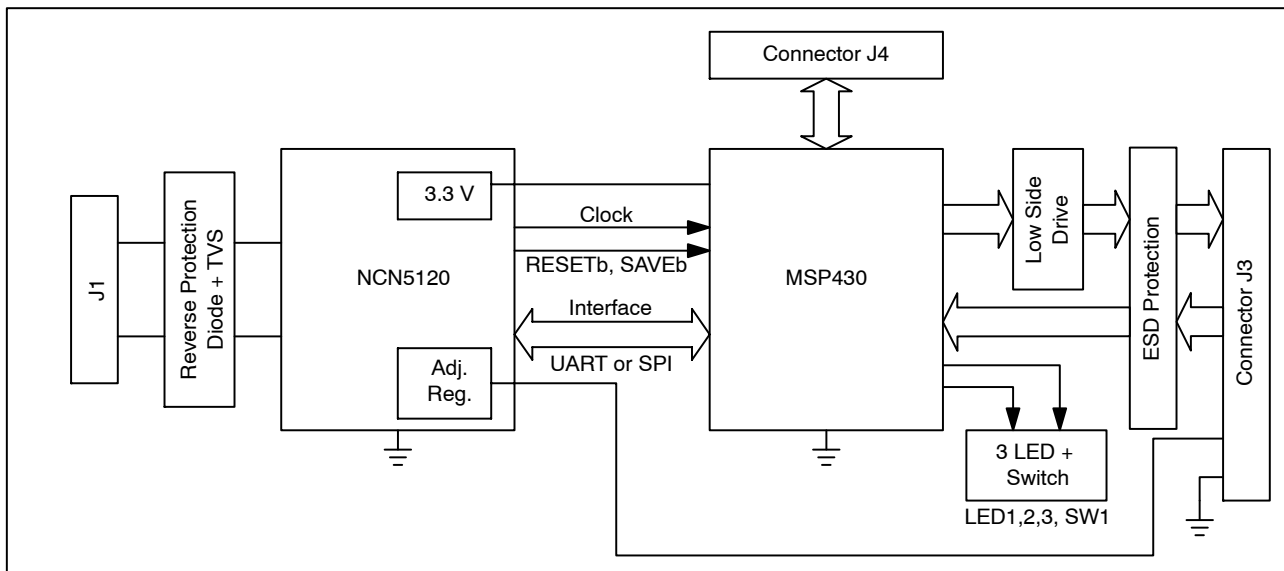
NCN51205GEVB

BLOCK DIAGRAM

Figure 2. NCN5120 Development Board Block Diagram

CONNECTOR DESCRIPTION

Table 1. CONNECTOR LIST AND DESCRIPTION

Connector	Description
J1	KNX Bus Connection
J2	Power Supply and UART Connection
J3	External Switch Inputs and External Outputs
J4	Microcontroller Debug Interface

TYPICAL APPLICATION

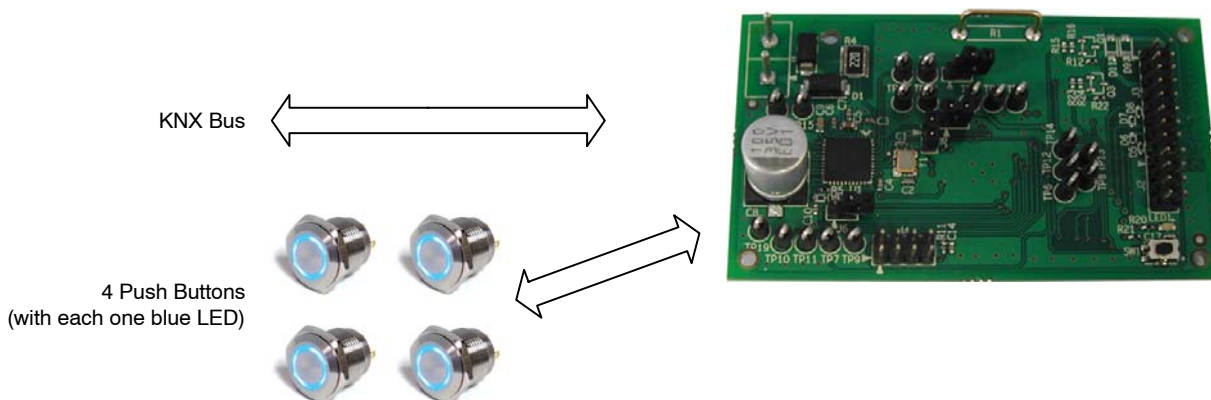KNX Bus

4 Push Buttons
(with each one blue LED)

Figure 3. Typical Application

ELECTRICAL SPECIFICATION

Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the development board. Note that the functionality of the development board outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 2. OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{BUS}	Voltage on Positive Pin of J1 (Note 1)	+20	+33	V
V_{DIG1}	Input Voltage on J4 and J3 (Pins 9, 11, 13 and 15) and J2 (Pin 8)	0	3.3	V
V_{DIG2}	Input Voltage on J3 (Pins 1, 3, 5 and 7) (Note 2)	0	5	V
V_{DD1}	Output Voltage on J2 (Pin 1)	0	3.3	V
V_{DD2}	Output Voltage on J3 (Pins 2, 4, 6 and 8) and J2 (Pins 3 and 7) (Note 3)	3.3	21	V
V_{20V}	Output Voltage on J2 (Pin 5)	0	22	V
T_a	Ambient Temperature	−25	+85	°C

1. Voltage indicates DC value. With equalization pulse bus voltage must be between 11 V and 45 V
2. Higher voltages are possible. See Adjustable DC−DC Converter page 15 for more details. Only valid if R12, R17, R22 and R25 are not mounted.
3. See Adjustable DC−DC Converter page 15 for the limitations!

Table 3. DC PARAMETERS

(The DC parameters are given for a development board operating within the Recommended Operating Conditions unless otherwise specified.)

Convention: currents flowing in the circuit are defined as positive.

Symbol	Con-nector	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
Power Supply								
V_{BUS}	J1	1	Bus DC Voltage	Excluding Active and Equalization Pulse	20		33	V
I_{BUS}			Bus Current Consumption	Normal Operating Mode, No External Load, DC1 and DC2 Enabled, Continuous Transmission of '0' on the KNX Bus by another KNX Device		5		mA
V_{BUSH}			Undervoltage Release Level	V_{BUS} Rising (Figure NO TAG)		18.0		V
V_{BUSL}			Undervoltage Trigger Level	V_{BUS} Falling (Figure NO TAG)		16.8		V
V_{BUS_Hyst}			Undervoltage Hysteresis		0.6			V
KNX Bus Coupler								
$I_{coupler\_lim}$	J1	1	Bus Coupler Current Limitation	J5 open	13		30	mA
				J5 shorted	26		60	mA
Fixed DC−DC Converter								
V_{DD1}	J2	1	Output Voltage		3.13	3.3	3.47	V
V_{DD1_rip}			Output Voltage Ripple	V_{BUS} = 26 V, I_{DD1} = 40 mA		40		mV
I_{DD1_lim}			Overcurrent Threshold		−100		−200	mA
η_{VDD1}			Power Efficiency	V_{in} = 26 V, I_{DD1} = 35 mA		90		%

Table 3. DC PARAMETERS (continued)

(The DC parameters are given for a development board operating within the Recommended Operating Conditions unless otherwise specified.)

Convention: currents flowing in the circuit are defined as positive.

Symbol	Con-nector	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
Adjustable DC−DC Converter								
V_{DD2}	J2, J3	3 (J2), 2, 4, 6 and 8 (J3)	Output Voltage	$V_{BUS} > V_{DD2}$	3.3		21	V
V_{DD2H}			Undervoltage Release Level	V_{DD2} Rising (Figure NO TAG)		$0.9 \times V_{DD2}$		V
V_{DD2L}			Undervoltage Trigger Level	V_{DD2} Faling (Figure NO TAG)		$0.8 \times V_{DD2}$		V
V_{DD2_rip}			Output Voltage Ripple	$V_{BUS} = 26$ V, $V_{DD2} = 3.3$ V, $I_{DD2} = 40$ mA		40		mV
I_{DD2_lim}			Overcurrent Threshold		−100		−200	mA
η_{VDD2}			Power Efficiency	$V_{in} = 26$ V, $V_{DD2} = 3.3$ V, $I_{DD2} = 35$ mA		90		%
20 V Regulator								
V_{20V}	J2	5	20 V Output Voltage	$I_{20V} < 4$ mA, $V_{BUS} > 25$ V	18	20	22	V
I_{20V_Lim}			20 V Output Current Limitation		−4		−11	mA
V_{20VH}			20 V Undervoltage Release Level	20 V Rising	12.6	13.4	14.2	V
V_{20VL}			20 V Undervoltage Trigger Level	20 V Falling	11.8	12.6	13.4	V
V_{20V_hys}			Overcurrent Threshold	$V_{20V\_hys} = V_{20VH} - V_{20VL}$		0.8		V
Digital Inputs								
V_{IL}	J2	7	Logic Low Threshold	Pin 1, 3, 5 and 7 (J3) only valid if R12, R17, R22 and/or R25 are mounted and Q1, Q2, Q3 and/or Q4 are not mounted.	0		0.7	V
	J3	1, 3, 5, 7, 9, 11, 13, 15						
	J4	2, 3, 4, 5, 6, 8						
V_{IH}	J2	7	Logic High Threshold		2.65		3.3	V
	J3	1, 3, 5, 7, 9, 11, 13, 15						
	J4	2, 3, 4, 5, 6, 8						
Digital Outputs								
V_{OL}	J2	7	Logic Low Output Level		0	–	0.6	V
V_{OH}			Logic High Output Level		$V_{DD1} - 0.6$	–	V_{DD1}	V
V_{OL_OD}	J3	1, 3, 5, 7	Logic Low Level Open Drain	$I_{OL} = 5$ mA	–	–	0.4	V

Table 4. AC PARAMETERS

(The AC parameters are given for a development board operating within the Recommended Operating Conditions unless otherwise specified.)

| Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
Power Supply							
t_{BUS_FILTER}	VBUS1	VBUS1 Filter Time	(Figure x3)	–	2	–	ms
MASTER Serial Peripheral Interface (MASTER SPI)							
t_{sck}	SCK	SPI Clock Period	SPI Baudrate Depending on Configuration Input Bits (see Interface Mode page 16). Tolerance is Equal to Xtal Oscillator Tolerance. (Figure 7)	–	2	–	μs
				–	8	–	μs
t_{SCK_HIGH}		SPI Clock High Time		–	$t_{sck} / 2$	–	
t_{SCK_LOW}		SPI Clock Low Time		–	$t_{sck} / 2$	–	
t_{SDI_SET}	SDI	SPI Data Input Setup Time		125	–	–	ns
t_{SDI_HOLD}		SPI Data Input Hold Time		125	–	–	ns
t_{SDO_VALID}	SDO	SPI Data Output Valid Time	C_L = 20 pF (Figure 7)	–	–	100	ns
t_{CS_HIGH}		SPI Chip Select High Time	(Figure 7)	$0.5 \times t_{SCK}$	–	–	
t_{CS_SET}	CSB	SPI Chip Select Setup Time		$0.5 \times t_{SCK}$	–	–	
t_{CS_HOLD}		SPI Chip Select Hold Time		$0.5 \times t_{SCK}$	–	–	
t_{TREQ_LOW}		TREQ Low Time	(Figure 7)	125	–	–	ns
t_{TREQ_HIGH}	TREQ	TREQ High Time		125	–	–	ns
t_{TREQ_SET}		TREQ Setup Time		125	–	–	ns
t_{TREQ_HOLD}		TREQ Hold Time		125	–	–	ns
Universal Asynchronous Receiver/Transmitter (UART)							
f_{UART}	TXD, RXD	UART Interface Baudrate	Baudrate Depending on Configuration Input Pins (see Interface Mode page 16).	–	19,200	–	Baud
			Tolerance is equal to tolerance of Xtal oscillator tolerance.	–	38,400	–	Baud
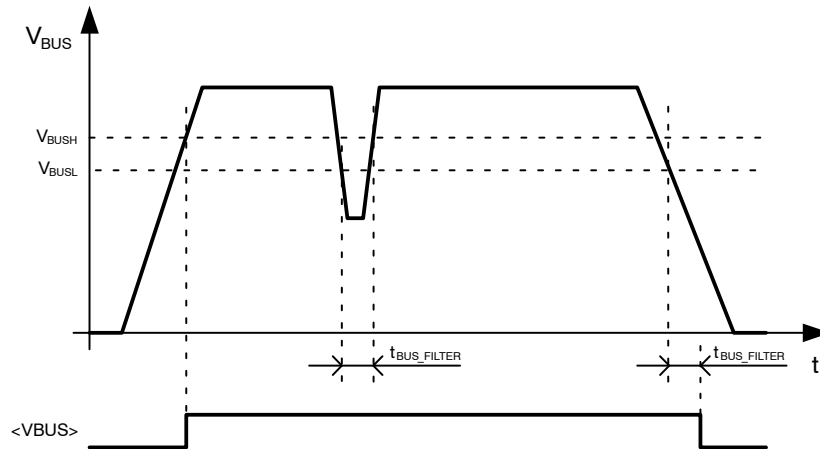
Comments:

<VBUS> is an internal signal which can be verified with the Internal State Service

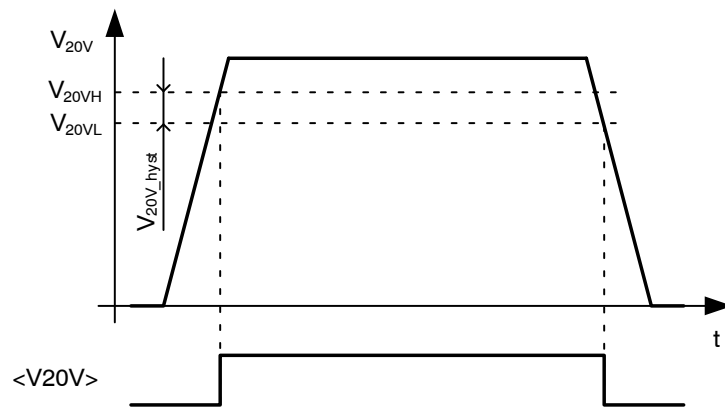**Figure 4. Bus Voltage Undervoltage Threshold**
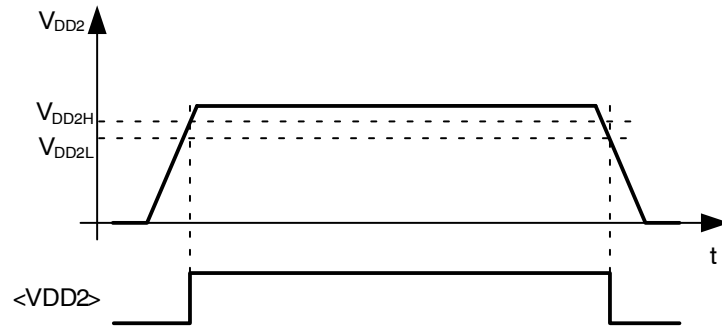
Comments:
<VDD2> is an internal signal which can be verified with the System State Service.

Figure 5. VDD2 Undervoltage Threshold

Comments:
<V20V> is an internal signal which can be verified with the System State Service.
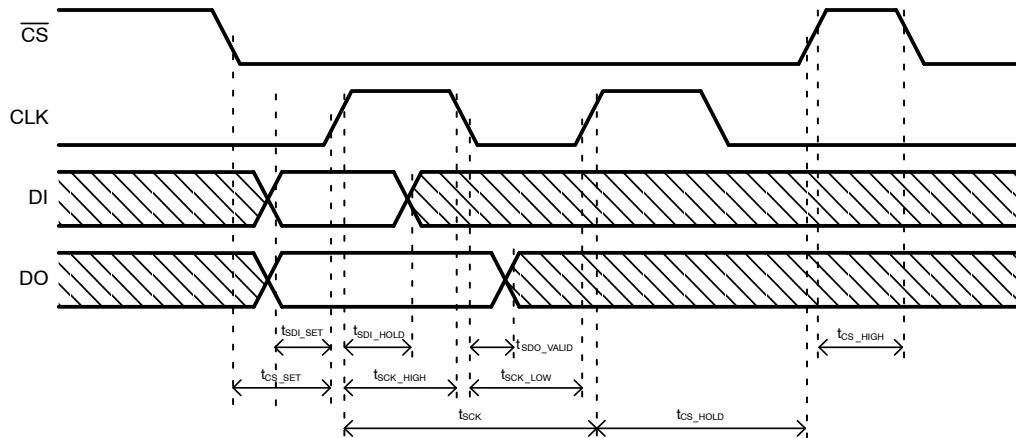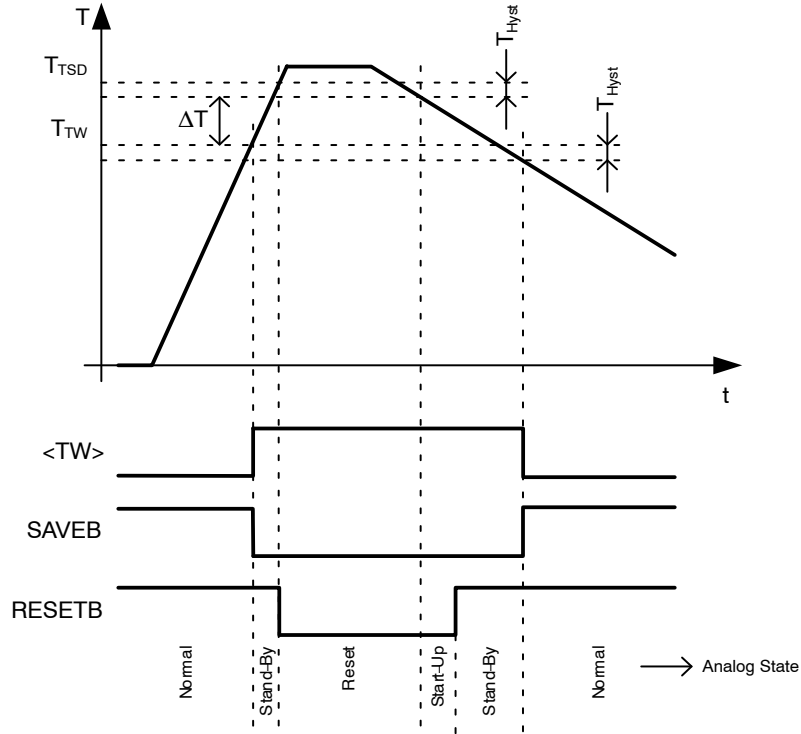
Figure 6. V20V Undervoltage Threshold levels

Figure 7. SPI Bus Timing Diagram

Comments :
  – <TW> is an internal signal which can be verified with the System State Service.
  – No SPI/ UART communication possible when RESETB is low!
  – It's assumed all voltage supplies are within their operating condition.

Figure 8. Temperature Monitoring Levels
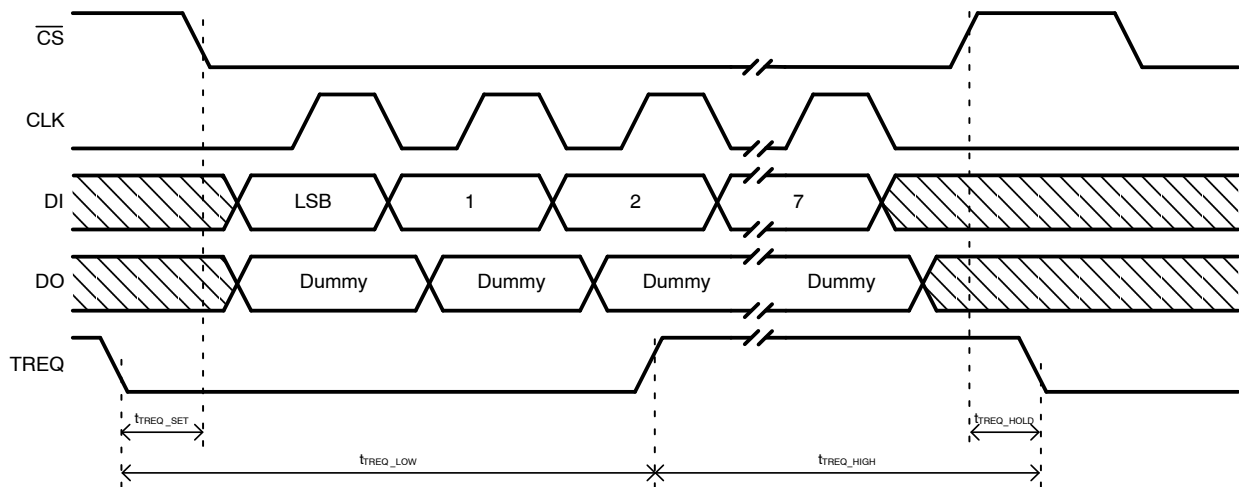
Figure 9. TREQ Timing Diagram
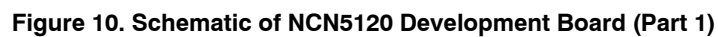
NCN51205GEVB

APPLICATION SCHEMATIC

Figure 10. Schematic of NCN5120 Development Board (Part 1)

APPLICATION SCHEMATIC
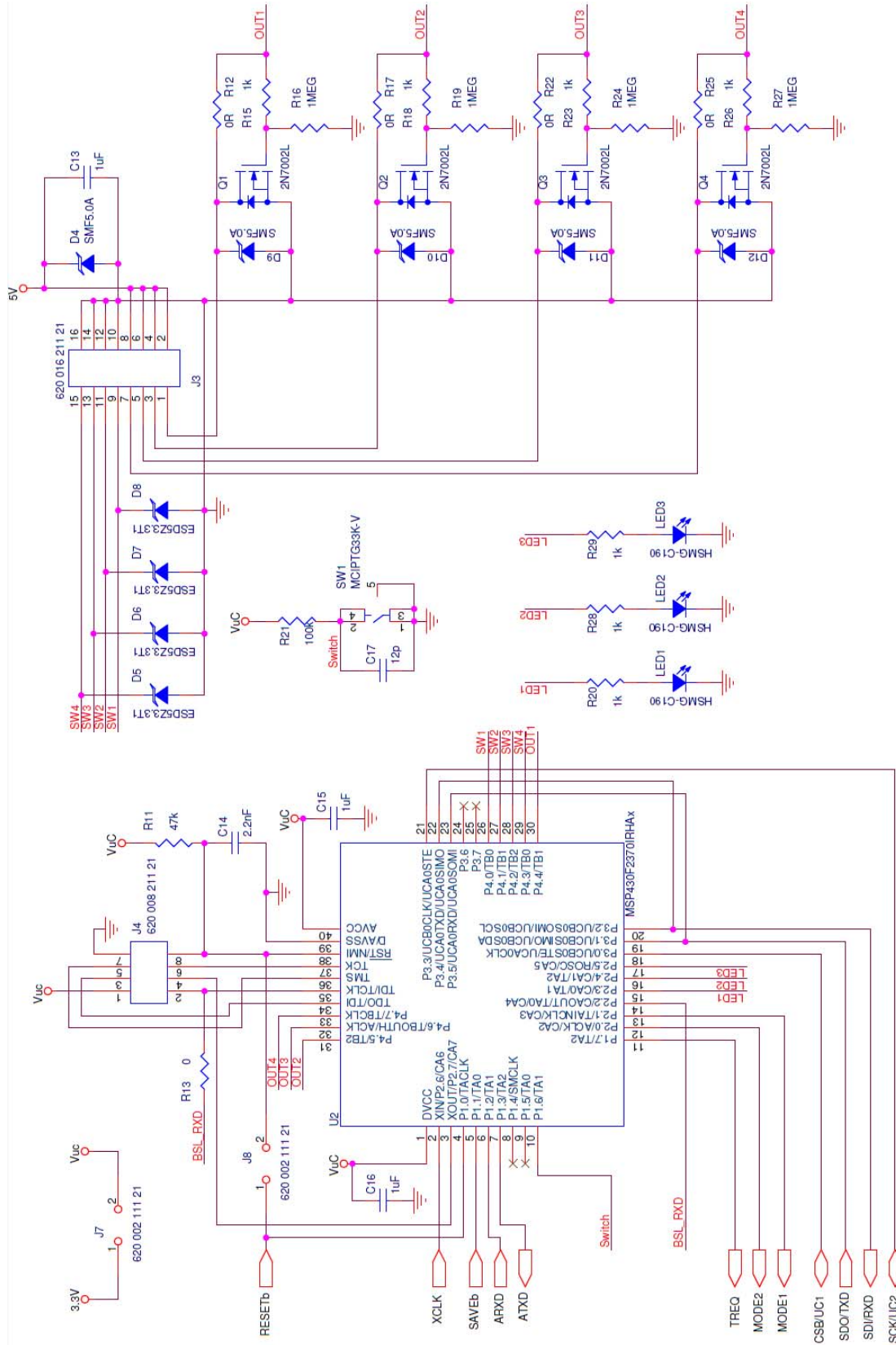
Figure 11. Schematic of NCN5120 Development Board (Part 2)
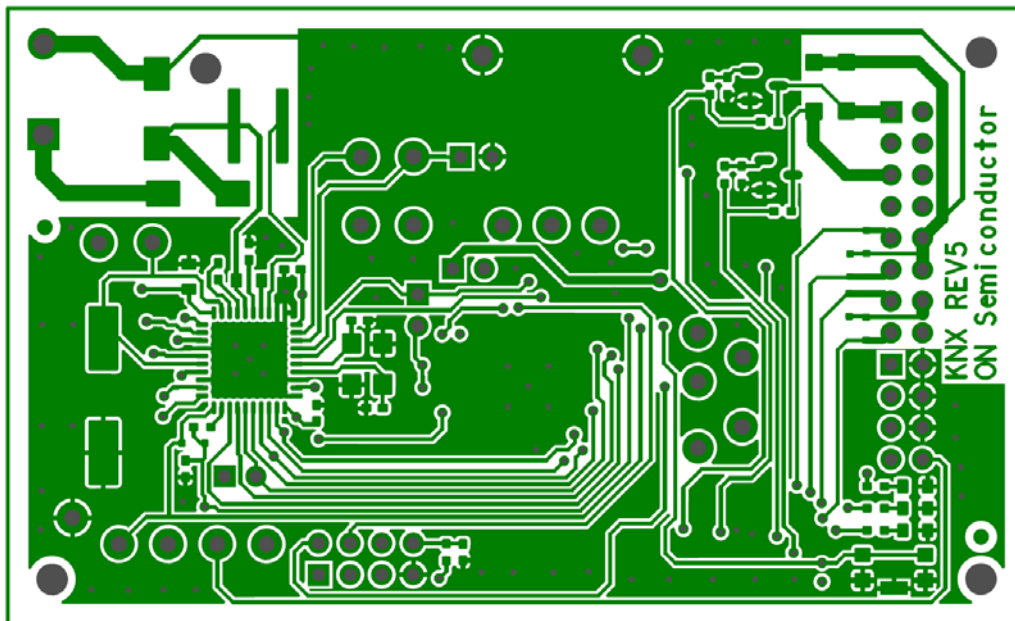
Figure 12. Top Layer of NCN5120 Development Board
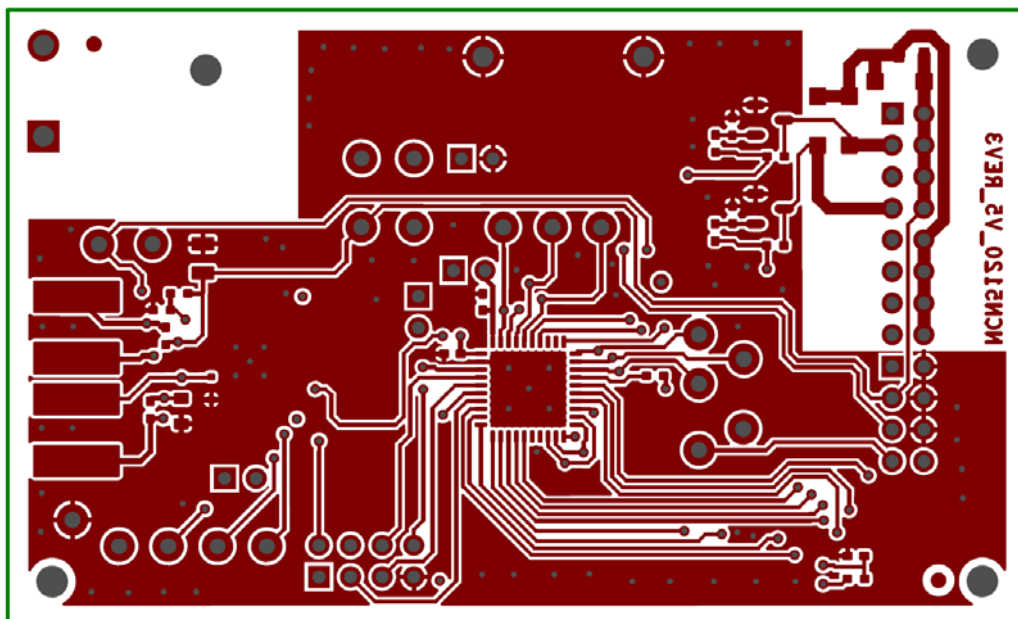
Figure 13. Bottom Layer of NCN5120 Development Board
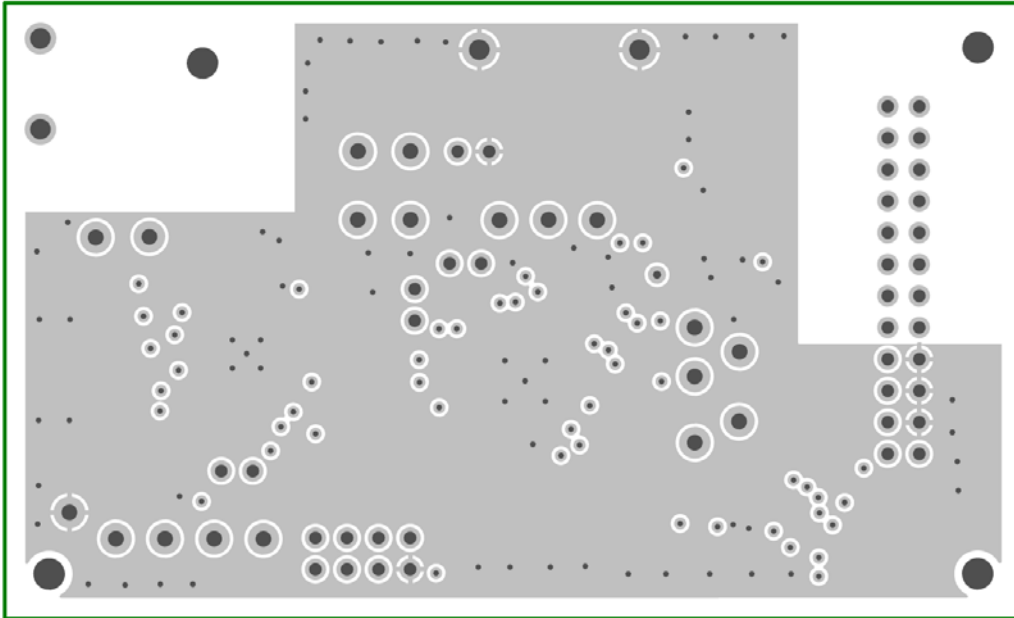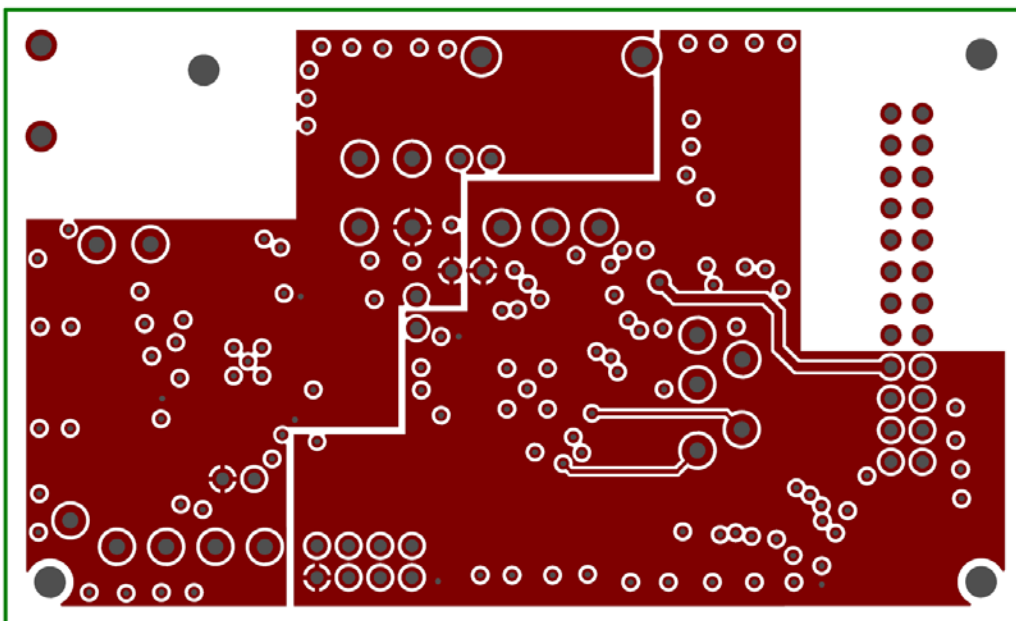
Figure 14. Inner Layer 1 of NCN5120 Development Board

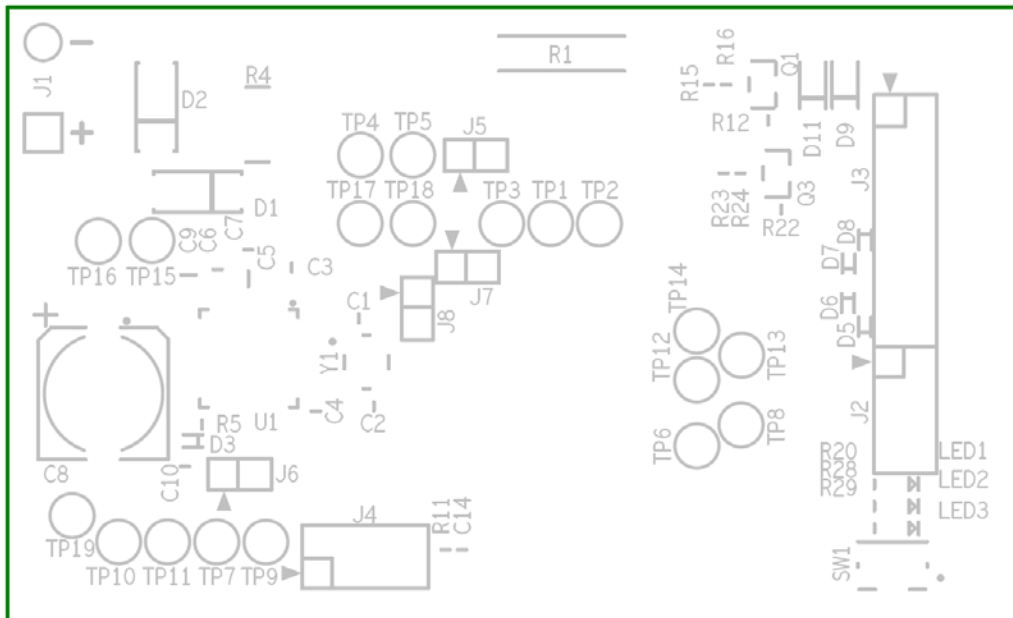Figure 15. Inner Layer 2 of NCN5120 Development Board

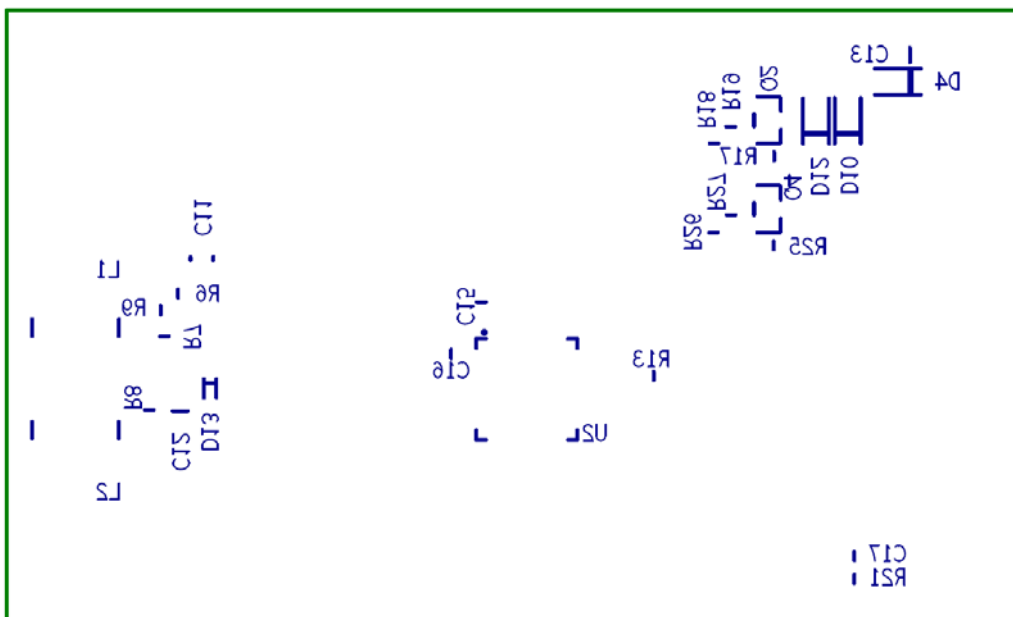**Figure 16. Top Silkscreen of NCN5120 Development Board**

Figure 17. Bottom Silkscreen of NCN5120 Development Board

NCN51205GEVB

Table 5. BILL OF MATERIALS (Note 1)

Reference	Part Number	Value	Voltage	Power	Tol	Type	Manufacturer	Footprint
CON1	243-211						Wago	NA
C1, C2	C1005COG1H100D	10 pF	6.3 V		±5%	Ceramic Multilayer	TDK	0402
C3, C4, C7	C1005X5R0J104M	100 nF	6.3 V		±20%	Ceramic Multilayer	TDK	0402
C5	C1608X5R1H473M	47 nF	50 V		±20%	Ceramic Multilayer	TDK	0603
C6	C1005X5R1H472K	4.7 nF	50 V		±10%	Ceramic Multilayer	TDK	0402
C8	B41145A7107M000	100 µF	35 V		±20%	Aluminum Electrolytic	Epcos	8 × 10
C9	C1608X5R1H105K	1 µF	35 V		±10%	Ceramic Multilayer	TDK	0603
C10 (Note 2)	C1005COG1H100D	10 pF	6.3 V		±5%	Ceramic Multilayer	TDK	0402
C11	C2012X5R1E106M	10 µF	25 V		±20%	Ceramic Multilayer	TDK	0805
C12	C1608X5R0J106M	10 µF	6.3 V		±20%	Ceramic Multilayer	TDK	0603
C13	C1608X5R1H105M	1 µF	50 V		±20%	Ceramic Multilayer	TDK	0603
C14 (Note 2)	C1005X5R1H222K	2.2 nF	6.3 V		±10%	Ceramic Multilayer	TDK	0402
C15, C16	C1005X5R0J105M	1 µF	6.3 V		±20%	Ceramic Multilayer	TDK	0402
C17	C1005C0G1H120J	12 pF	6.3 V		±5%	Ceramic Multilayer	TDK	0402
D1	SS16T3G						ON Semiconductor	SMA
D2	1SMA40AT3G						ON Semiconductor	SMA
D3, D13 (Note 2)	NSR0520V2T1G						ON Semiconductor	SOD-523
D4, D9, D10, D11, D12	SMF5.0AT1G						ON Semiconductor	SOD-123FL
D5, D6, D7, D8	ESD5Z3.3T1G						ON Semiconductor	SOD-523
J1	RT−01T−1.0B(LF)						JST	5.75 mm pitch
J2 (Note 2)	620 008 211 21						Wurth Elektronik	2 mm pitch
J3	620 016 211 21						Wurth Elektronik	2 mm pitch
J4	620 008 211 21						Wurth Elektronik	2 mm pitch
J5, J6, J7, J8	620 002 111 21						Wurth Elektronik	2 mm pitch
L1, L2	DA54NP−221K	220 µH			±10%		Coils Electronic	See Datasheet
LED1, LED2, LED3	HSMG−C190						Avago Technologies	1.6 × 0.8
Q1, Q2, Q3, Q4	2N7002L						ON Semiconductor	SOT-23
R1	D3082F05						Harwin	See datasheet
R4	RC1218JK−xx22RL	22 Ω		1 W	±10%	Thick Film	Yageo	1218
R5	RC0402JR−xx0RL	0 Ω		0.0625 W	NA	Thick Film	Yageo	0402
R6	RC0402JR−xx33KL	33 kΩ		0.0625 W	±5%	Thick Film	Yageo	0402
R7, R8	RC0402JR−xx1RL	1 Ω		0.0625 W	±5%	Thick Film	Yageo	0402
R9	RC0402JR−xx180KL	180 kΩ		0.0625 W	±5%	Thick Film	Yageo	0402
R11 (Note 2)	RC0402JR−xx47KL	47 kΩ		0.0625 W	±5%	Thick Film	Yageo	0402
R12, R17, R22, R25 (Note 2)	RC0402JR−xx0RL	0 R		0.0625 W	NA	Thick Film	Yageo	0402
R13 (Note 2)	RC0402JR−xx0RL	0 R		0.0625 W	NA	Thick Film	Yageo	0402
R15, R18, R23, R26	RC0402JR−xx1KL	1 kΩ		0.0625 W	±5%	Thick Film	Yageo	0402
R16, R19, R24, R27	RC0402JR−xx1ML	1 MΩ		0.0625 W	±5%	Thick Film	Yageo	0402

1. All devices are Pb-Free.
2. Not mounted.

Table 5. BILL OF MATERIALS (continued)(Note 1)

Reference	Part Number	Value	Voltage	Power	Tol	Type	Manufacturer	Footprint
R20, R28, R29	RC0402JR–xx1KL	1 kΩ		0.0625 W	±5%	Thick Film	Yageo	0402
R21	RC0402JR–xx100KL	100 kΩ		0.0625 W	±5%	Thick Film	Yageo	0402
SW1	MCIPTG33K–V						Multicomp	See Datasheet
TP1 … TP19	20–2137						Vero	1.02 mm
U1	NCN5120						ON Semiconductor	QFN-40
U2	MSP430F2370IRHAx						Texas Instruments	VQFN-40
Y1	FA-238, 16 MHz, 50 ppm, 10 pF						Epson Toyocom	3.2 × 2.5

1. All devices are Pb-Free.
2. Not mounted.

NCN51205GEVB

FUNCTIONAL DESCRIPTION

Because the NCN5120 Development Board contains the NCN5120 KNX Transceiver (KNX Certified) no details on KNX will be given in this document. Detailed information on the Certified KNX Transceiver NCN5120 can be found in the NCN5120 datasheet (www.onsemi.com). Detailed information on the KNX Bus can be found on the KNX website and in the KNX standards (www.knx.org).

KNX Bus Connection

Connection to the KNX bus is done by means of J1. A standard Wago connector (type 243−211) can be used for this (see Figure 18). A reverse protection diode (D1, Figure 11) is foreseen (mandatory) as also a Transient Voltage Suppressor (D2, Figure 11).

Figure 18. KNX Bus Connector

Adjustable DC−DC Converter

NCN5120 provides the power for the complete reference design. It has also a second power supply which can be used to drive external loads. The voltage is programmable between 3.3V and 21V by means of an external resistor divider (R6 and R9, see Figure 11). The voltage divider can be calculated as next:

$$R_6 = \frac{R_9 \times R_{VDD2M}}{R_9 + R_{VDD2M}} \times \frac{V_{DD2} - 3.3}{3.3} \qquad (eq. 1)$$

R_{VDD2M} is between 60 kΩ and 140 kΩ (typical 100 kΩ). The DC value of the KNX bus should be higher than V_{DD2}. Be aware that when changing the V_{DD2} voltage, D9 … D12 (see Figure 11) need to be replaced. Check the SMFxxA product family for possible replacements (www.onsemi.com).

Although V_{DD2} is capable of delivering 100 mA, the maximum current capability will not always be usable. One needs to make sure that the KNX bus power consumption stays within the KNX specification. The maximum allowed current for V_{DD2} can be calculated as next:

$$V_{BUS} \times I_{BUS} \geq 2 \times \left[0.033 + \left(V_{DD2} \times I_{DD2} \right) \right] \qquad (eq. 2)$$

I_{BUS} is limited by NCN5120. If J5 is open, I_{BUS} can maximum be 12.5 mA. If J5 is shorted, I_{BUS} can maximum be 25 mA. I_{BUS} will however also be limited by the KNX standard. Minimum V_{BUS} is 20 V (see KNX standard).

Above formula gives only an estimation and will mainly depend on the firmware loaded on the microcontroller (U2, see Figure 11). One must always verify that the KNX bus loading is in line with the KNX Specification under all operating conditions!

Xtal Oscillator

A crystal of 16 MHz (Y1, see Figure 11) is foreseen on the development board. This clock signal is also supplied to the microcontroller. See the NCN5120 datasheet (www.onsemi.com) for more details on this signal.

RESETB and SAVEB

The KNX transceiver NCN5120 controls the reset state of the microcontroller by means of the RESETB signal. An additional signal SAVEB can be monitored by the microcontroller to detect possible issues. See NCN5120 datasheet for more details on these two signals.

Voltage Supervisors

NCN5120 has different voltage supervisors. Please check the NCN5120 datasheet for more details.

Temperature Monitor

NCN5120 produces an over-temperature warning (TW) and a thermal shutdown warning (TSD). Please check the NCN5120 datasheet for more details.

External IO

The development board has the possibility to monitor up to 8 inputs (pin 1, 3, 5, 7, 9, 11, 13 and 15 of J3) and control up to 4 outputs (pin 1, 3, 5 and 7 of J3). Notice that 4 of the inputs are shared with 4 of the outputs (pin 1, 3, 5 and 7 of J3). By default the board has 4 inputs (pin 9, 11, 13 and 15 of J3) and 4 outputs (pin 1, 3, 5 and 7 of J3). To use the additional 4 inputs, Q1 … Q4 need to be removed and R12, R17, R22 and R25 need to be mounted. The input pins are 3.3 V compliant and ESD protected (D5 … D8, Figure 11). J3 is connected in such a way that an easy connection between the input and ground is possible (pin 9, 11, 13 and 15 of J3). The microcontroller (U2, see Figure 11) should be configured with an internal pull-up (see microcontroller datasheet on how to do this).

The external outputs are driven by means of low-side drivers (Q1 … Q4, see Figure 11). A gate resistor is foreseen for slope control (R15, R18, R23 and R26 of Figure 11). J3 is routed in such a way that the load can easily be connected between the output (low-side driver) and V_{DD2}. Q1 … Q4 can be used over the complete V_{DD2} voltage range. ESD diodes D9 … D12 need to be replaced if V_{DD2} is increased (see also Adjustable DC-DC Converter).

Push Button and LED's

One push button (SW1) and 3 LED's (LED1 … LED3) are foreseen on the reference design. These are freely usable.

Jumpers

Several jumpers are located on the board (J5 ... J8). J5 can be used to set the Fan-In. Mount the jumper for the highest Fan-In setting.

J6 is required when one wants to force NCN5120 in Analog Mode (make sure microcontroller is in reset to avoid conflicts!).

J7 can be used to disconnect the microcontroller from the fixed DC/DC converter of NCN5120. Be aware that if the microcontroller is not powered, NCN5120 could start powering the microcontroller over the IO-pins. It's advised to always short J7.

J8 can be used to disconnect the RESETB-signal from the RST-pin of the microcontroller.

Microcontroller Debug Interface

J4 is the microcontroller debug interface. See the microcontroller datasheet for more info on how to use this interface.

Interface Mode

The device can communicate with the host controller by means of a UART interface or an SPI interface. The selection of the interface is done by the pins MODE1, MODE2, TREQ, SCK/UC2 and CSB/UC1 which are connected to the microcontroller (see Figure 11). More details on the different interfaces can be found back in Table 6 and the NCN5120 datasheet.

Digital Description

The implementation of the Data Link Layer as specified in the KNX standard is divided in two parts. All functions related to communication with the Physical Layer and most of the Data Link Layer services are inside NCN5120, the rest of the functions and the upper communication layers are implemented into the microcontroller (see Figure 11 and Figure 19).

The host controller is responsible for handling:

- Checksum
- Parity
- Addressing
- Length

The NCN5120 is responsible for handling:

- Checksum
- Parity
- Acknowledge
- Repetition
- Timing

Services

All services can be found back in the NCN5120 datasheet (www.onsemi.com).

Firmware

No special firmware is provided with the development board. There will be some basic firmware flashed on the microcontroller (U2, Figure 11) but this is only used to verify the development board before shipment. The user has the possibility to develop his own firmware but help on programming the microcontroller will not be provided my ON Semiconductor.

NCN5120 contains the physical layer and a part of the data link layer (see Figure 19). ON Semiconductor can provide a library for the microcontroller to complete the data link layer. By no means will ON Semiconductor provide any of the higher layer stacks (Network Layer, Transport Layer, …). Sufficient 3rd party companies are available which have certified higher layer stacks.

FAQs

1. *Is this development board KNX Certified?*
   No, only NCN5120 is KNX Certified. The development board may only be used for evaluation of NCN5120. It is not allowed to use the development board in a final product or to sell it as a KNX Certified product. Contact ON Semiconductor if you want to use the development board as a final product.

2. *What 3rd party companies do you recommend for the higher layer stacks?*
   ON Semiconductor does not recommend any 3rd party company in particular. Several 3rd party companies have KNX Certified stacks and it's always advised to use one of these stacks. Some companies have experience with NCN5120. Contact ON Semiconductor for more information.

3. *Can we freely reuse the schematic and layout of this development board?*
   It is allowed to reuse the schematic, components and layout of the NCN5120 development board for your own application. Because the operating conditions of your design are not known by ON Semiconductor, one must always fully verify the design even if it's based on this development board. Contact ON Semiconductor if additional information is required.

4. *Can we request ON Semiconductor to supply the higher layer stacks?*
   By no means will ON Semiconductor provide any higher layer stacks. Certified higher layer stacks can be provided by 3rd party companies (see also Firmware).

5. *How much load can the outputs drive?*
   The maximum allow load can be calculated with the formula as given in Adjustable DC-DC Converter (page x13). I_{DD2} defines the maximum load the outputs can drive in total.

6. *What is the usage of ARXD and ATXD (Figure 11)?*
These pins have no meaning and cannot be used.

7. *I've tried all possible R6 and R9 combinations but I'm not capable of setting V_{DD2} above 6 V. How does this come?*
As can be seen in Figure 10, V_{DD2} (5 V) is connected to an ESD protection diode (D14). This is a 5 V ESD protection diode. Whenever one tries to set V_{DD2} above 5 V, this ESD diode will trigger and limit the V_{DD2} voltage to about 6 V.
This issue can be solved by, or removing D14 (in an ESD safe area this should not be an issue), or by replacing this 5 V ESD diode with a higher voltage version (see the SMFxxA datasheet for other versions (www.onsemi.com)).

8. *Is it possible to test all interfaces (UART, SPI, Analog Mode) with KNX REV5?*
Yes, the KNX REV5 board can be used with all possible interfaces. One has to be careful however when using the Analog Mode. In the Analog Mode the digital of NCN5120 is bypassed. If the microcontroller would force the RXD−pin (pin 29) of NCN5120 low, NCN5120 would pull the KNX bus low which could lead to issues.

9. *Is it possible to bypass the microcontroller on the KNX REV5 board and connect NCN5120 directly with our microcontroller board?*
Although the board is not designed for this, this is possible. One could connect NCN5120 directly to your microcontroller board by soldering some wires on the KNX REV5 board. It is however advised to remove the microcontroller from the KNX REV5 board or to put the microcontroller in reset (short pins 8 and 7 of J4 (see Figure 10)).
In case one wants to use the UART interface (9-bit UART, 19 200 bps) or Analog Mode, one could even use connector J2. The KNX_TXD and KNX_RXD give a direct connection to the TXD- and RXD-pin of NCN5120. Because the MODE1-, MODE2- and TREQ-pin have an internal pull down, one does not even need to connect these pins for UART mode. For Analog Mode one can use J6 to make the TREQ-pin high.

10. *I'm trying to sink more than 13 mA from the KNX bus with KNX REV5 but I'm having issues with the voltage regulators whenever I'm going above 16 mA. What could be the issue?*
To be able to take more than 13 mA from the KNX bus one needs to pull the FANIN/WAKE−pin of NCN5120 low. This can be done by shorting J5 (add jumper).
See NCN5120 datasheet for more info on the FANIN/WAKE−pin.

Table 6. INTERFACE SELECTION

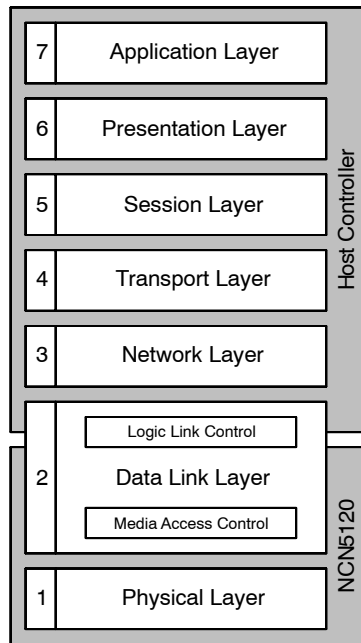| TREQ	MODE2	MODE1	SCK/UC2	SCB/UC1	SDI/RXD	SDO/TXD	Description
0	0	0	0	0	RXD	TXD	9-bit UART-Mode, 19,200 bps
0	0	0	0	1			9-bit UART-Mode, 38,400 bps
0	0	0	1	0			8-bit UART-Mode, 19,200 bps
0	0	0	1	1			8-bit UART-Mode, 38,400 bps
1	0	0	X	X	Driver	Receiver	Analog Mode
TREQ	0	1	SCK (out)	CSB (out)	SDI	SDO	SPI Master, 125 kbps
TREQ	1	0					SPI Master, 500 kbps

NOTE: X = Don't Care

Figure 19. OSI Model Reference

NCN51205GEVB

BOARD DIMENSIONS
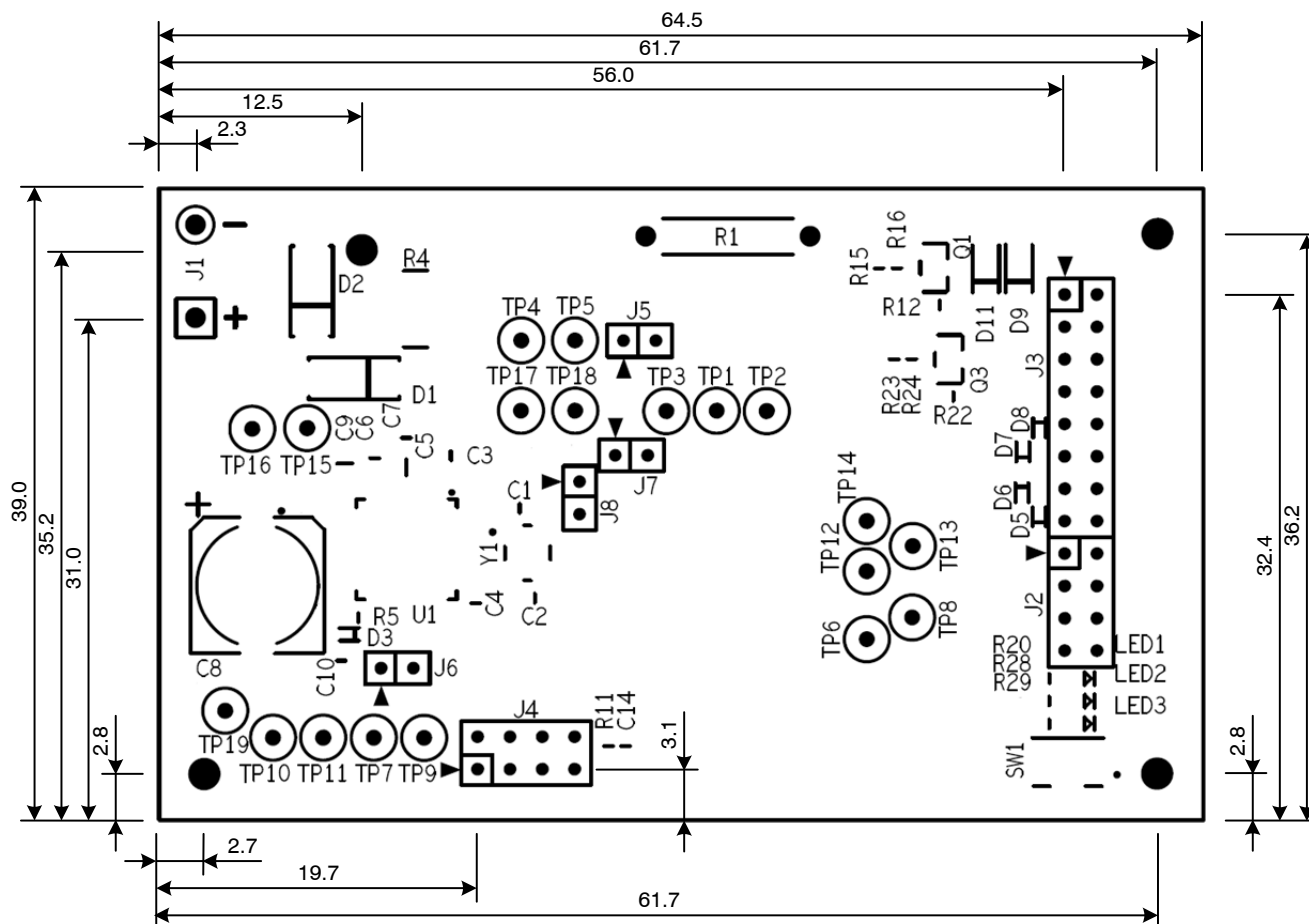
−Above dimensions are in mm
−Height C8 = 11 mm
−Height J1 = 7 mm (pins only)
−Height J2, J3, J4 = 6 mm
−Height L1 and L2 (bottom side of PCB) = 4.8 mm

The product described herein may be covered by one or more US patents pending.

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«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

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