2ED020I12FA

Dual IGBT Driver IC
SP001054678

1 Overview

Main Features

- Dual channel isolated IGBT Driver
- For 600V/1200V IGBTs
- 2 A rail-to-rail output
- Vcesat-detection
- Active Miller Clamp

Product Highlights

- Coreless transformer isolated driver
- Basic insulation according to DIN EN 60747-5-2
- Basic insulation recognized under UL 1577
- Integrated protection features
- Suitable for operation at high ambient temperature
- AEC Qualified

Typical Application

- Drive inverters for HEV and EV
- Auxiliary inverters for HEV and EV
- High Power DC/DC inverters

Description

The 2ED020I12FA is a galvanic isolated dual channel IGBT driver in PG-DSO-36 package (32 pins) that provides two fully independent driver outputs with a current capability of typically 2A.

All logic pins are 5V CMOS compatible and could be directly connected to a microcontroller.
The data transfer across galvanic isolation is realized by the integrated Coreless Transformer Technology.
The 2ED020I12FA provides several protection features like IGBT desaturation protection, active Miller clamping and active shut down.

Type	Package	Marking
2ED020I12FA	PG-DSO-36	2ED020I12FA

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2 Block Diagram

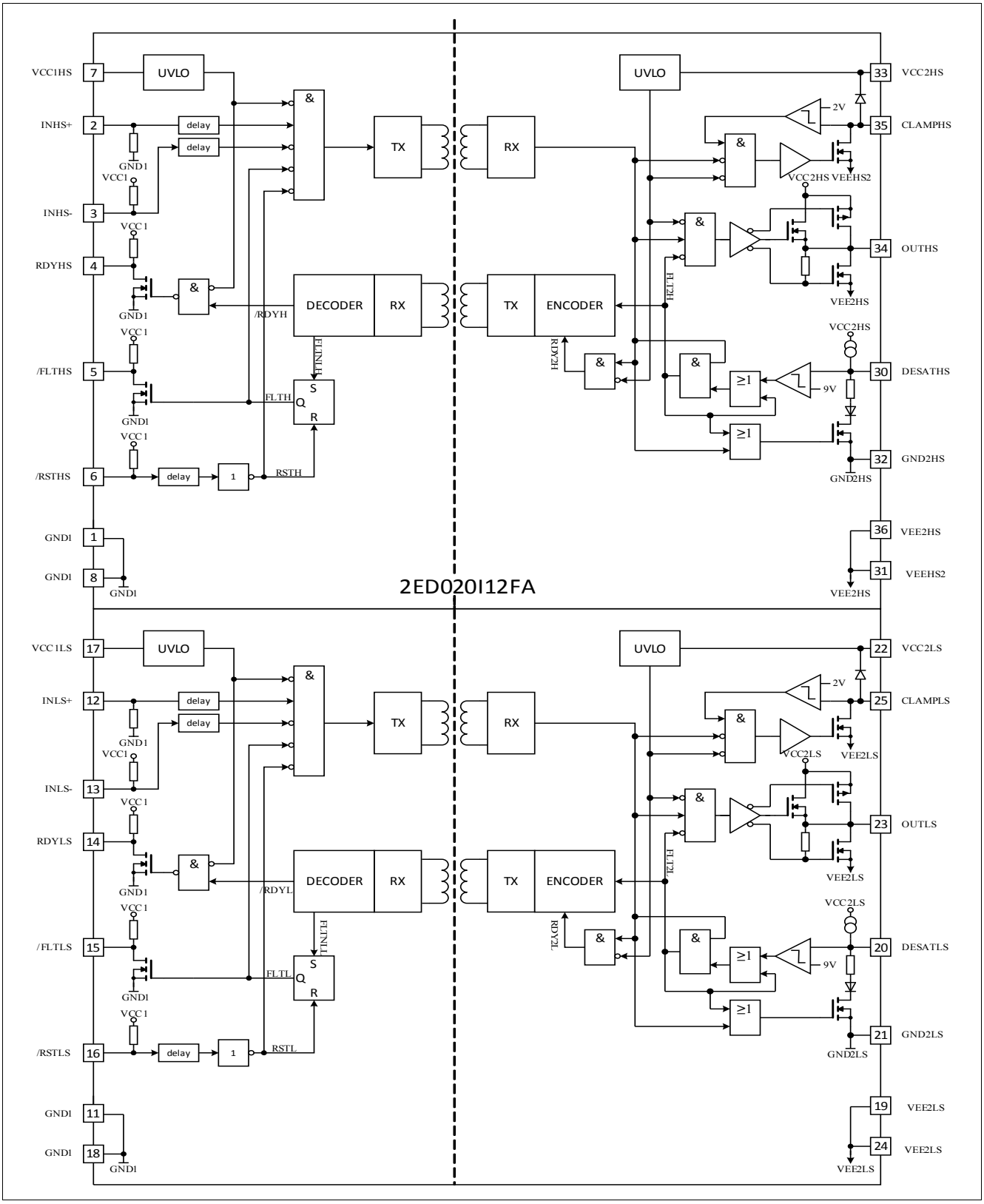


Figure 1 Block Diagram 2ED020I12FA

3 Pin Configuration and Functionality

3.1 Pin Configuration

Table 1 Pin Configuration

Pin No.	Name	Function
1	GND1	Common ground input side
2	INHS+	Non inverted driver input high side
3	INHS-	Inverted driver input high side
4	RDYHS	Ready output high side
5	/FLTHS	Inverted fault output high side
6	/RSTHS	Inverted reset input high side
7	VCC1HS	Positive power supply input high side
8	GND1	Common ground input side
9	NC	Not used, internally connected to Pin 10
10	NC	Not used, internally connected to Pin 9
11	GND1	Common ground input side
12	INLS+	Non inverted driver input low side
13	INLS-	Inverted driver input low side
14	RDYLS	Ready output low side
15	/FLTLS	Inverted fault output low side
16	/RSTLS	Inverted reset input low side
17	VCC1LS	Positive power supply input low side
18	GND1	Common ground input side
19	VEE2LS	Negative power supply low side driver
20	DESATLS	Desaturation protection low side driver
21	GND2LS	Signal ground low side driver
22	VCC2LS	Power supply low side driver
23	OUTLS	Output low side driver
24	VEE2LS	Negative power supply low side driver
25	CLAMPLS	Miller clamping low side driver
26		Pin not existing, cut out
27		Pin not existing, cut out
28		Pin not existing, cut out
29		Pin not existing, cut out
30	DESATHS	Desaturation protection high side driver
31	VEE2HS	Negative power supply high side driver

Table 1 **Pin Configuration** (cont'd)

Pin No.	Name	Function
32	GND2HS	Signal ground high side driver
33	VCC2HS	Power supply high side driver
34	OUTHS	Output high side driver
35	CLAMPHS	Miller clamping high side driver
36	VEE2HS	Negative power supply high side driver

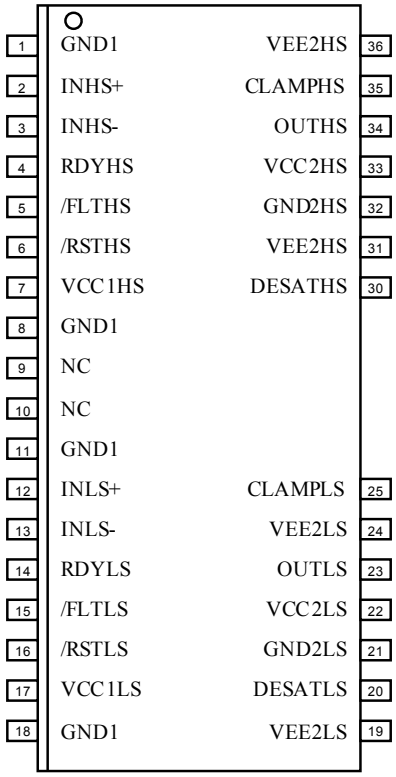


Figure 2 PG-DSO-36 (top view)

3.2 Pin Functionality

Remark: xxxHS and xxxLS at the end of pin name only indicates an order for description, both drivers are isolated and could be used as high side or low side without any preference.

GND1

Common ground connection of the input side.

INHS+, INLS+ Non Inverting Driver Input

Positive control signal for the driver output (see Figure 6).

A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal pull-down-resistor ensures IGBT off-state.

INHS–, INLS– Inverting Driver Input

Negative control signal for the driver output (see Figure 6)..

A minimum pulse width is defined to make the IC robust against glitches at INxx–. An internal pull-up-resistor ensures IGBT off-state.

/RSTHS, /RSTLS Reset Input

Function 1: Enable/shutdown of the input chip (The IGBT is off if /RSTxx = low). A minimum pulse width is defined to make the IC robust against glitches at /RSTxx.

Function 2: Resets the DESAT-FAULT-state of the chip if /RSTxx is low for a time T_{RST}. An internal pull-up-resistor is used to ensure /FLTxx status output.

/FLTHS, /FLTLS Fault Output

Open-drain output to report a desaturation error of the IGBT (/FLTxx is low if desaturation occurs).

RDYHS, RDYLS Ready Status Output

Open-drain output to report the correct operation of the device (RDYxx = high if both chips are above the UVLO level and the internal chip transmission is faultless).

VCC1HS, VCC1LS Positive Supply

5 V power supply of the input chip

VEE2HS, VEE2LS Negative Supply

Negative power supply pins of the output chip. If no negative supply voltage is available, each pins has to be connected to its respective GND2xx.

DESATHS, DESATLS Desaturation Detection Input

Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short circuits. If OUT is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

CLAMPHS, CLAMPLS Miller Clamping

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT.During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below V_{CLAMP_TH}.

GND2HS, GND2LS Reference Ground

Reference ground of the output chip.

OUTHS, OUTLS Driver Output

Output pin to drive an IGBT. The voltage is switched between VEE2xx and VCC2xx. In normal operating mode Vout is controlled by INxx+, INxx- and /RSTxx. During error mode (UVLO, internal error or DESATxx Vout is driven to VEE2xx independent of the input control signals.

VCC2HS, VCC2LS Positive Supply

Positive power supply pin of the output side.

4 Functional Description

4.1 Introduction

The 2ED020I12FA is an advanced IGBT dual gate driver that can be also used for driving power MOS devices. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated driver. The input can be directly connected to a standard 5 V DSP or microcontroller with CMOS in/output and the output driver are connected to the high side and low side switch.

The rail-to-rail driver outputs enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes IGBT desaturation protection with FAULT status outputs.

Two READY status outputs reports if the device is supplied and operates correctly.

4.2 Supply

The driver 2ED020I12FA is designed to support two different supply configurations, bipolar supply and unipolar supply.

In bipolar supply the driver is typically supplied with a positive voltage of 15V at VCC2 and a negative voltage of -8V at VEE2, please refer to Figure 3. Negative supply prevents a dynamic turn on due to the additional charge which is generated from IGBT input capacitance times negative supply voltage. If an appropriate negative supply voltage is used, connecting CLAMPxx to IGBT gate is redundant and therefore typically not necessary.

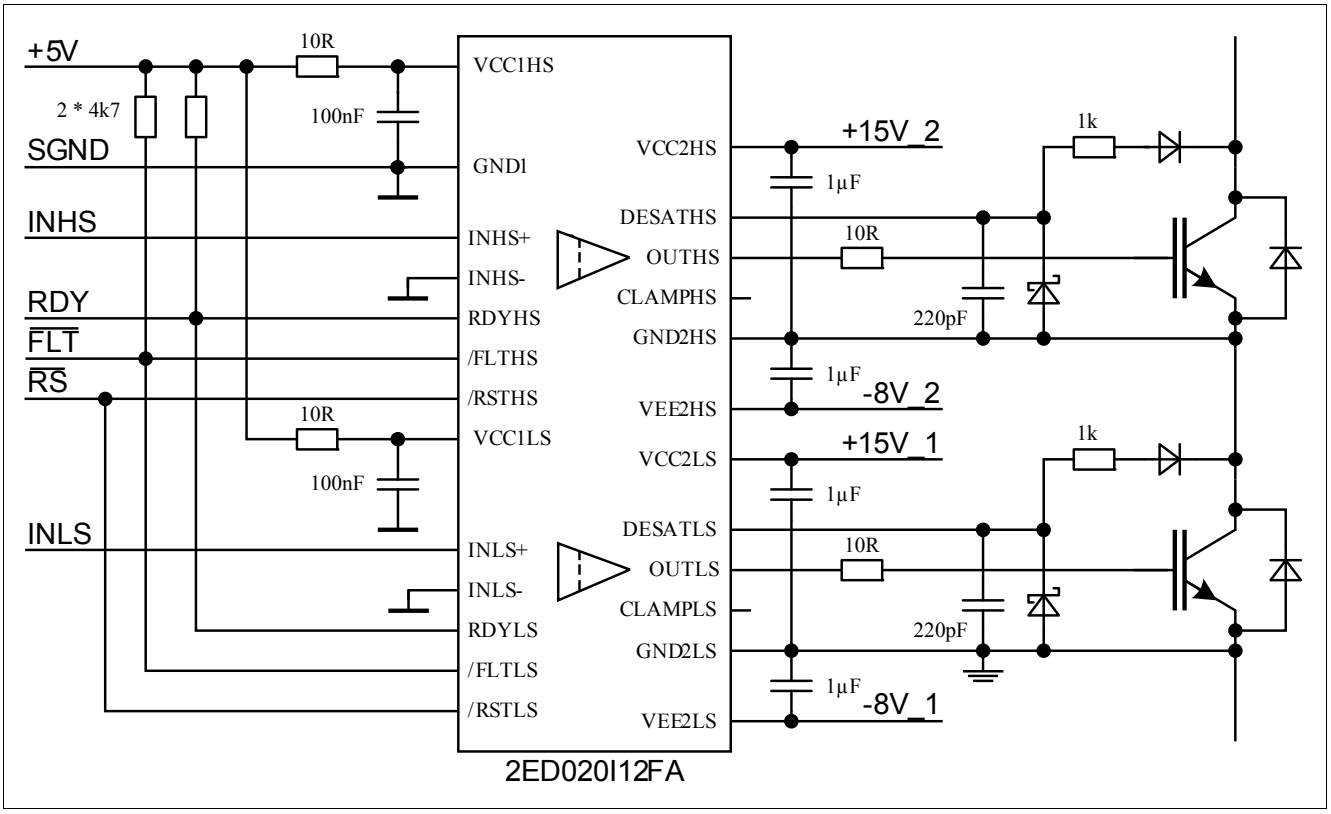


Figure 3 Application Example Bipolar Supply

For unipolar supply configuration the driver is typically supplied with a positive voltage of 15V at VCC2. Erratically dynamic turn on of the IGBT could be prevented with active Miller clamp function, so CLAMP output is directly connected to IGBT gate, please refer to Figure 4.

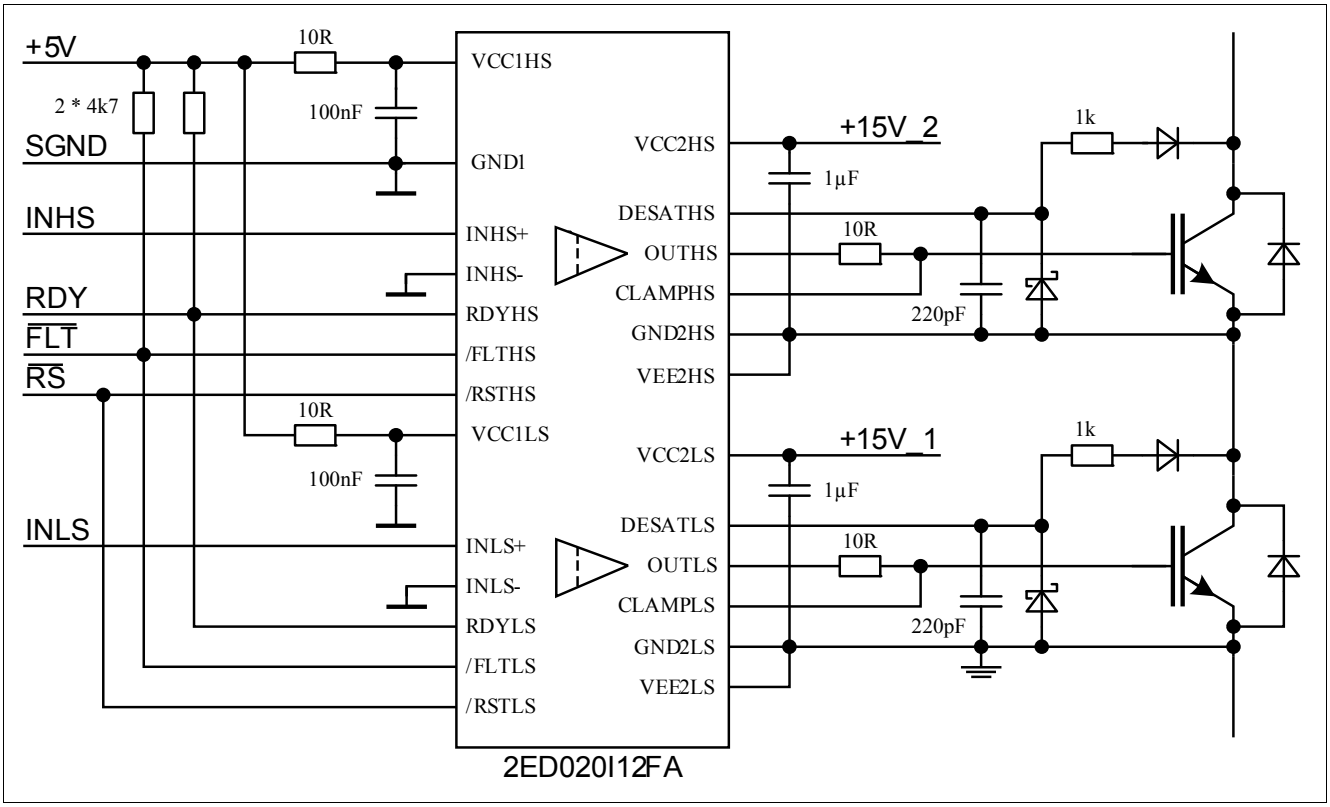


Figure 4 Application Example Unipolar Supply

4.3 Internal Protection Features

4.3.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with undervoltage lockout for all driver outputs as well as for input section, please see Figure 8.

If the power supply voltage V_{VCC1xx} of the input section drops below V_{UVLOL1} a turn-off signal is sent to the output driver before power-down. The IGBT is switched off and the signals at INxx+ and INxx- are ignored as long as V_{VCC1xx} reaches the power-up voltage V_{UVLOH1}.

If the power supply voltage V_{VCC2xx} of the output driver goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored as long as V_{VCC2xx} reaches the power-up voltage V_{UVLOH2}. VEE2xx is not monitored.

4.3.2 READY Status Output

The READY outputs shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission after a short delay

It is not necessary to reset the READY signal since its state only depends on the status of the former mentioned protection signals.

4.3.3 Watchdog Timer

During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the READY output reports an internal error.

4.3.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply, IGBT gate is clamped at OUTxx to VEE2xx.

4.4 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode INxx+ controls the driver output while INxx- is set to low. At inverting mode INxx- controls the driver output while INxx+ is set to high, please see Figure 6. A minimum input pulse width is defined to filter occasional glitches.

4.5 Driver Outputs

The output driver sections uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop, switching behavior of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

4.6 External Protection Features

4.6.1 Desaturation Protection

A desaturation protection ensures the protection of the IGBT at short circuit. When the DESAT voltage goes up and reaches $V_{DESAT\_TH,}$ the output is driven low. Further, the FAULT output is activated, please refer to Figure 7. A configurable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

4.6.2 Active Miller Clamp

In a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore in many applications, the use of a negative supply voltage can be avoided.

During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below V_{CLAMP_TH}. The clamp is designed for a Miller current up to I_{CLAMPL}.

4.6.3 Short Circuit Clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUTxx and CLAMPxx limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10 µs may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

4.7 RESET

The reset inputs have two functions.

Firstly, /RSTxx is in charge of setting back the FAULT output. If /RSTxx is low longer than a given time, /FLTxx will be cleared at the rising edge of /RSTxx; otherwise, it will remain unchanged. Moreover, it works as enable/shutdown of the input logic.

5 Electrical Parameters

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1. The specification for all driver signals is valid for HS and LS with out special notice, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS.

Table 2 Absolute Maximum Ratings [1)]

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Positive power supply output side	V_{VCC2}	-0.3	20	V	Referenced to GND2
Negative power supply output side	V_{VEE2}	-12	0.3	V	Referenced to GND2
Maximum power supply voltage output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	28	V	–
Gate driver output	V_{OUT}	V_{VEE2}-0.3	V_{VCC2}+0.3	V	–
			V_{VCC2}+ V_{CLPout}	V	time< t_{CLPmax}, I_{OUT}<500 mA (see Table 9)
Gate driver high output maximum current	I_{OUT}	–	2.4	A	t = 2 µs
Gate & Clamp driver low output maximum current	I_{OUT}	–	2.4	A	t = 2 µs
Maximum short circuit clamping time	t_{CLP}	–	10	µs	$I_{CLAMP/OUT}$ = 500 mA
Positive power supply input side	V_{VCC1}	-0.3	6.5	V	–
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	$_{VCC1}$ + 0.3	V	–
			6.5	V	–
Opendrain Logic output voltage ($\overline{FLT}$)	$V_{FLT\#}$	-0.3	6.5V	V	–
Opendrain Logic output voltage (RDY)	V_{RDY}	-0.3	6.5V	V	–
Opendrain Logic output current ($\overline{FLT}$)	$I_{FLT\#}$	–	10	mA	–
Opendrain Logic output current (RDY)	I_{RDY}	–	10	mA	–
Pin DESAT voltage	V_{DESAT}	-0.3	V_{VCC2} +0.3	V	Referenced to GND2

Table 2 Absolute Maximum Ratings (cont'd)[1)]

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Pin CLAMP voltage	V_{CLAMP}	V_{VEE2}-0.3	V_{VCC2}+0.3	V	–
		V_{VEE2}-0.3	V_{VCC2}+ $V_{CLPclamp}$	V	time< t_{CLPmax}, I_{CLAMP}<500 mA (see Table 9)
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_S	-55	150	°C	–
Power dissipation, per input part	$P_{D, IN}$	–	100	mW	2) @T_A = 25°C
Power dissipation, per output part	$P_{D, OUT}$	–	400	mW	2) @T_A = 25°C
Power dissipation, total	$P_{D, tot}$	–	1000	mW	2) @T_A = 25°C
Thermal resistance (Input part)	$R_{THJA,IN}$	–	375	K/W	2) @T_A = 25°C, P_{D, IN_HS+LS} = 200 mW, P_{D, OUT_HS+LS} = 800 mW
Thermal resistance (Output part)	$R_{THJA,OUT}$	–	110	K/W	2) @T_A = 25°C, P_{D, IN_HS+LS} = 200 mW, P_{D, OUT_HS+LS} = 800 mW
ESD Capability	V_{ESD}	–	1	kV	Human Body Model[3)]

1) Not subject to production test. Absolute maximum Ratings are verified by design / characterization
2) IC power dissipation is derated linearly at 12 mW/°C above 65°C. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.
3) According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

5.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1. The specification for all driver signals is valid for HS and LS with out special notice, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS.

Table 3 Operating Parameters

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Positive power supply output side	V_{VCC2}	13	20	V	referenced to GND2
Negative power supply output side	V_{VEE2}	-12	0	V	referenced to GND2
Maximum power supply voltage output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	28	V	–
Positive power supply input side	V_{VCC1}	4.5	5.5	V	–
Pin CLAMP voltage	V_{CLAMP}	V_{VEE2}	V_{VCC2}	V	referenced to GND2
Pin DESAT voltage	V_{DESAT}	0	V_{VCC2}	V	referenced to GND2
Ambient temperature	T_A	-40	125	°C	–
Common mode transient immunity	$\|DV_{ISO}/dt\|$	–	50	kV/µs	@ 500 V, [1)]

1) The parameter is not subject to production test - verified by design/characterization

5.3 Recommended Operating Parameters

Note: Unless otherwise noted all parameters refer to GND1. The specification for all driver signals is valid for HS and LS with out special notice, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS.

Table 4 Recommended Operating Parameters

Parameter	Symbol	Value	Unit	Note / Test Condition
Positive power supply output side	V_{VCC2}	15	V	referenced to GND2
Negative power supply output side	V_{VEE2}	-8	V	referenced to GND2
Positive power supply input side	V_{VCC1}	5	V	referenced to GND1

5.4 Electrical Characteristics

Note: The electrical characteristics involve the spread of values for the supply voltages, load and junction temperatures given below. Typical values represent the median values, which are related to production processes at T = 25°C. Unless otherwise noted all voltages are given with respect to GND. The specification for all driver signals is valid for HS and LS with out special notice, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS.

5.4.1 Voltage Supply

Table 5 Voltage Supply

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
UVLO Threshold Input Chip	V_{UVLOH1}	–	4.1	4.3	V	–
	V_{UVLOL1}	3.5	3.8	–	V	–
UVLO Hysteresis Input Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	0.15	–	–	V	–
UVLO Threshold Output Chip	V_{UVLOH2}	–	12.0	12.6	V	–
	V_{UVLOL2}	10.4	11.0	–	V	–
UVLO Hysteresis Output Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS2}	0.7	0.9	–	V	–
Quiescent Current Input Chip	I_{Q1}	–	7	9	mA	V_{VCC1} = 5 V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High
Quiescent Current Output Chip	I_{Q2}	–	4	6	mA	V_{VCC2} = 15 V V_{VEE2} = -8 V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High

5.4.2 Logic Input and Output

Table 6 Logic Input and Output

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
IN+,IN-, $\overline{\text{RST}}$ Low Input Voltage	V_{IN+L}, V_{IN-L}, $V_{RSTL\#}$	0	–	1.5	V	–
IN+,IN-, $\overline{\text{RST}}$ High Input Voltage	V_{IN+H}, V_{IN-H}, $V_{RSTH\#}$	3.5	–	V_{VCC1}	V	–
IN-, $\overline{\text{RST}}$ Input Current	I_{IN-}, $I_{RST\#}$	–	100	400	µA	V_{IN-} = GND1 $V_{RST\#}$ = GND1
IN+ Input Current	I_{IN+},	–	100	400	µA	V_{IN+} = VCC1
RDY,$\overline{\text{FLT}}$ Pull Up Current	I_{PRDY}, $I_{PFLT\#}$	–	100	400	µA	V_{RDY} = GND1 $V_{FLT\#}$ = GND1
Input Pulse Suppression IN+, IN-	T_{MININ+}, T_{MININ-}	30	40	–	ns	
Input Pulse Suppression $\overline{\text{RST}}$for ENABLE/SHUTDOWN	T_{MINRST}	30	40	–	ns	–
Pulse Width $\overline{\text{RST}}$ for Resetting $\overline{\text{FLT}}$	T_{RST}	800	–	–	ns	–
$\overline{\text{FLT}}$ Low Voltage	V_{FLTL}	–	–	300	mV	$I_{SINK(FLT\#)}$ = 5 mA
RDY Low Voltage	V_{RDYL}	–	–	300	mV	$I_{SINK(RDY)}$ = 5 mA

5.4.3 Gate Driver

Table 7 Gate Driver

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
High Level Output Voltage	V_{OUTH1}	V_{CC2} -1.2	V_{CC2} -0.8	–	V	I_{OUTH} = -20 mA
	V_{OUTH2}	V_{CC2} -2.5	V_{CC2} -2.0	–	V	I_{OUTH} = -200 mA
	V_{OUTH3}	V_{CC2} -9	V_{CC2} -5	–	V	I_{OUTH} = -1 A
	V_{OUTH4}		V_{CC2} -10	–	V	I_{OUTH} = -2 A [1]
High Level Output Peak Current	I_{OUTH}	-1.5	-2.0	–	A	IN+ = High, IN- = Low; OUT = High
Low Level Output Voltage	V_{OUTL1}	–	V_{VEE2} +0.04	V_{VEE2}+0.09	V	I_{OUTL} = 20 mA
	V_{OUTL2}	–	V_{VEE2} +0.3	V_{VEE2}+0.85	V	I_{OUTL} = 200 mA
	V_{OUTL3}	–	V_{VEE2} +2.1	V_{VEE2}+5	V	I_{OUTL} = 1 A
	V_{OUTL4}	–	V_{VEE2} +7	–	V	I_{OUTL} = 2 A[1]
Low Level Output Peak Current	I_{OUTL}	1.5	2.0	–	A	IN+ = Low, IN- = Low; OUT = Low, V_{VCC2} = 15 V, V_{VEE2} = -8 V

1) Not subject to production test. Absolute maximum Ratings are verified by design / characterization

5.4.4 Active Miller Clamp

Table 8 Active Miller Clamp

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Low Level Clamp Voltage	$V_{CLAMPL1}$	–	V_{VEE2}+0.03	V_{VEE2} +0.08	V	I_{CLAMP} = 20 mA
	$V_{CLAMPL2}$	–	V_{VEE2}+0.3	V_{VEE2} +0.8	V	I_{CLAMP} = 200 mA
	$V_{CLAMPL3}$	–	V_{VEE2}+1.9	V_{VEE2} +4.8	V	I_{CLAMP} = 1 A
Low Level Clamp Current	I_{CLAMPL}	2	–	–	A	[1]
Clamp Threshold Voltage	V_{CLAMP_TH}	1.6	2.1	2.4	V	Related to VEE2

1) The parameter is not subject to production test - verified by design/characterization

5.4.5 Short Circuit Clamping

Table 9 Short Circuit Clamping

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Clamping voltage (OUT) (V_{OUT} - V_{VCC2})	V_{CLPout}	–	0.8	1.3	V	IN+ = High, IN- = Low, OUT = High I_{OUT} = 500 mA pulse test, t_{CLPmax} = 10 µs)
Clamping voltage (CLAMP) (V_{VCLAMP}-V_{VCC2})	$V_{CLPclamp}$	–	1.3	–	V	IN+ = High, IN- = Low, OUT = High I_{CLAMP} = 500 mA (pulse test, t_{CLPmax} = 10 µs)[1)]
		–	0.7	1.1	V	IN+ = High, IN- = Low, OUT = High I_{CLAMP} = 20 mA

1) Not subject to production test. Absolute maximum Ratings are verified by design / characterization

5.4.6 Dynamic Characteristics

Table 10 Dynamic Characteristics[1)]

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Input IN to output propagation delay ON	T_{PDON}	145	170	195	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @ 25°C
Input IN to output propagation delay OFF	T_{PDOFF}	145	165	190	ns	
Input IN to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-35	-5	25	ns	
Input IN to output propagation delay ON variation due to temp	T_{PDONt}	160	190	220	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT} = 50% @ 125°C
Input IN to output propagation delay OFF variation due to temp	T_{PDOFFt}	165	195	225	ns	
Input IN to output propagation delay distortion (T_{PDOFF} - T_{PDON})	$T_{PDISTOt}$	-25	5	35	ns	

Table 10 Dynamic Characteristics[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Input IN to output propagation delay ON variation due to temp	T_{PDONt}	135	165	195	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT} = 50% @ -40°C
Input IN to output propagation delay OFF variation due to temp	T_{PDOFFt}	125	155	185	ns	
Input IN to output propagation delay distortion (T_{PDOFF} - T_{PDON})	$T_{PDISTOt}$	-40	-10	20	ns	
Rise Time	T_{RISE}	10	30	60	ns	C_{LOAD} = 1 nF V_L 10%, V_H 90%
		200	400	800	ns	C_{LOAD} = 34 nF V_L 10%, V_H 90%
Fall Time	T_{FALL}	10	50	90	ns	C_{LOAD} = 1 nF V_L 10%, V_H 90%
		200	350	600	ns	C_{LOAD} = 34 nF V_L 10%, V_H 90%

1) Measured under the following conditions: V_{VCC1}=5V, V_{VEE2}=-8V, V_{VCC2}=15V

5.4.7 Desaturation Protection

Table 11 Desaturation Protection

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Blanking Capacitor Charge Current	I_{DESATC}	450	500	550	µA	V_{VCC2} =15 V, V_{VEE2}=- 8 V V_{DESAT} = 2 V
Blanking Capacitor Discharge Current	I_{DESATD}	9.0	14	–	mA	V_{VCC2} =15 V, V_{VEE2} = -8 V V_{DESAT} = 6 V
Desaturation Reference Level	V_{DESAT_TH}	8.3	9	9.5	V	V_{VCC2} = 15 V
Desaturation Filter Time	$T_{DESATfilter}$	–	250	–	ns	V_{VCC2} = 15 V, V_{VEE2} = -8 V V_{DESAT} = 9 V[1)]
Desaturation Sense to OUT Low Delay	$T_{DESATOUT}$	–	350	430	ns	V_{OUT} = 90% C_{LOAD} = 1 nF
Desaturation Sense to FLT Low Delay	$T_{DESATFLT}$	–	–	2.25	µs	$V_{FLT\#}$ = 10%; $I_{FLT\#}$ = 5 mA
Desaturation Low Voltage	V_{DESATL}	0.4	0.6	0.95	V	IN+ = Low, IN- = Low, OUT = Low
Leading edge blanking	$T_{DESATleb}$	–	400	–	ns	1)

1) Not subject to production test. This parameter is verified by design / characterization

5.4.8 Active Shut Down

Table 12 Active Shut Down

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Active Shut Down Voltage	V_{ACTSD}	–	–	2.0	V	I_{OUT} = -200 mA, V_{CC2} open, referenced to VEE2

6 Insulation Characteristics

Insulation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

This coupler is suitable for “basic insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.1 Certified according to DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01. Basic Insulation

Table 13 According to DIN EN 60747-5-2

Description	Symbol	Characteristics	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage ≤ 150 V_{RMS} for rated mains voltage ≤ 300 V_{RMS} for rated mains voltage ≤ 600 V_{RMS}		 I-IV I-III I-II	–
Climatic Classification		55/125/21	–
Pollution Degree (EN 60664-1)		2	–
Minimum External Clearance between input and driver section	CLR	8.2	mm
Minimum External Creepage between input and driver section	CPG	8.2	mm
Minimum External Clearance between HS- and LS-driver output		2.75	mm
Minimum External Creepage between HS- and LS-driver output		2.85	mm
Minimum Comparative Tracking Index	CTI	175	
Maximum Repetitive Insulation Voltage	V_{IORM}	1420	V_{PEAK}
Highest Allowable Overvoltage	V_{IOTM}	6000	V_{PEAK}
Maximum Surge Insulation Voltage	V_{IOSM}	6000	V

6.2 Recognized under UL 1577

Table 14 Recognized under UL 1577

Description	Symbol	Characteristics	Unit
Insulation Withstand Voltage / 1 min	V_{ISO}	3750	V_{rms}
Insulation Test Voltage / 1 s	V_{ISO}	4500	V_{rms}

6.3 Reliability

For Qualification Report please contact your local Infineon Technologies office.

7 Timing Diagrams

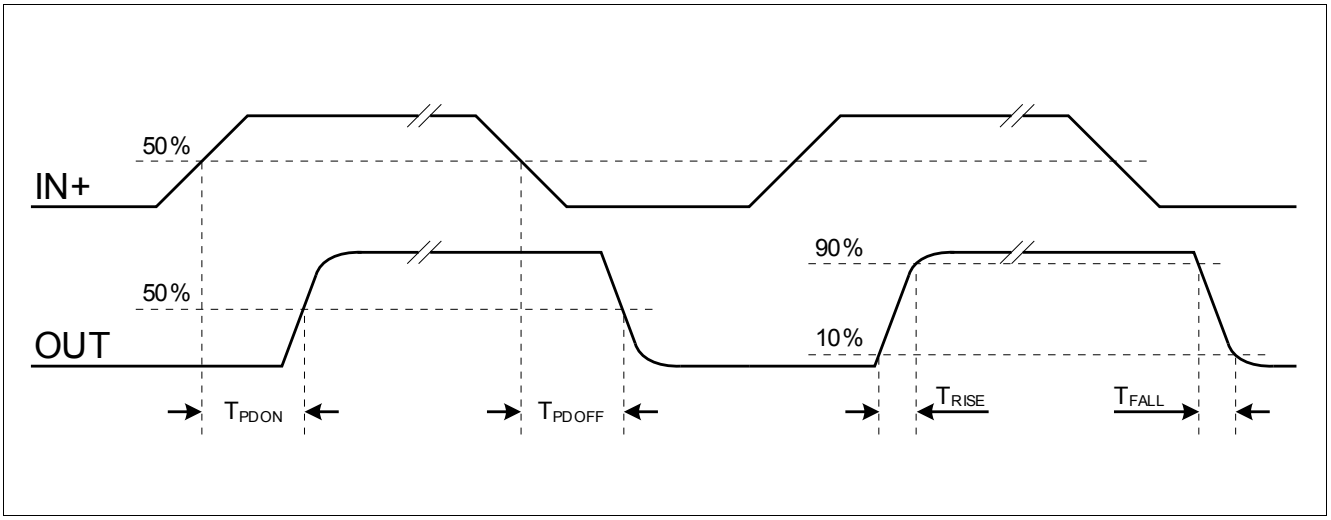


Figure 5 Propagation Delay, Rise and Fall Time

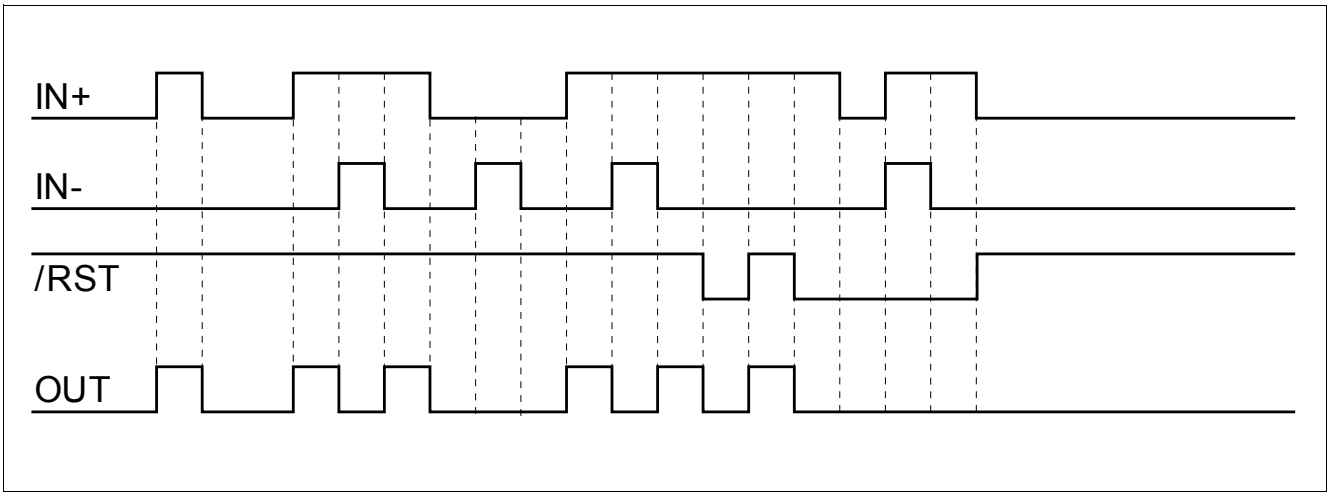


Figure 6 Typical Switching Behavior

Timing Diagrams

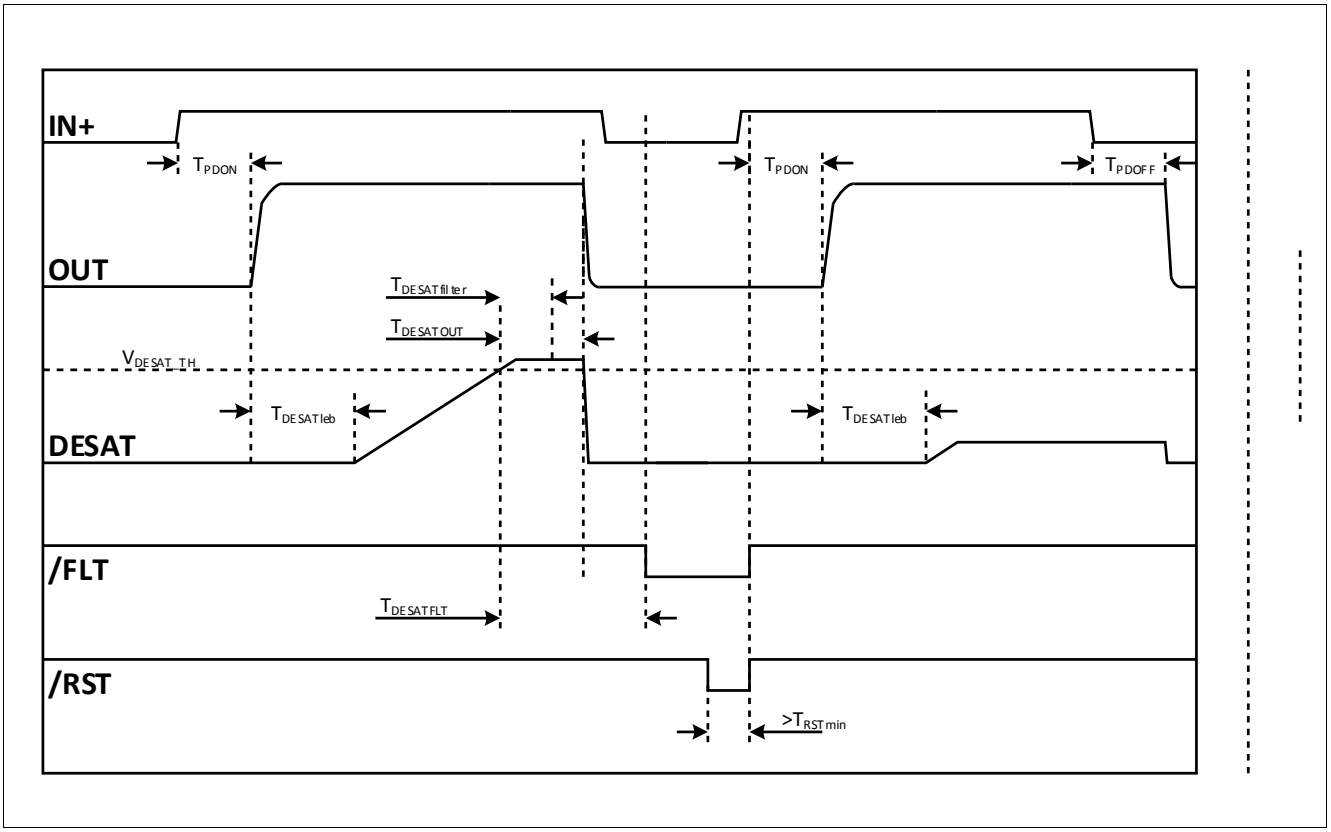


Figure 7 DESAT Switch-Off Behavior

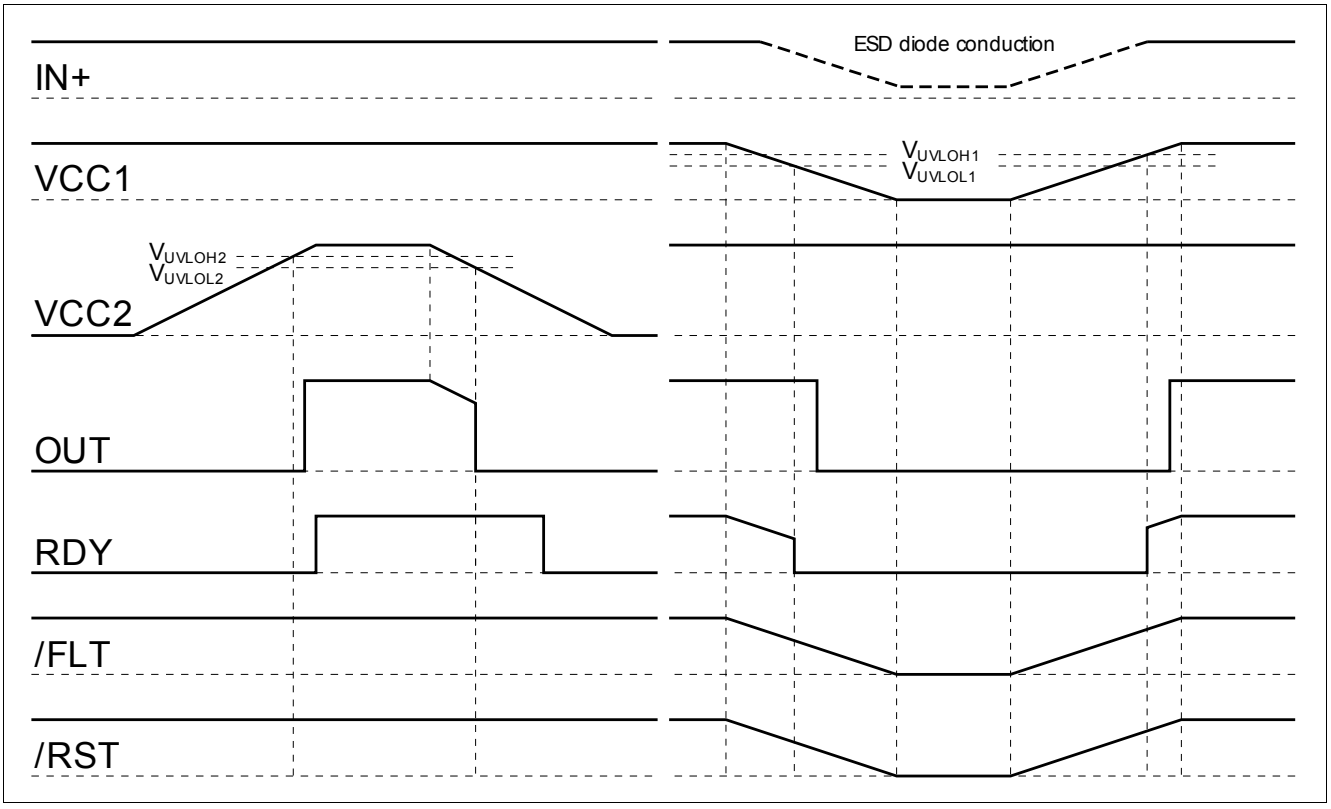
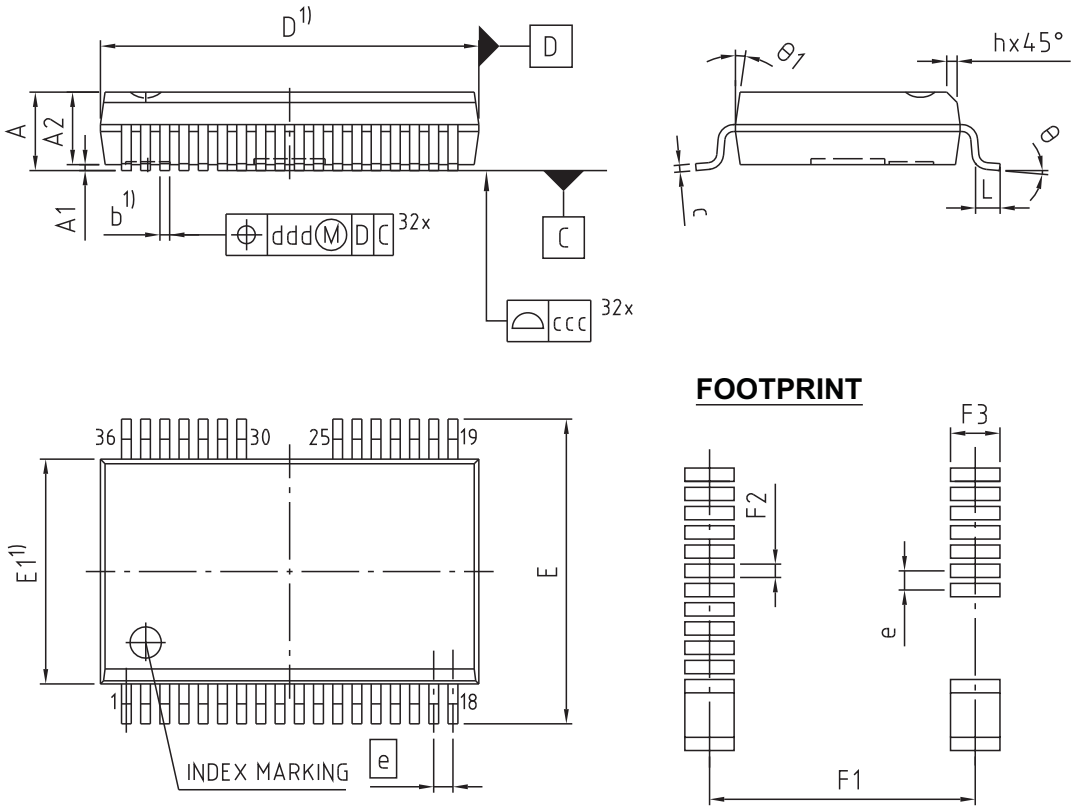


Figure 8 UVLO Behavior

8 Package Outlines



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2.65	-	0.104
A1	0.10	0.20	0.004	0.008
A2	2.25	2.45	0.089	0.096
b	0.25	0.41	0.010	0.016
c	0.23	0.32	0.009	0.013
D	12.60	12.80	0.496	0.504
E	10.00	10.60	0.394	0.417
E1	7.40	7.60	0.291	0.299
e	0.65 BSC		0.026 BSC	
N	32		32	
L	0.50	0.90	0.020	0.035
h	0.25	0.45	0.010	0.018
T	0°	8°	0°	8°
T1	0°	8°	0°	8°
ccc	0.10		0.004	
ddd	0.17		0.007	
F1	9.73		0.383	
F2	0.45		0.018	
F3	1.67		0.066	

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SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

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02

Figure 9 **PG-DSO-36** (Plastic (Green) Dual Small Outline Package)

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev 3.1, 2016-04-05	
Rev 3.0, 2015-11-27	
All	Update latest template
Page 7	Removed Figure 1 “Typical Application”.
Page 5	Updated **Figure 1**.
Page 7	Updated INHS+ and INLS+ description.
Page 8	Updated INHS- and INLS- description.
Page 14	Updated **Table 2**.
Page 16	Updated **Table 3**.
Page 18	Updated **Table 6**.
Page 19	Updated **Table 7** (added footnote).
Page 20	Updated **Table 9** (added footnote).

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