RL78/G1F

RENESAS MCU

R01DS0246EJ0110
Rev. 1.10
Aug 12, 2016

True Low Power Platform (as low as 66 µA/MHz, and 0.57 µA for RTC + LVD), 1.6 V to 5.5 V operation, 32/64 Kbyte Flash, Max.32 MHz CPU operation, Enhanced analog functions, for General Purpose Applications

# 1. OUTLINE

## 1.1 Features

Ultra-low power consumption technology

- $V_{DD}$ = single power supply voltage of 1.6 to 5.5 V which can operate a 1.8 V device at a low voltage
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 µs: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 µs: @ 32.768 kHz operation with subsystem clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 5.5 KB

Code flash memory

- Code flash memory: 32/64 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 4 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: $V_{DD}$ = 1.8 to 5.5 V

High-speed on-chip oscillator

- Select from 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% ($V_{DD}$ = 1.8 to 5.5 V, $T_A$ = -20 to +85°C)

Operating ambient temperature

- $T_A$ = –40 to +85°C (A: Consumer applications)
- $T_A$ = –40 to +105°C (G: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

Event link controller (ELC)

- Event signals of 22 types can be linked to the specified peripheral function.

Serial interfaces

- CSI: 3 to 6 channels
- UART/UART (LIN-bus supported): 3 channels
- $I^2C$/simplified $I^2C$: 3 to 6 channels
- IrDA: 1 channel

Timer

- 16-bit timer: 9 channels (Timer Array Unit (TAU): 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels (with PWMOPA), Timer RG: 1 channel, Timer RX: 1 channel)
- 12-bit interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter

- 8/10-bit resolution A/D converter ($V_{DD}$ = 1.6 to 5.5 V)
- Analog input: 8 to 17 channels
- Internal reference voltage (1.45 V) and temperature sensor

D/A converter

- 8-bit resolution D/A converter ($V_{DD}$ = 1.6 to 5.5 V)
- Analog output: 1 or 2 channels
- Output voltage: 0 V to $V_{DD}$
- Real-time output function

Comparator

- 2 channels (pin selector is provided for 1 channel)
- Incorporates a function for the output of a timer window in combination with the timer array unit.
- The external reference voltage or internal reference voltage can be selected as the reference voltage.

Programmable gain amplifier (PGA)

- 1 channel

I/O port

- I/O port: 20 to 58 (N-ch open drain I/O [withstand voltage of 6 V]: 2 to 4, N-ch open drain I/O [VDD withstand voltage/EVDD withstand voltage]: 10 to 16)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

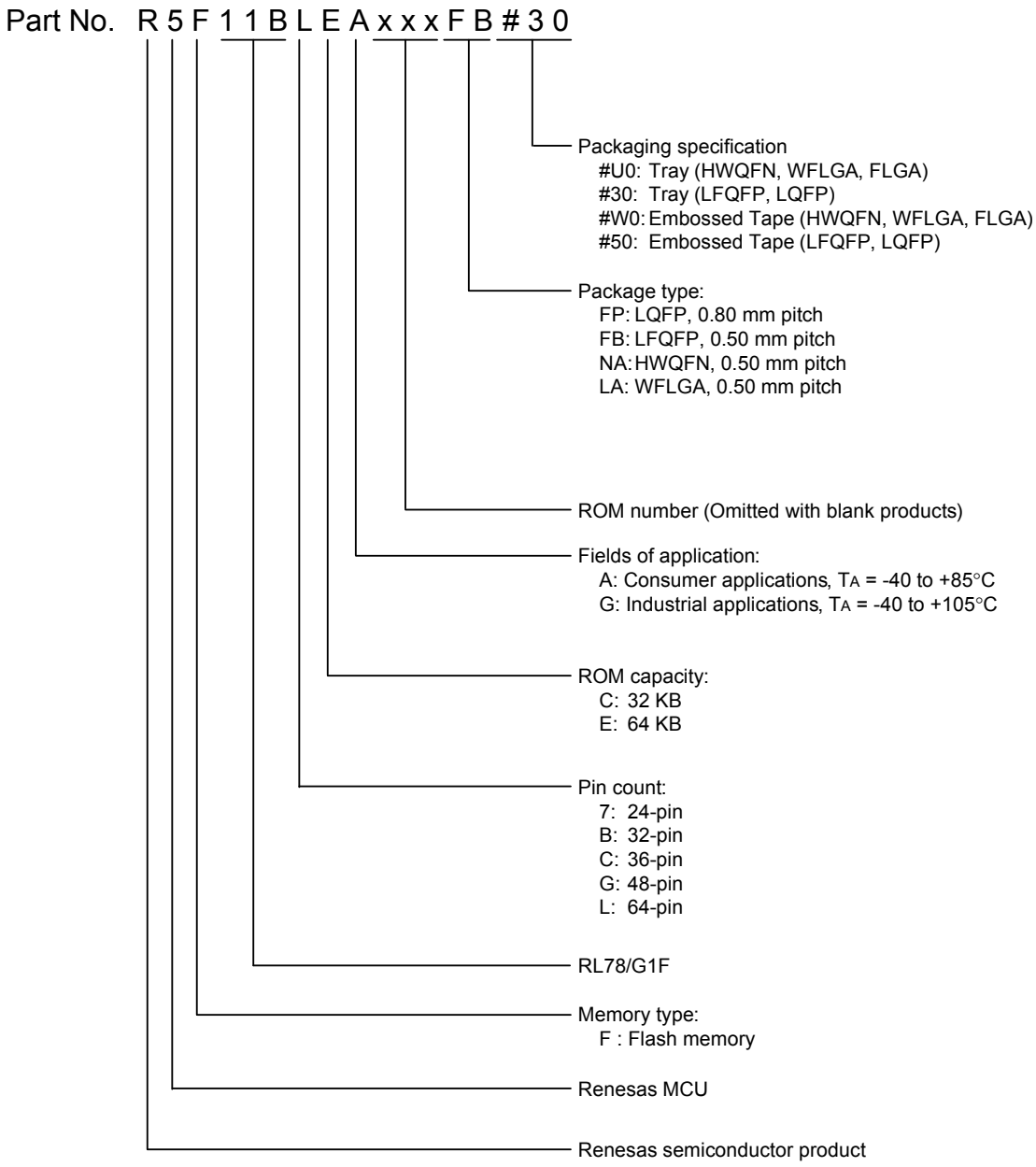
○ ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G1F | | | | |
|---|---|---|---|---|---|---|---|
| | | | 24 pins | 32 pins | 36 pins | 48 pins | 64 pins |
| 64 KB | 4 KB | 5.5 KB Note | R5F11B7E | R5F11BBE | R5F11BCE | R5F11BGE | R5F11BLE |
| 32 KB | 4 KB | 5.5 KB Note | R5F11B7C | R5F11BBC | R5F11BCC | R5F11BGC | R5F11BLC |

**Note** This is about 4.5 KB when performing self-programming and rewriting the data flash memory (For details, see **CHAPTER 3 CPU ARCHITECTURE** in the RL78/G1F User's Manual).

## 1.2 Ordering Information

**Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1F**



| Pin count | Package | Fields of Application[Note] | Ordering Part Number |
|---|---|---|---|
| 24 pins | 24-pin plastic HWQFN (4 × 4, 0.5 mm pitch) | A | R5F11B7CANA#U0, R5F11B7EANA#U0, R5F11B7CANA#W0, R5F11B7EANA#W0 |
| | | G | R5F11B7CGNA#U0, R5F11B7EGNA#U0, R5F11B7CGNA#W0, R5F11B7EGNA#W0 |
| 32 pins | 32-pin plastic LQFP (7 × 7, 0.8 mm pitch) | A | R5F11BBCAFP#30, R5F11BBEAFP#30, R5F11BBCAFP#50, R5F11BBEAFP#50 |
| | | G | R5F11BBCGFP#30, R5F11BBEGFP#30, R5F11BBCGFP#50, R5F11BBEGFP#50 |
| 36 pins | 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch) | A | R5F11BCCALA#U0, R5F11BCEALA#U0, R5F11BCCALA#W0, R5F11BCEALA#W0 |
| | | G | R5F11BCCGLA#U0, R5F11BCEGLA#U0, R5F11BCCGLA#W0, R5F11BCEGLA#W0 |
| 48 pins | 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch) | A | R5F11BGCAFB#30, R5F11BGEAFB#30, R5F11BGCAFB#50, R5F11BGEAFB#50 |
| | | G | R5F11BGCGFB#30, R5F11BGEGFB#30, R5F11BGCGFB#50, R5F11BGEGFB#50 |
| 64 pins | 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch) | A | R5F11BLCAFB#30, R5F11BLEAFB#30, R5F11BLCAFB#50, R5F11BLEAFB#50 |
| | | G | R5F11BLCGFB#30, R5F11BLEGFB#30, R5F11BLCGFB#50, R5F11BLEGFB#50 |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1F**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

## 1.3 Pin Configuration (Top View)

### 1.3.1 24-pin products

• 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

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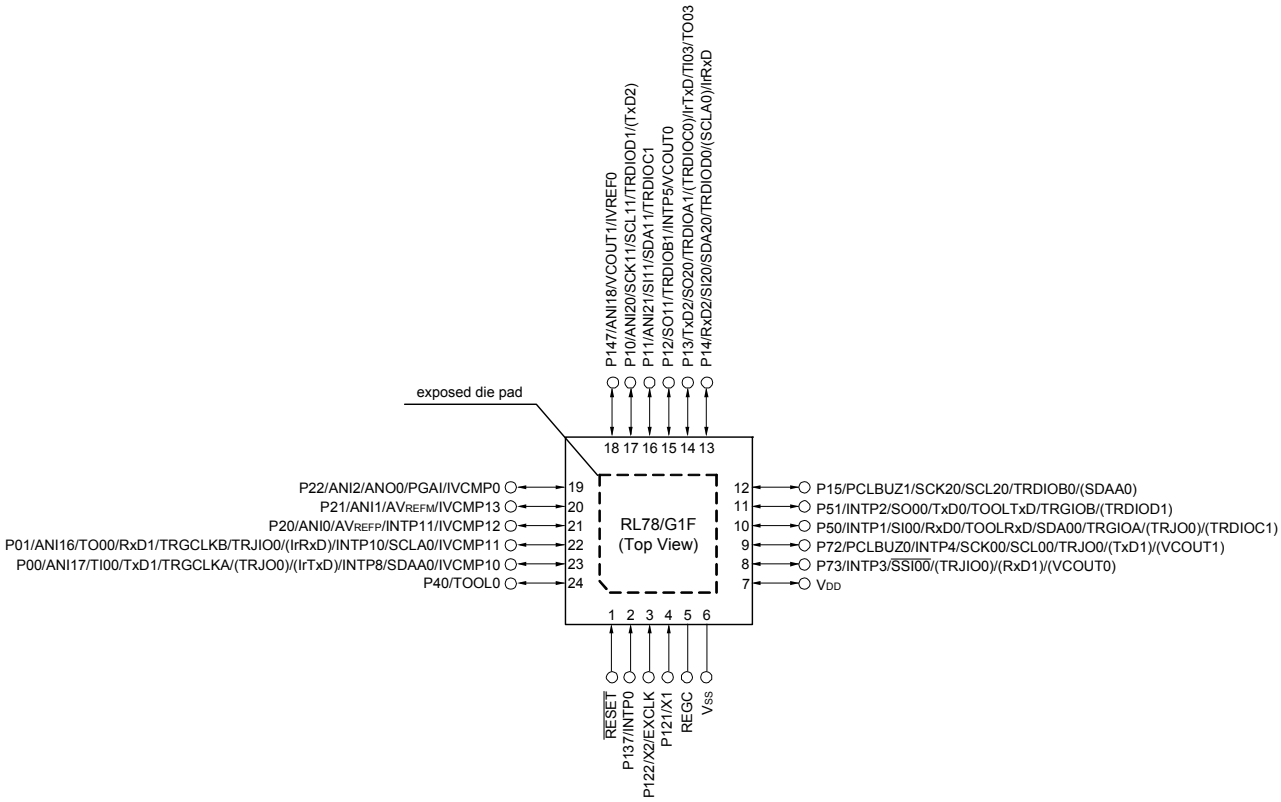


**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

### 1.3.2 32-pin products

• 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)

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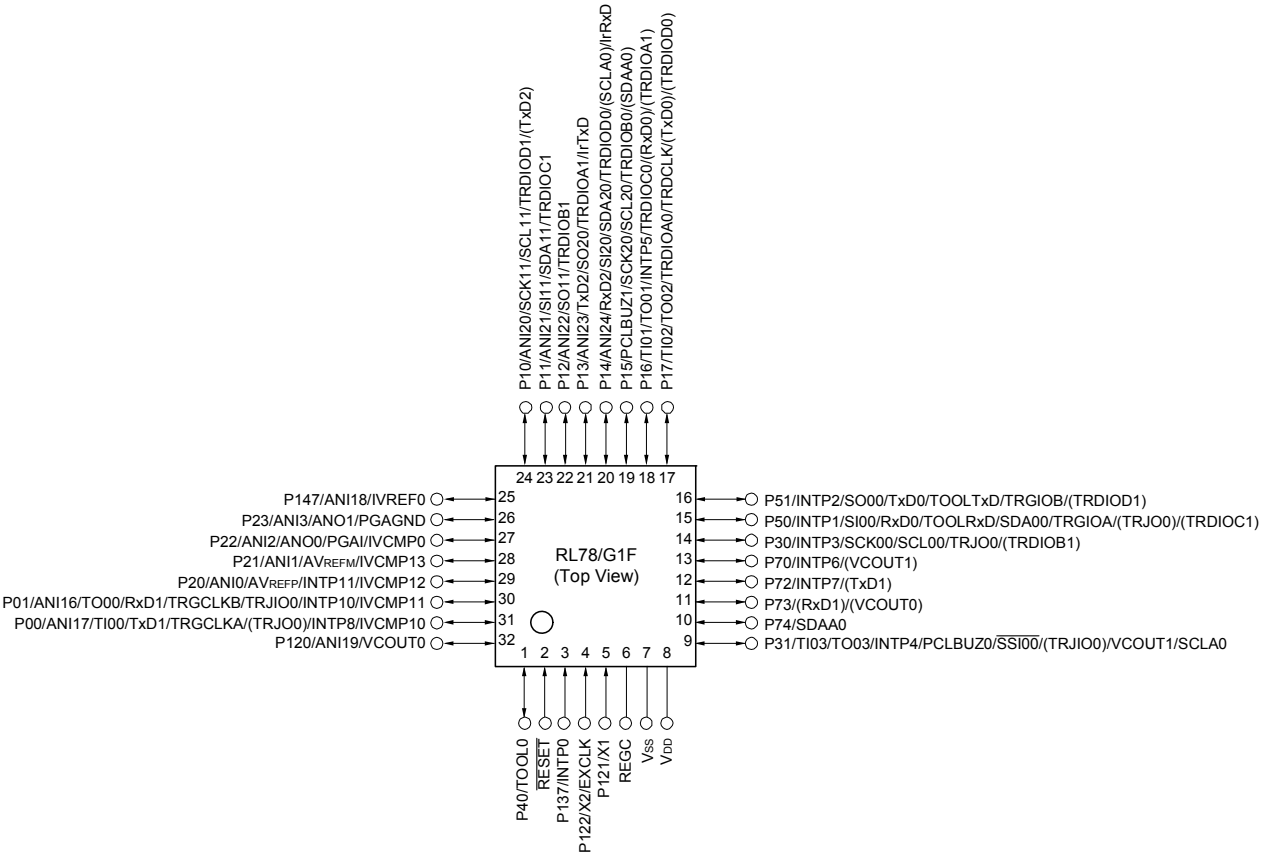


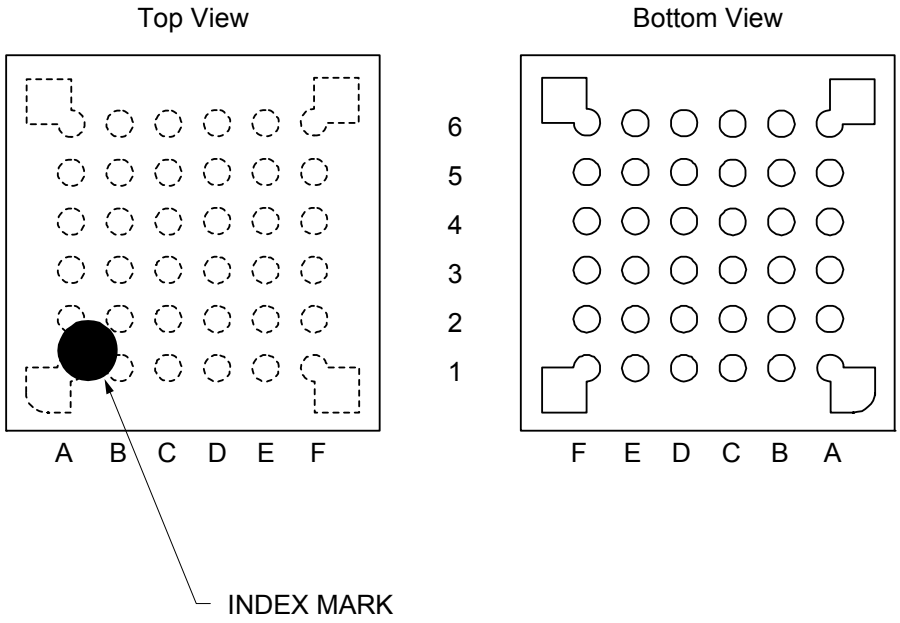

**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

### 1.3.3 36-pin products

• 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)




| | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|
| 6 | $EV_{DD0}$ | $V_{DD}$ | P121/X1 | P122/X2/EXCLK | P137/INTP0 | P40/TOOL0 | 6 |
| 5 | P61/SDAA0 | P60/SCLA0 | $V_{SS}$ | REGC | RESET | P124/XT2/ EXCLKS | 5 |
| 4 | P31/TI03/TO03/ INTP4/PCLBUZ0/ $\overline{\text{SSI00}}$/(TRJIO0)/ VCOUT1 | P14/ANI24/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0)/IrRxD | P20/ANI0/ $AV_{REFP}$/IVCMP12/ INTP11 | P21/ANI1/ $AV_{REFM}$/IVCMP13 | P01/ANI16/TO00/ RxD1/TRGCLKB/ TRJIO0/INTP10/ IVCMP11 | P123/XT1 | 4 |
| 3 | P50/INTP1/SI00/ RxD0/TOOLRxD/ SDA00/TRGIOA/ (TRJO0)/ (TRDIOC1) | P70/INTP6/ (VCOUT0)/ (VCOUT1) | P15/PCLBUZ1/ SCK20/SCL20/ TRDIOB0/ (SDAA0) | P23/ANI3/ANO1/ PGAGND | P00/ANI17/TI00/ TxD1/TRGCLKA/ (TRJO0)/INTP8/ IVCMP10 | P120/ANI19/ VCOUT0 | 3 |
| 2 | P30/INTP3/ RTC1HZ/SCK00/ SCL00/TRJO0/ (TRDIOB1) | P16/TI01/TO01/ INTP5/TRDIOC0/ (RxD0)/ (TRDIOA1) | P12/ANI22/SO11/ TRDIOB1 | P11/ANI21/SI11/ SDA11/TRDIOC1 | P24/ANI4 | P22/ANI2/ANO0/ PGAI/IVCMP0 | 2 |
| 1 | P51/INTP2/SO00/ TxD0/TOOLTxD/ TRGIOB/ (TRDIOD1) | P17/TI02/TO02/ TRDIOA0/ TRDCLK0/(TxD0)/ (TRDIOD0) | P13/ANI23/TxD2/ SO20/TRDIOA1/ IrTxD | P10/ANI20/ SCK11/SCL11/ TRDIOD1/(TxD2) | P147/ANI18/ IVREF0 | P25/ANI5 | 1 |
| | A | B | C | D | E | F | |

**Caution 1. Connect the REGC pin to $V_{SS}$ pin via a capacitor (0.47 to 1 μF).**

**Caution 2. Make $V_{DD}$ pin the potential that is higher than $EV_{DD0}$ pin.**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

**Remark 3.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins.

### 1.3.4 48-pin products

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

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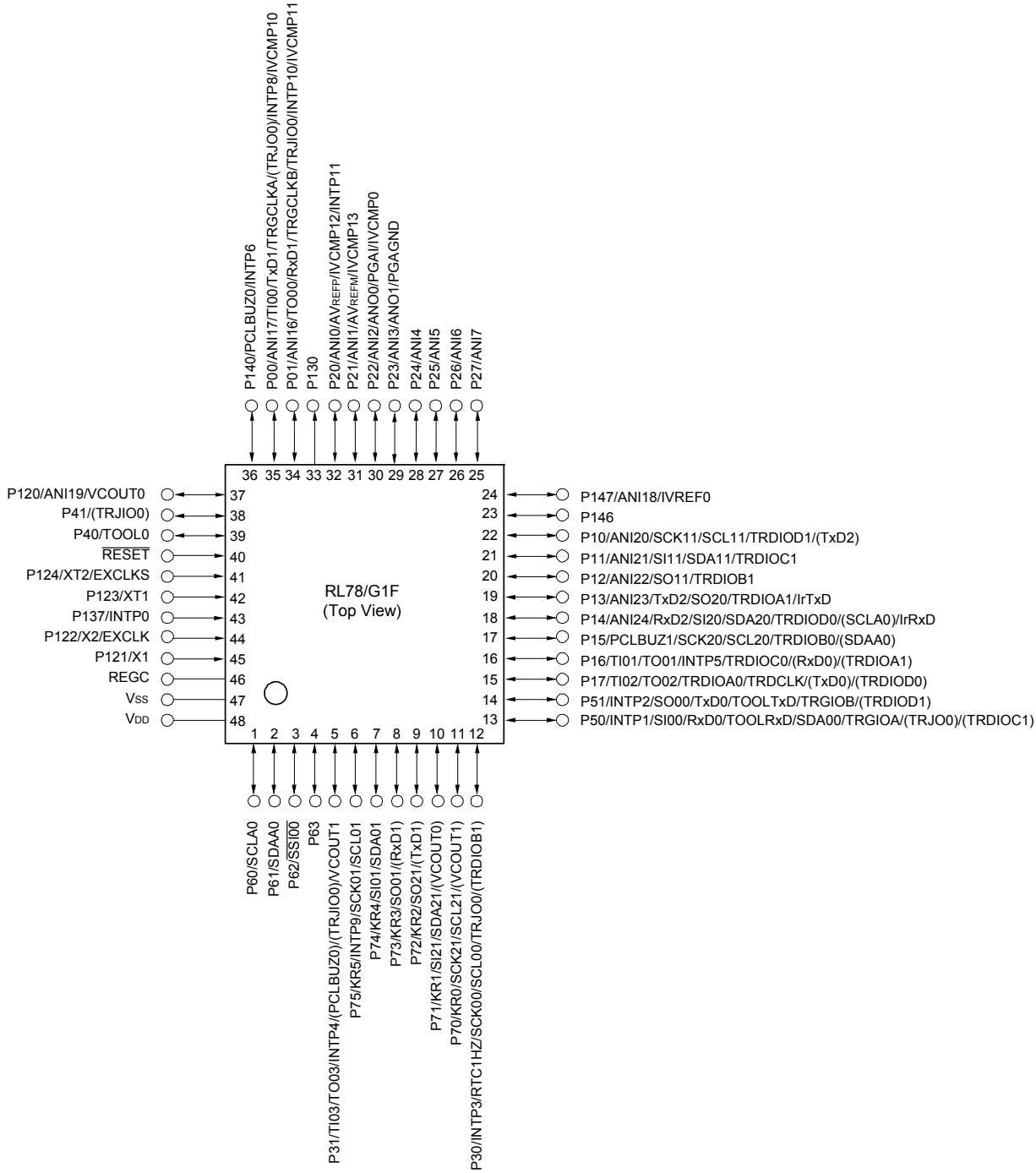


**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

### 1.3.5 64-pin products

• 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

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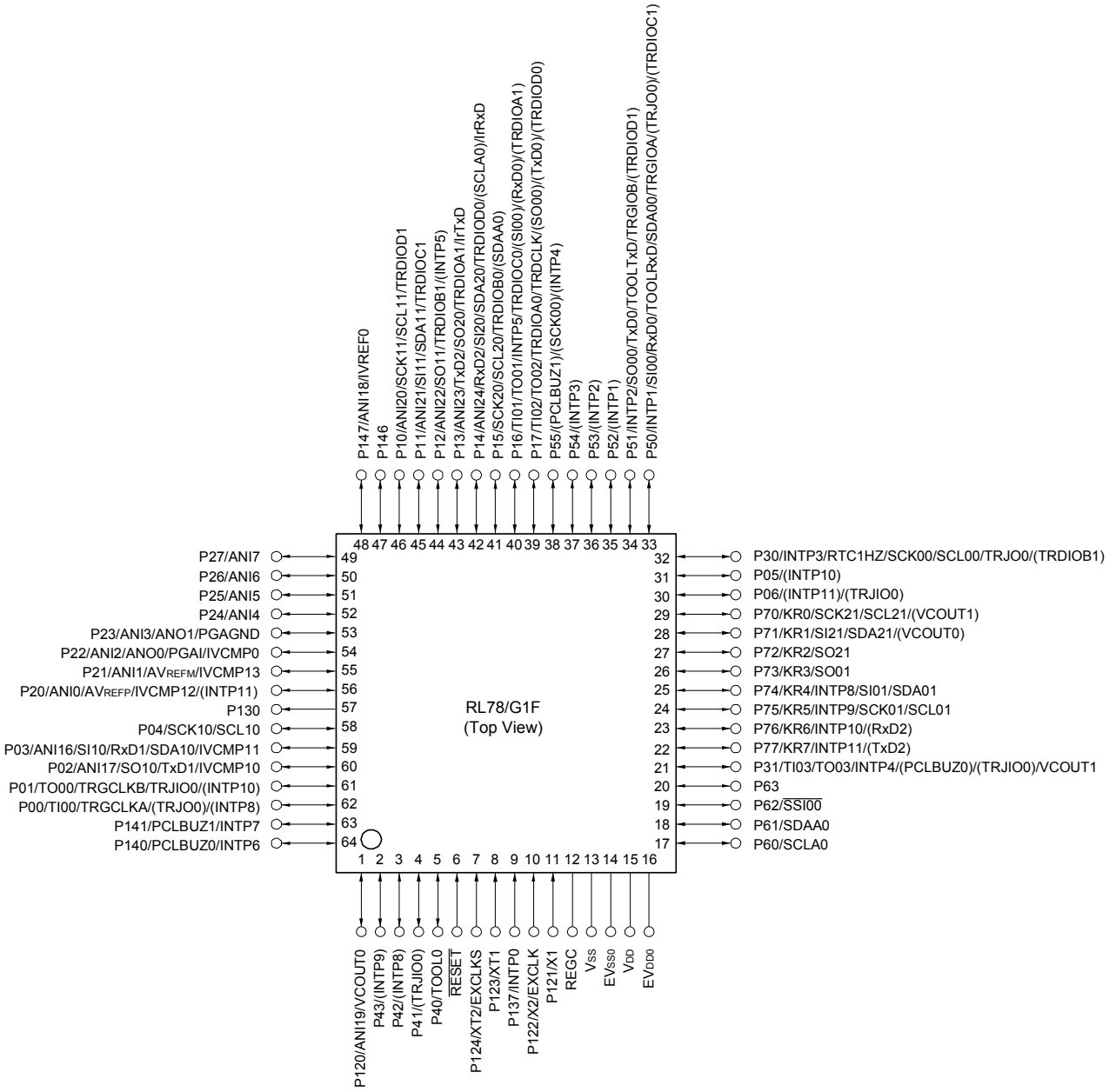



**Caution 1. Make EVSS0 pin the same potential as VSS pin.**

**Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.**

**Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

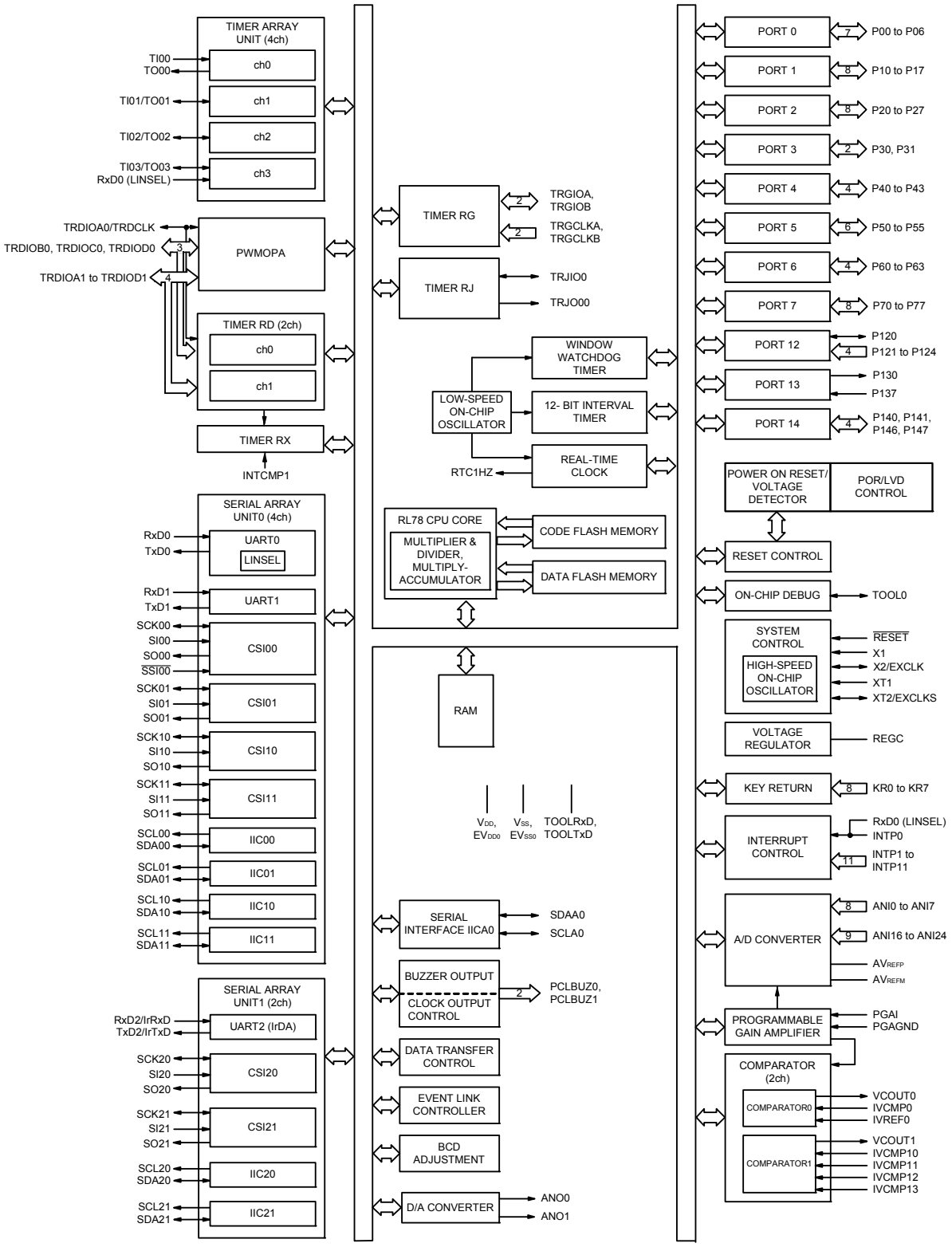
**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

## 1.4 Pin Identification

| | | | |
|---|---|---|---|
| ANI0 to ANI7: | Analog input | PGAI: | PGA input |
| ANI16 to ANI24: | Analog input | PGAGND: | PGA input |
| ANO0, ANO1: | Analog output | RTC1HZ: | Real-time clock correction clock (1 Hz) output |
| $AV_{REFM}$: | Analog reference voltage minus | RxD0 to RxD2: | Receive data |
| $AV_{REFP}$: | Analog reference voltage plus | SCK00, SCK01, SCK10: | Serial clock input/output |
| | | SCK11, SCK20, SCK21: | Serial clock input/output |
| $EV_{DD0}$: | Power supply for port | SCLA0: | Serial clock input/output |
| $EV_{SS0}$: | Ground for port | SCL00, SCL01, SCL10, SCL11: | Serial clock output |
| EXCLK: | External clock input (main system clock) | SCL20,SCL21: | Serial clock output |
| | | SDAA0: | Serial data input/output |
| EXCLKS: | External clock input (subsystem clock) | SDA00, SDA01, SDA10: | Serial data input/output |
| | | SDA11, SDA20, SDA21: | Serial data input/output |
| INTP0 to INTP11: | External interrupt input | SI00, SI01, SI10, SI11: | Serial data input |
| IrRxD: | Receive Data for IrDA | SI20, SI21: | Serial data input |
| IrTxD: | Transmit Data for IrDA | SO00, SO01, SO10: | Serial data output |
| IVCMP0: | Comparator 0 input | SO11, SO20, SO21: | Serial data output |
| IVCMP10 to IVCMP13: | Comparator 1 input / reference input | $\overline{SSI00}$: | Serial interface chip select input |
| | | TI00 to TI03: | Timer input |
| IVREF0: | Comparator 0 reference input | TO00 to TO03: | Timer output |
| | | TRJO0: | Timer output |
| KR0 to KR7: | Key return | TOOL0: | Data input/output for tool |
| P00 to P06: | Port 0 | TOOLRxD, TOOLTxD: | Data input/output for external device |
| P10 to P17: | Port 1 | TRDCLK, TRGCLKA: | Timer external input clock |
| P20 to P27: | Port 2 | TRGCLKB: | Timer external Input clock |
| P30, P31: | Port 3 | TRDIOA0, TRDIOB0: | Timer input/output |
| P40 to P43: | Port 4 | TRDIOC0, TRDIOD0: | Timer input/output |
| P50 to P55: | Port 5 | TRDIOA1, TRDIOB1: | Timer input/output |
| P60 to P63: | Port 6 | TRDIOC1, TRDIOD1: | Timer input/output |
| P70 to P77: | Port 7 | TRGIOA, TRGIOB, TRJIO0: | Timer input/output |
| P120 to P124: | Port 12 | TxD0 to TxD2: | Transmit data |
| P130, P137 | Port 13 | VCOUT0, VCOUT1: | Comparator output |
| P140, P141, P146, P147: | Port 14 | $V_{DD}$: | Power supply |
| | | $V_{SS}$: | Ground |
| PCLBUZ0, PCLBUZ1: | Programmable clock output/ buzzer output | X1, X2: | Crystal oscillator (main system clock) |
| | | XT1, XT2: | Crystal oscillator (subsystem clock) |
| REGC: | Regulator capacitance | | |
| $\overline{RESET}$: | Reset | | |

## 1.5 Block Diagram




**Remark** Block diagram of 64-pin products is shown as an example. For difference of the block diagram other than 64-pin products, refer to **1.6 Outline of Functions**.

## 1.6 Outline of Functions

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 24-pin | 32-pin | 36-pin | 48-pin | 64-pin |
|---|---|---|---|---|---|---|
| | | R5F11B7x (x = C, E) | R5F11BBx (x = C, E) | R5F11BCx (x = C, E) | R5F11BGx (x = C, E) | R5F11BLx (x = C, E) |
| Code flash memory (KB) | | 32, 64 | 32, 64 | 32, 64 | 32, 64 | 32, 64 |
| Data flash memory (KB) | | 4 | 4 | 4 | 4 | 4 |
| RAM (KB) | | 5.5 Note | 5.5 Note | 5.5 Note | 5.5 Note | 5.5 Note |
| Address space | | 1 MB | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 2.7 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 1.8 V) | | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | |
| Subsystem clock | | — | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | |
| | | — | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | |
| I/O port | Total | 20 | 28 | 31 | 44 | 58 |
| | CMOS I/O | 17 (N-ch O.D. output [$V_{DD}$ withstand voltage]: 10) | 25 (N-ch O.D. output [$V_{DD}$ withstand voltage]: 12) | 24 (N-ch O.D. output [$V_{DD}$ withstand voltage]: 10) | 34 (N-ch O.D. output [$V_{DD}$ withstand voltage]: 12) | 48 (N-ch O.D. output [$V_{DD}$ withstand voltage]: 12) |
| | CMOS input | 3 | 3 | 5 | 5 | 5 |
| | CMOS output | — | — | — | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | — | — | 2 | 4 | 4 |
| Timer | 16-bit timer | 9 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels (with PWMOPA), Timer RX: 1 channel, Timer RG: 1 channel) | | | | |
| | Watchdog timer | 1 channel | | | | |
| | Real-time clock (RTC) | 1 channel | | | | |
| | 12-bit interval timer | 1 channel | | | | |
| | Timer output | Timer outputs: 13 channels<br>PWM outputs: 8 channels | Timer outputs: 16 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | — | | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | |

**Note** This is about 4.5 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G1F User's Manual).

(2/2)

| Item | | 24-pin | 32-pin | 36-pin | 48-pin | 64-pin |
|---|---|---|---|---|---|---|
| | | R5F11B7x (x = C, E) | R5F11BBx (x = C, E) | R5F11BCx (x = C, E) | R5F11BGx (x = C, E) | R5F11BLx (x = C, E) |
| Clock output/buzzer output | | 2 | 2 | 2 | 2 | 2 |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation) | | | | |
| 8/10-bit resolution A/D converter | | 8 channels | 13 channels | 15 channels | 17 channels | 17 channels |
| 8-bit D/A converter | | 1 channel | 2 channels | | | |
| Comparator | | 2 channels | | | | |
| Programmable gain amplifier (PGA) | | 1 channel | | | | |
| Serial interface | | [24-pin, 32-pin, 36-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>[48-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$:2 channels<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>[64-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | | | | |
| | $I^2C$ bus | 1 channel | 1 channel | 1 channel | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 30 sources | 32 sources | 31 sources | 32 sources | 33 sources |
| Event link controller (ELC) | Event input | 21 | 21 | 21 | 22 | 22 |
| | Event trigger output | 9 | 10 | 10 | 10 | 10 |
| Vectored interrupt sources | Internal | 25 | 25 | 25 | 25 | 25 |
| | External | 9 | 11 | 10 | 12 | 13 |
| Key interrupt | | — | — | — | 6 | 8 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | | | | |
| Voltage detector | | [$T_A$ = –40 to +85°C]<br>• Rising edge: 1.67 ±0.03 V to 4.00 ±0.08 V (14 stages)<br>• Falling edge: 1.63 ±0.03 V to 3.98 ±0.08 V (14 stages)<br>[$T_A$ = –40 to +105°C (G: Industrial applications)]<br>• Rising edge: 2.61 ±0.1 V to 4.06 ±0.16 V (8 stages)<br>• Falling edge: 2.55 ±0.1 V to 3.98 ±0.15 V (8 stages) | | | | |
| On-chip debug function | | Provided | | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = –40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = –40 to +105°C) | | | | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C (A: Consumer applications), $T_A$ = –40 to +105°C (Industrial applications), | | | | |

The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

# 2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A$ = −40 to +85°C
R5F11BxxAxx
G: Industrial applications when $T_A$ = −40 to +105°C products is used in the range of $T_A$ = −40 to +85°C
R5F11BxxGxx

**Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. With products not provided with an $EV_{DD0}$, $EV_{SS0}$ pin, replace $EV_{DD0}$ with $V_{DD}$, or replace $EV_{SS0}$ with $V_{SS}$.**

**Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G1F User's Manual.**

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings** **(1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to +6.5 | V |
| | $EV_{DD0}$ | | -0.5 to +6.5 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to +2.8 and -0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27 | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI24 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $AV_{REF}(+)$ +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI7 | -0.3 to $V_{DD}$ +0.3 and -0.3 to $AV_{REF}(+)$ +0.3 Notes 2, 3 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 6.5 V or lower.

**Note 3.** Do not exceed $AV_{REF}$ (+) + 0.3 V in case of A/D conversion target pin.

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF}$ (+): + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Absolute Maximum Ratings** **(2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | -40 | mA |
| | | Total of all pins -170 mA | P00 to P04, P40 to P43,P120, P130, P140, P141 | -70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147 | -100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40-P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147 | 40 | mA |
| | | Total of all pins 170 mA | P00 to P04, P40 to P47, P120, P130, P140, P141 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +85 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Resonator | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$) Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | 1.0 | | 8.0 | |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | 1.0 | | 4.0 | |
| XT1 clock oscillation frequency ($f_{XT}$) Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G1F User's Manual.

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1 | | 32 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | 1 | | 16 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | 1 | | 8 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | 1 | | 4 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | $T_A$ = -20 to +85°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | -1 | | 1 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | -5 | | 5 | % |
| | | $T_A$ = -40 to -20°C | 1.8 V ≤ $V_{DD}$ < 5.5 V | -1.5 | | 1.5 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | -5.5 | | 5.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | | | | -10.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -55.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -10.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | -5.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | -2.5 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P53, P70 to P77, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -80.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -19.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | -10.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | -5.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | -135.0 Note 4 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27 | | | | -0.1 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | -1.5 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $EV_{DD0}$, $V_{DD}$ pins to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Note 4.** The applied current for the products for industrial application (R5F11BxxGxx) is -100 mA.

**Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77,P120, P130, P140, P141, P146, P147 | | | | 20.0 Note 2 | mA |
| | | Per pin for P60 to P63 | | | | 15.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 70.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 15.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 9.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 4.5 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 35.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 20.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 10.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 150.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27 | | | | 0.4 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$ and $V_{SS}$ pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | Normal input buffer | 0.8 $EV_{DD0}$ | | $EV_{DD0}$ | V |
| | $V_{IH2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P50, P53 to P55, | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 2.2 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 2.0 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD0}$ < 3.3 V | 1.5 | | $EV_{DD0}$ | V |
| | $V_{IH3}$ | P20 to P27 (when P20 is used as a port pin) | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60 to P63 | | 0.7 $EV_{DD0}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P123, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ (when P20 is used as INTP11 pin) | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | Normal input buffer | 0 | | 0.2 $EV_{DD0}$ | V |
| | $V_{IL2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P50, P53 to P55, | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD0}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27 (when P20 is used as a port pin) | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL4}$ | P60 to P63 | | 0 | | 0.3 $EV_{DD0}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ (when P20 is used as INTP11 pin) | | 0 | | 0.2 $V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 is $EV_{DD0}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -10.0 mA | $EV_{DD0}$ - 1.5 | | | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -3.0 mA | $EV_{DD0}$ - 0.7 | | | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -2.0 mA | $EV_{DD0}$ - 0.6 | | | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -1.5 mA | $EV_{DD0}$ - 0.5 | | | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $I_{OH1}$ = -1.0 mA | $EV_{DD0}$ - 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = -100 μA | $V_{DD}$ - 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 20.0 mA | | | 1.3 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.3 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 μA | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 1.0 mA | | | 0.4 | V |

**Caution** **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | $V_I$ = $EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | $V_I$ = $EV_{SS0}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P20 to P27, P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| On-chip pull-up resistance | $R_U$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.3.2 Supply current characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.2 | 8.7 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.2 | 8.7 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 8.1 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 8.1 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.1 | 6.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.1 | 6.9 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.8 | 6.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.8 | 6.3 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.6 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 2.1 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 2.1 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 1.9 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 1.9 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | mA |
| | | | | | | Resonator connection | | 3.5 | 5.5 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | |
| | | | | | | Resonator connection | | 3.5 | 5.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | mA |
| | | | | | | Resonator connection | | 1.2 | 2 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | |
| | | | | | | Resonator connection | | 1.2 | 2 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.7 | 6.1 | µA |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.7 | 6.1 | |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.8 | 6.7 | |
| | | | | | | Resonator connection | | 4.8 | 6.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.8 | 3.09 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.8 | 3.09 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.54 | 2.4 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.54 | 2.4 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.4 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.4 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 1.83 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 1.83 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 1.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 1.38 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 790 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 790 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 830 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 830 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.55 | mA |
| | | | | | Resonator connection | | 0.49 | 1.74 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.55 | |
| | | | | | Resonator connection | | 0.49 | 1.74 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.3 | 0.93 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.3 | 0.93 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 640 | μA |
| | | | | | Resonator connection | | 145 | 680 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 95 | 640 | |
| | | | | | Resonator connection | | 145 | 680 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = 25°C | Square wave input | | 0.3 | 0.57 | |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = 50°C | Square wave input | | 0.36 | 1.17 | |
| | | | | | Resonator connection | | 0.59 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = 70°C | Square wave input | | 0.49 | 1.97 | |
| | | | | | Resonator connection | | 0.72 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = 85°C | Square wave input | | 0.97 | 3.37 | |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.1 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.9 | |
| | | | $T_A$ = +85°C | | | | 0.9 | 3.3 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.2 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75 | | μA |
| D/A converter operating current | $I_{DAC}$ Notes 1, 11 | Per D/A converter channel | | | | 1.5 | mA |
| PGA operating current | | Operation | | | 480 | 700 | μA |
| Comparator operating current | $I_{CMP}$ Notes 1, 12 | Operation (per comparator channel, constant current for comparator included) | When the internal reference voltage is not in use | | 50 | 100 | μA |
| | | | When the internal reference voltage is in use | | 60 | 110 | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 7 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.5 | 12.2 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 8 | | | | 2.5 | 12.2 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.5 | 0.6 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.2 | 1.44 | |
| | | CSI/UART operation | | | 0.7 | 0.84 | |
| | | DTC operation | | | 3.1 | | |

**Note 1.** Current flowing to $V_{DD}$.

**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**Note 8.** Current flowing during programming of the data flash.

**Note 9.** Current flowing during self-programming.

**Note 10.** For shift time to the SNOOZE mode, see **26.3.3 SNOOZE mode** in the RL78/G1F User's Manual.

**Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DAC}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit is in operation.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 2.4 AC Characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| | | | LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| | | | LV (low-voltage main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 1.0 | | 4.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 120 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI03 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 Note | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 100 | | | ns |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | 300 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 500 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{TJIH}$, $t_{TJIL}$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 40 | | | ns |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | 120 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 200 | | | ns |

**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
1.8 V ≤ $EV_{DD0}$ < 2.7 V: MIN. 125 ns
1.6 V ≤ $EV_{DD0}$ < 1.8 V: MIN. 250 ns

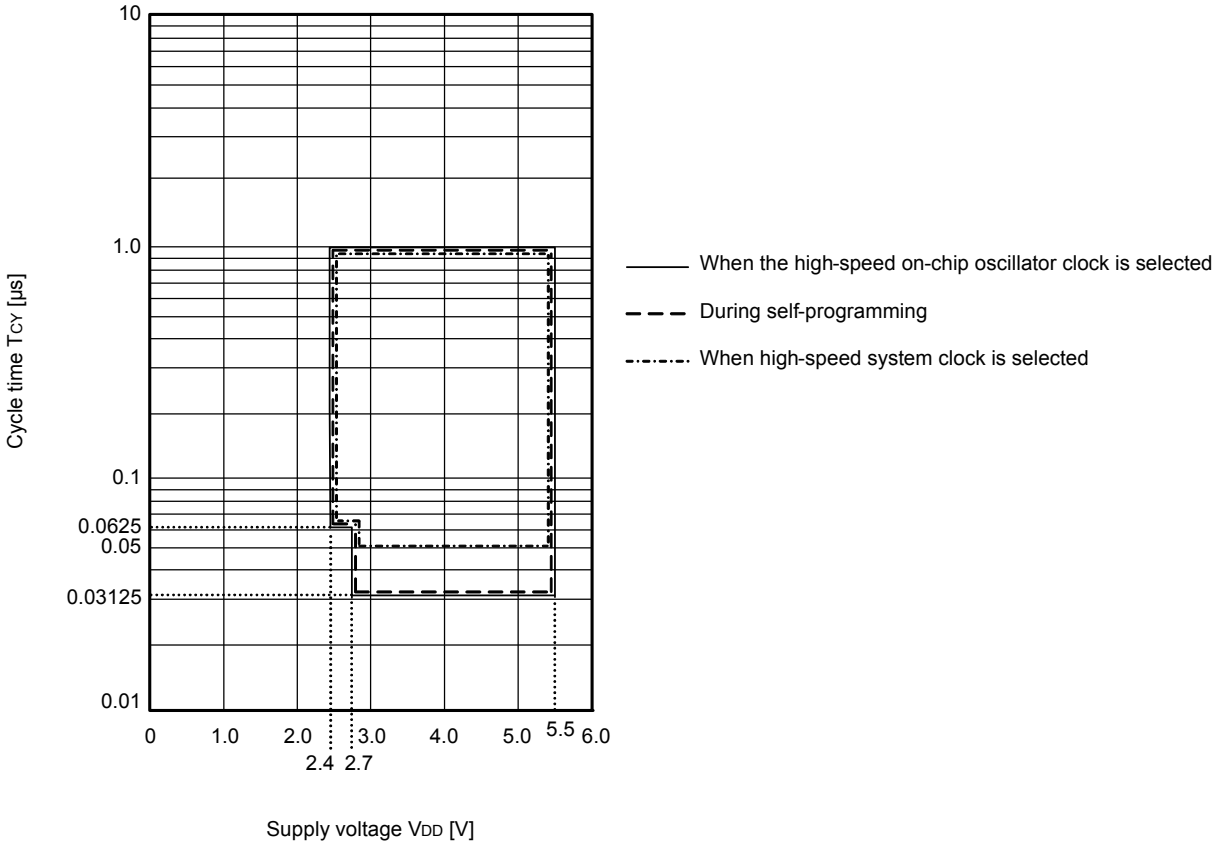
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

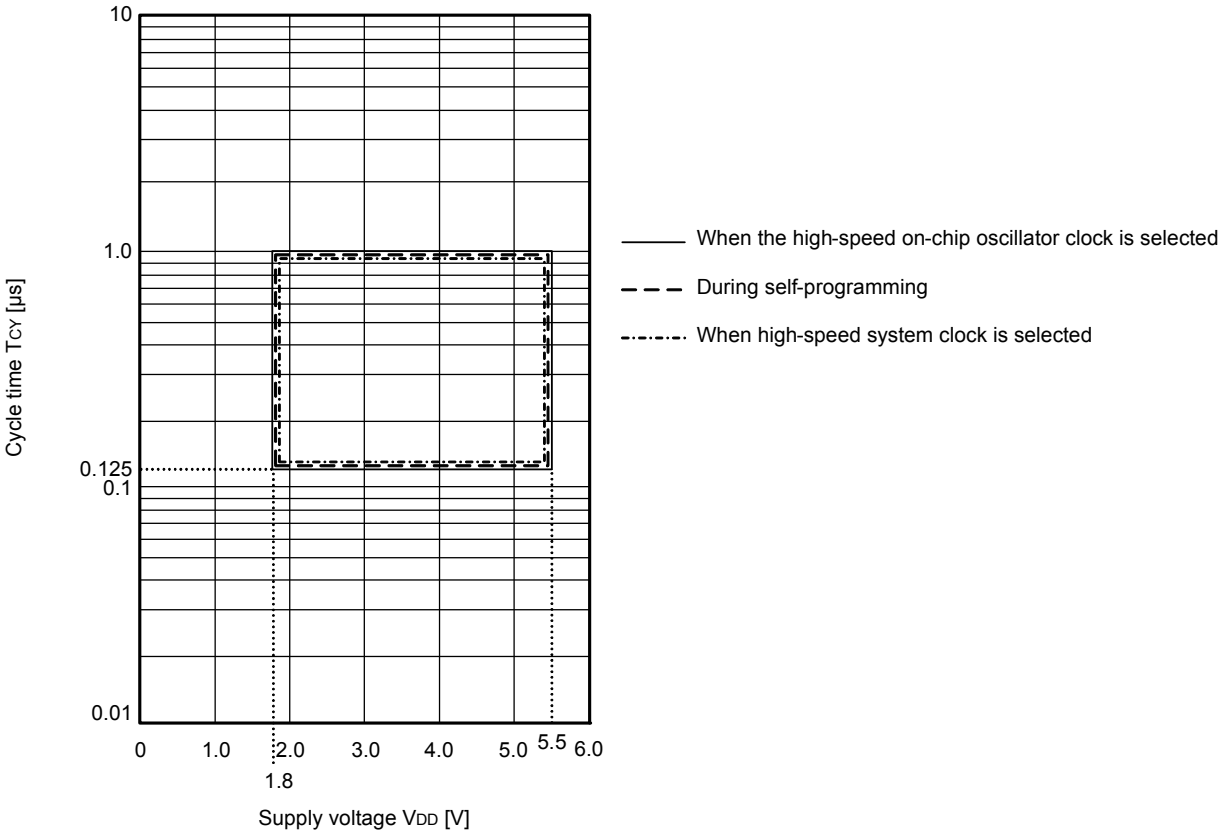
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Timer RD input high-level width, low-level width | $t_{TDIH}$, $t_{TDIL}$ | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | | 3/$f_{CLK}$ | | | ns |
| Timer RD forced cutoff signal input low-level width | $t_{TDSIL}$ | P130/INTP0 | 2MHz < $f_{CLK}$ ≤ 32 MHz | 1 | | | µs |
| | | | $f_{CLK}$ ≤ 2 MHz | 1/$f_{CLK}$ + 1 | | | |
| Timer RG input high-level width, low-level width | $t_{TGIH}$, $t_{TGIL}$ | TRGIOA, TRGIOB | | 2.5/$f_{CLK}$ | | | ns |
| TO00 to TO03, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency | $f_{TO}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 2 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | µs |
| | | INTP1 to INTP11 | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 1 | | | µs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

Minimum Instruction Execution Time during Main System Clock Operation

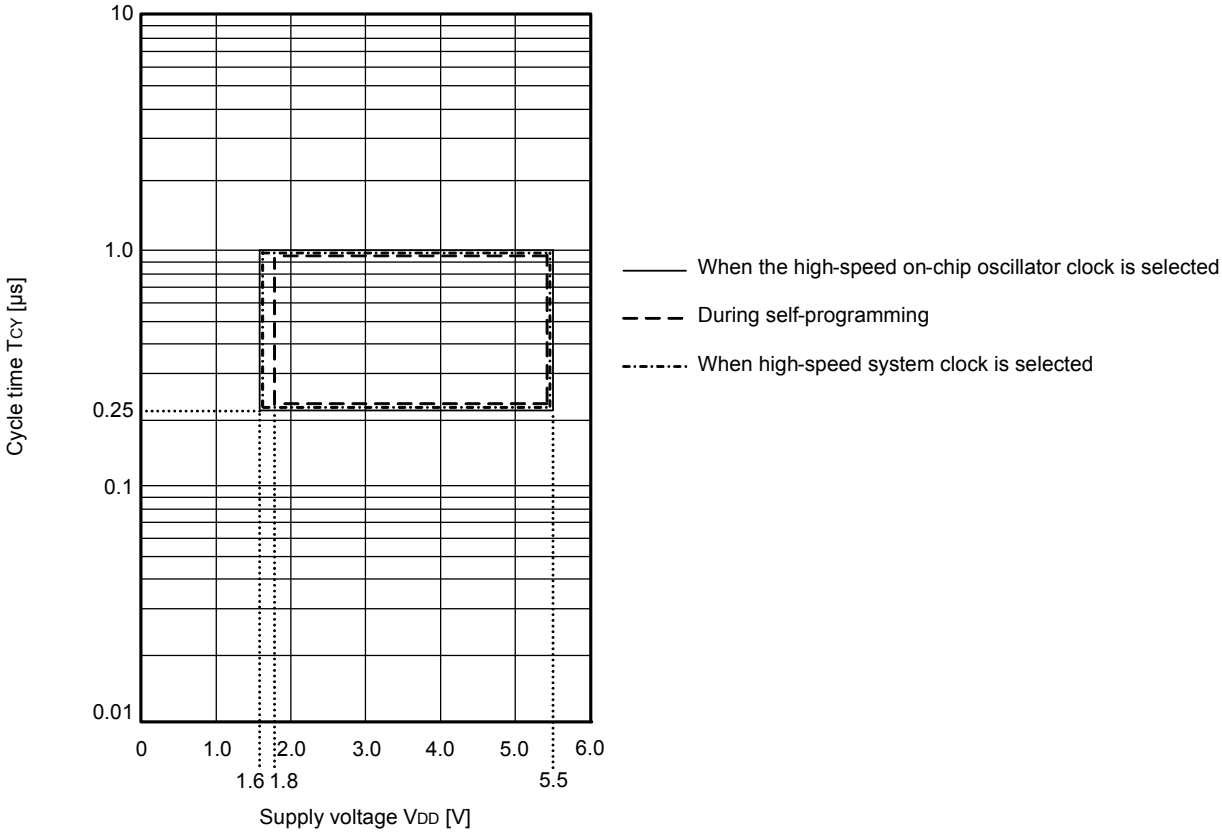
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



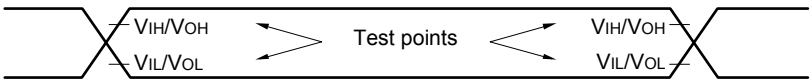
$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



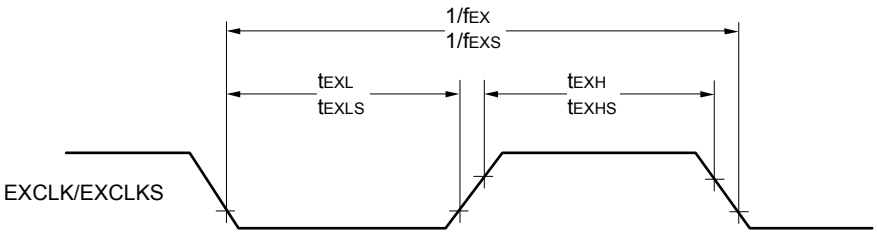

$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



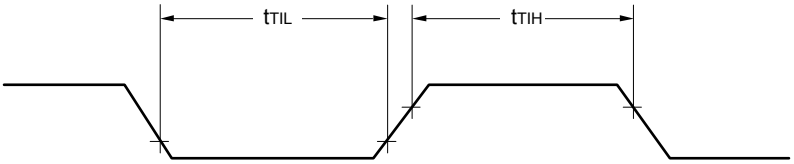
AC Timing Test Points

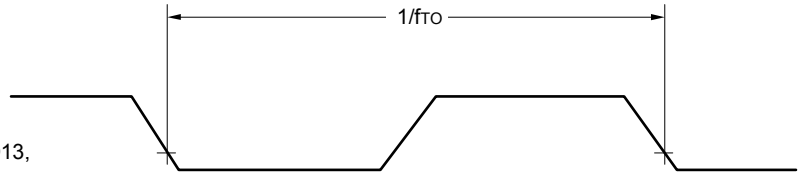


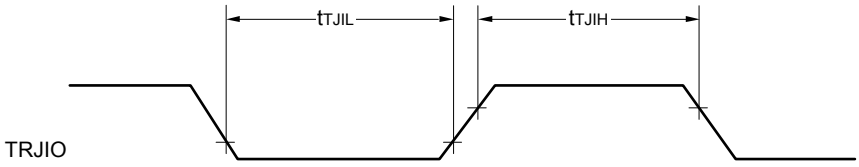

External System Clock Timing

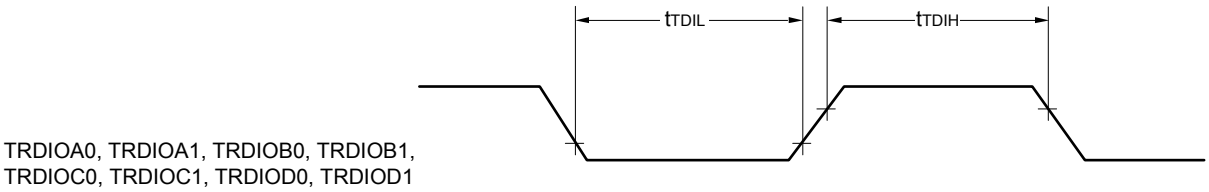


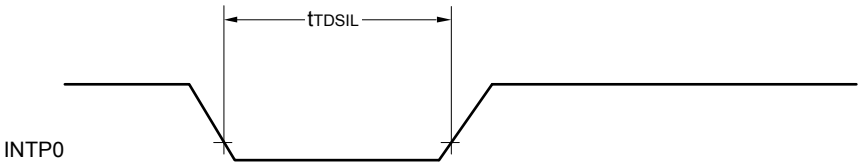

TI/TO Timing

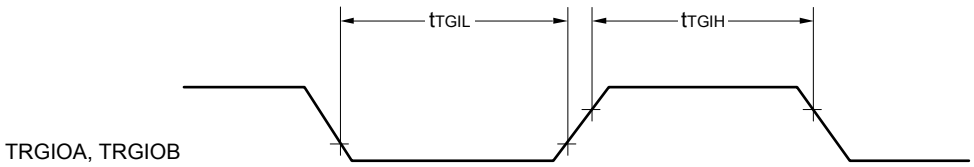


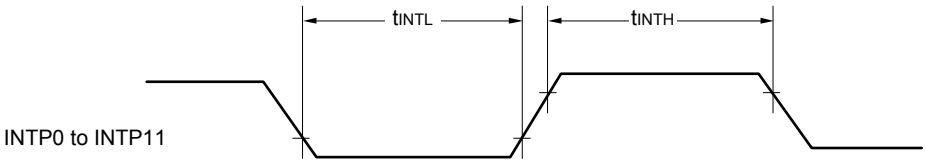

tTJIL
tTJIH
TRJIO


tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1

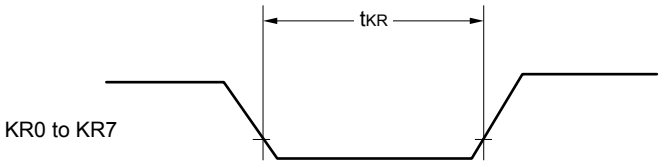

tTDSIL
INTP0


tTGIL
tTGIH
TRGIOA, TRGIOB

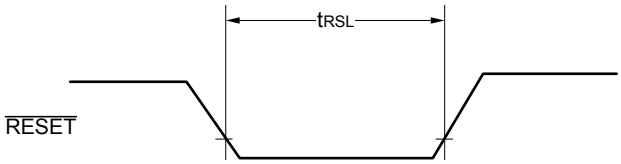
Interrupt Request Input Timing




Key Interrupt Input Timing

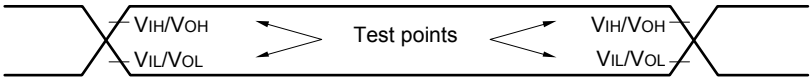



$\overline{\text{RESET}}$ Input Timing



## 2.5 Peripheral Functions Characteristics

AC Timing Test Points




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | — | | | 1.3 | | 0.6 | Mbps |

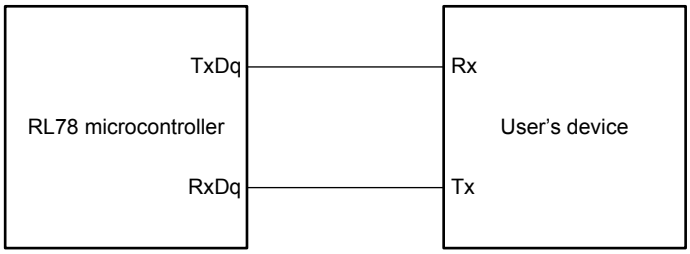
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V: MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V: MAX. 0.6 Mbps

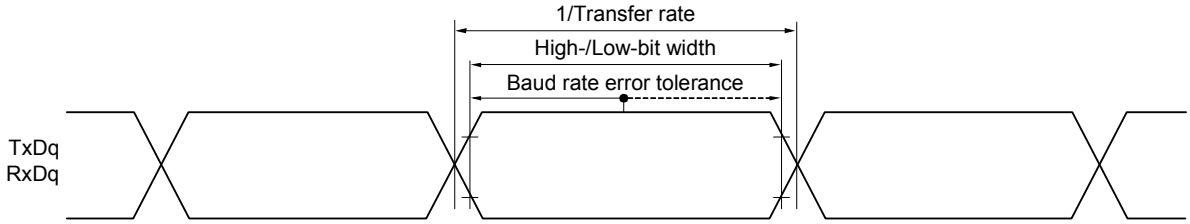
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

### (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 62.5 | | 250 | | 500 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 83.3 | | 250 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 7 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 10 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 23 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 20 pF Note 4 | | | 10 | | 10 | | 10 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** This value is valid only when CSI00's peripheral I/O redirect function is not used.

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

### (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 125 | | 500 | | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 500 | | 1000 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | 500 | | 1000 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1000 | | 1000 | | 1000 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1000 | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 38 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 110 | | 110 | | 110 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 220 | | 220 | | 220 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 220 | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | 25 | | 25 | | 25 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | — | | 25 | | 25 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 , 5, 7)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

### (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | — | | — | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | — | | — | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 750 | | 6/$f_{MCK}$ and 750 | | 6/$f_{MCK}$ and 750 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 7 | | $t_{KCY2}$/2 - 7 | | $t_{KCY2}$/2 - 7 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 66 | | $t_{KCY2}$/2 - 66 | | $t_{KCY2}$/2 - 66 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | $t_{KCY2}$/2 - 66 | | $t_{KCY2}$/2 - 66 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | 1/$f_{MCK}$ + 40 | | 1/$f_{MCK}$ + 40 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 1/$f_{MCK}$ + 40 | | 1/$f_{MCK}$ + 40 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 250 | | 1/$f_{MCK}$ + 250 | | 1/$f_{MCK}$ + 250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 1/$f_{MCK}$ + 250 | | 1/$f_{MCK}$ + 250 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 75 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 100 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 220 | | 2/$f_{MCK}$ + 220 | | 2/$f_{MCK}$ + 220 | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 2/$f_{MCK}$ + 220 | | 2/$f_{MCK}$ + 220 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3, 5, 7)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10, 11))

### (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

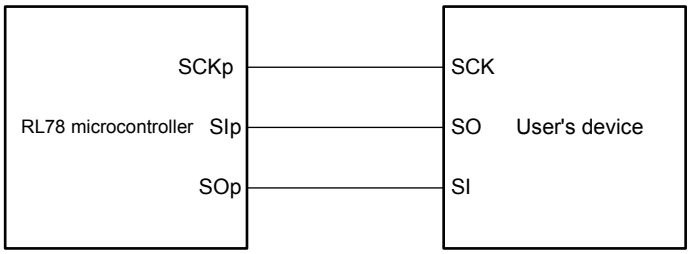
**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $\overline{SSI00}$ setup time | $t_{SSIK}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 120 | | 120 | | 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 200 | | 200 | | 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | 400 | | 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 400 | | 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| $\overline{SSI00}$ hold time | $t_{KSSI}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 120 | | 120 | | 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 200 | | 200 | | 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | 400 | | 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 400 | | 400 | | ns |

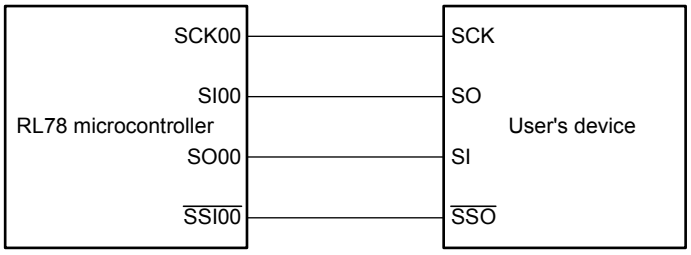
**Caution** **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

**CSI mode connection diagram (during communication at same potential)**

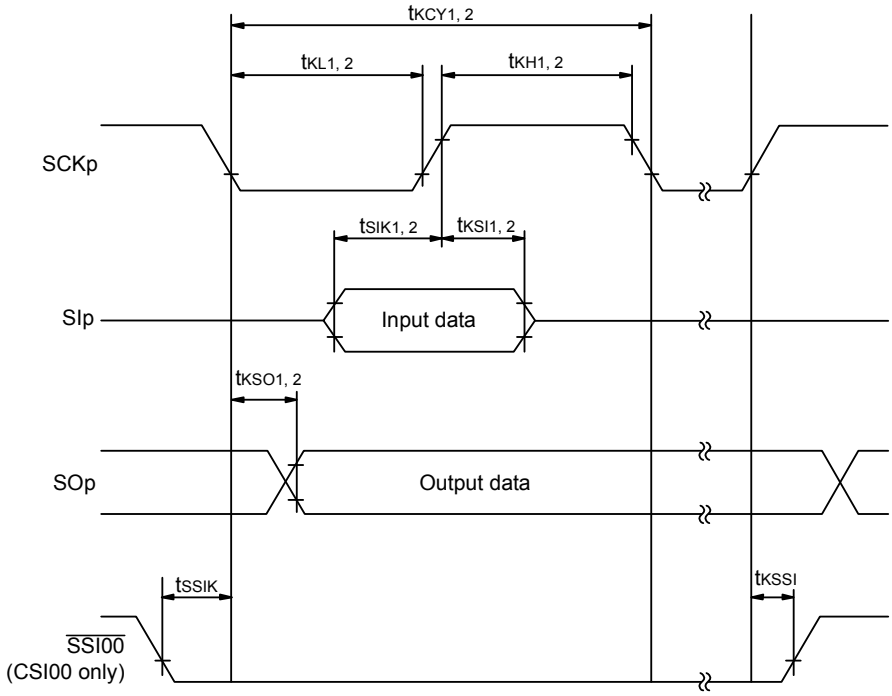



**CSI mode connection diagram (during communication at same potential)**
**(Slave Transmission of slave select input function (CSI00))**

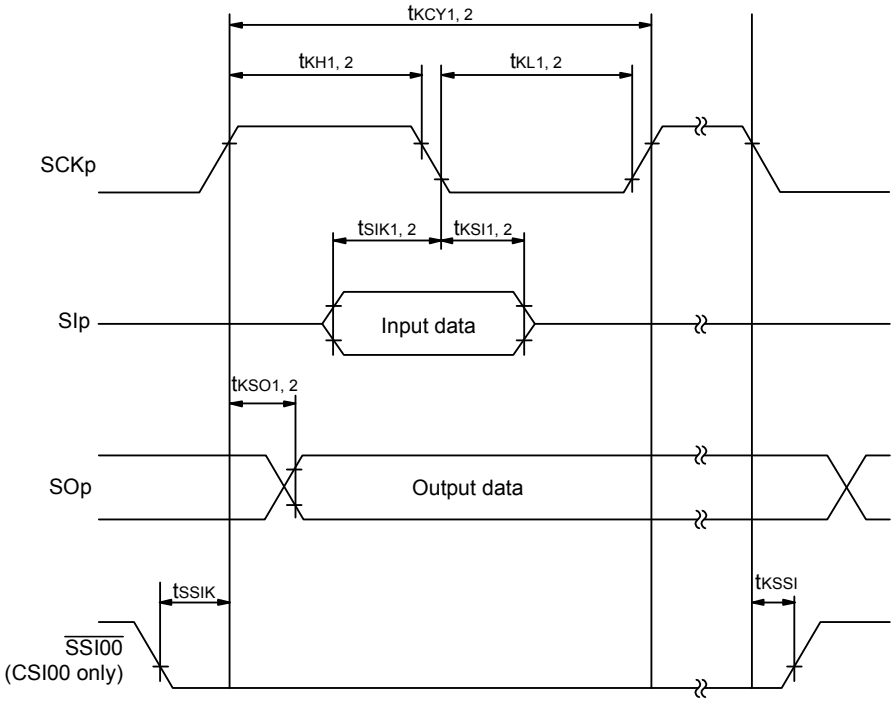



**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

### (5) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 250 Note 1 | | 250 Note 1 | | 250 Note 1 | kHz |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | — | | 250 Note 1 | | 250 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 1850 | | 1850 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 1850 | | 1850 | | ns |

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

### (5) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 85 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 0 | 405 | 0 | 405 | ns |

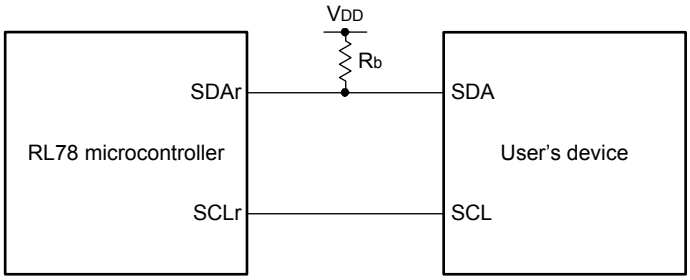
**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

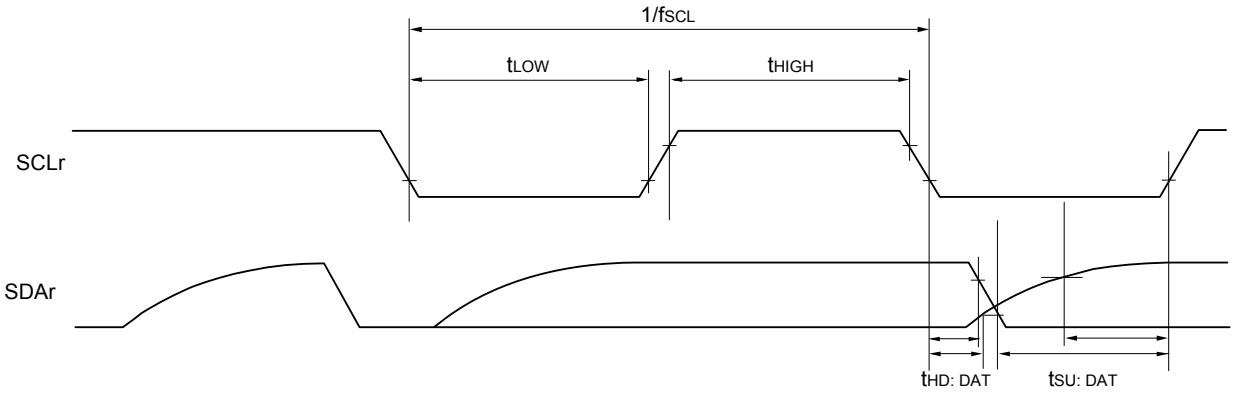
**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 3, 5, 7),
h: POM number (h = 0, 1, 3, 5, 7)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/6 Notes 1, 2, 3 | | $f_{MCK}$/6 Notes 1, 2 | | $f_{MCK}$/6 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** Use it with $EV_{DD0} \geq V_b$.

**Note 3.** The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V: MAX. 1.3 Mbps

**Note 4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$ [V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5, 7)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | transmission | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | Note 1 | | Note 1 | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.8 Note 2 | | 2.8 Note 2 | | 2.8 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | Note 3 | | Note 3 | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | | 1.2 Note 4 | | 1.2 Note 4 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | Notes 5, 6 | | Notes 5, 6 | | Notes 5, 6 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 7 | | 0.43 Note 7 | | 0.43 Note 7 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

**Note 4.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Note 6.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

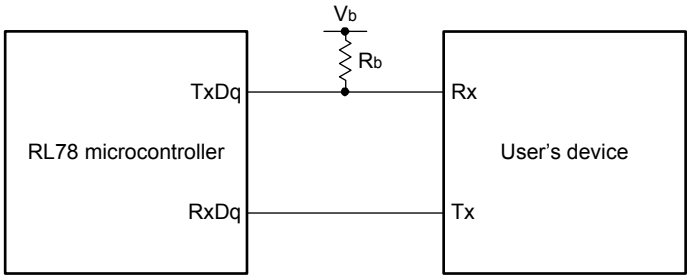
* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 7.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

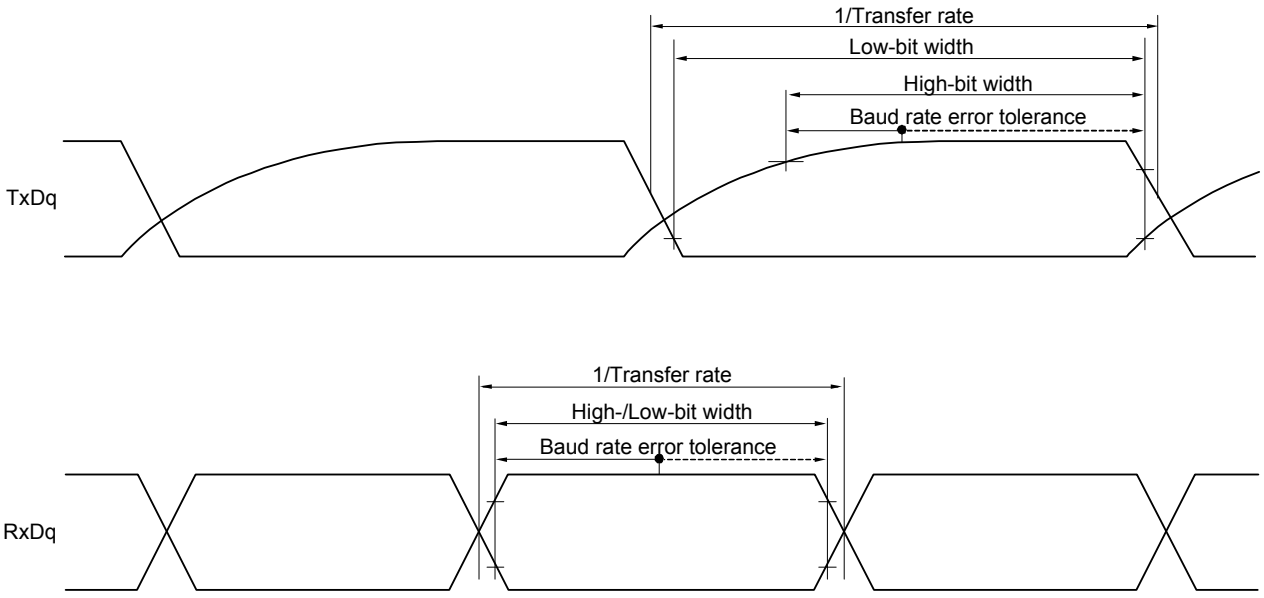
**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5, 7)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 7 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 10 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | | 60 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | | 130 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

### (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 23 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Remark 4.** This value is valid only when CSI00's peripheral I/O redirect function is not used.

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(1/3)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | 1150 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 75 | | $t_{KCY1}$/2 - 75 | | $t_{KCY1}$/2 - 75 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |

**Note** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 81 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | 479 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 100 | | 100 | | 100 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | | 195 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | | 483 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (3/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | | 25 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | | 25 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | | 25 | ns |

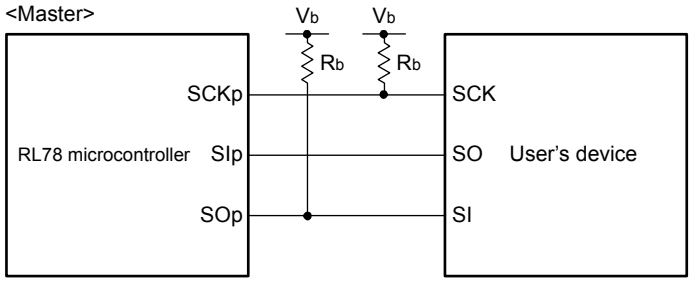
**Note 1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**



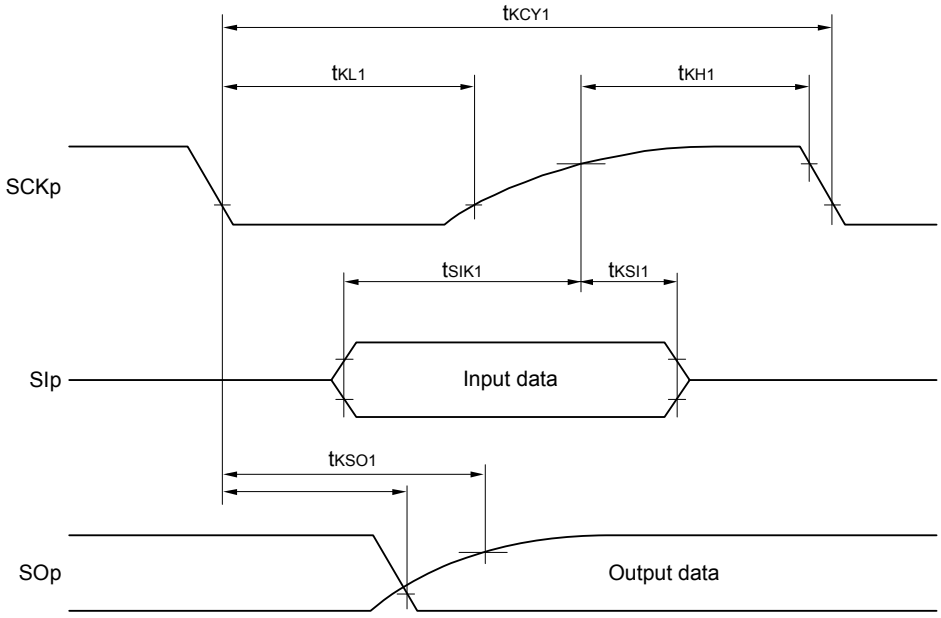

**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

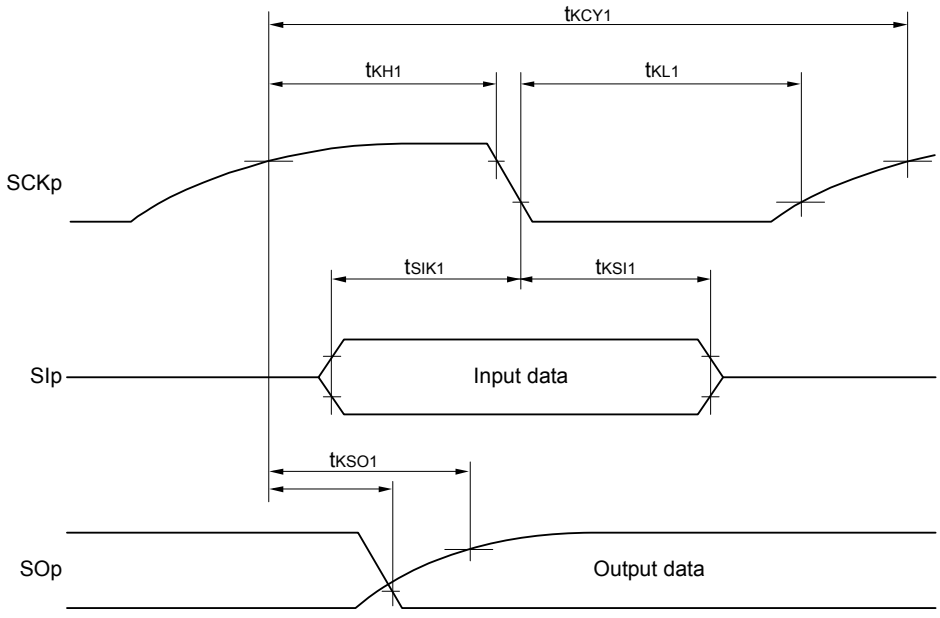
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Remark 4.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

### (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 14/$f_{MCK}$ | | — | | — | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 20/$f_{MCK}$ | | — | | — | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | — | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 24 MHz < $f_{MCK}$ | 48/$f_{MCK}$ | | — | | — | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | — | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 - 12 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_v$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

(**Notes**, **Cautions**, and **Remarks** are listed on the next page.)

**Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Note 2.** Use it with $EV_{DD0} \geq V_b$.

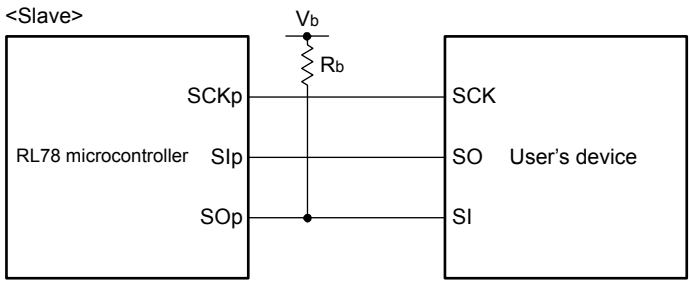
**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**CSI mode connection diagram (during communication at different potential)**



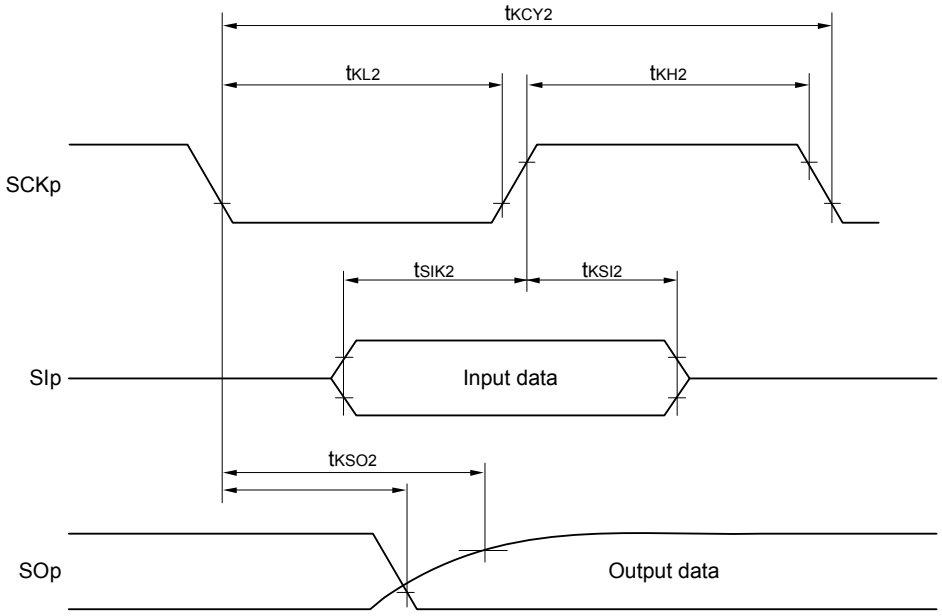

**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

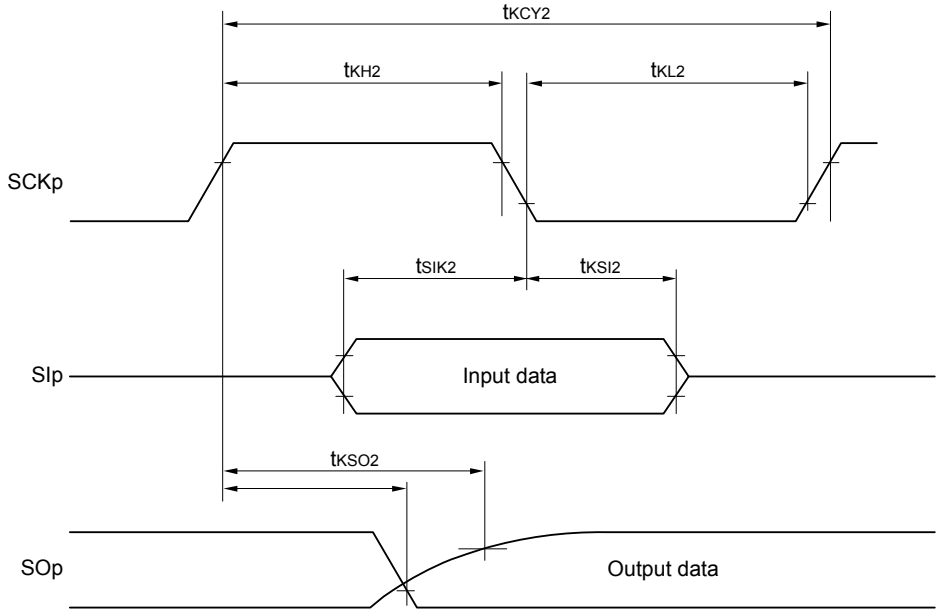
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10))

**Remark 4.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

### (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 245 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 675 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | ns |

### (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

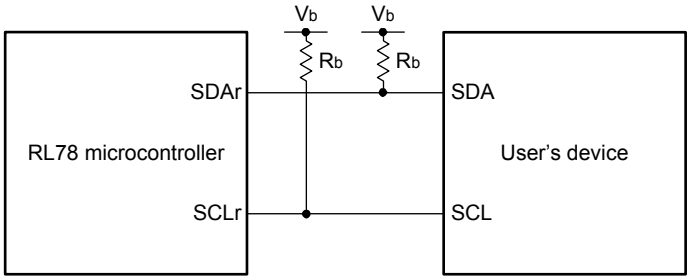
**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Note 3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

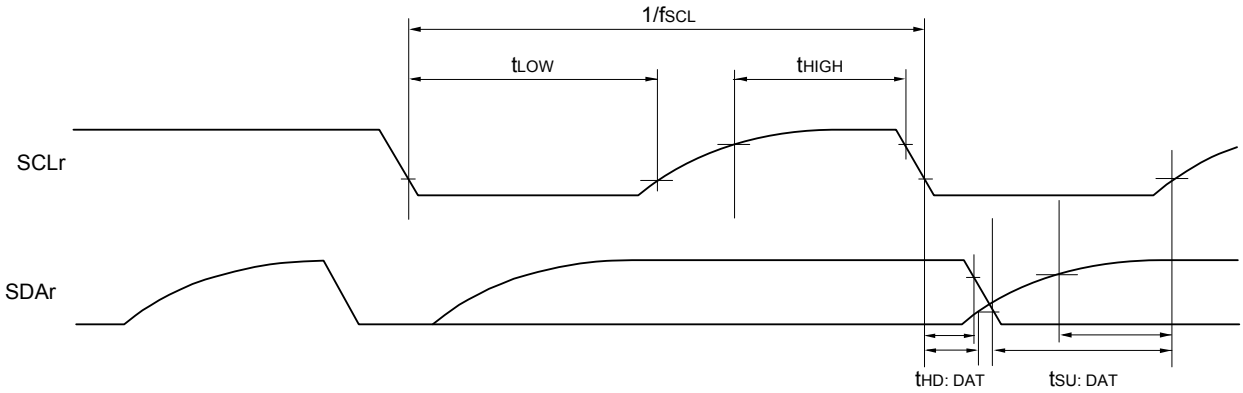
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20), g: PIM, POM number (g = 0, 1, 3, 5, 7)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10)

## 2.5.2 Serial interface IICA

### (1) $I^2C$ standard mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | µs |

(**Notes**, **Caution**, and **Remark** are listed on the next page.)

### (1) $I^2C$ standard mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 250 | | 250 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 250 | | 250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 250 | | 250 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 0 | 3.45 | 0 | 3.45 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 4.0 | | 4.0 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 4.7 | | 4.7 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

### (2) $I^2C$ fast mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

### (3) $I^2C$ fast mode plus

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode plus: $f_{CLK}$ ≥ 10 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 1000 | — | | — | | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | — | | — | | µs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 50 | | — | | — | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.45 | — | | — | | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | — | | — | | µs |

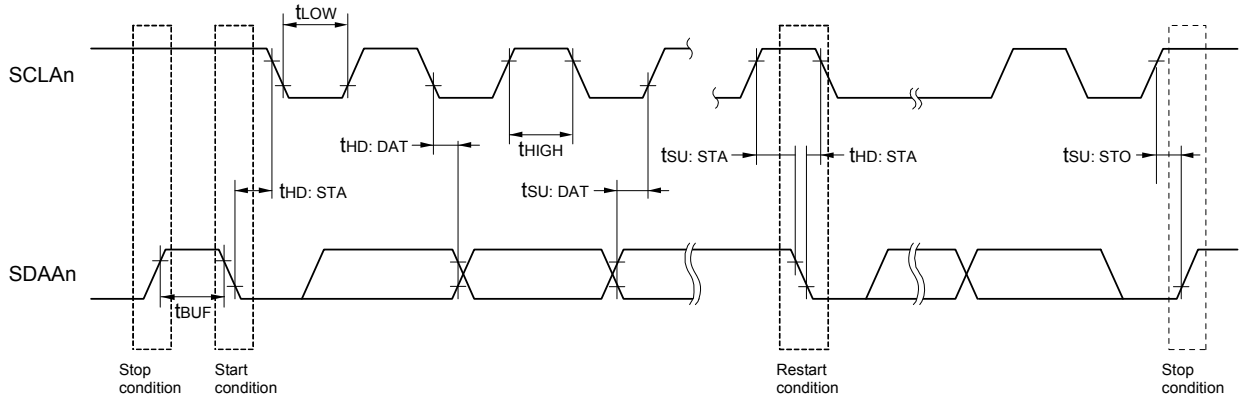
**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: $C_b$ = 120 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark** n = 0, 1

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input channel | Reference voltage (+) = $AV_{REFP}$ Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$ Reference voltage (-) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$ Reference voltage (-)= $AV_{REFM}$ |
|---|---|---|---|
| ANI0 to ANI7 | Refer to **2.6.1 (1)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (4)**. |
| ANI16 to ANI24 | Refer to **2.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **2.6.1 (1)**. | | — |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI7, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±5.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI7 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 5 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 5 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** Values when the conversion time is set to 57 µs (min.) and 95 µs (max.).

**Note 5.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI24**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | 1.2 | ±8.5 | LSB |
| Conversion time | tCONV | 10-bit resolution<br>Target ANI pin: ANI16 to ANI24 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | μs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±6.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±2.5 | LSB |
| Analog input voltage | VAIN | ANI16 to ANI24 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $EV_{DD0}$ ≤ $AV_{REFP}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 5.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

### (3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI17, ANI16 to ANI24, internal reference voltage, and temperature sensor output voltage

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (-) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | 1.2 | ±10.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI7, ANI16 to ANI24 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | µs |
| | | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±6.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI7 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI24 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** When the conversion time is set to 57 µs (min.) and 95 µs (max.).

**Note 4.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI7, ANI16 to ANI24**

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (-) = $AV_{REFM}$ = 0 V Note 4, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**Note 4.** When reference voltage (-) = $V_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

### 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.6.3 D/A converter characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{SS0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Settling time | $t_{SET}$ | Cload = 20 pF | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 3 | μs |
| | | | 1.6 V ≤ $V_{DD}$ < 2.7 V | | | 6 | μs |

## 2.6.4 Comparator

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IOCMP}$ | | | | ±5 | ±40 | mV |
| Input voltage range | $V_{ICMP}$ | | | 0 | | $V_{DD}$ | V |
| Internal reference voltage deviation | $\Delta V_{IREF}$ | CmRVM register value : 7FH to 80H (m = 0, 1) | | | | ±2 | LSB |
| | | Other than above | | | | ±1 | LSB |
| Response Time | $t_{CR}$, $t_{CF}$ | Input amplitude±100mV | | | 70 | 150 | ns |
| Operation stabilization time[Note 1] | $t_{CMP}$ | CMPn = 0→1 | $V_{DD}$ = 3.3 to 5.5 V | | | 1 | µs |
| | | | $V_{DD}$ = 2.7 to 3.3 V | | | 3 | µs |
| Reference voltage stabilization wait time | $t_{VR}$ | CVRE : 0→1[Note 2] | | | | 20 | µs |
| Operation current | $I_{CMPDD}$ | Separately, it is defined as the operation current of peripheral functions. | | | | | |

**Note 1.** Time taken until the comparator satisfies the DC/AC characteristics after the comparator operation enable signal is switched (CMPnEN = 0 → 1).

**Note 2.** Enable comparator output (CnOE bit = 1; n = 0 to 1) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; m = 0 to 1) and waiting for the operation stabilization time to elapse.

## 2.6.5 PGA

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IOPGA}$ | | | | | ±10 | mV |
| Input voltage range | $V_{IPGA}$ | | | 0 | | 0.9 × $V_{DD}$/ Gain | V |
| Output voltage range | $V_{IOHPGA}$ | | | 0.93 × $V_{DD}$ | | | V |
| | $V_{IOLPGA}$ | | | | | 0.07 × $V_{DD}$ | V |
| Gain error | | x4, x8 | | | | ±1 | % |
| | | x16 | | | | ±1.5 | % |
| | | x32 | | | | ±2 | % |
| Slew rate | $SR_{RPGA}$ | Rising When Vin= 0.1$V_{DD}$/gain to 0.9$V_{DD}$/gain. 10 to 90% of output voltage amplitude | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (Other than x32) | 3.5 | | | V/µs |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 4.0V | 0.5 | | | |
| | $SR_{FPGA}$ | Falling When Vin= 0.1$V_{DD}$/gain to 0.9$V_{DD}$/gain. 90 to 10% of output voltage amplitude | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (Other than x32) | 3.5 | | | |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 4.0V | 0.5 | | | |
| Reference voltage stabilization wait time-[Note 1] | $t_{PGA}$ | x4, x8 | | | | 5 | µs |
| | | x16, x32 | | | | 10 | µs |
| Operation current | $I_{PGADD}$ | Separately, it is defined as the operation current of peripheral functions. | | | | | |

**Note 1.** Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

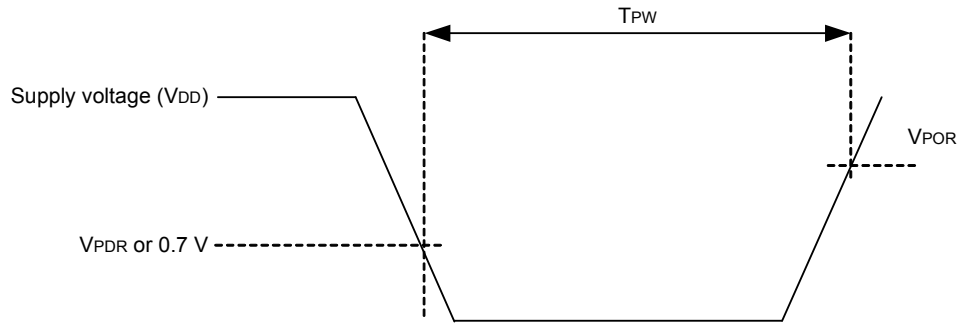
## 2.6.6 POR circuit characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power on/down reset threshold | $V_{POR}$ | Voltage threshold on $V_{DD}$ rising | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Voltage threshold on $V_{DD}$ falling Note 1 | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note 2 | $T_{PW}$ | | 300 | | | μs |

**Note 1.** However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in **2.4 AC Characteristics**.

**Note 2.** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 2.6.7 LVD circuit characteristics

### (1) Reset Mode and Interrupt Mode

**($T_A$ = -40 to +85°C, $V_{PDR} \le EV_{DD0} \le V_{DD} \le$ 5.5 V, $V_{SS} = EV_{SS0}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | Supply voltage level | $V_{LVD0}$ | Rising edge | 3.98 | 4.06 | 4.14 | V |
| | | | Falling edge | 3.90 | 3.98 | 4.06 | V |
| | | $V_{LVD1}$ | Rising edge | 3.68 | 3.75 | 3.82 | V |
| | | | Falling edge | 3.60 | 3.67 | 3.74 | V |
| | | $V_{LVD2}$ | Rising edge | 3.07 | 3.13 | 3.19 | V |
| | | | Falling edge | 3.00 | 3.06 | 3.12 | V |
| | | $V_{LVD3}$ | Rising edge | 2.96 | 3.02 | 3.08 | V |
| | | | Falling edge | 2.90 | 2.96 | 3.02 | V |
| | | $V_{LVD4}$ | Rising edge | 2.86 | 2.92 | 2.97 | V |
| | | | Falling edge | 2.80 | 2.86 | 2.91 | V |
| | | $V_{LVD5}$ | Rising edge | 2.76 | 2.81 | 2.87 | V |
| | | | Falling edge | 2.70 | 2.75 | 2.81 | V |
| | | $V_{LVD6}$ | Rising edge | 2.66 | 2.71 | 2.76 | V |
| | | | Falling edge | 2.60 | 2.65 | 2.70 | V |
| | | $V_{LVD7}$ | Rising edge | 2.56 | 2.61 | 2.66 | V |
| | | | Falling edge | 2.50 | 2.55 | 2.60 | V |
| | | $V_{LVD8}$ | Rising edge | 2.45 | 2.50 | 2.55 | V |
| | | | Falling edge | 2.40 | 2.45 | 2.50 | V |
| | | $V_{LVD9}$ | Rising edge | 2.05 | 2.09 | 2.13 | V |
| | | | Falling edge | 2.00 | 2.04 | 2.08 | V |
| | | $V_{LVD10}$ | Rising edge | 1.94 | 1.98 | 2.02 | V |
| | | | Falling edge | 1.90 | 1.94 | 1.98 | V |
| | | $V_{LVD11}$ | Rising edge | 1.84 | 1.88 | 1.91 | V |
| | | | Falling edge | 1.80 | 1.84 | 1.87 | V |
| | | $V_{LVD12}$ | Rising edge | 1.74 | 1.77 | 1.81 | V |
| | | | Falling edge | 1.70 | 1.73 | 1.77 | V |
| | | $V_{LVD13}$ | Rising edge | 1.64 | 1.67 | 1.70 | V |
| | | | Falling edge | 1.60 | 1.63 | 1.66 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

**(2) Interrupt & Reset Mode**

**($T_A$ = -40 to +85°C, $V_{PDR} \le EV_{DD0} \le V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Voltage detection threshold | $V_{LVDA0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 0, falling reset voltage | | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V |
| | | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V |
| | | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

## 2.6.8 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

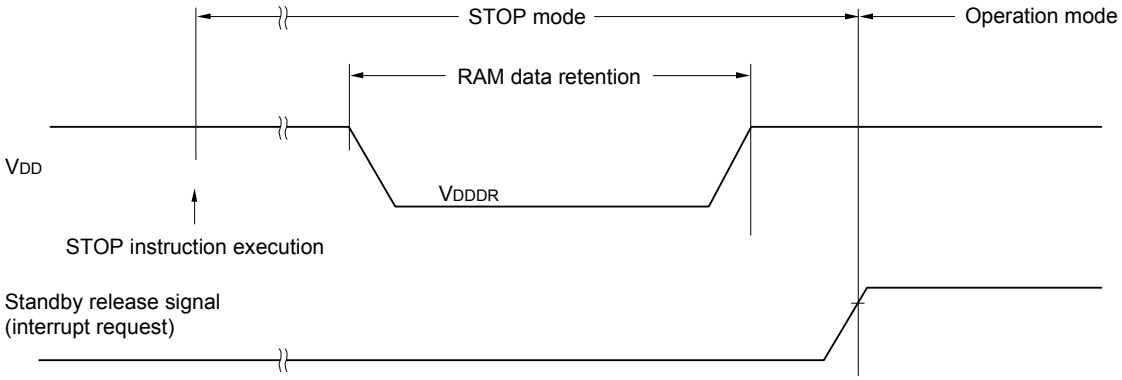
## 2.7 RAM Data Retention Characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0V))**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Notes 1, 2 | | 5.5 | V |

**Note 1.** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

**Note 2.** Enter STOP mode before the supply voltage falls below the recommended operating voltage.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | 1 | | 32 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years | $T_A$ = 85°C | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year | $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years | $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years | $T_A$ = 85°C | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

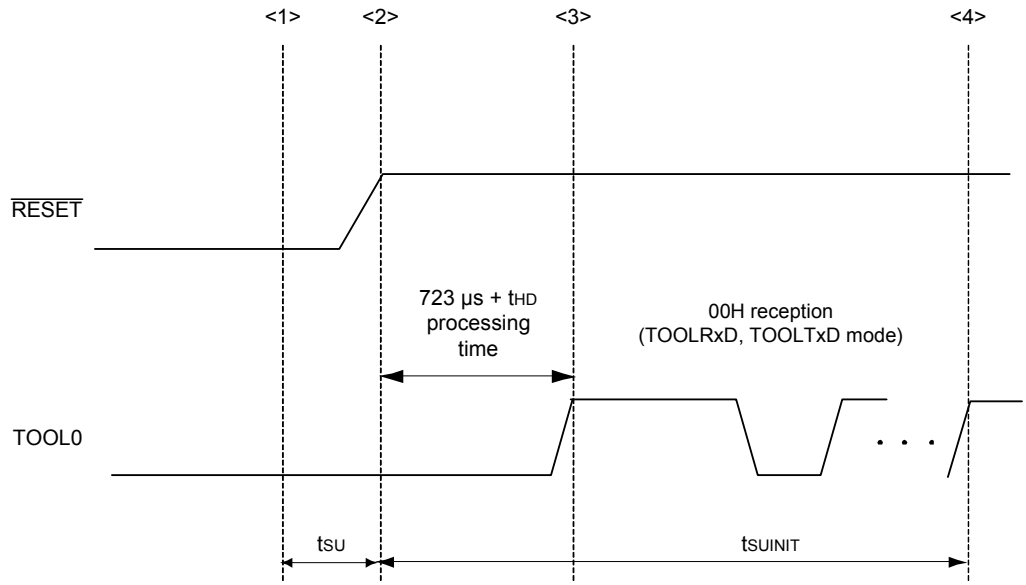
**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 2.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

$t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

# 3. ELECTRICAL SPECIFICATIONS (G: $T_A$ = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A$ = −40 to +105°C
R5F11BxxGxx

**Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. With products not provided with an $EV_{DD0}$, or $EV_{SS0}$ pin, replace $EV_{DD0}$ with $V_{DD}$, or replace $EV_{SS0}$ with $V_{SS}$.**

**Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G1F User's Manual.**

**Caution 4. Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark** When the products "G: Industrial applications" is used in the range of $T_A$ = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)**.

Operation of products rated “G: Industrial applications ($T_A$ = -40 to + 105°C)” at ambient operating temperatures above 85°C differs from that of products rated “A: Consumer applications” in the ways listed below.

| Parameter | A: Consumer applications | G: Industrial applications |
|---|---|---|
| Operating ambient temperature | $T_A$ = -40 to +85°C | $T_A$ = -40 to +105°C |
| Operating mode<br>Operating voltage range | HS (high-speed main) mode:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz<br>LS (low-speed main) mode:<br>1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz<br>LV (low-voltage main) mode:<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz | HS (high-speed main) mode only:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| High-speed on-chip oscillator clock accuracy | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±1.0% @ $T_A$ = -20 to +85°C<br>±1.5% @ $T_A$ = -40 to -20°C<br>2.4 V ≤ $V_{DD}$ < 1.8 V:<br>±5.0% @ $T_A$ = -20 to +85°C<br>±5.5% @ $T_A$ = -40 to -20°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±2.0% @ $T_A$ = +85 to +105°C<br>±1.0% @ $T_A$ = -20 to +85°C<br>±1.5% @ $T_A$ = -40 to -20°C |
| Serial array unit | UART<br>CSI: $f_{CLK}$/2 (16 Mbps supported), $f_{CLK}$/4<br>Simplified $I^2C$ communication | UART<br>CSI: $f_{CLK}$/4<br>Simplified $I^2C$ communication |
| IICA | Standard mode<br>Fast mode<br>Fast mode plus | Standard mode<br>Fast mode |
| Voltage detector | • Rising: 1.67 V to 4.06 V (14 stages)<br>• Falling: 1.63 V to 3.98 V (14 stages) | • Rising: 2.61 V to 4.06 V (8 stages)<br>• Falling: 2.55 V to 3.98 V (8 stages) |

**Remark** The electrical characteristics of products rated “G: Industrial applications ($T_A$ = -40 to + 105°C)” at ambient operating temperatures above 85°C differ from those of products “A: Consumer applications”. For details, refer to **3.1** to **3.10**.

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings** **(1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to +6.5 | V |
| | $EV_{DD0}$ | | -0.5 to +6.5 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to +2.8 and -0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27 | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI24 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $AV_{REF}(+)$ +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI7 | -0.3 to $V_{DD}$ +0.3 and -0.3 to $AV_{REF}(+)$ +0.3 Notes 2, 3 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 6.5 V or lower.

**Note 3.** Do not exceed $AV_{REF}$ (+) + 0.3 V in case of A/D conversion target pin.

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF}$ (+): + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Absolute Maximum Ratings** **(2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | -40 | mA |
| | | Total of all pins -170 mA | P00 to P04, P40 to P43,P120, P130, P140, P141 | -70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147 | -100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40-P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147 | 40 | mA |
| | | Total of all pins 170 mA | P00 to P04, P40 to P47, P120, P130, P140, P141 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.2 Oscillator Characteristics

### 3.2.1 X1, XT1 characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Resonator | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$) Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | |
| XT1 clock oscillation frequency ($f_{XT}$) Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G1F User's Manual.

### 3.2.2 On-chip oscillator characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1 | | 16 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | $T_A$ = +85 to +105°C | -2 | | 2 | % |
| | | $T_A$ = -20 to +85°C | -1 | | 1 | % |
| | | $T_A$ = -40 to -20°C | -1.5 | | 1.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | -15 | | +15 | % |

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | | | | -3.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -10.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | -5.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P53, P70 to P77, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -19.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | -10.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | -60.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27 | | | | -0.1 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | -1.5 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $EV_{DD0}$, $V_{DD}$ pins to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77,P120, P130, P140, P141, P146, P147 | | | | 8.5 Note 2 | mA |
| | | Per pin for P60 to P63 | | | | 15.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 15.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 1.8 V | | | 9.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 35.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 1.8 V | | | 20.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 80.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27 | | | | 0.4 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$ and $V_{SS}$ pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | Normal input buffer | 0.8 $EV_{DD0}$ | | $EV_{DD0}$ | V |
| | $V_{IH2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P50, P53 to P55, | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 2.2 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 2.0 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD0}$ < 3.3 V | 1.5 | | $EV_{DD0}$ | V |
| | $V_{IH3}$ | P20 to P27 (when P20 is used as a port pin) | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60 to P63 | | 0.7 $EV_{DD0}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P123, P137, EXCLK, EXCLKS, $\overline{RESET}$ (when P20 is used as INTP11 pin) | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | Normal input buffer | 0 | | 0.2 $EV_{DD0}$ | V |
| | $V_{IL2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P50, P53 to P55, | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD0}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27 (when P20 is used as a port pin) | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL4}$ | P60 to P63 | | 0 | | 0.3 $EV_{DD0}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$ (when P20 is used as INTP11 pin) | | 0 | | 0.2 $V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 is $EV_{DD0}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -3.0 mA | $EV_{DD0}$ - 0.7 | | | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -2.0 mA | $EV_{DD0}$ - 0.6 | | | V |
| | | | 2.4 V ≤ $EV_{DD0}$ < 5.5 V, $I_{OH1}$ = -1.5 mA | $EV_{DD0}$ - 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = -100 μA | $V_{DD}$ - 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 μA | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |

**Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | $V_I$ = $EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | $V_I$ = $EV_{SS0}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P20 to P27, P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| On-chip pull-up resistance | $R_U$ | P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.3.2 Supply current characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.2 | 9.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.2 | 9.3 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 8.7 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 8.7 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.1 | 7.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.1 | 7.3 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.8 | 6.7 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.8 | 6.7 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.9 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.3 | 5.7 | mA |
| | | | | | | Resonator connection | | 3.5 | 5.8 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.3 | 5.7 | |
| | | | | | | Resonator connection | | 3.5 | 5.8 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.0 | 3.4 | |
| | | | | | | Resonator connection | | 2.1 | 3.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.0 | 3.4 | |
| | | | | | | Resonator connection | | 2.1 | 3.5 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.7 | 6.1 | µA |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.7 | 6.1 | |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.8 | 6.7 | |
| | | | | | | Resonator connection | | 4.8 | 6.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 7.2 | 21.0 | |
| | | | | | | Resonator connection | | 7.3 | 21.1 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 4.36 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 4.36 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.54 | 3.67 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.54 | 3.67 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.42 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.42 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 2.85 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 2.85 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.40 | 2.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.40 | 2.08 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 2.45 | mA |
| | | | | | Resonator connection | | 0.49 | 2.57 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 2.45 | |
| | | | | | Resonator connection | | 0.49 | 2.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.30 | 1.36 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.30 | 1.36 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.25 | 0.57 | µA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.36 | 1.17 | |
| | | | | | Resonator connection | | 0.59 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.49 | 1.97 | |
| | | | | | Resonator connection | | 0.72 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 0.97 | 3.37 | |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +105°C | Square wave input | | 3.20 | 17.10 | |
| | | | | | Resonator connection | | 3.40 | 17.50 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.18 | 0.51 | µA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 3.10 | 17.00 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.2 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75 | | μA |
| D/A converter operating current | $I_{DAC}$ Notes 1, 11 | Per D/A converter channel | | | | 1.5 | mA |
| PGA operating current | | Operation | | | 480 | 700 | μA |
| Comparator operating current | $I_{CMP}$ Notes 1, 12 | Operation (per comparator channel, constant current for comparator included) | When the internal reference voltage is not in use | | 50 | 100 | μA |
| | | | When the internal reference voltage is in use | | 60 | 110 | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 7 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.2 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 8 | | | | 2.50 | 12.2 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 2.04 | |
| | | CSI/UART operation | | | 0.70 | 1.54 | |
| | | DTC operation | | | 3.10 | | |

**Note 1.** Current flowing to $V_{DD}$.

**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**Note 8.** Current flowing during programming of the data flash.

**Note 9.** Current flowing during self-programming.

**Note 10.** For shift time to the SNOOZE mode, see **26.3.3 SNOOZE mode** in the RL78/G1F User's Manual.

**Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DAC}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit is in operation.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 3.4 AC Characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 30 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI03 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 Note | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 100 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 300 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{TJIH}$, $t_{TJIL}$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 40 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 120 | | | ns |

**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MIN. 125 ns

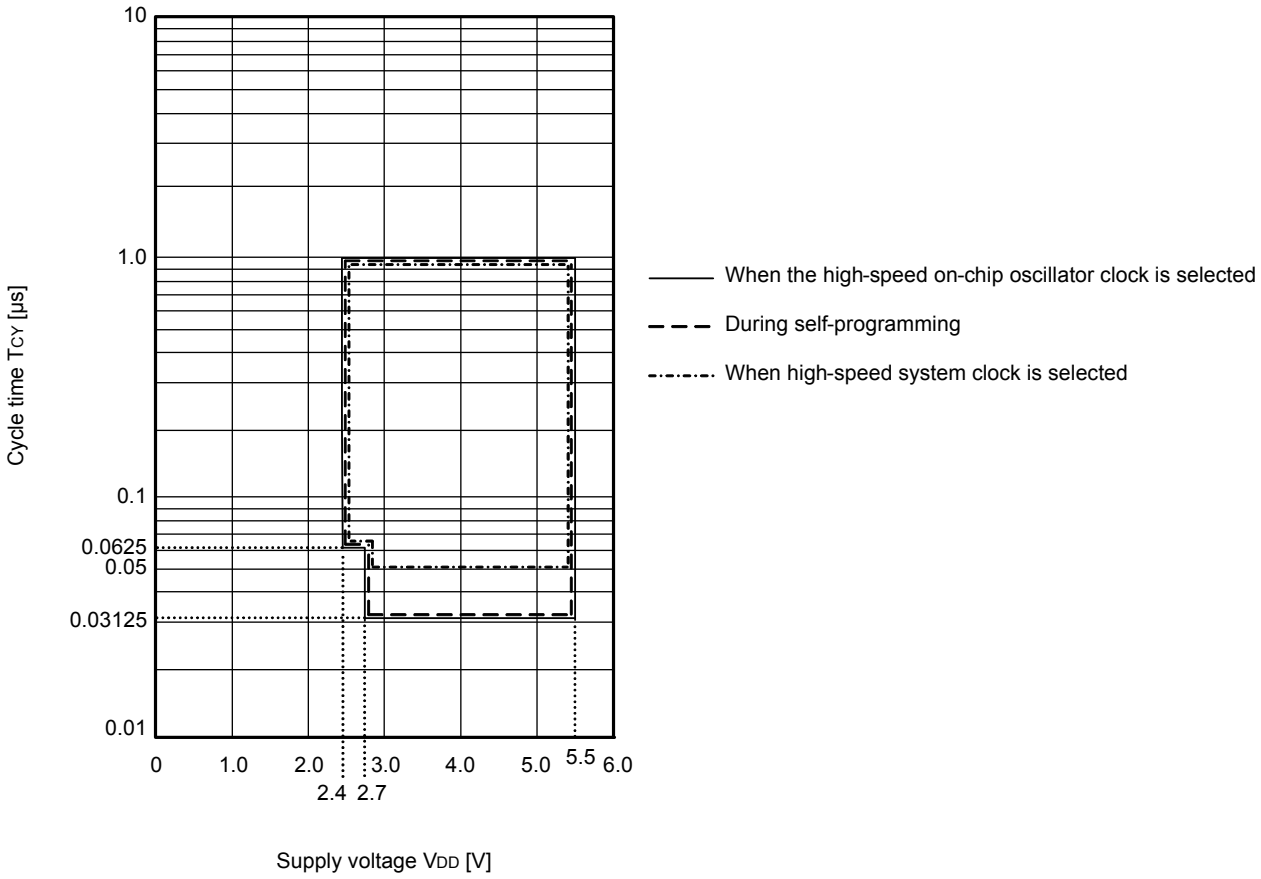
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

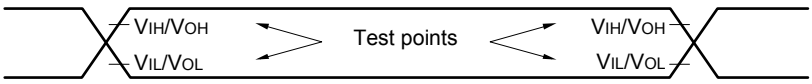
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Timer RD input high-level width, low-level width | $t_{TDIH}$, $t_{TDIL}$ | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | | 3/$f_{CLK}$ | | | ns |
| Timer RD forced cutoff signal input low-level width | $t_{TDSIL}$ | P130/INTP0 | 2MHz < $f_{CLK}$ ≤ 32 MHz | 1 | | | µs |
| | | | $f_{CLK}$ ≤ 2 MHz | 1/$f_{CLK}$ + 1 | | | |
| Timer RG input high-level width, low-level width | $t_{TGIH}$, $t_{TGIL}$ | TRGIOA, TRGIOB | | 2.5/$f_{CLK}$ | | | ns |
| TO00 to TO03, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency | $f_{TO}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | µs |
| | | INTP1 to INTP11 | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

Minimum Instruction Execution Time during Main System Clock Operation

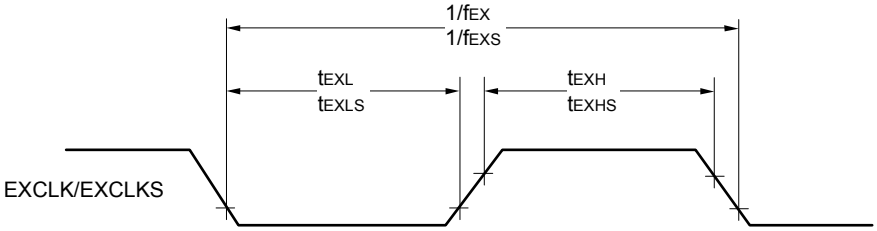
TCY vs VDD (HS (high-speed main) mode)



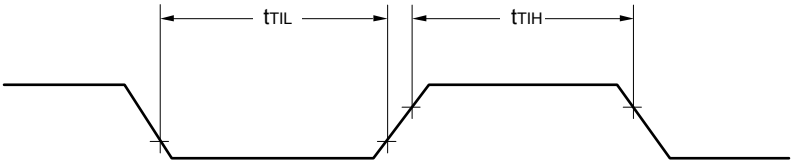
AC Timing Test Points



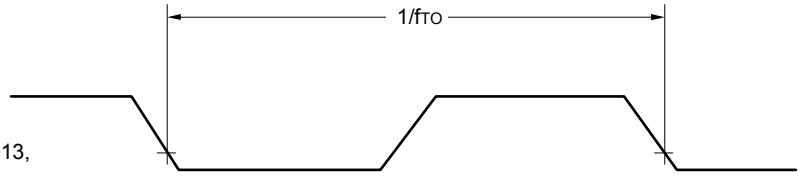

External System Clock Timing



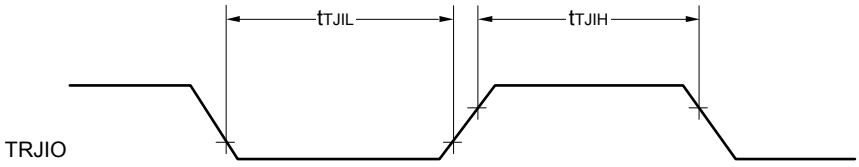

TI/TO Timing

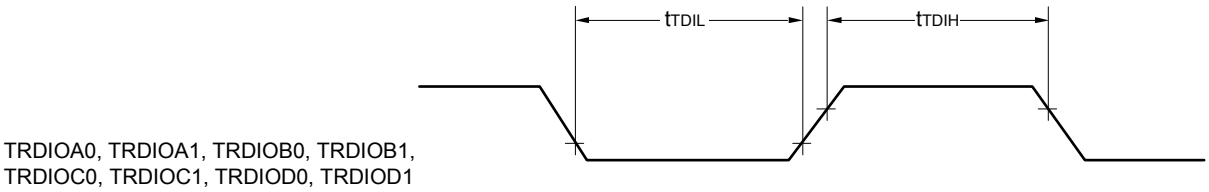


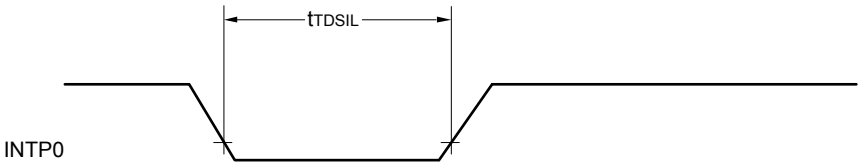

TI00 to TI03, TI10 to TI13

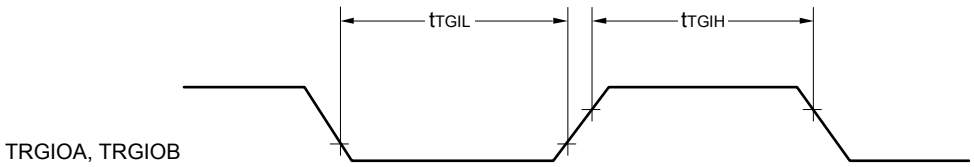



TO00 to TO03, TO10 to TO13,
TRJIO0, TRJO0,
TRDIOA0, TRDIOA1,
TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1,
TRDIOD0, TRDIOD1,
TRGIOA, TRGIOB

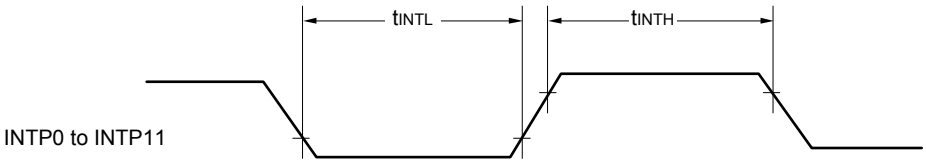

tTJIL
tTJIH
TRJIO


tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1

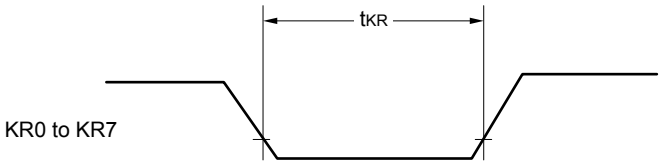

tTDSIL
INTP0


tTGIL
tTGIH
TRGIOA, TRGIOB

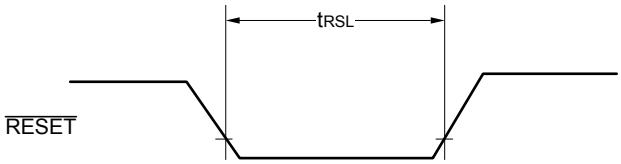
Interrupt Request Input Timing




Key Interrupt Input Timing

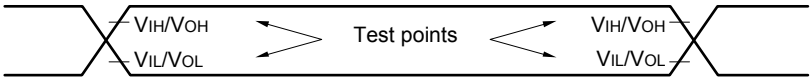



$\overline{\text{RESET}}$ Input Timing



## 3.5 Peripheral Functions Characteristics

AC Timing Test Points




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/12 Note 2 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |

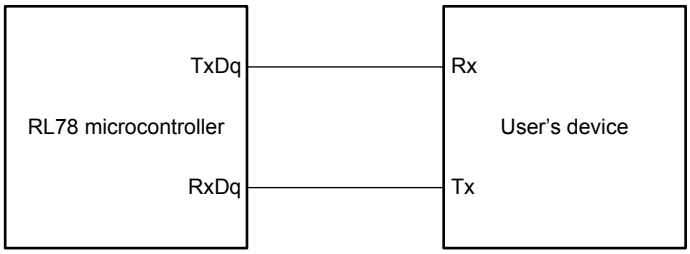
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX.1.3 Mbps

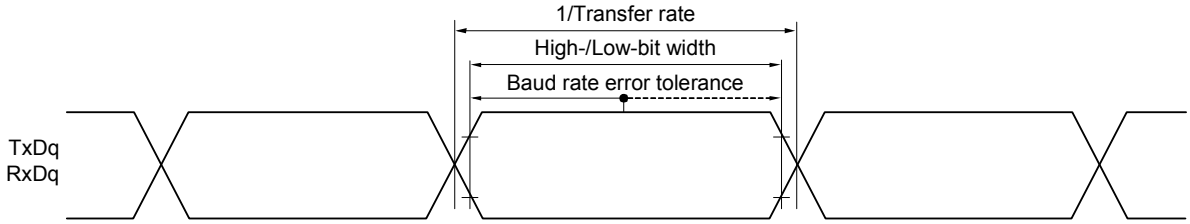
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

### (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 76 | | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 113 | | |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 20 pF Note 4 | | | 50 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 , 5, 7)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 14 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 16 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 66 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 113 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3, 5, 7)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10, 11))

### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

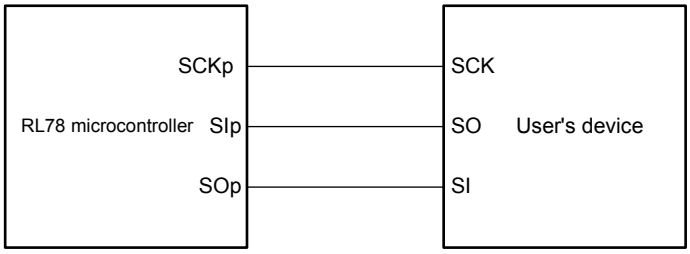
**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| $\overline{SSI00}$ setup time | $t_{SSIK}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | ns |
| $\overline{SSI00}$ hold time | $t_{KSSI}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | ns |

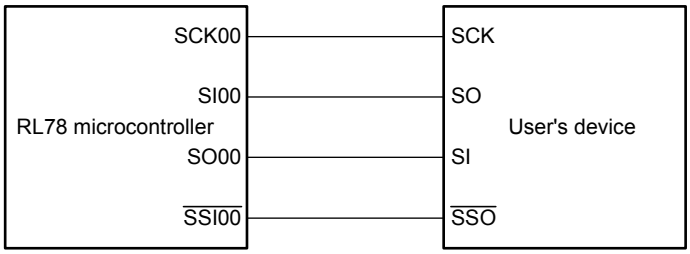
**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

**CSI mode connection diagram (during communication at same potential)**

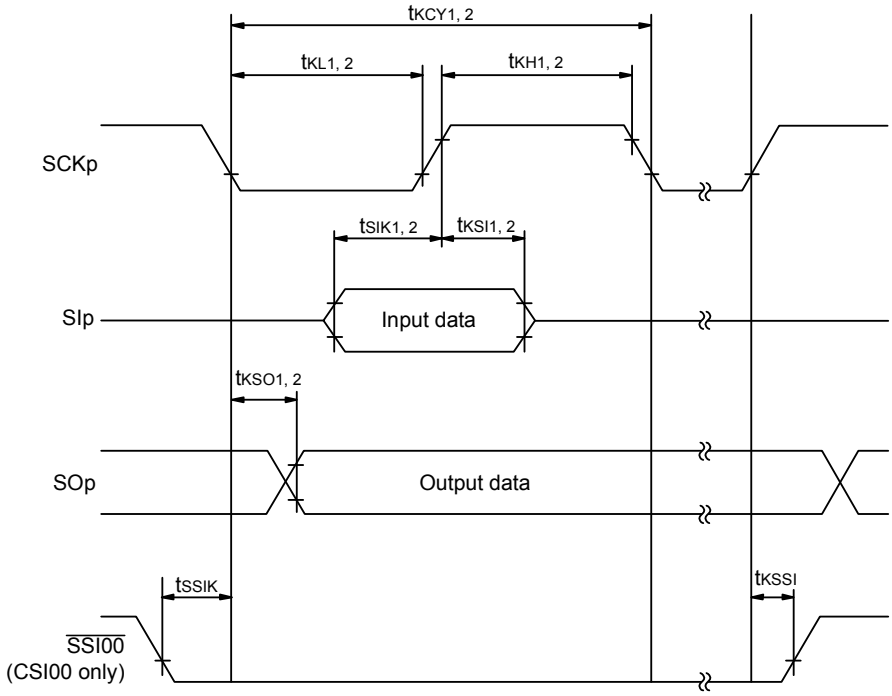



**CSI mode connection diagram (during communication at same potential)**
**(Slave Transmission of slave select input function (CSI00))**

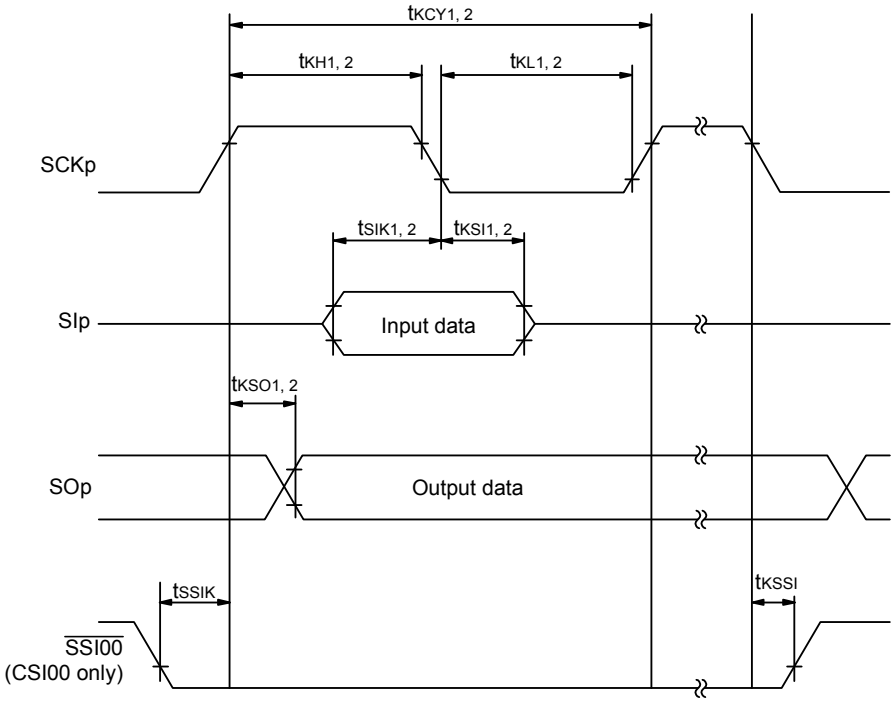



**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

### (4) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 220 Note 2 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

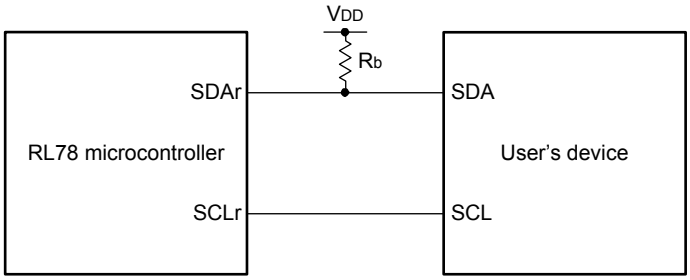
**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

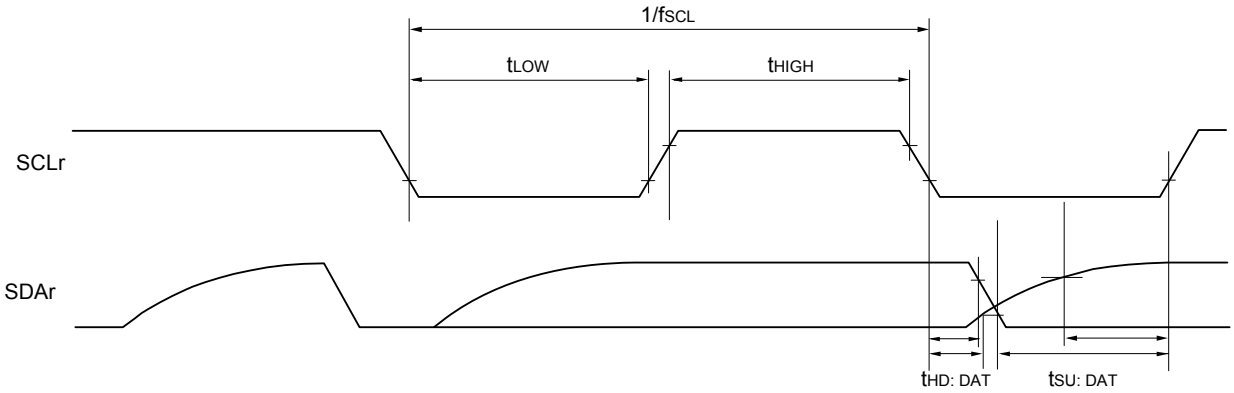
**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 3, 5, 7),
h: POM number (h = 0, 1, 3, 5, 7)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11)

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate | | reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 1.3 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V: MAX. 1.3 Mbps

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$ [V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5, 7)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate | | transmission | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.6 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | Note 5 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 6 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 4.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

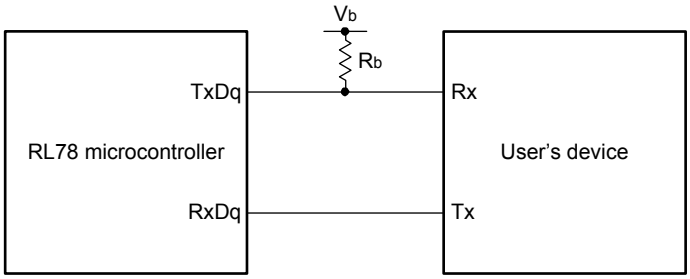
* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 6.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

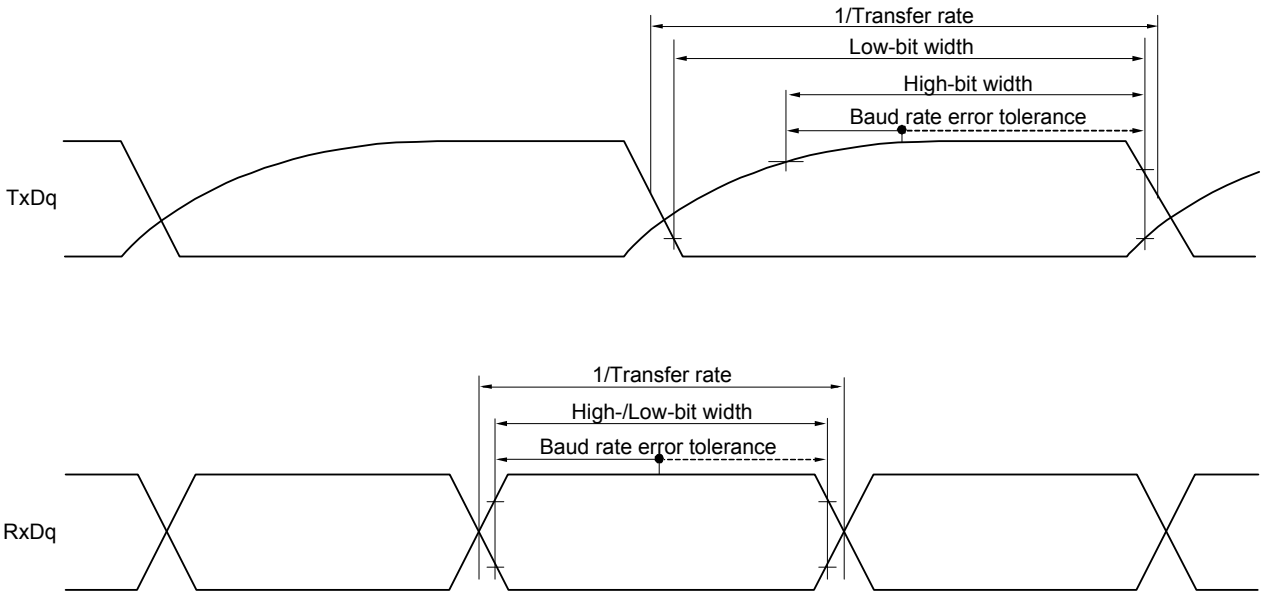
**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5, 7)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 150 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 340 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 100 | | ns |

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(3/3)**

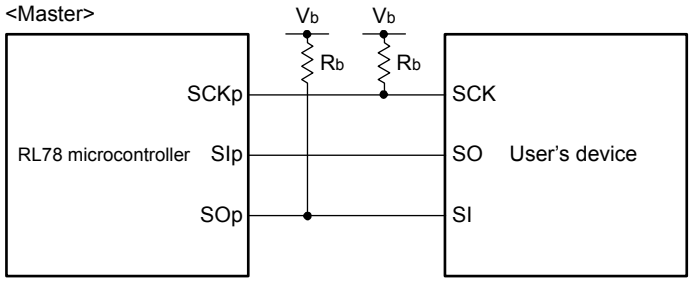
| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential**



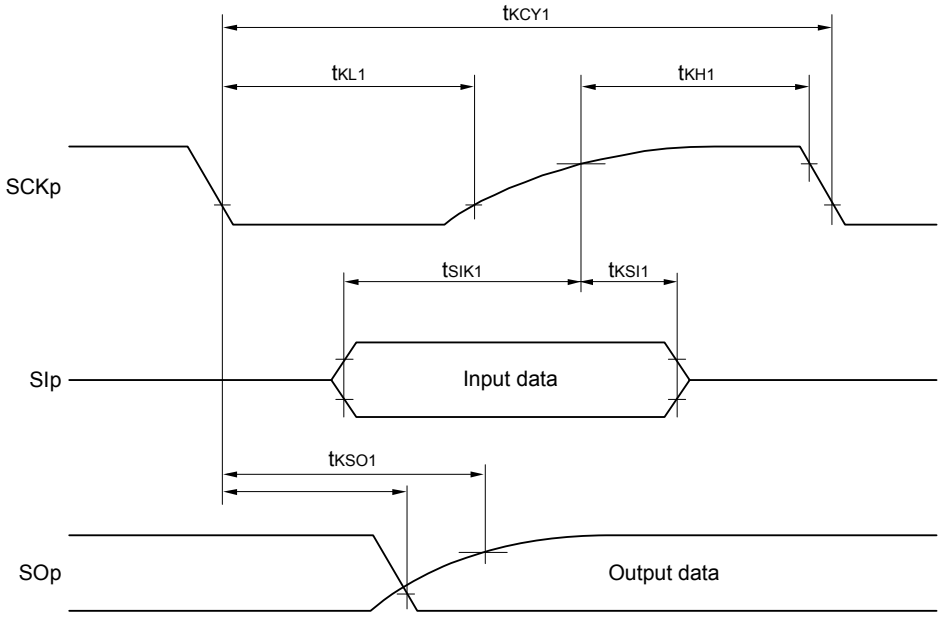

**Remark 1.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

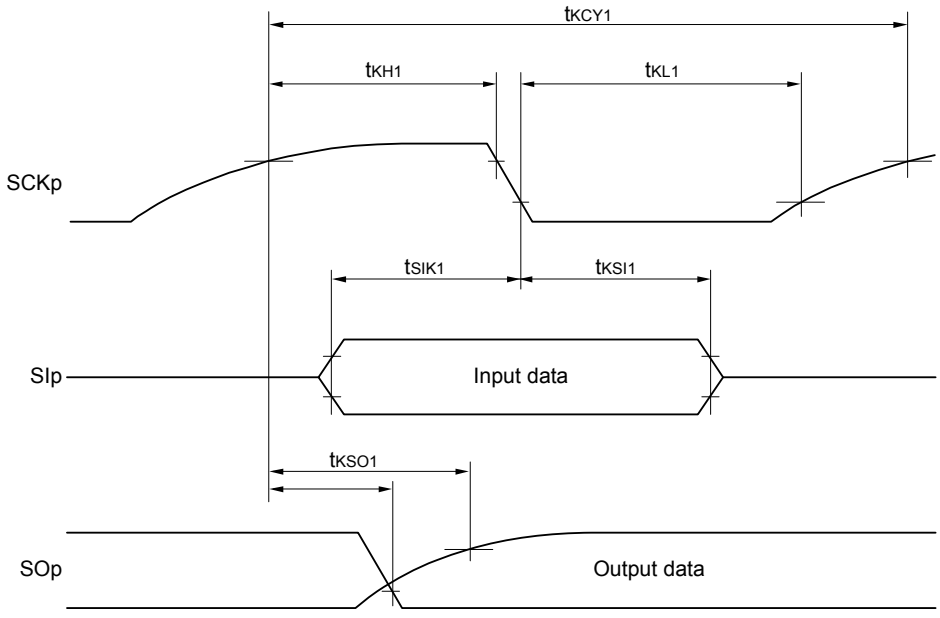
**Remark 3.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Remark 4.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**Remark 3.** Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), mn = 00, 01, 02, 10)

### (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 28/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 40/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 24 MHz < $f_{MCK}$ | 96/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_v$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

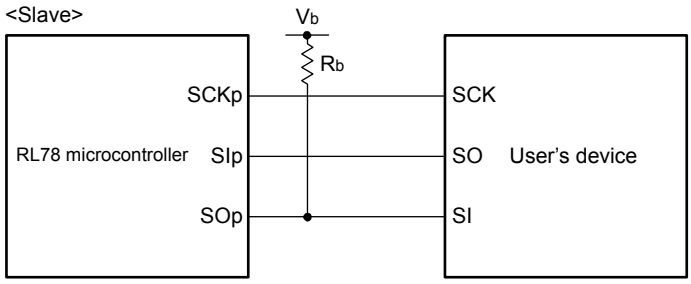
**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 5.** **Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output ($V_{DD}$ tolerance (for the 48, 32, 24-pin products)/$EV_{DD}$ tolerance (for the 64, 36-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**CSI mode connection diagram (during communication at different potential)**



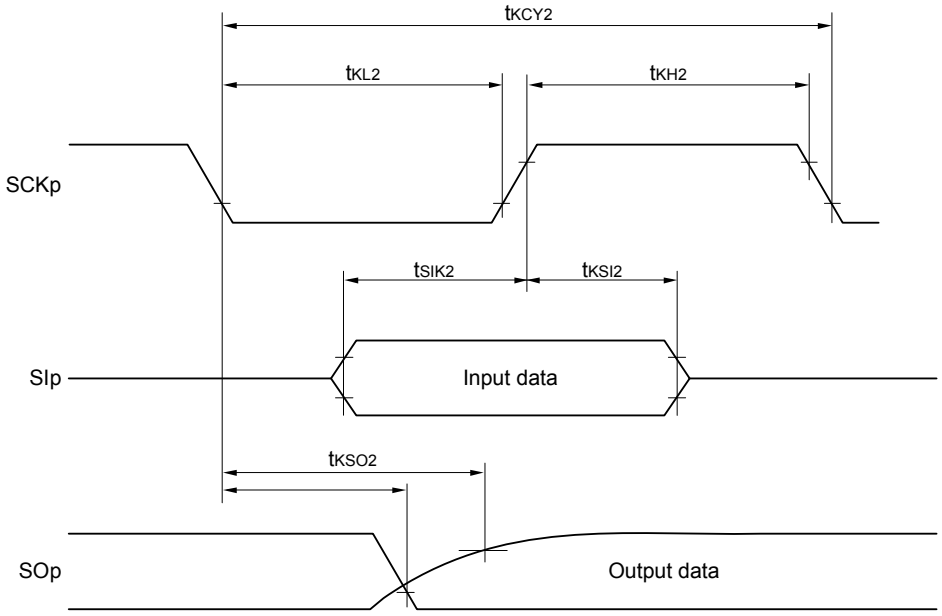

**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

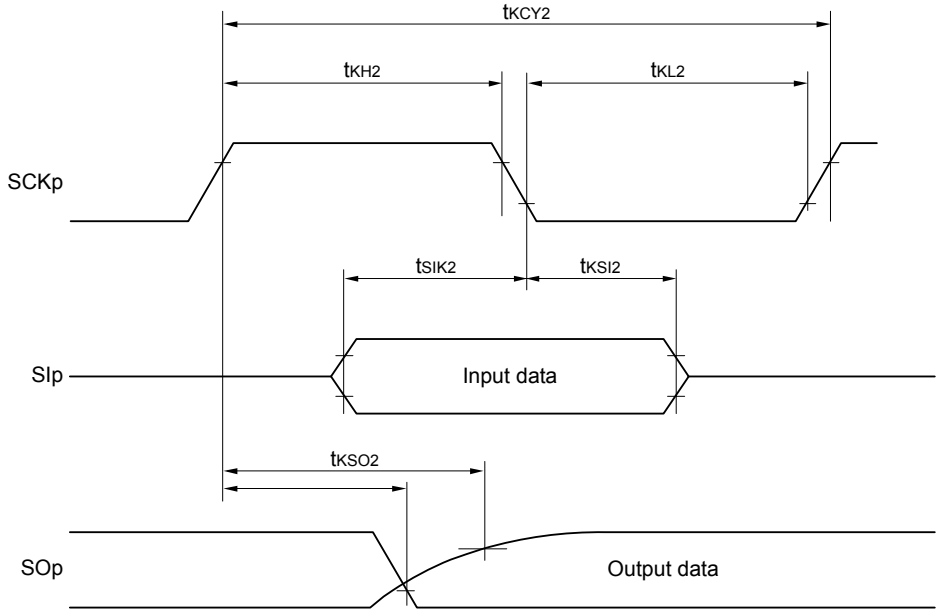
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10))

**Remark 4.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 100 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 100 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 4600 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 620 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 500 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 2700 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1830 | | ns |

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 2 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 570 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 1420 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

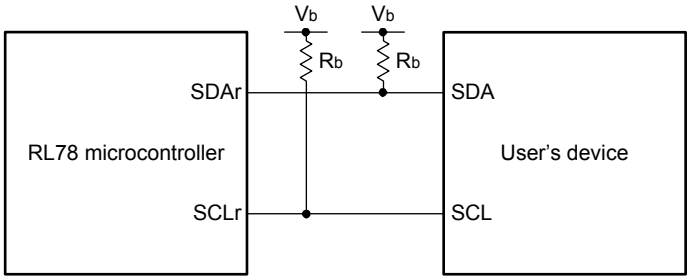
**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

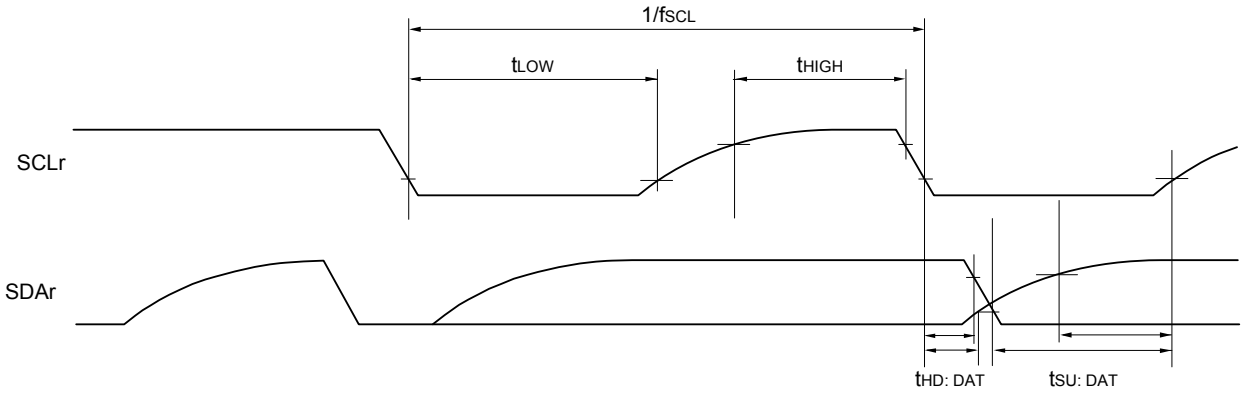
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/$EV_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remark 1.** Rb[Ω]: Communication line (SDAr, SCLr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance, Vb[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20), g: PIM, POM number (g = 0, 1, 3, 5, 7)

**Remark 3.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10)

## 3.5.2 Serial interface IICA

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard mode | | Fast mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | — | — | 0 | 400 | kHz |
| | | Standard mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | — | — | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | | 4.7 | | 0.6 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | | 4.0 | | 0.6 | | µs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | | 4.7 | | 1.3 | | µs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | | 4.0 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | | 0 | 3.45 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | | 4.0 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

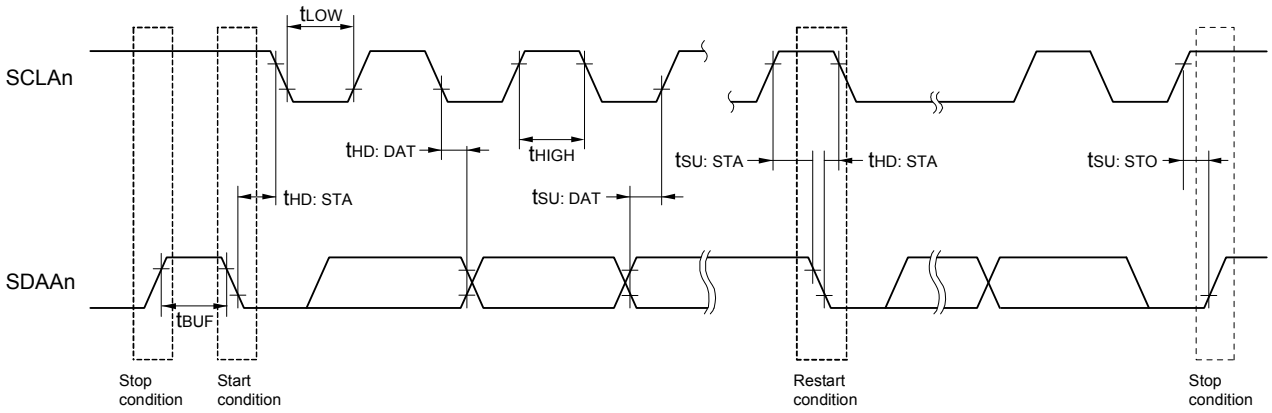
**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark** n = 0, 1

## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input channel | Reference voltage (+) = $AV_{REFP}$ Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$ Reference voltage (-) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$ Reference voltage (-)= $AV_{REFM}$ |
|---|---|---|---|
| ANI0 to ANI7 | Refer to **3.6.1 (1)**. | Refer to **3.6.1 (3)**. | Refer to **3.6.1 (4)**. |
| ANI16 to ANI24 | Refer to **3.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **3.6.1 (1)**. | | — |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI7, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI7 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage output<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI24**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target ANI pin: ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI24 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $EV_{DD0}$ ≤ $AV_{REFP}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI7, ANI16 to ANI24, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (-) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI14, ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI7 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI24 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 3 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 3 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI7, ANI16 to ANI24**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (-) = $AV_{REFM}$ = 0 V Note 4, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**Note 4.** When reference voltage (-) = $V_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

### 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 3.6.3 D/A converter characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{SS0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Settling time | $t_{SET}$ | Cload = 20 pF | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 3 | μs |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 6 | μs |

## 3.6.4 Comparator

**($T_A$ = -40 to +105°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IOCMP}$ | | | | ±5 | ±40 | mV |
| Input voltage range | $V_{ICMP}$ | | | 0 | | $V_{DD}$ | V |
| Internal reference voltage deviation | $\Delta V_{IREF}$ | CmRVM register value : 7FH to 80H (m = 0, 1) | | | | ±2 | LSB |
| | | Other than above | | | | ±1 | LSB |
| Response Time | $t_{CR}$, $t_{CF}$ | Input amplitude±100mV | | | 70 | 150 | ns |
| Operation stabilization time[Note 1] | $t_{CMP}$ | CMPn = 0→1 | $V_{DD}$ = 3.3 to 5.5 V | | | 1 | µs |
| | | | $V_{DD}$ = 2.7 to 3.3 V | | | 3 | µs |
| Reference voltage stabilization wait time | $t_{VR}$ | CVRE : 0→1[Note 2] | | | | 20 | µs |
| Operation current | $I_{CMPDD}$ | Separately, it is defined as the operation current of peripheral functions. | | | | | |

**Note 1.** Time taken until the comparator satisfies the DC/AC characteristics after the comparator operation enable signal is switched (CMPnEN = 0 → 1).

**Note 2.** Enable comparator output (CnOE bit = 1; n = 0 to 1) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; m = 0 to 1) and waiting for the operation stabilization time to elapse.

## 3.6.5 PGA

**($T_A$ = -40 to +105°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IOPGA}$ | | | | | ±10 | mV |
| Input voltage range | $V_{IPGA}$ | | | 0 | | 0.9 × $V_{DD}$/ Gain | V |
| Output voltage range | $V_{IOHPGA}$ | | | 0.93 × $V_{DD}$ | | | V |
| | $V_{IOLPGA}$ | | | | | 0.07 × $V_{DD}$ | V |
| Gain error | | x4, x8 | | | | ±1 | % |
| | | x16 | | | | ±1.5 | % |
| | | x32 | | | | ±2 | % |
| Slew rate | $SR_{RPGA}$ | Rising When Vin= 0.1$V_{DD}$/gain to 0.9$V_{DD}$/gain. 10 to 90% of output voltage amplitude | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (Other than x32) | 3.5 | | | V/µs |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 4.0V | 0.5 | | | |
| | $SR_{FPGA}$ | Falling When Vin= 0.1$V_{DD}$/gain to 0.9$V_{DD}$/gain. 90 to 10% of output voltage amplitude | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (Other than x32) | 3.5 | | | |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 4.0V | 0.5 | | | |
| Reference voltage stabilization wait time-[Note 1] | $t_{PGA}$ | x4, x8 | | | | 5 | µs |
| | | x16, x32 | | | | 10 | µs |
| Operation current | $I_{PGADD}$ | Separately, it is defined as the operation current of peripheral functions. | | | | | |

**Note 1.** Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

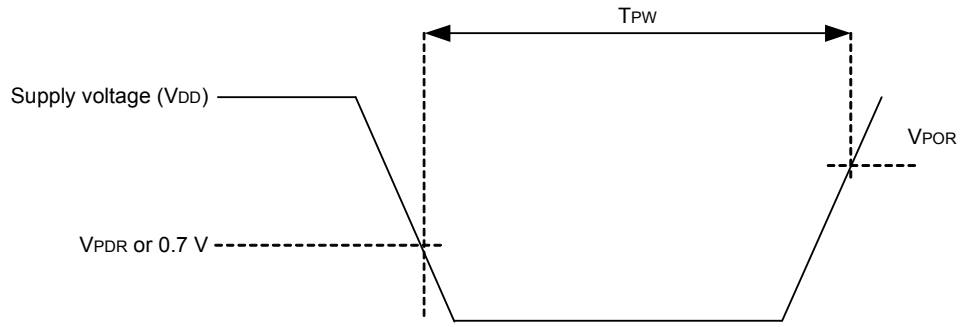
### 3.6.6 POR circuit characteristics

**(TA = -40 to +105°C, Vss = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power on/down reset threshold | VPOR | Voltage threshold on VDD rising | 1.45 | 1.51 | 1.55 | V |
| | VPDR | Voltage threshold on VDD falling Note 1 | 1.44 | 1.50 | 1.54 | V |
| Minimum pulse width Note 2 | TPW | | 300 | | | μs |

**Note 1.** However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in **3.4 AC Characteristics**.

**Note 2.** Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 3.6.7 LVD circuit characteristics

**(1) Reset Mode and Interrupt Mode**

**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | Supply voltage level | $V_{LVD0}$ | Rising edge | 3.90 | 4.06 | 4.22 | V |
| | | | Falling edge | 3.83 | 3.98 | 4.13 | V |
| | | $V_{LVD1}$ | Rising edge | 3.60 | 3.75 | 3.90 | V |
| | | | Falling edge | 3.53 | 3.67 | 3.81 | V |
| | | $V_{LVD2}$ | Rising edge | 3.01 | 3.13 | 3.25 | V |
| | | | Falling edge | 2.94 | 3.06 | 3.18 | V |
| | | $V_{LVD3}$ | Rising edge | 2.90 | 3.02 | 3.14 | V |
| | | | Falling edge | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | Rising edge | 2.81 | 2.92 | 3.03 | V |
| | | | Falling edge | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | Rising edge | 2.70 | 2.81 | 2.92 | V |
| | | | Falling edge | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | Rising edge | 2.61 | 2.71 | 2.81 | V |
| | | | Falling edge | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | Rising edge | 2.51 | 2.61 | 2.71 | V |
| | | | Falling edge | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

**(2) Interrupt & Reset Mode**

**($T_A$ = -40 to +105°C, $V_{PDR} \le V_{DD} \le$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

## 3.6.8 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $SV_{DD}$ | | | | 54 | V/ms |

**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

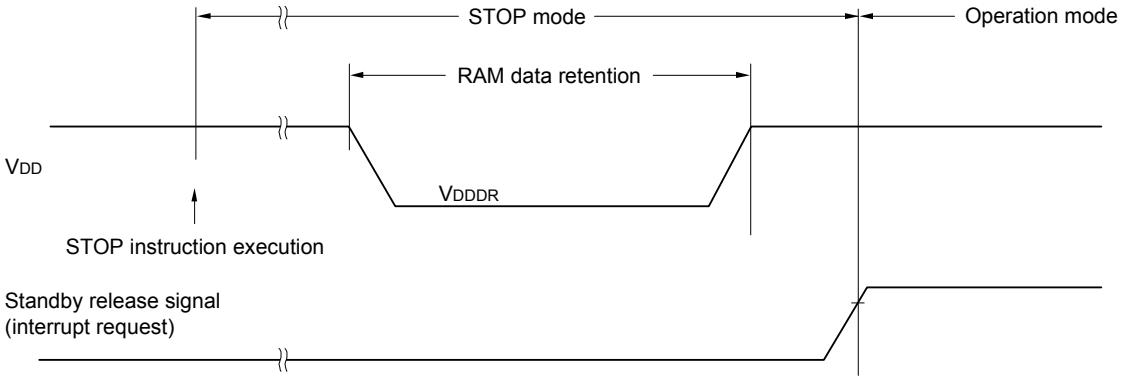
## 3.7 RAM Data Retention Characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44 Notes 1, 2 | | 5.5 | V |

**Note 1.** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

**Note 2.** Enter STOP mode before the supply voltage falls below the recommended operating voltage.




## 3.8 Flash Memory Programming Characteristics

**($T_A$ = -40 to +105°C, 2.4 V $\le V_{DD} \le$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | 2.4 V $\le V_{DD} \le$ 5.5 V | 1 | | 32 | MHz |

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years | $T_A$ = 85°C | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year | $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years | $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years | $T_A$ = 85°C | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 3.9 Dedicated Flash Memory Programmer Communication (UART)

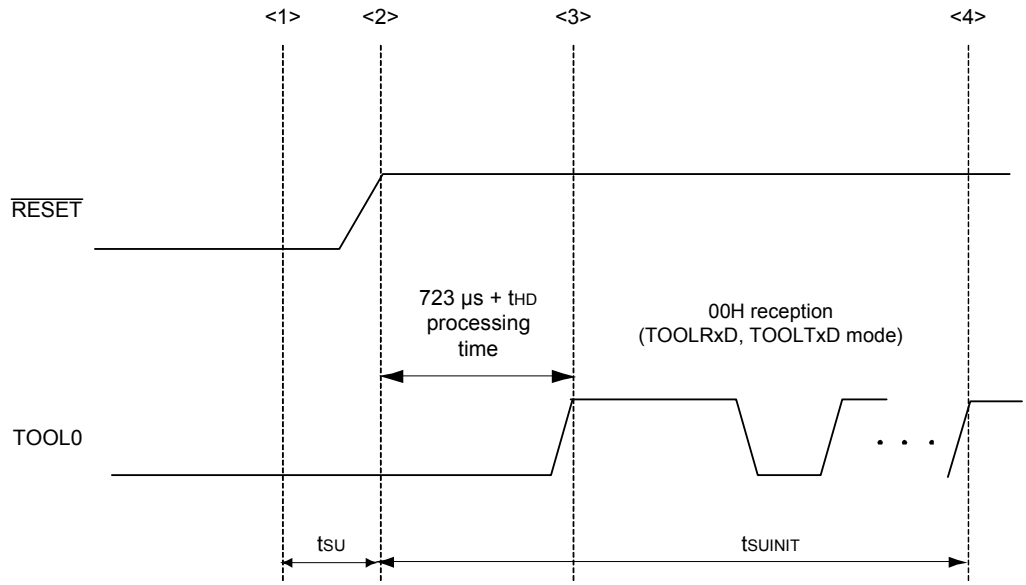
**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 3.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

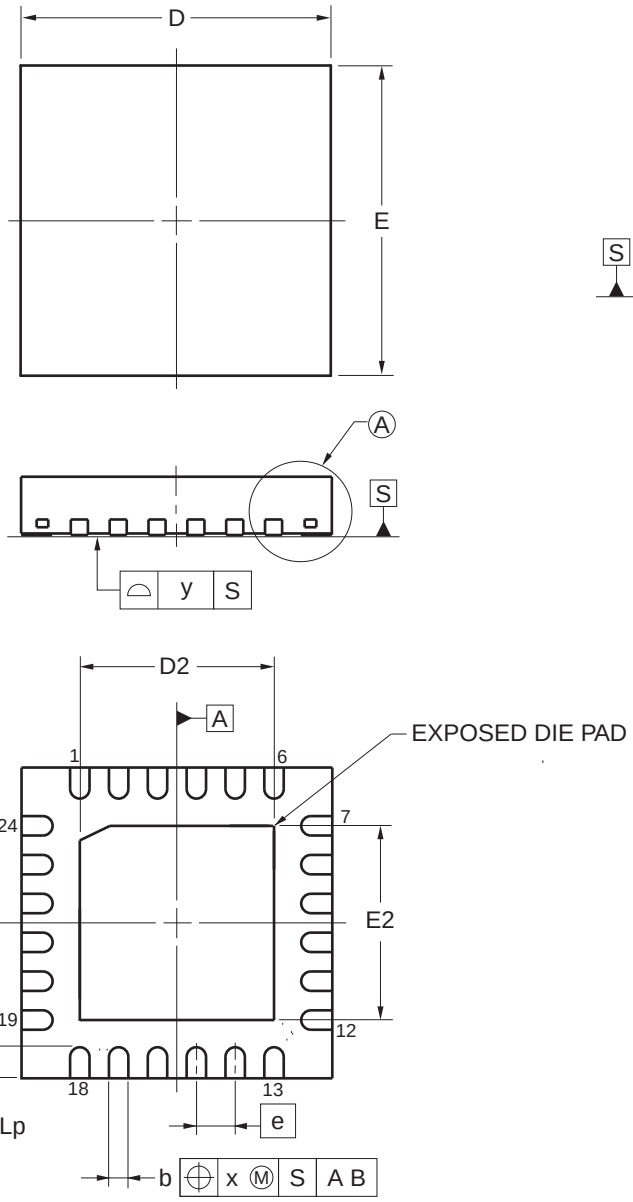
**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

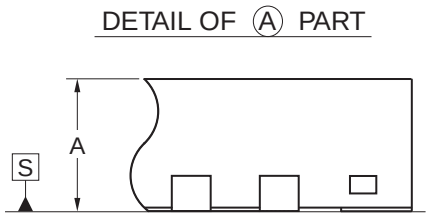
# 4. PACKAGE DRAWINGS

## 4.1 24-pin products

R5F11B7CANA, R5F11B7EANA, R5F11B7CGNA, R5F11B7EGNA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-1 | 0.04 |




(UNIT:mm)

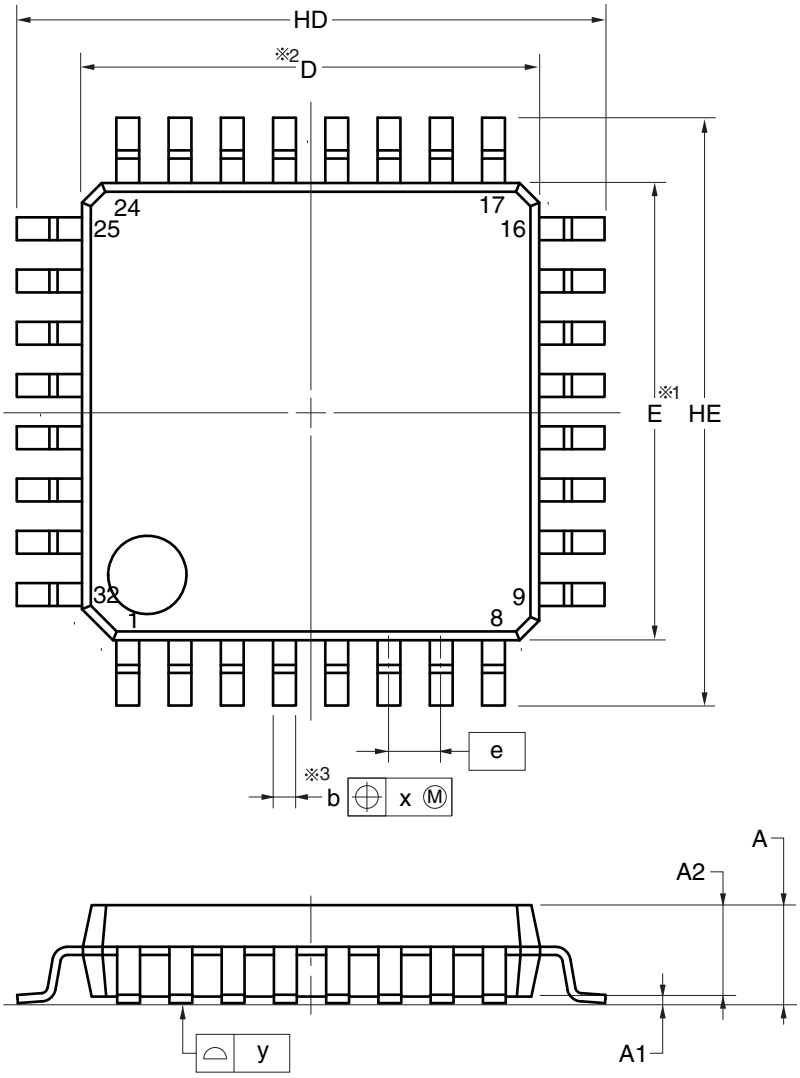
| ITEM | DIMENSIONS |
|---|---|
| D | 4.00±0.05 |
| E | 4.00±0.05 |
| A | 0.75±0.05 |
| b | $0.25^{+0.05}_{-0.07}$ |
| e | 0.50 |
| Lp | 0.40±0.10 |
| x | 0.05 |
| y | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 2.45 | 2.50 | 2.55 | 2.45 | 2.50 | 2.55 |

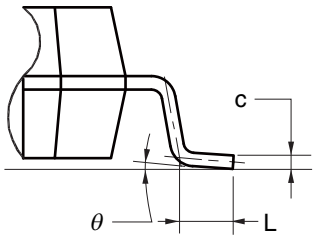
## 4.2 32-pin products

R5F11BBCAFP, R5F11BBEAFP, R5F11BBCGFP, R5F11BBEGFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP32-7x7-0.80 | PLQP0032GB-A | P32GA-80-GBT-1 | 0.2 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.10 |
| E | 7.00±0.10 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.40 |
| b | 0.37±0.05 |
| c | 0.145±0.055 |
| L | 0.50±0.20 |
| θ | 0° to 8° |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |

**NOTE**

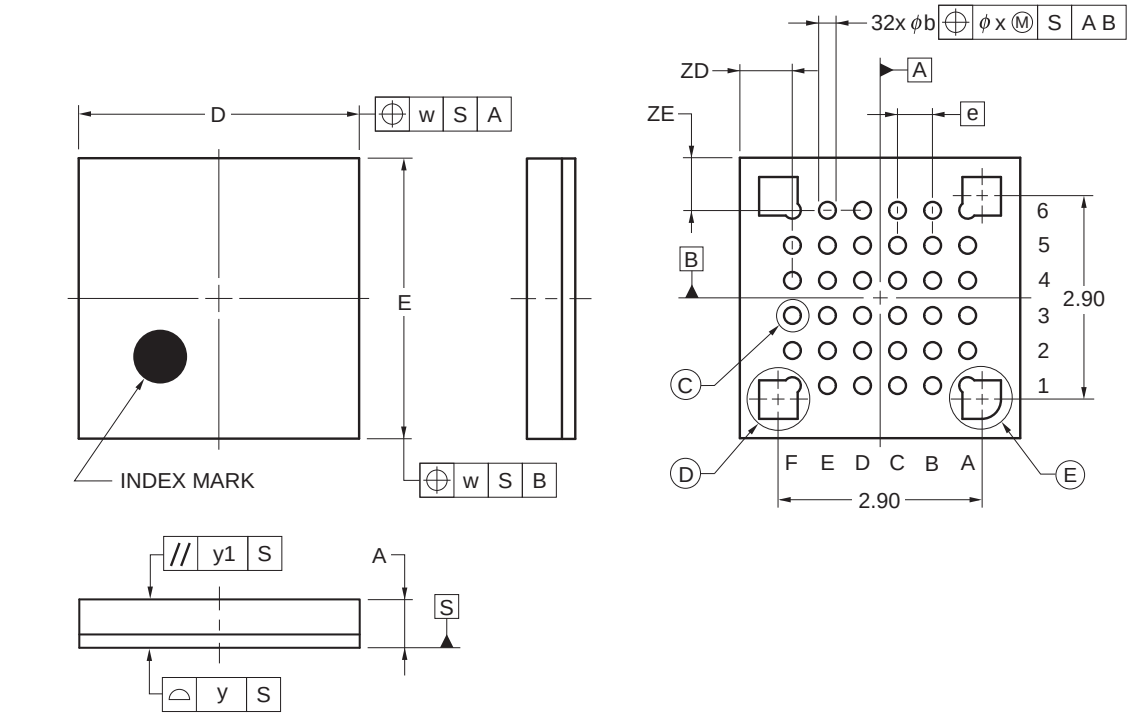
1.Dimensions "※1" and "※2" do not include mold flash.

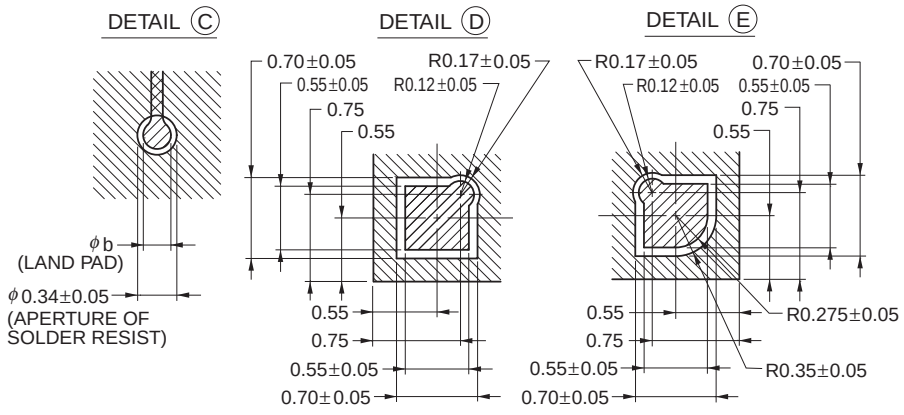
2.Dimension "※3" does not include trim offset.

## 4.3 36-pin products

R5F11BCCALA, R5F11BCEALA, R5F11BCCGLA, R5F11BCEGLA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-WFLGA36-4x4-0.50 | PWLG0036KA-A | P36FC-50-AA4-2 | 0.023 |



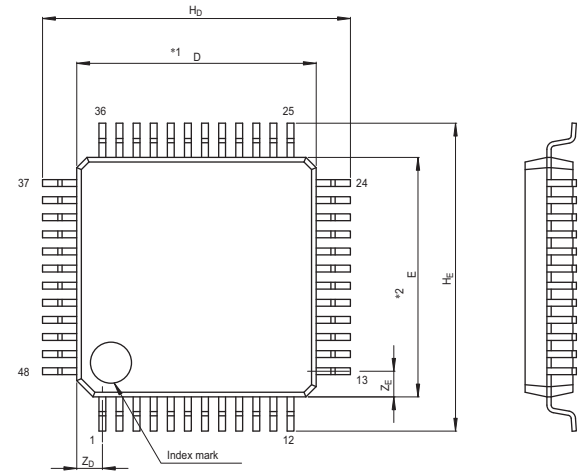

(UNIT:mm)

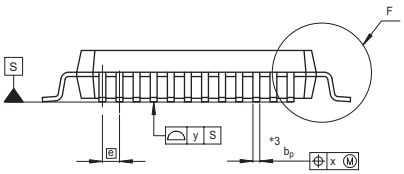
| ITEM | DIMENSIONS |
|---|---|
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

## 4.4 48-pin products

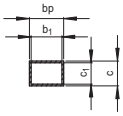
R5F11BGCAFB, R5F11BGEAFB, R5F11BGCGFB, R5F11BGEGFB

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KB-A | 48P6Q-A | 0.2g |

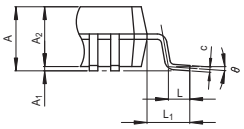





Terminal cross section




Detail F

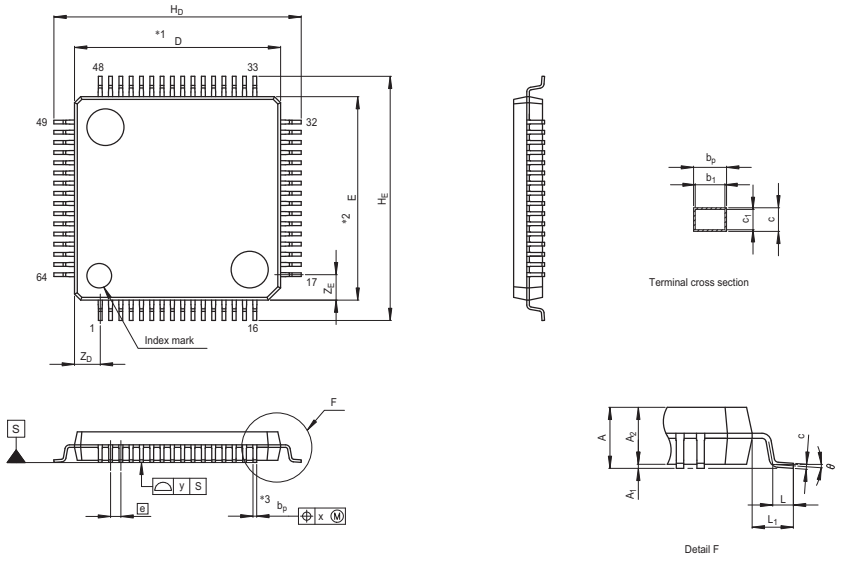
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

## 4.5 64-pin products

R5F11BLCAFB, R5F11BLEAFB, R5F11BLCGFB, R5F11BLEGFB

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| REVISION HISTORY | RL78/G1F Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.10 | | — | First Edition issued |
| 0.50 | Jan 14, 2015 | 3 | Modification of description in Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1F |
| | | 10 | Addition of description in 1.4 Pin Identification |
| | | 11 | Modification of description in 1.5 Block Diagram |
| | | 12, 13 | Modification of description in 1.6 Outline of Functions |
| | | 14 | Addition of target products to the beginning |
| | | 17 | Modification of 2.2.2 On-chip oscillator characteristics |
| | | 18 | Addition of note 4 in 2.3.1 Pin characteristics |
| | | 23, 25, 27 | Modification of 2.3.2 Supply current characteristics |
| | | 73 | Modification of 2.6.4 Comparator |
| | | 73 | Modification of 2.6.5 PGA |
| | | 77 | Renamed to 2.7 RAM Data Retention Characteristics |
| | | 79 | Addition of target products to the beginning |
| | | 83 | Modification of 3.2.2 On-chip oscillator characteristics |
| | | 87 | Modification of “Output voltage, low” |
| | | 89, 91, 93 | Modification of 3.3.2 Supply current characteristics |
| | | 130 | Modification of 3.6.4 Comparator |
| | | 130 | Modification of 3.6.5 PGA |
| | | 133 | Renamed to 3.7 RAM Data Retention Characteristics |
| 1.00 | Jan 14, 2015 | All | Modification of the unit symbol (PWMOP into PWMOPA) |
| | | 1 | Modification of descriptions in 1.1 Features |
| | | 10 | Modification of 1.4 Pin Identification |
| | | 13 | Modification of 1.6 Outline of Functions |
| | | 73 | Modification of 2.6.5 PGA |
| | | 130 | Modification of 3.6.5 PGA |
| 1.10 | Aug 12, 2016 | 5 | Addition of product name (RL78/G1F) and description (Top View) in 1.3.1 24-pin products |
| | | 6 | Addition of product name (RL78/G1F) and description (Top View) in 1.3.2 32-pin products |
| | | 8 | Addition of product name (RL78/G1F) and description (Top View) in 1.3.4 48-pin products |
| | | 9 | Addition of product name (RL78/G1F) and description (Top View) in 1.3.5 64-pin products |

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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