Dual/Quad Low Power, High Speed JFET Operational Amplifiers

OP282/OP482

FEATURES

High slew rate: 9 V/µs
Wide bandwidth: 4 MHz
Low supply current: 250 µA/amplifier max
Low offset voltage: 3 mV max
Low bias current: 100 pA max
Fast settling time
Common-mode range includes V+
Unity-gain stable

APPLICATIONS

Active filters
Fast amplifiers
Integrators
Supply current monitoring

GENERAL DESCRIPTION

The OP282/OP482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. The slew rate is typically 9 V/µs with a supply current under 250 µA per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the OP282/OP482 ensures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

With a wide output swing, within 1.5 V of each supply, low power consumption, and high slew rate, the OP282/OP482 are ideal for battery-powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP282/OP482 an excellent choice for high-side signal conditioning.

The OP282/OP482 are specified over the extended industrial temperature range. The OP282 is available in the standard 8-lead narrow SOIC and MSOP packages. The OP482 is available in PDIP and narrow SOIC packages.

PIN CONNECTIONS

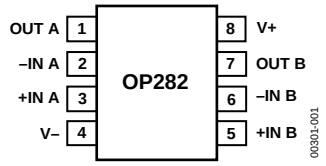

Figure 1. 8-Lead Narrow-Body SOIC (S-Suffix) [R-8]

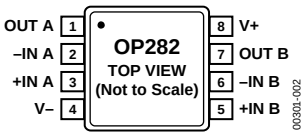

Figure 2. 8-Lead MSOP [RM-8]

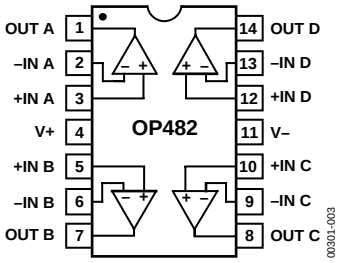

Figure 3. 14-Lead PDIP (P-Suffix) [N-14]

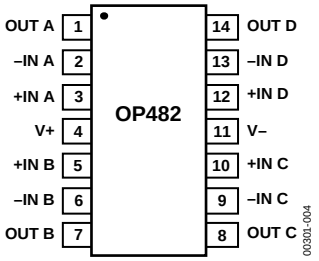

Figure 4. 14-Lead Narrow-Body SOIC (S-Suffix) [R-14]

Rev. F

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REVISION HISTORY

10/04—Data Sheet Changed from Rev. E to Rev. F

Deleted 8-Lead PDIP ..... Universal
Added 8-Lead MSOP ..... Universal
Changes to Format and Layout ..... Universal
Changes to Features 1
Changes to Pin Configurations 1
Changes to General Description 1
Changes to Specifications 3
Changes to Absolute Maximum Ratings 4
Changes to Table 3 4
Added Figure 5 through Figure 20; Renumbered Successive Figures 5
Updated Figure 21 and Figure 22 7
Updated Figure 23 and Figure 27 8
Updated Figure 29 9
Updated Figure 35 and Figure 36 10
Updated Figure 43 11
Changes to Applications Information 12
Changes to Figure 44 12
Deleted OP282/OP482 Spice Macro Model Section 9
Deleted Figure 4 9
Deleted OP282 Spice Marco Model 10
Updated Outline Dimensions 14
Changes to Ordering Guide 14

10/02—Data Sheet Changed from Rev. D to Rev. E

Edits to 8-Lead Epoxy DIP (P-Suffix) Pin 1
Edits to Ordering Guide 3
Edits to Outline Dimensions 11

9/02—Data Sheet Changed from Rev. C to Rev. D

Edits to 14-Lead SOIC (S-Suffix) Pin 1
Replaced 8-Lead SOIC (S-Suffix) 11

4/02—Data Sheet changed from Rev. B to Rev. C

Wafer Test Limits Deleted 2
Edits to Absolute Maximum Ratings 3
Dice Characteristics Deleted 3
Edits to Ordering Guide 3
Edits to Figure 1 7
Edits to Figure 3 8
20-Position Chip Carrier (RC Suffix) Deleted 11

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At V_S = ±15.0 V, T_A = 25°C, unless otherwise noted; applies to both A and G grade.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP282		0.2	3	mV
		OP282, −40°C ≤ T_A ≤ +85°C			4.5	mV
	V_{OS}	OP482		0.2	4	mV
		OP482, −40°C ≤ T_A ≤ +85°C			6	mV
Input Bias Current	I_B	V_{CM} = 0 V		3	100	pA
		V_{CM} = 0 V[1]			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	50	pA
		V_{CM} = 0 V[1]			250	pA
Input Voltage Range			−11		+15	V
Common-Mode Rejection Ratio	CMRR	−11 V ≤ V_{CM} ≤ +15 V, −40°C ≤ T_A ≤ +85°C	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, −40°C ≤ T_A ≤ +85°C	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	+13.5	+13.9		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ		−13.9	−13.5	V
Short-Circuit Limit	I_{SC}	Source	3	10		mA
		Sink		−12	−8	mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, −40°C ≤ T_A ≤ +85°C		25	316	µV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, −40°C ≤ T_A ≤ 85°C		210	250	µA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Full-Power Bandwidth	BW_P	1% distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$Ø_O$			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

[1] The input bias and offset currents are characterized at T_A = T_J = 85°C. Bias and offset currents are guaranteed but not tested at −40°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Ratings
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[1]	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
P-Suffix (N), S-Suffix (R), RM Packages	−65°C to +150°C
Operating Temperature Range	
OP282G, OP282A, OP482G	−40°C to +85°C
Junction Temperature Range	
P-Suffix (N), S-Suffix (R), RM Packages	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP [RM]	206	44	°C/W
8-Lead SOIC (S-Suffix) [R]	157	56	°C/W
14-Lead PDIP (P-Suffix) [N]	83	39	°C/W
14-Lead SOIC (S-Suffix) [R]	104	36	°C/W

[1] θ_{JA} is specified for the worst-case conditions; i.e., θ_{JA} is specified for device in socket for CERDIP, PDIP; θ_{JA} is specified for device soldered in circuit board for SOIC or MSOP package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

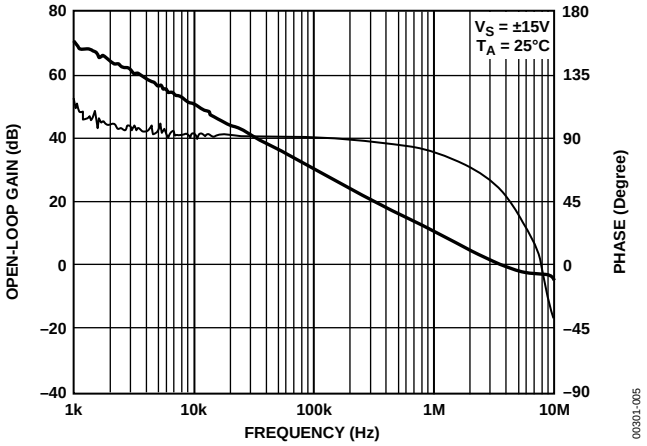


Figure 5. OP282 Open-Loop Gain and Phase vs. Frequency

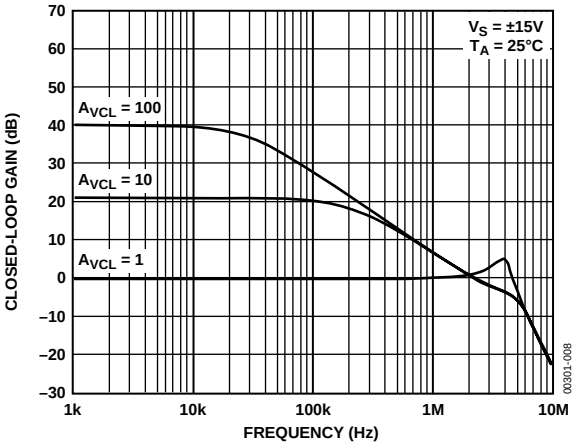


Figure 8. OP282 Closed-Loop Gain vs. Frequency

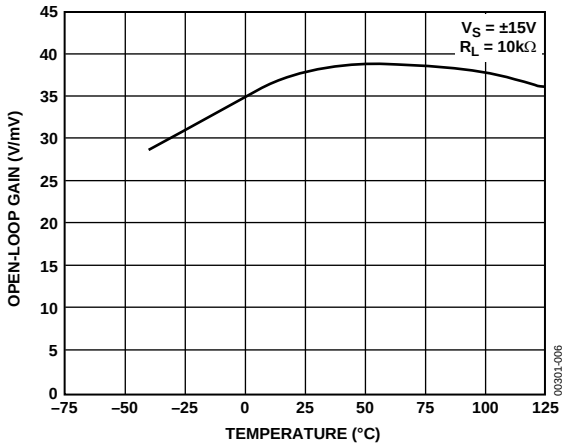


Figure 6. OP282 Open-Loop Gain vs. Temperature

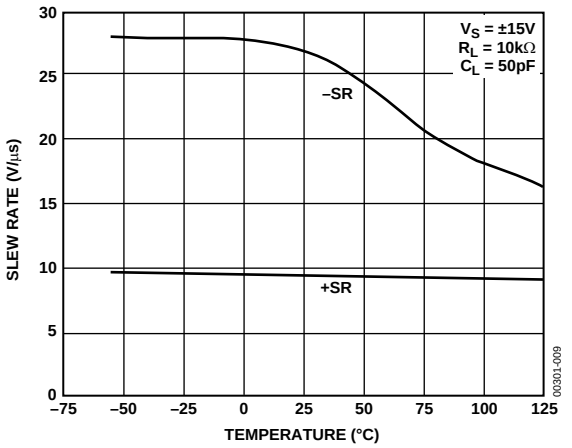


Figure 9. OP282 Slew Rate vs. Temperature

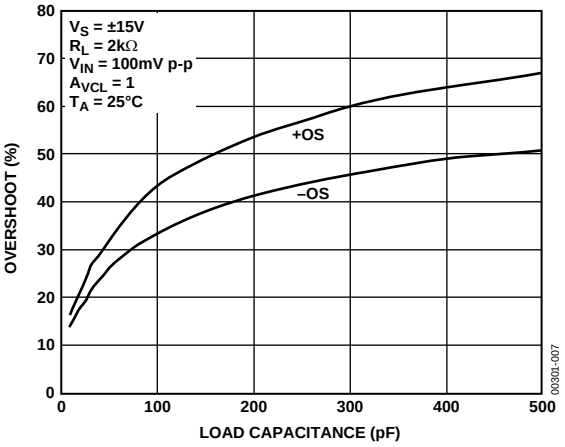


Figure 7. OP282 Small Signal Overshoot vs. Load Capacitance

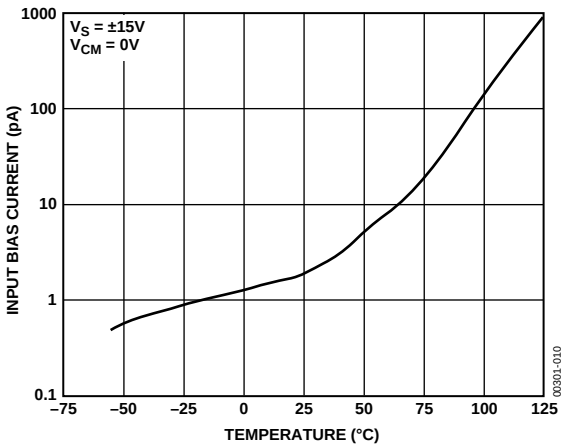


Figure 10. OP282 Input Bias Current vs. Temperature

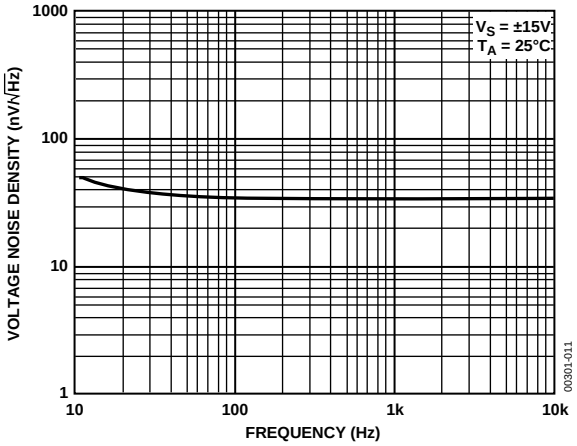


Figure 11. OP282 Voltage Noise Density vs. Frequency

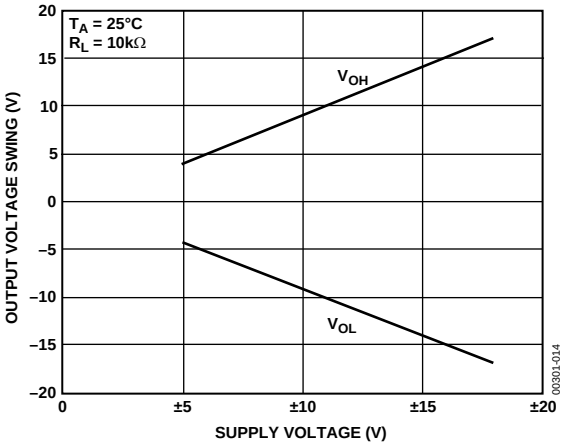


Figure 14. OP282 Output Voltage Swing vs. Supply Voltage

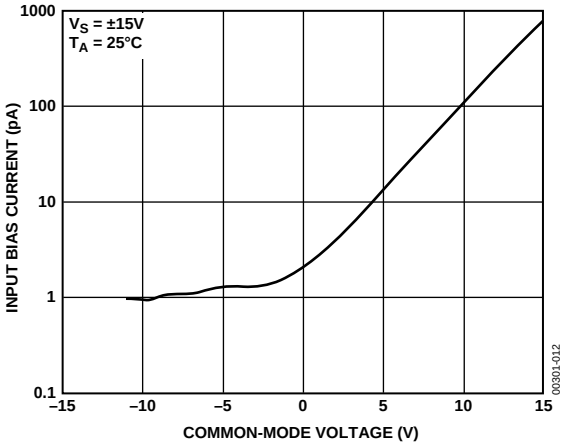


Figure 12. OP282 Input Bias Current vs. Common-Mode Voltage

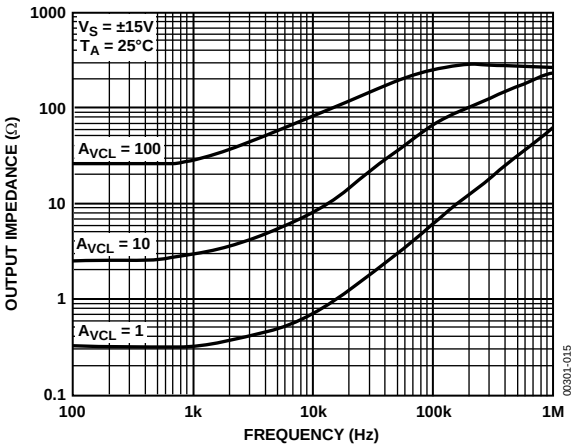


Figure 15. OP282 Closed-Loop Output Impedance vs. Frequency

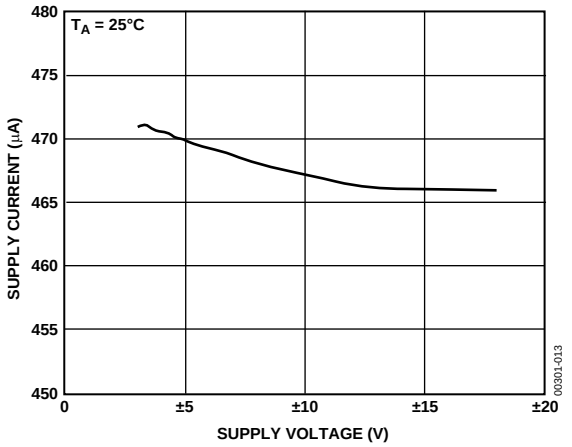


Figure 13. OP282 Supply Current vs. Supply Voltage

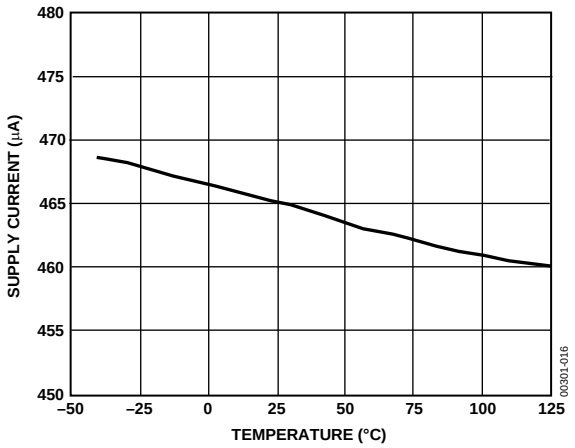


Figure 16. OP282 Supply Current vs. Temperature

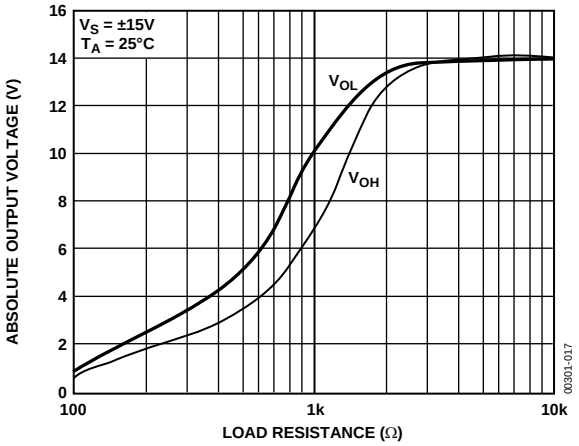


Figure 17. OP282 Absolute Output Voltage vs. Load Resistance

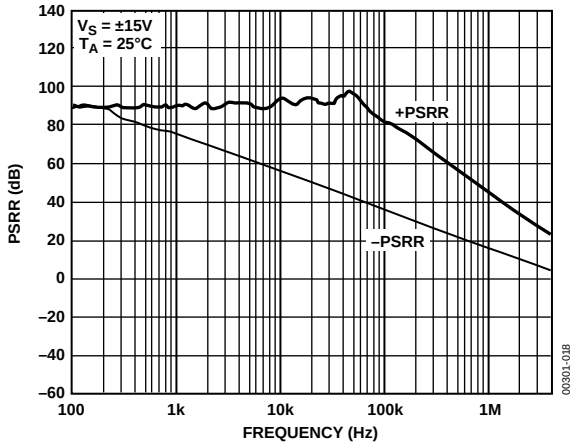


Figure 18. OP282 PSRR vs. Frequency

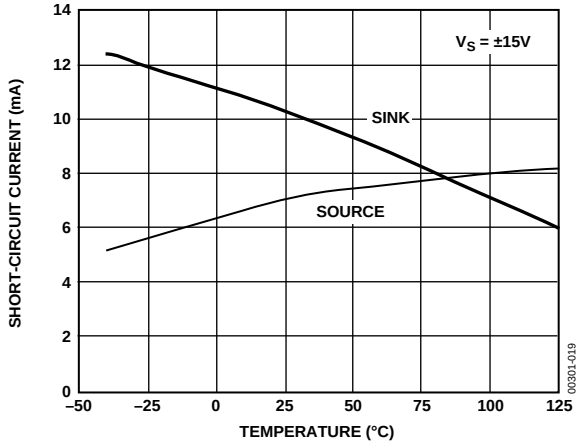


Figure 19. OP282 Short-Circuit Current vs. Temperature

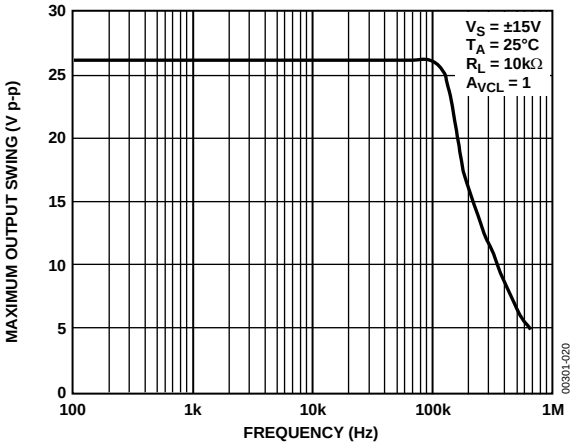


Figure 20. OP282 Maximum Output Swing vs. Frequency

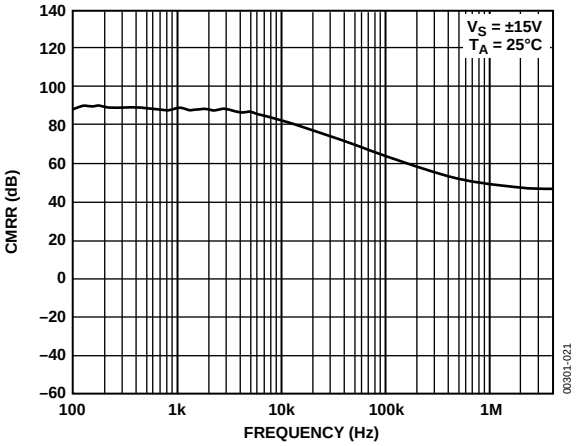


Figure 21. OP282 CMRR vs. Frequency

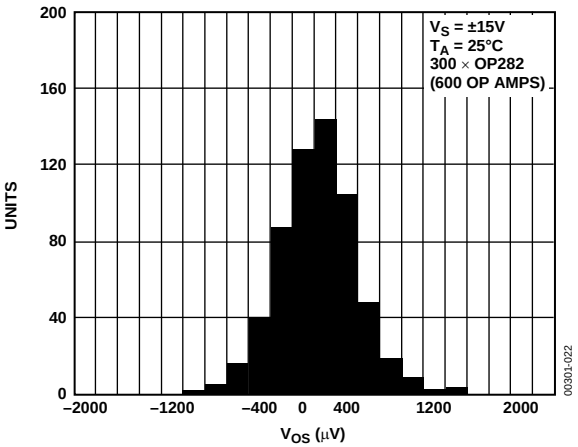


Figure 22. OP282 V_{OS} Distribution SOIC Package

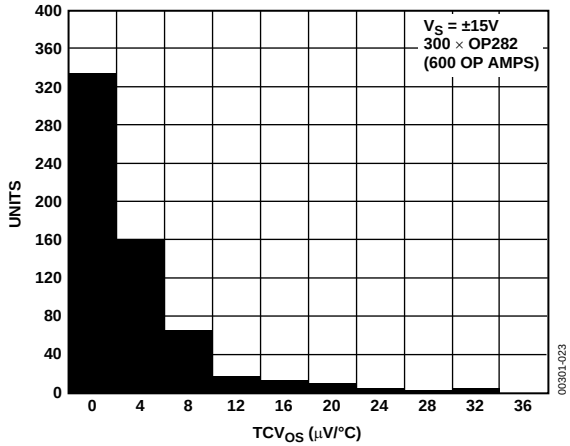


Figure 23. OP282 TCV_{OS} Distribution SOIC Package

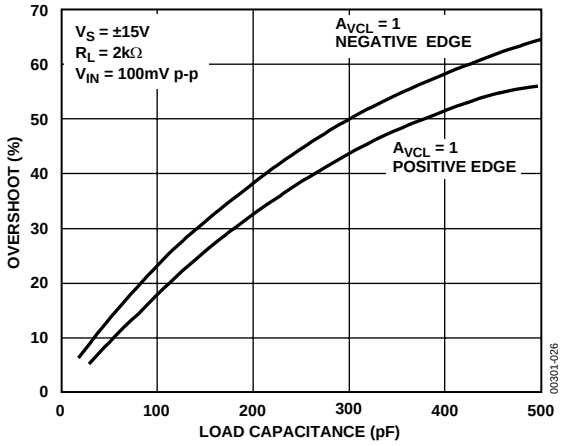


Figure 26. OP482 Small Signal Overshoot vs. Load Capacitance

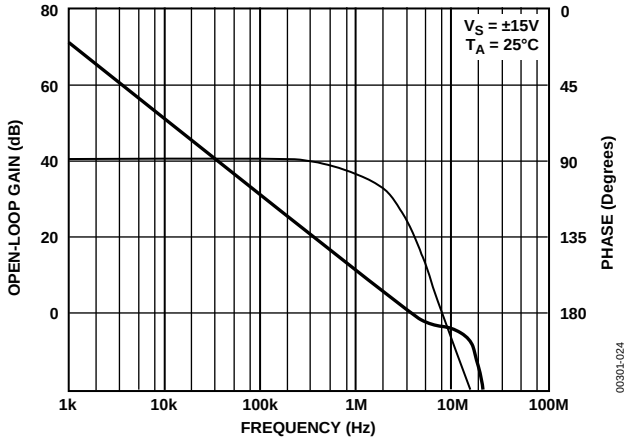


Figure 24. OP482 Open-Loop Gain, Phase vs. Frequency

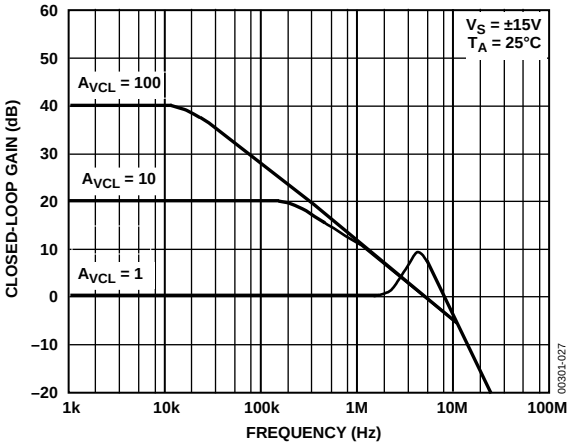


Figure 27. OP482 Closed-Loop Gain vs. Frequency

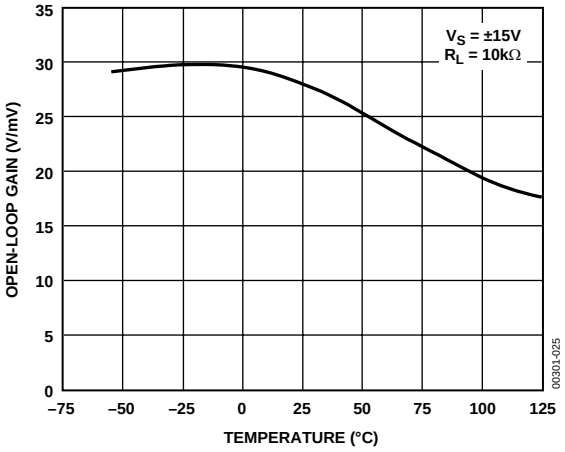


Figure 25. OP482 Open-Loop Gain (V/mV)

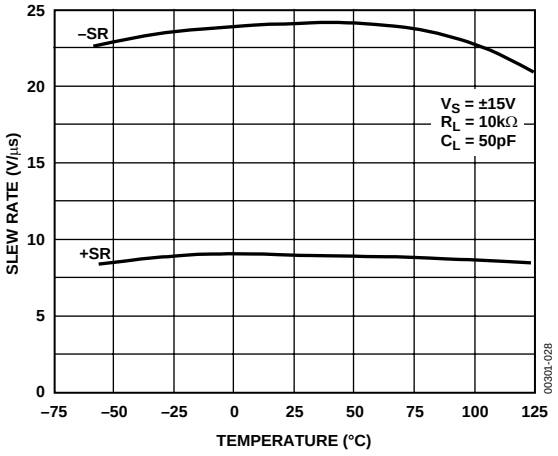


Figure 28. OP482 Slew Rate vs. Temperature

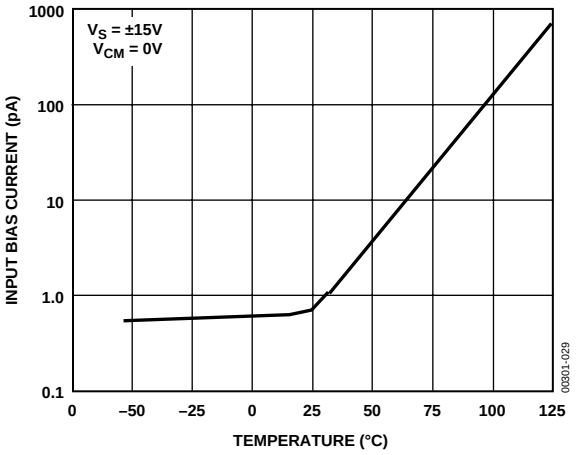


Figure 29. OP482 Input Bias Current vs. Temperature

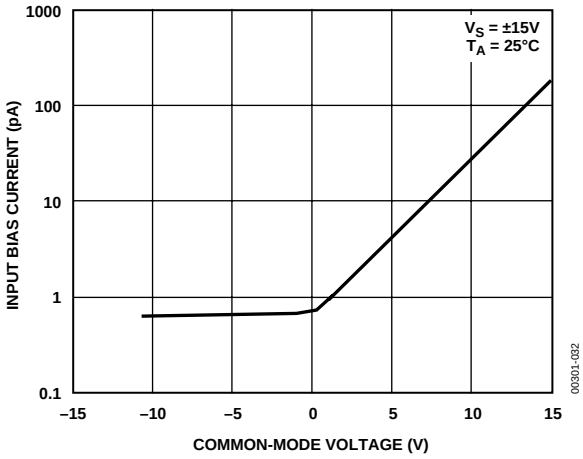


Figure 32. OP482 Input Bias Current vs. Common-Mode Voltage

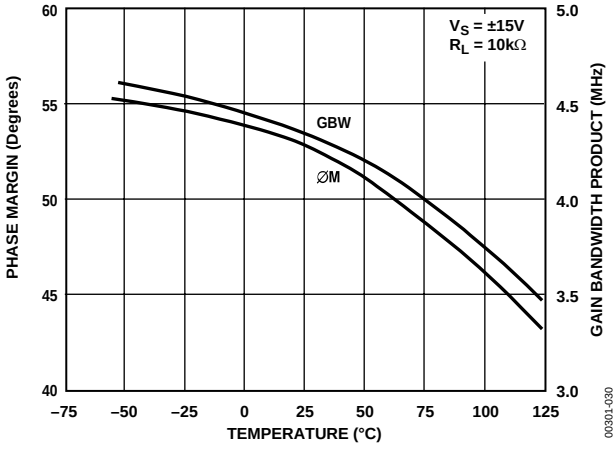


Figure 30. OP482 Phase Margin and Gain Bandwidth Product vs. Temperature

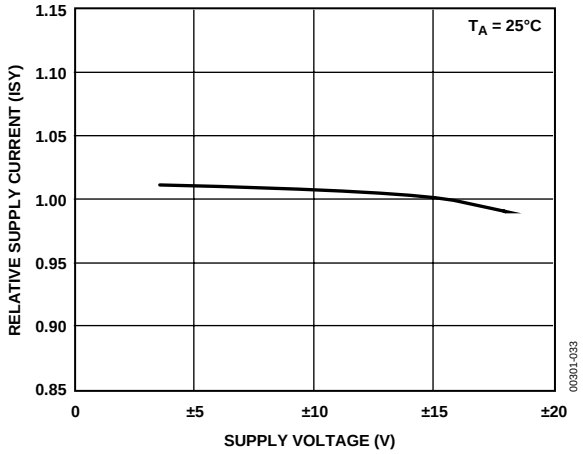


Figure 33. OP482 Relative Supply Current vs. Supply Voltage

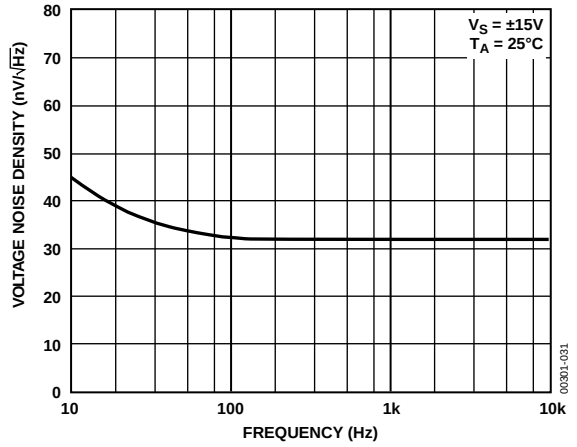


Figure 31. OP482 Voltage Noise Density vs. Frequency

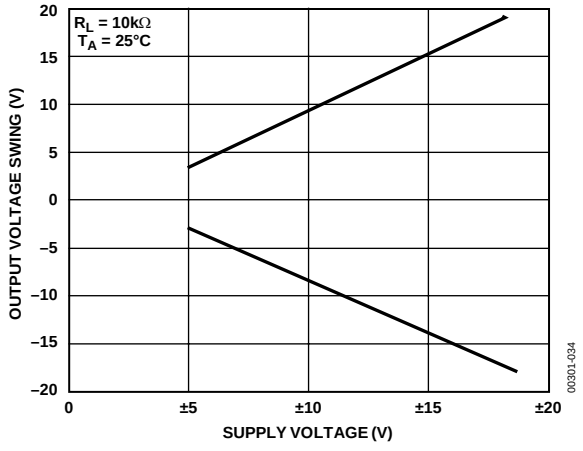


Figure 34. OP482 Output Voltage Swing vs. Supply Voltage

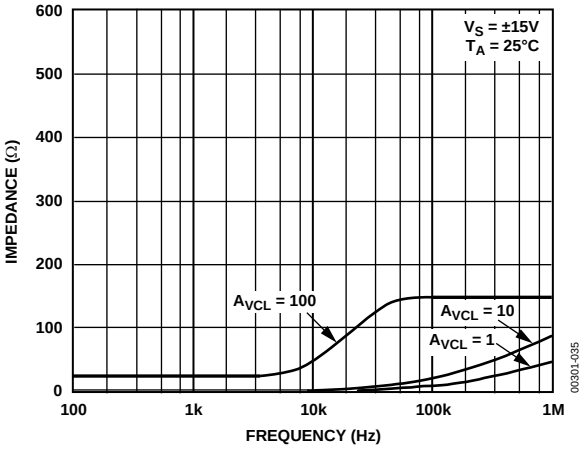


Figure 35. OP482 Closed-Loop Output Impedance vs. Frequency

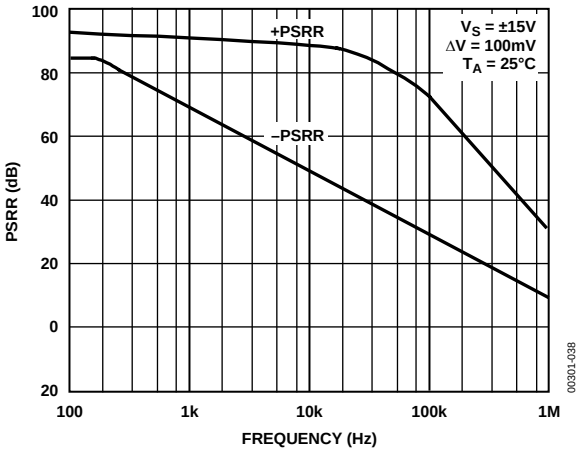


Figure 38. OP482 Power Supply Rejection Ratio (PSRR) vs. Frequency

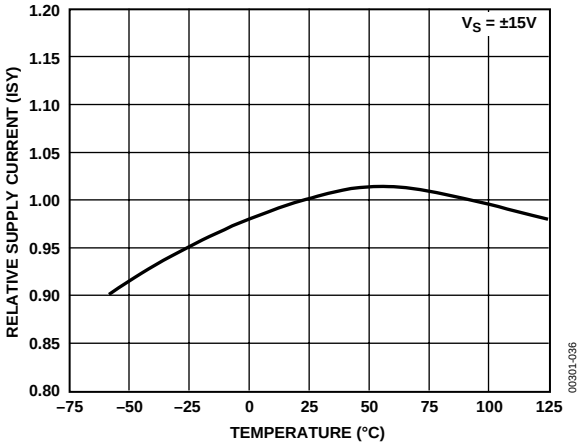


Figure 36. OP482 Relative Supply Current vs. Temperature

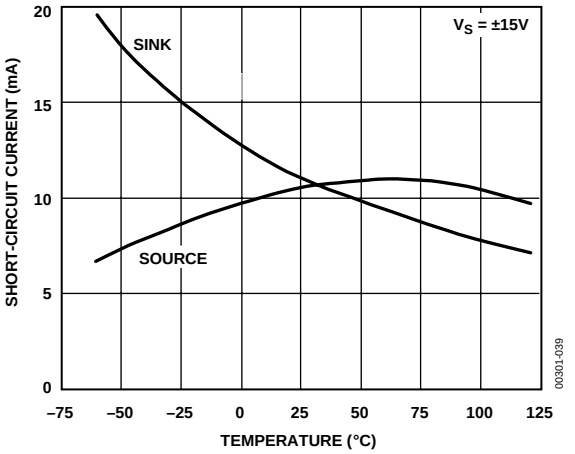


Figure 39. OP482 Short-Circuit Current vs. Temperature

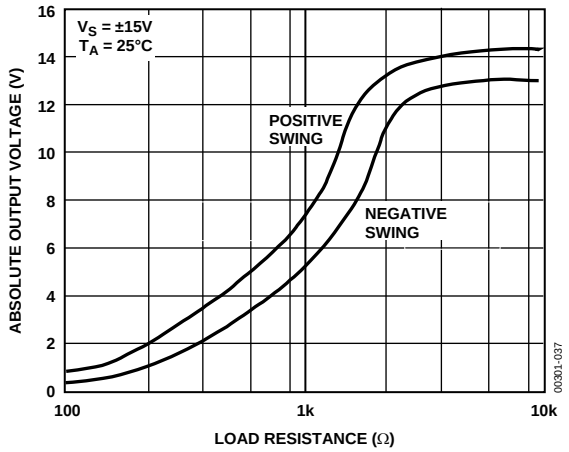


Figure 37. OP482 Maximum Output Voltage vs. Load Resistance

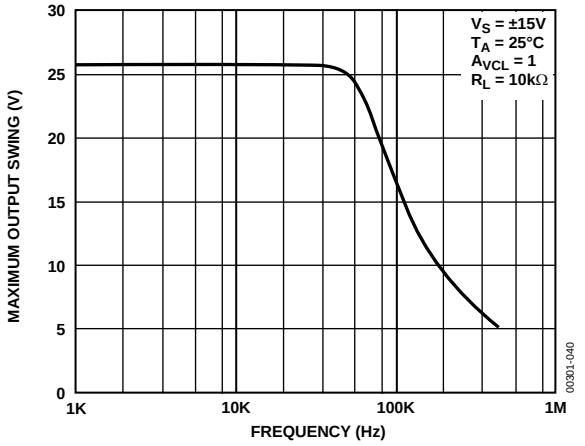


Figure 40. OP482 Maximum Output Swing vs. Frequency

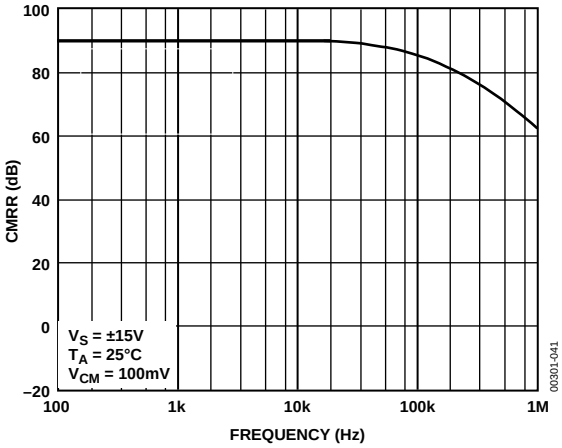


Figure 41. OP482 Common-Mode Rejection Ratio (CMRR) vs. Frequency

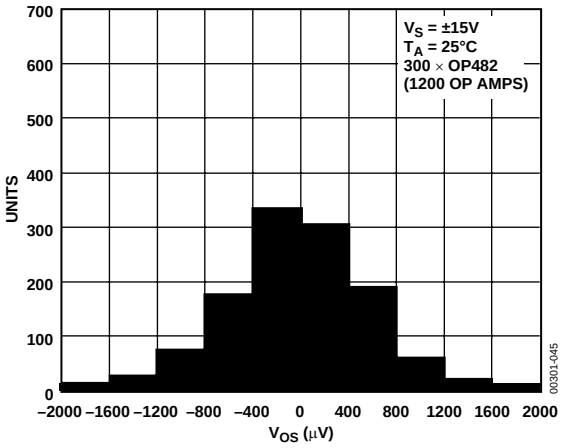


Figure 42. OP482 V_{OS} Distribution P Package

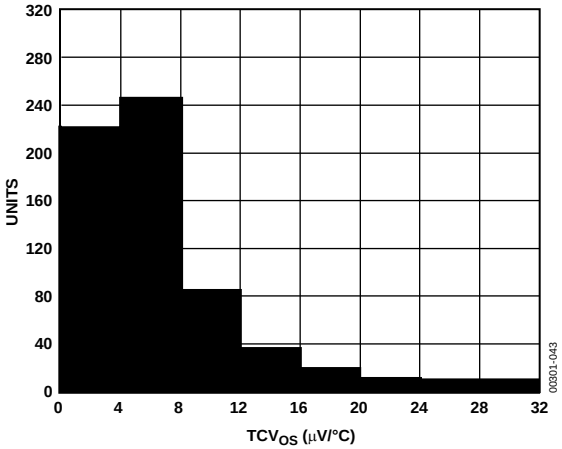


Figure 43. OP482 TCV_{OS} Distribution P Package

APPLICATIONS INFORMATION

The OP282 and OP482 are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

HIGH-SIDE SIGNAL CONDITIONING

There are many applications that require the sensing of signals near the positive rail. OP282s and OP482s were tested and are guaranteed over a common-mode range ($-11\ V \le V_{CM} \le +15\ V$) that includes the positive supply.

One application where this is commonly used is in the sensing of power supply currents. This enables it to be used in current sensing applications, such as the partial circuit shown in Figure 44. In this circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown here, is amplified and compared to 7.5 V. The output can then be used for current limiting.

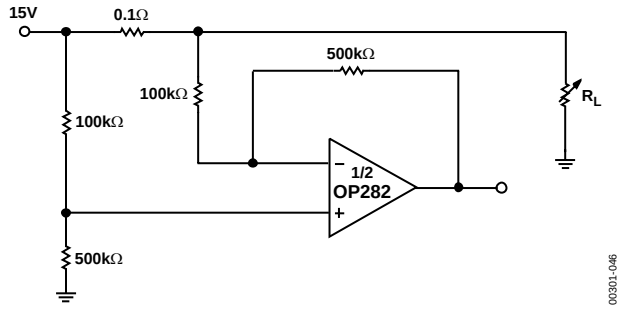


Figure 44. High-Side Signal Conditioning

PHASE INVERSION

Most JFET-input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the OP282/OP482, negative signals in excess of approximately 14 V cause phase inversion. The cause of this effect is saturation of the input stage leading to the forward-biasing of a drain-gate diode. A simple fix for this in noninverting applications is to place a resistor in series with the noninverting input. This limits the amount of current through the forward-biased diode and prevents the shutting down of the output stage. For the OP282/OP482, a value of 200 kΩ has been found to work; however, this adds a significant amount of noise.

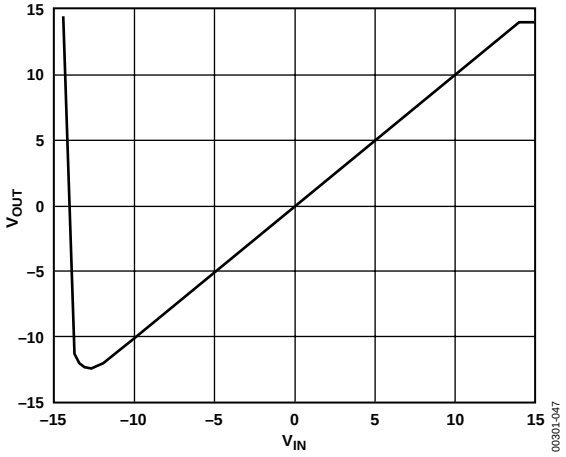


Figure 45. OP282 Phase Reversal

ACTIVE FILTERS

The wide bandwidth and high slew rates of the OP282/OP482 make either an excellent choice for many filter applications.

There are many active filter configurations, but the four most popular configurations are Butterworth, Elliptical, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic as shown in Table 4.

Table 4.

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good		Maximum Flat	
Chebyshev	Good	Moderate	Nonlinear	Equal Ripple	
Elliptical	Best	Poor		Equal Ripple	Equal Ripple
Bessel (Thompson)	Poor	Best	Linear		

PROGRAMMABLE STATE-VARIABLE FILTER

The circuit shown in Figure 46 can be used to accurately program the Q, the cutoff frequency f_C, and gain of a 2-pole state variable filter. OP482s have been used in this design because of their high bandwidths, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are used in the voltage mode; therefore, many values are dependent on the accuracy of the DAC only and not on the absolute values of the DAC's resistive ladders. This makes this circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1. This cutoff frequency can now be expressed as

$$fc = \frac{1}{2\pi R1C1}\left(\frac{D1}{256}\right)$$

where *D1* is the digital code for the DAC.

The gain of this circuit is set by adjusting *D3*. The gain equation is

$$Gain = \frac{R4}{R5}\left(\frac{D3}{256}\right)$$

DAC 2 is used to set the Q of the circuit. Adjusting this DAC controls the amount of feedback from the band-pass node to the input summing node. Note that the digital value of the DAC is in the numerator; therefore, zero code is not a valid operating point.

$$Q = \frac{R2}{R3}\left(\frac{256}{D2}\right)$$

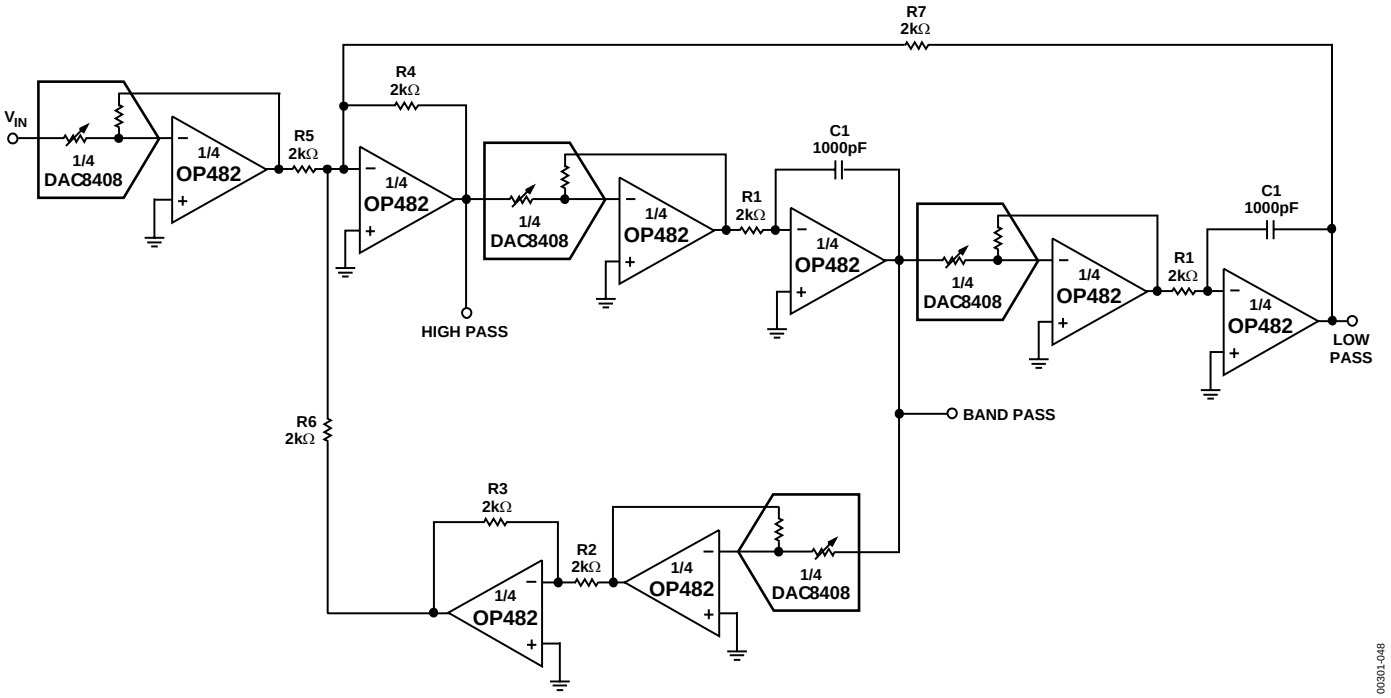
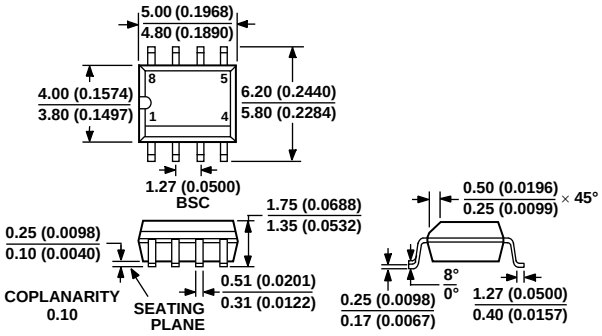


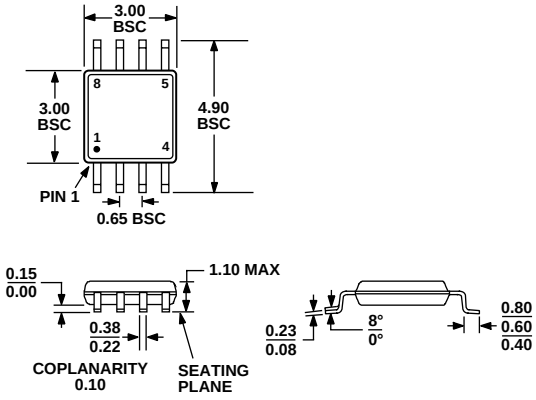
Figure 46.

OUTLINE DIMENSIONS



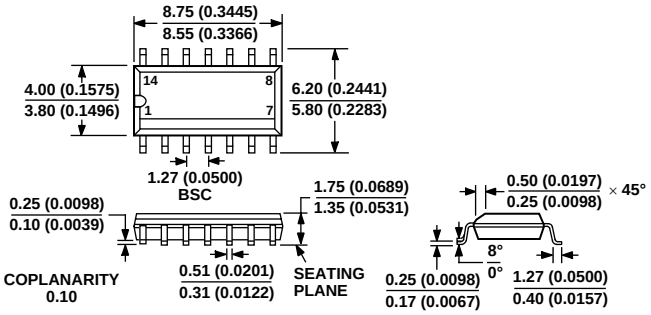
COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 47. 8-Lead Standard Small Outline Package [SOIC]
Narrow-Body S-Suffix (R-8)
Dimensions shown in millimeters and (inches)



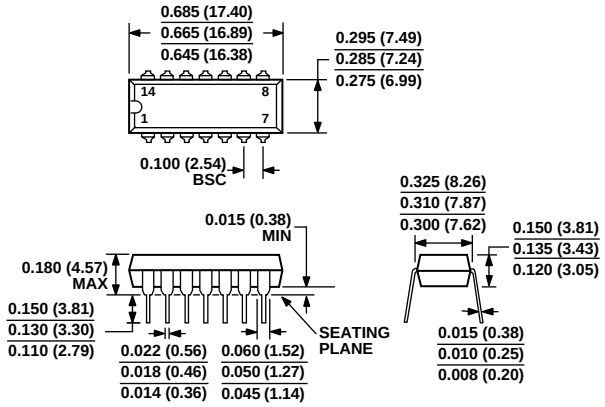
COMPLIANT TO JEDEC STANDARDS MO-187AA

Figure 48. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 49. 14-Lead Standard Small Outline Package [SOIC]
Narrow-Body S-Suffix (R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-095-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 50. 14-Lead Plastic Dual-in-Line Package [PDIP]
P-Suffix (N-14)
Dimension shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
OP282ARMZ-R2[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282GS	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)	
OP282GS-REEL	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)	
OP282GS-REEL7	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)	
OP282GSZ[1]	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)	
OP282GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)	
OP282GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)	
OP482GP	−40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)	
OP482GS	−40°C to +85°C	14-Lead SOIC	S-Suffix (R-14)	
OP482GS-REEL	−40°C to +85°C	14-Lead SOIC	S-Suffix (R-14)	
OP482GS-REEL7	−40°C to +85°C	14-Lead SOIC	S-Suffix (R-14)	
OP482GSZ[1]	−40°C to +85°C	14-Lead SOIC	S-Suffix (R-14)	
OP482GSZ-REEL[1]	−40°C to +85°C	14-Lead SOIC	S-Suffix (R-14)	
OP482GSZ-REEL7[1]	−40°C to +85°C	14-Lead SOIC	S-Suffix (R-14)	

[1] Z = Pb-free part.

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