LTC1668
16-Bit, 50Msps DAC

DESCRIPTION

Demonstration circuit 2459A features the LTC®1668, 16-bit, 50Msps current output DAC in a 28-lead SSOP package. Pin-compatible 14-bit and 12-bit versions are available for lower resolution requirements, but all DC2459A assembly types are populated with the LTC1668.

DC2459A can be connected directly to a digital pattern generator or customer circuit. The DC2459A is also compatible with several popular low cost FPGA development boards for Altera and Xilinx devices. These include the Arrow SoCkit (Altera Cyclone 5 SoC), C5G (Altera Cyclone 5), DE0 Nano (Altera Cyclone 4), Embedded Micro Mojo (Xilinx Spartan 6), and Numato Labs Mimas (Xilinx Spartan 6) boards[1].

Design files for this circuit board are available at http://www.linear.com/demo/DC2459A

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1. Refer to Design Files for Parts List/Bill of Materials.

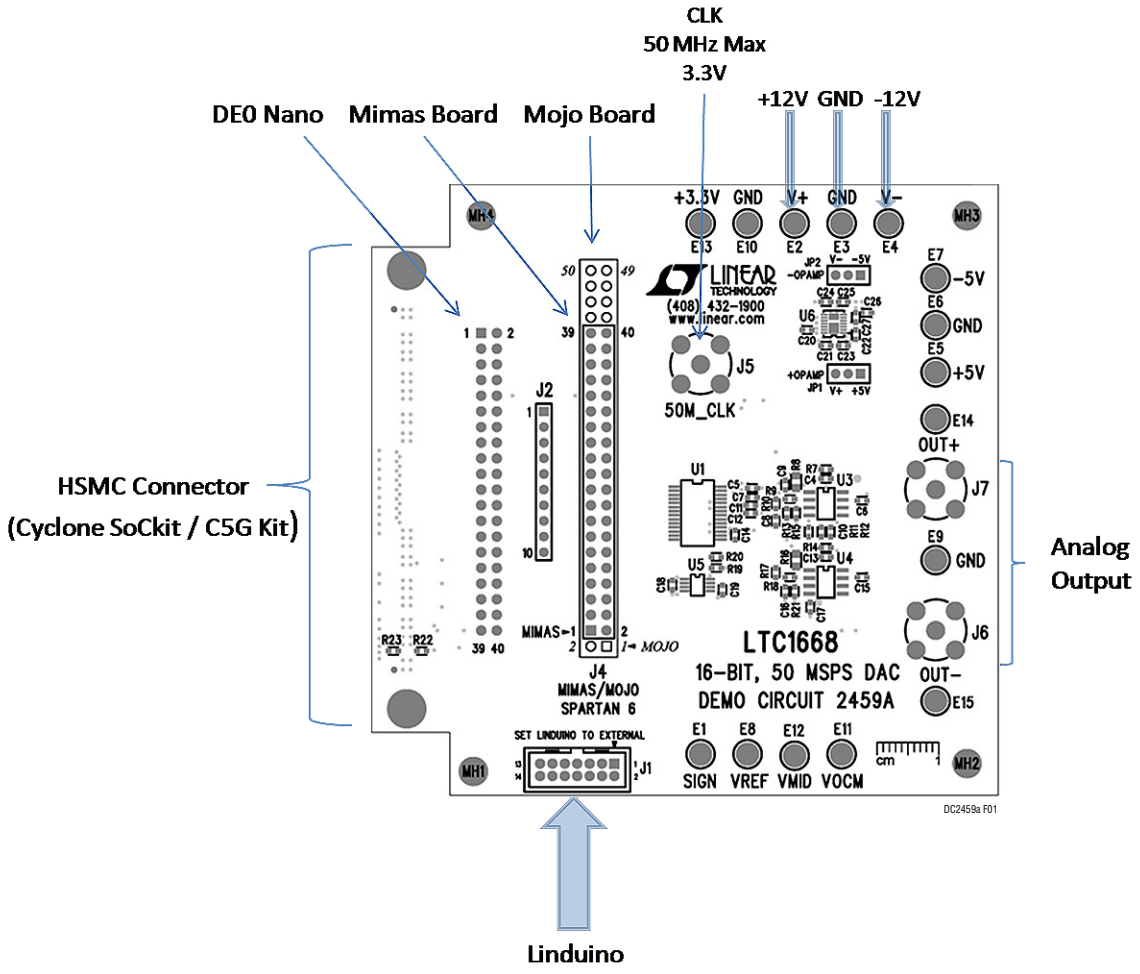

Figure 1. Basic Connections

ASSEMBLY OPTIONS

Table 1. Demonstration Circuit Output Options

ASSEMBLY TYPE	OP AMP	OUTPUT
DC2459A-A	LT1812	Single-Ended: ±1V ($2V_{P-P}$)
DC2459A-B	LT6600	Differential: ±0.25V ($1V_{P-P}$)
DC2459A-C	LT1468	Single-Ended: ±10V ($20V_{P-P}$)

QUICK START PROCEDURE

The LTC1668 is a general purpose DAC with a wide range of applications. Depending on the end application, the best data source for evaluating the LTC1668 may be a digital pattern generator or the actual customer application circuit. However, a basic test of distortion and signal-to-noise ratio using a sinewave output can be a valuable first step in evaluating the performance of the LTC1668. As such, several example FPGA programs are provided that produce a sinewave output.

1. There are several options for providing digital data to the DC2459A, shown in Figures 2 to 6. Connect the DC2459A to a digital pattern generator (which can be the customer application circuit) or supported low cost FPGA board. Do not enable the data source until power is applied to the DC2459A.

   When using the Mojo board, install a 0Ω resistor on R28, which is located on the bottom of the board. This routes the clock signal to the correct input for the Mojo board.

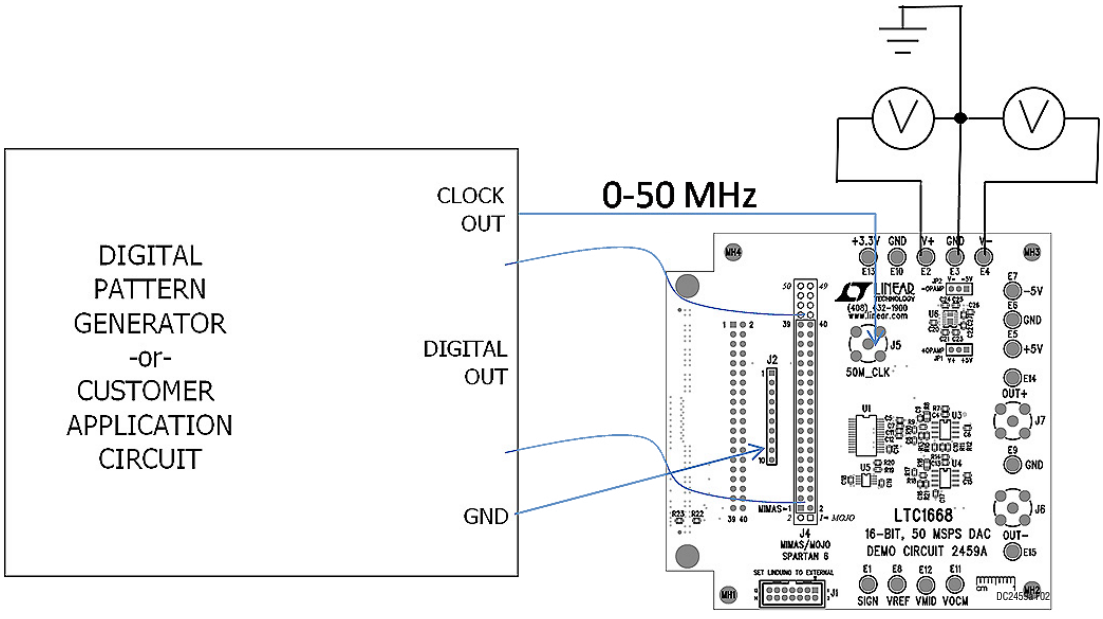

Figure 2. Basic Connection to Digital Pattern Generator

QUICK START PROCEDURE

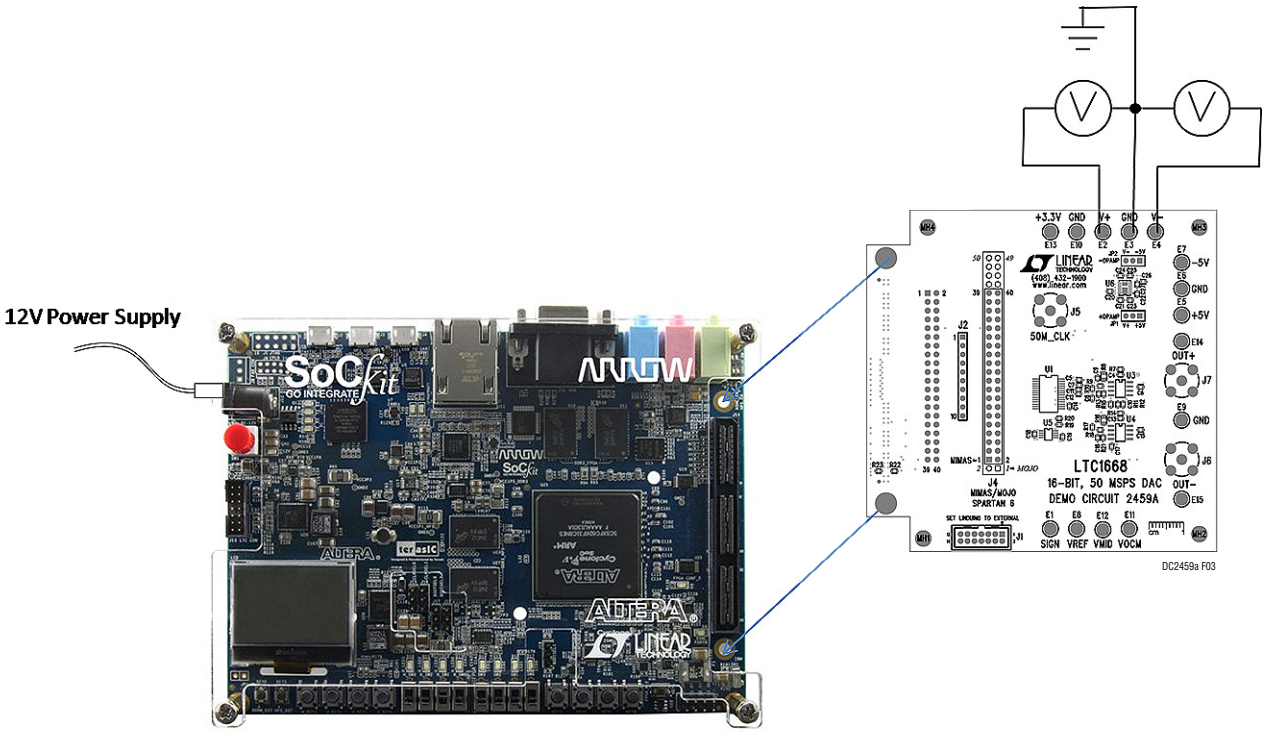

Figure 3. DC2459A Connected to the SoCkit

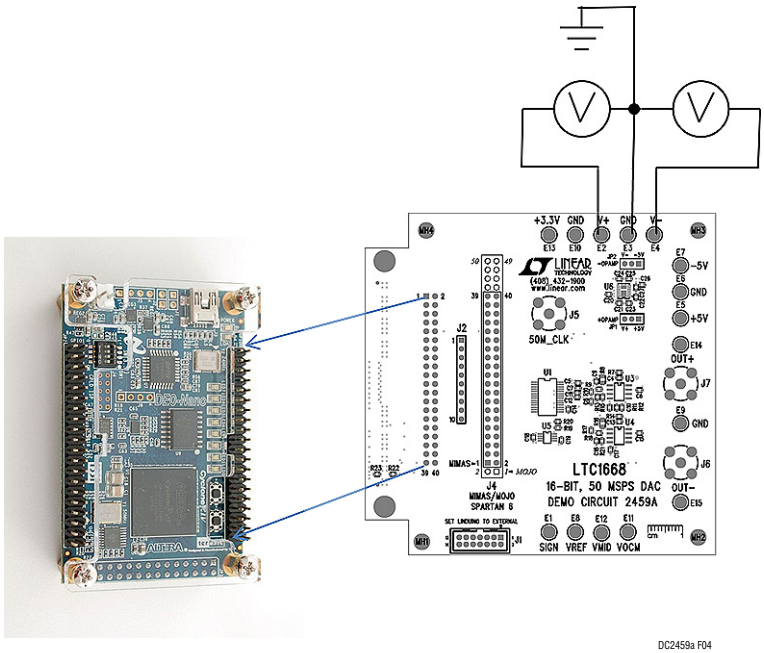

Figure 4. DC2459A Connected to the DE0 Nano

QUICK START PROCEDURE

Table 2. Jumper Configurations

ASSEMBLY TYPE	JP1	JP2
DC2459A-A	5V	–5V
DC2459A-B	5V	–5V
DC2459A-C	V^+	V^-

2. Ensure JP1 and JP2 are set to the correct position as shown by Table 2.
3. Connect ±12V to the V^+ and V^- turret posts. Apply a 3.3V, 50MHz clock to J5.
4. Enable the digital data source. If an FPGA board is being used, apply power, and load the bitstream into the FPGA. Bitstreams are included in the design files, available at http://www.linear.com/demo/2459. Refer to the FPGA user manual for uploading bitstream files.
5. The FPGA bitstreams default to a 10kHz sinusoidal output. Refer to Table 1 for demo board assembly output configuration and voltages.

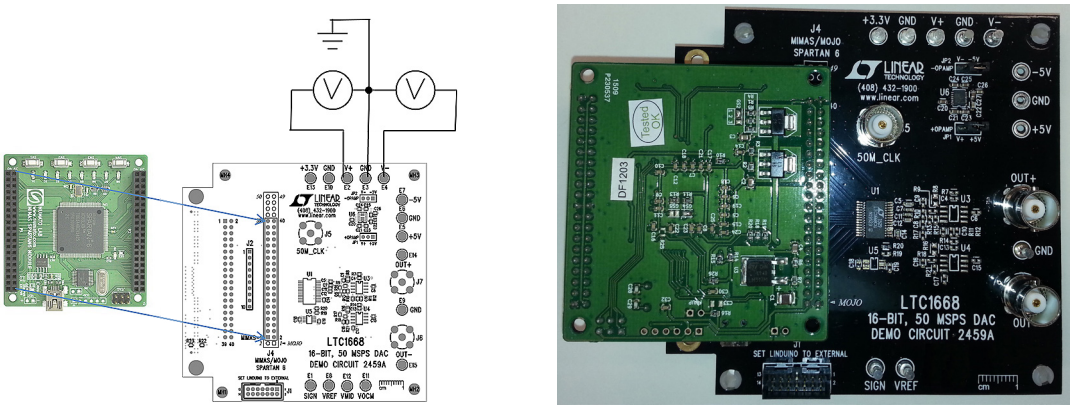

Figure 5. DC2459A Connected to the Mimas Board

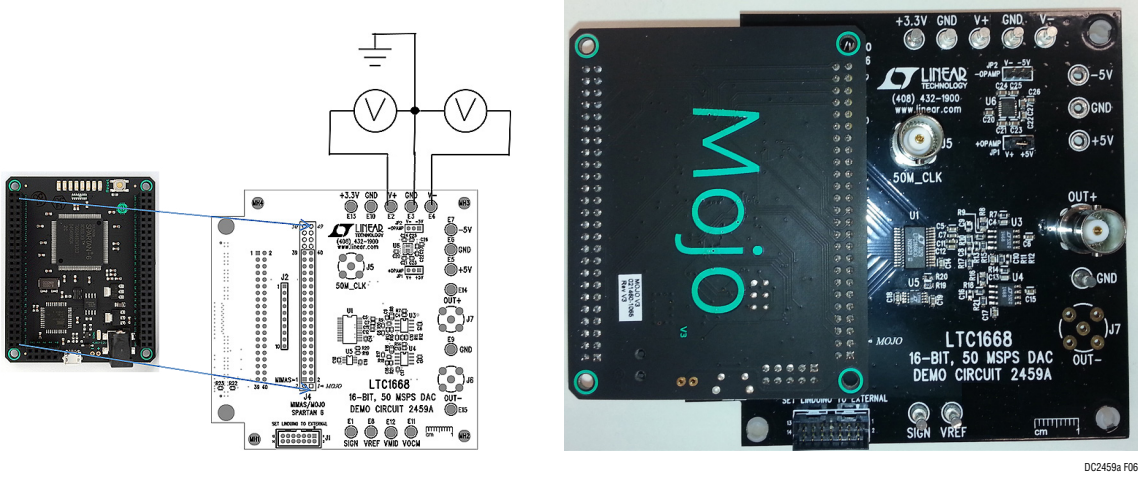

Figure 6. DC2459A Connected to the Mojo Board

QUICK START PROCEDURE

Analog Circuit Descriptions

Assembly type A implements a differential resistor loaded output to a differential to single-ended output shown in Figure 7. The circuit delivers good AC distortion performance at signal frequencies of a few MHz down to DC. The capacitor adds a single real pole of filtering and helps reduce distortion by limiting the high frequency signal amplitude at the op amp inputs. The circuit swings ±1V around ground.

This demo board option is the simplest configuration and allows the most flexibility for modifications.

Assembly version B implements a differential amplifier using the LT6600-2.5, a 4th order, 2.5MHz lowpass filter as shown in Figure 8. The outputs each swing ±0.25V around ground for a total differential output of $1V_{P-P}$.

Assembly version C implements a dual op amp current to voltage converter shown in Figure 9. The circuit delivers good distortion and AC performance to a few kHz. The output swings ±10V around ground.

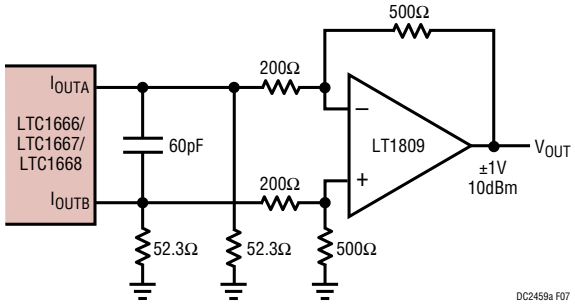

Figure 7. Differential to Single-Ended Op Amp I-V Converter

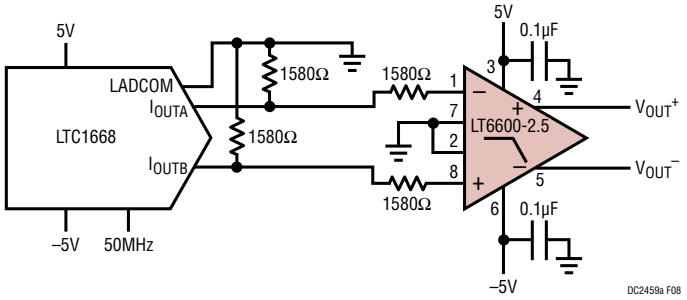

Figure 8. Differential Op Amp I-V Converter

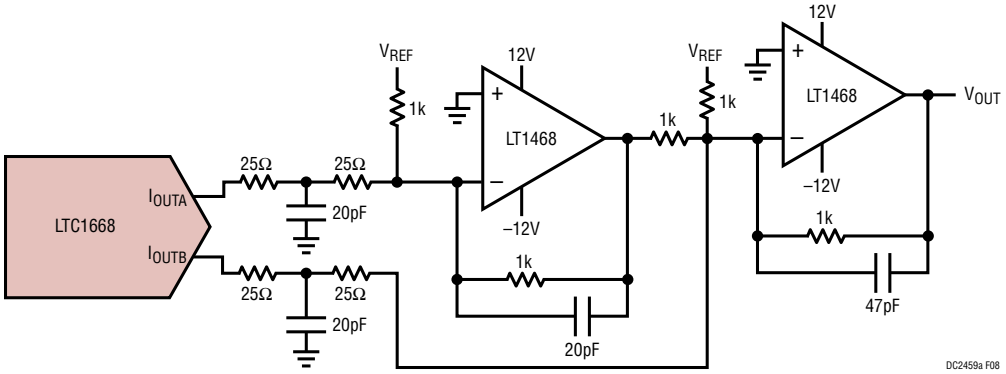

Figure 9. Dual Op Amp Differential to Single-Ended Op Amp I-V Converter

EXTERNAL CONNECTIONS

GND: Four ground turrets are provided. These are connected directly to the ground plane and are the common connection for all supplies and signals.

V^+ and V^-: Power Supply Turrets. ±12V supply. The ±5V supplies for the LTC1668 and op amp circuits are derived from this supply.

3.3V: FPGA Power Rail. Do not connect this turret to a power supply, it is for monitoring the 3.3V supply on the connected FPGA board.

50M_CLK: Input Clock. Frequency range is DC to 50MHz. Logic level should be 3.3V when used with an FPGA board. The logic level can be up to 5V when used with a digital pattern generator.

OUT^+: Voltage from the noninverting DAC output amplifiers. Assembly options A and C use this connector as the single-ended output. Assembly option B uses this connector for the noninverting differential output.

OUT^-: Voltage from the inverting DAC output amplifier. Assembly option B uses this connector for the inverting differential output.

P1: This connector is used to connect to Altera's SoCkit board. The pins are 3.3V logic level.

J1: Linduino Connector. Provides a SPI interface to the FPGA board. The pins are 3.3V logic level.

J2: All pins are ground. These connections are intended for logic analyzer or digital pattern generator grounds.

J3: This connector is used to connect to the DE0 Nano FPGA board. The pins are 3.3V to 5V (TTL compatible) logic level.

J4: This connector is used for the Mimas board and the Mojo FPGA board. Follow the footprint on the silkscreen to ensure proper placement. The pins are 3.3V to 5V (TTL compatible) logic level.

Setting the Frequency of the FPGA Digital Pattern Generator

The FPGA examples generate a digital sinusoidal output using either a numerically controlled oscillator (NCO, for Altera examples) or direct digital synthesizer (DDS, Xilinx examples). The input to these generators is a 32-bit word that sets the output frequency according to Equation 1. A simple SPI interface allows the 32-bit word to be set using a 4-wire interface from a SPI master such as a Linduino microcontroller. The MISO output returns the previous 32-bit configuration word, shown in Figure 10.

Equation 1:

$$\text{CONFIGURE WORD} = \frac{\text{DESIRED FREQUENCY}}{\text{SYSTEM CLOCK FREQUENCY}} \bullet (2^{32} - 1)$$

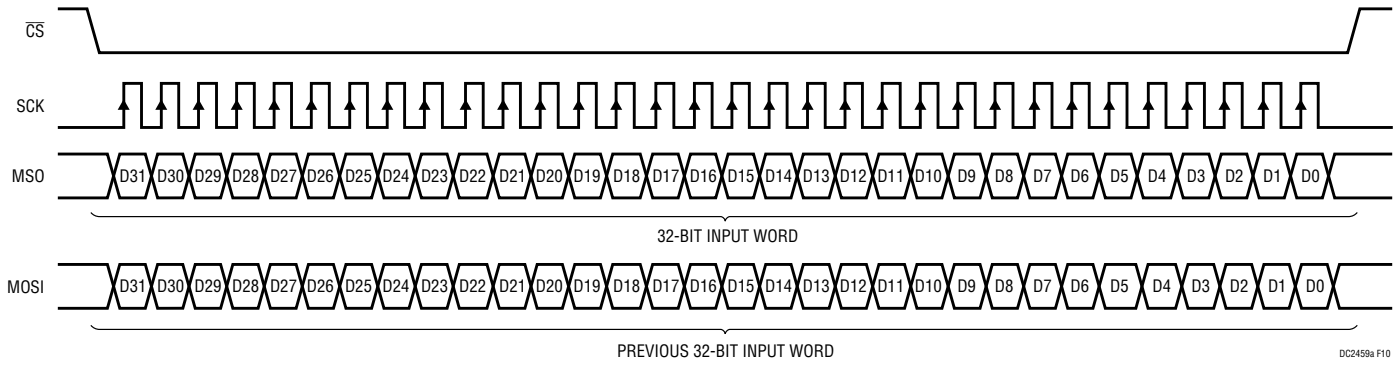

Figure 10. SPI Interface Data Format

EXTERNAL CONNECTIONS

Using the Linduino® as a USB to SPI Interface for LinearLabTools

The Linduino can be used to configure the FPGA via a SPI port with a Python program included in LinearLabTools.

Linduino Interface

1. DC2459A example designs use the default Linduino firmware (DC590 emulator.) If the Linduino has been reprogrammed, follow the procedure in the Linduino (DC2026) demo manual to reprogram the DC590 emulator.
2. Set JP3 to EXT (This causes the Linduino to use the FPGA board's 3.3V supply to set the logic levels.)

Software Installation for LinearLabTools

1. Download and install LinearLabTools from: http://www.linear.com/solutions/linearlabtools
2. Follow the Quick Start procedure for installing LinearLabTools.
3. Examples for the DC2459 are written in Python; Anaconda distribution is used as an example below.

Running the LinearLabTools DC2459A Script

1. Open the Spyder IDE. In the File menu select Linear_lab_tools folder → python → app_examples → LTC1668 → DC2459A.py

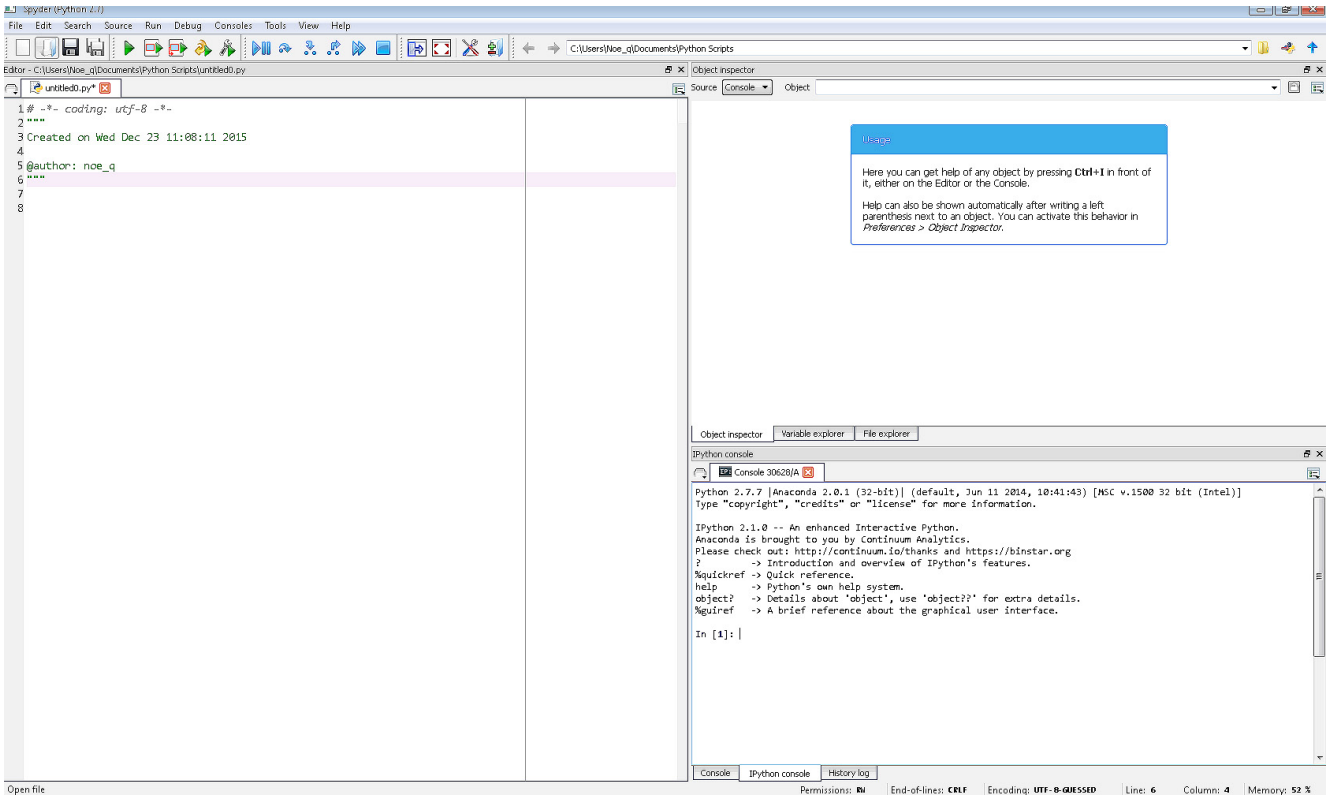

Figure 11. Spyder IDE

EXTERNAL CONNECTIONS

A new tab will appear with the script.

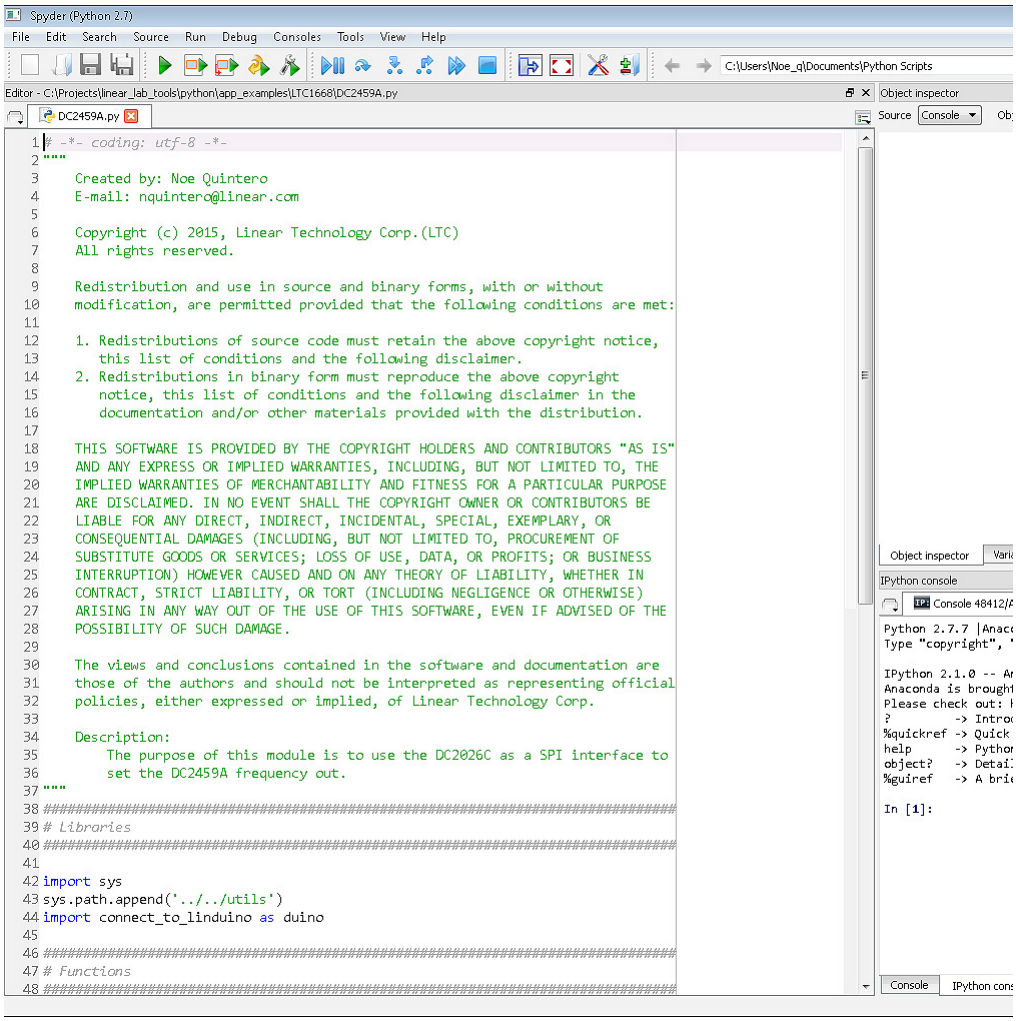

Figure 12. DC2459A Python Script

EXTERNAL CONNECTIONS

2. Run the script by clicking the run button:

   The IPython console will show the simple program interface.

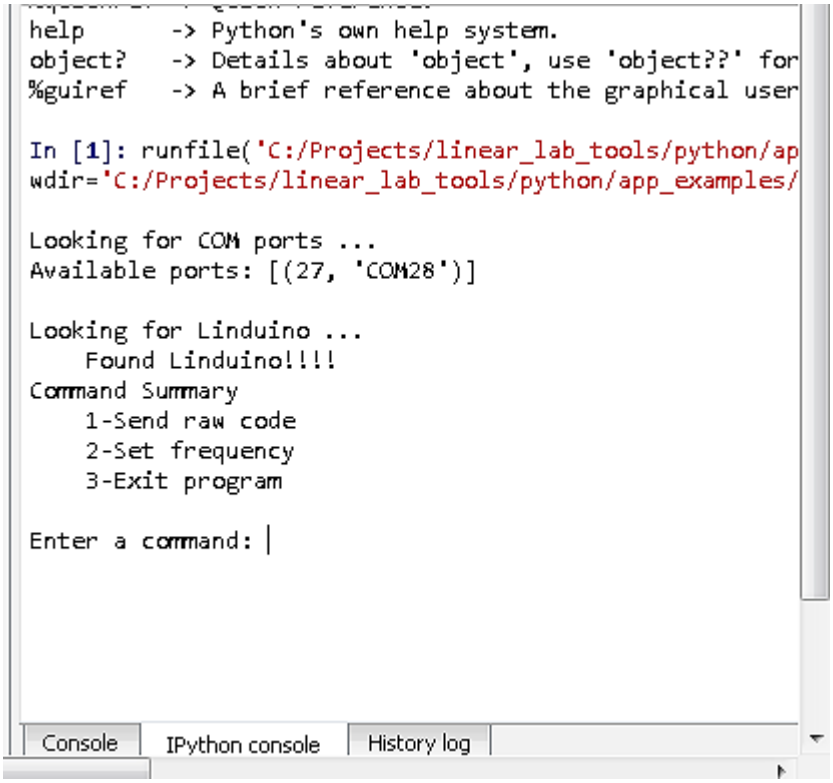

Figure 13. Simple Text Interface

3. To use the interface, enter the commands next to the “Enter a command:” text and hit enter.

```
Enter a command: 2

Enter desired frequency(Hz): 15000
```

Figure 14. Entered Data

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