DrMOS Integrated Power Stage

DESCRIPTION

The SiC772 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency and high power density performance. Packaged in Vishay's proprietary 6 mm x 6 mm MLP package, SiC772 enables voltage regulator design to deliver in excess of 40 A per phase current.

The internal Power MOSFETs utilizes Vishay's state-of-the-art TrenchFET Gen IV technology that delivers industry bench-mark performance to significantly reduce switching and conduction losses.

The SiC772 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, and integrated bootstrap Schottky diode; a thermal warning (THWn) alerts the system of excessive junction temperature. This driver is also compatible with wide range of PWM controllers with the support of Tri-state PWM, 5 V PWM Logic, and skip mode (SMOD) for improve light load efficiency.

FEATURES

- Thermally enhanced PowerPAK MLP6x6-40L package
- Industry benchmark MOSFET with integrated Schottky diode
- Delivers in excess of 40 A continuous current
- 86 % peak efficiency at 19 V to 1 V and 18 A
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 19 V input stage
- 5 V PWM Logic with Tri-state and hold-off
- SMOD logic for light load efficiency boost
- Low PWM propagation delay (< 20 ns)
- Thermal monitor flag
- Faster enable/disenable (10 ns)
- V_{CIN} UVLO
- Compliant with Intel DrMOS 4.0 specification
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb Available
RoHS* Available
HALOGEN FREE

Note:
* This datasheet provides information about parts that are RoHS-compliant and/or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information/tables in this datasheet for details.

APPLICATIONS

- Synchronous buck converters
- Multi-phase VRDs for CPU, GPU, and memory
- DC/DC POL modules
- Notebook computers

TYPICAL APPLICATION DIAGRAMM

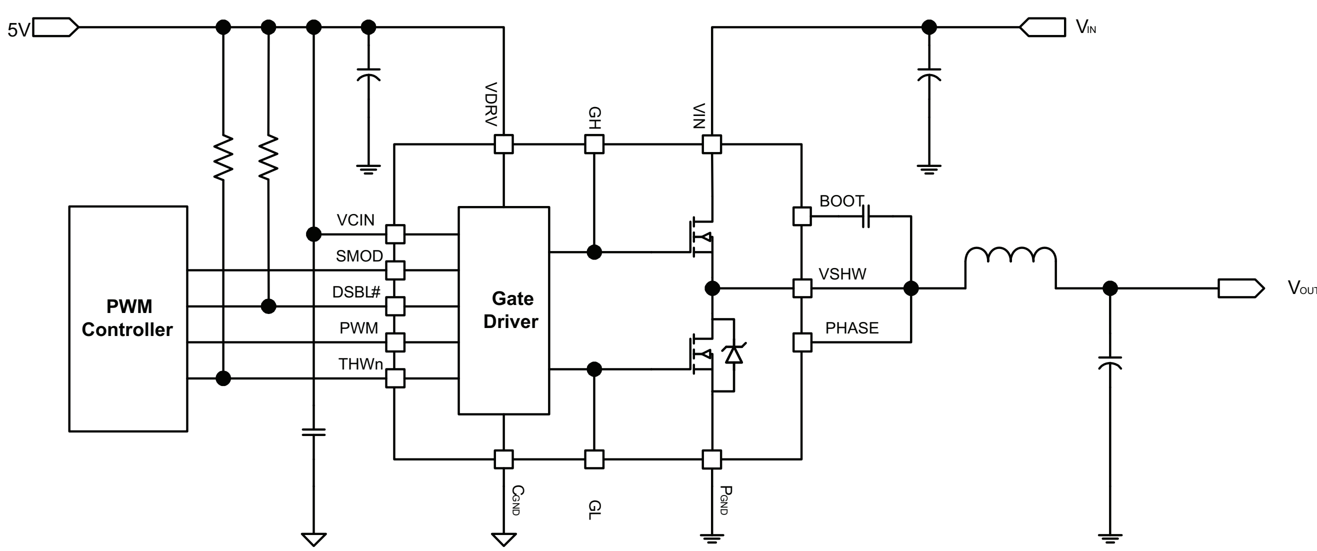

Figure 1: SiC772 Typical Application Diagram

PIN CONFIGURATION

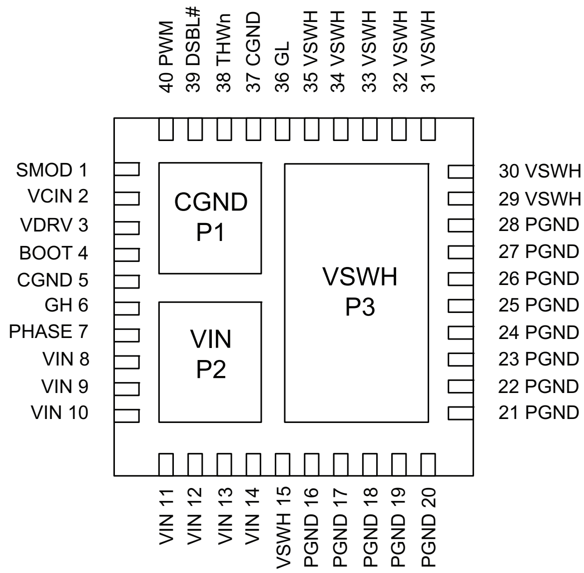

Figure 2 - SiC772 Pin Configuration

PIN DESCRIPTION

Pin Number	Symbol	Description
1	SMOD#	LS FET Turn-OFF Logic. Active low
2	V_{CIN}	Supply voltage for internal logic circuitry
3	V_{DRV}	Supply voltage for internal gate driver
4	BOOT	High side driver bootstrap voltage
5, 37, P1	C_{GND}	Analog ground for the driver IC
6	GH	High side gate signal
7	PHASE	Return path of HS Gate Driver
8 to 14, P2	V_{IN}	Power stage input voltage. Drain of high side MOSFET
15, 29 to 35, P3	V_{SWH}	Phase node of the power stage
16 to 28	P_{GND}	Power ground
36	GL	Low side gate signal
38	THWn	Thermal warning open drain output
39	DSBL#	Disable pin. Active low
40	PWM	PWM input logic

ORDERING INFORMATION

Part Number	Package	Marking Code
SiC772CD-T1-GE3	PowerPAK MLP66-40L	SiC772CD
SiC772DB	Reference Board	

ABSOLUTE MAXIMUM RATINGS (1)

Electrical Parameter	Symbol	Limits	Unit
Input Voltage	V_{IN}	- 0.3 to 30	V
Control Input Voltage	V_{CIN}	- 0.3 to 7	
Drive Input Voltage	V_{DRV}	- 0.3 to 7	
Switch Node (DC)	V_{SW}	- 0.3 to 30	
Switch Node (AC) (2)	V_{SW}	- 8 to 35	
Boot Voltage (DC Voltage)	V_{BS}	- 0.3 to 33	
Boot to Switching Node (DC Voltage)	V_{BS_SW}	- 0.3 to 7	
All Logic Inputs and Outputs (PWM, DSBL, SMOD and THWn)		- 0.3 to V_{CIN} + 0.3	
Max. Operating Junction Temperature	T_J	150	°C
Ambient Temperature	T_A	- 40 to 125	
Storage Temperature		- 65 to 150	

Note:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The specification values indicated "AC" is V_{SW} to P_{GND} - 8 V (< 20 ns, 10 µJ), min. and 35 V (< 50 ns), max.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Input Voltage (V_{IN})	4.5		24	V
Drive Input Voltage (V_{DRV})	4.5	5	5.5	
Control Input Voltage (V_{CIN})	4.5	5	5.5	
Switching Node (LX, DC Voltage)			27	
BOOT-SW	4	4.5	5.5	

THERMAL RESISTANCE RATINGS

Parameter	Min.	Typ.	Max.	Unit
Thermal Resistance from Junction to Case (to P3 PAD (V_{SHW})		2.5		°C/W
Thermal Resistance from Junction to PCB		5		

ELECTRICAL SPECIFICATIONS						
Parameter	**Symbol**	**Test Conditions Unless Specified** $V_{DSBL\#} = V_{SMOD} = 5$ V, $V_{IN} = 19$ V, $V_{DRV} = V_{CIN} = 5$ V, $T_A = 25$ °C	**Min.**	**Typ.**[(3)]	**Max.**[(5)]	**Unit**
Power Supplies						
V_{CIN} Control Input Current	I_{VCIN}	$V_{DSBL\#} = 0$ V, no switching		100		µA
		$V_{DSBL\#} = 5$ V, no switching		300		
		$V_{DSBL\#} = 5$ V, $f_s = 300$ kHz, D = 0.1		300		
Drive Input Current (Dynamic)	I_{VDRV}	$f_s = 300$ kHz, D = 0.1		16	25	mA
		$f_s = 1$ MHz, D = 0.1		60		
		$V_{DSBL\#} = 0$ V, no switching		30		µA
		$V_{DSBL\#} = 5$ V, no switching		60		
Bootstrap Supply						
Bootstrap Switch Forward Voltage	V_F	$V_{CIN} = 5$ V, forward bias current 2 mA			0.4	V
PWM Control Input						
Rising Threshold	PWM_{th_r}		3.4	3.7	4.2	V
Falling Threshold	PWM_{th_f}		0.7	0.9	1.2	
Tri-state Voltage	V_{tri}	PWM pin floating		2.3		
Tri-state Falling Threshold	$V_{tri\_th\_f}$		0.9	1.2	1.5	
Tri-state Rising Threshold	$V_{tri\_th\_r}$		3	3.4	3.7	
Tri-state Rising Threshold Hysteresis	$V_{tri\_hys\_r}$			225		mV
Tri-state Falling Threshold Hysteresis	$V_{tri\_hys\_f}$			325		
PWM Input Current	I_{PWM}	$V_{PWM} = 5$ V			500	µA
		$V_{PWM} = 0$ V			- 500	

Notes:
3. Typical limits are established by characterization and are not production tested.
4. Guaranteed by design.
5. Min. and max. not 100 % production tested.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified $V_{DSBL\#} = V_{SMOD} = 5$ V, $V_{IN} = 19$ V, $V_{VDRV} = V_{VCIN} = 5$ V, $T_A = 25$ °C	Min.	Typ.[3]	Max.[5]	Unit
DSBL#, SMOD INPUT						
DSBL# Logic Input Voltage	V_{DSBL}	Enable	2			V
		Disenable			0.8	
SMOD Logic Input Voltage	V_{SMOD}	High State	2			
		Low State			0.8	
Protection						
Under Voltage Lockout	V_{UVLO}	Rising, on Threshold		3.7	4.3	V
		Falling, off Threshold	2.7	3.2		
Under Voltage Lockout Hysteresis				550		mV
THDn Flag Set[4]				160		°C
THDn Flag Clear[4]				135		
THDn Flag Hysteresis[4]				25		
THDn Output Low				0.02		V
Timing Specifications						
Tri-State to GH/GL Rising Propagation Delay	$t_{pd\_r\_tri}$	No load, see fig.4		20		ns
Tri-state Hold-off Time	t_{tsho}			150		
GH - Turn off Propagation Delay	$t_{pd\_off\_GH}$			20		
GH - Turn on Propagation Delay (Dead Time Rising)	$t_{pd\_on\_GH}$			10		
GL - Turn off Propagation Delay	$t_{pd\_off\_GL}$			10		
GL - Turn on Propagation Delay (Dead Time Falling)	$t_{pd\_on\_GL}$			10		

Notes:
3. Typical limits are established by characterization and are not production tested.
4. Guaranteed by design.
5. Min. and max. not 100 % production tested.

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate Tri-state logic (H, L, and Tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{th\_pwm\_r}$ the low side is turned OFF and the high side is turned ON. When PWM input is driven below $V_{th\_pwm\_f}$ the high side turns off and the low side turns on. For Tri-state logic, the PWM input operates as above for driving the MOSFETs. However, there is an third state that is entered into as the PWM output of Tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC772 to pull the PWM input into the Tri-state region (see the Tri-state Voltage Threshold Diagram below). If the PWM input stays in this region for the Tri-state hold-off period, t_{TSHO}, both high side and low side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a schottky diode clamp. The PWM and Tri-state regions are separated by hysteresis to prevent false triggering. The SiC772CD incorporates PWM voltage thresholds that are compatible with 5 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFET. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to C_{GND} and shut down the IC.

Diode Emulation Mode (SMOD) Skip

When SMOD pin is low the diode emulation mode is enabled and GL is turned off. This is a non-synchronous conversion mode that improves light load efficiency by reducing switching losses. Conducted losses that occur in synchronous buck regulators when inductor current is negative can also be reduced. Circuitry in the external controller IC detects when inductor current crosses zero and drive SMOD Lo turning the low side MOSFET off. See SMOD Operation diagram for additional details. If SMOD is left unconnected, an internal pull up resistor will pull the pin up to V_{CIN} (Logic High) to disable the SMOD function.

Thermal Shutdown Warning (THDn)

The THDn pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 kΩ to pull this pin up to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THDn flag is set. When the junction temperature drops below 135 °C the device will clear the THDn signal. The SiC772 does not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side Power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The Switch node V_{SWH} is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the Printed Circuit Board should be such that the inductance separating the C_{GND} and P_{GND} should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin. Shoot-Through Protection and Adaptive Dead Time

Shoot-Through Protection and Adaptive Dead Time (AST)

The SiC772 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on until the other's gate voltage is sufficiently low (1 V), that and built in delays ensure the one Power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC772 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

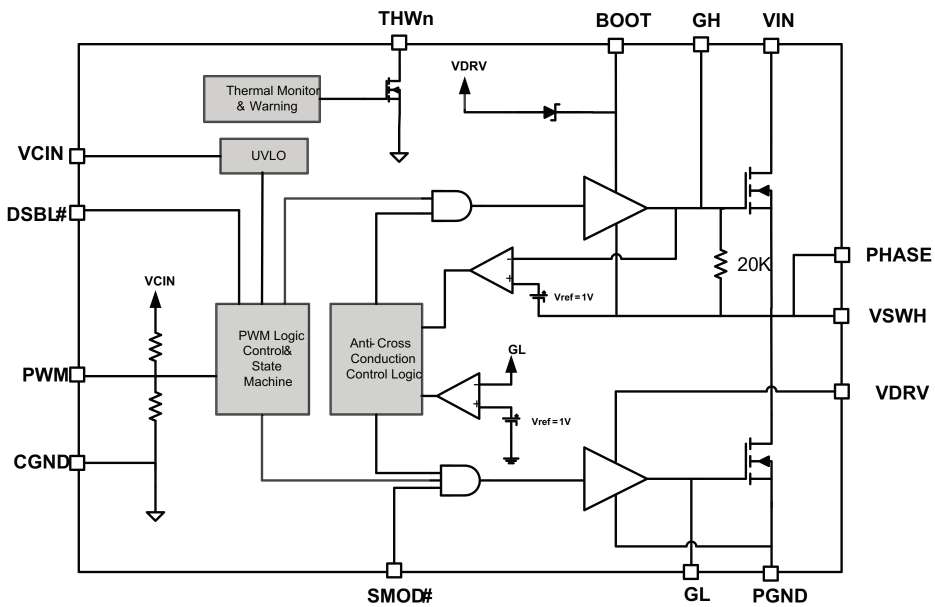

Figure 3: SiC772 Functional Block Diagram

DEVICE TRUTH TABLE				
DSBL#	**SMOD**	**PWM**	**GH**	**GL**
Open	X	X	L	L
L	X	X	L	L
H	L	L	L	L
H	L	H	H	L
H	H	H	H	L
H	H	L	L	H
H	L	Tri-state	L	L
H	H	Tri-state	L	L

PWM TIMING DIAGRAM

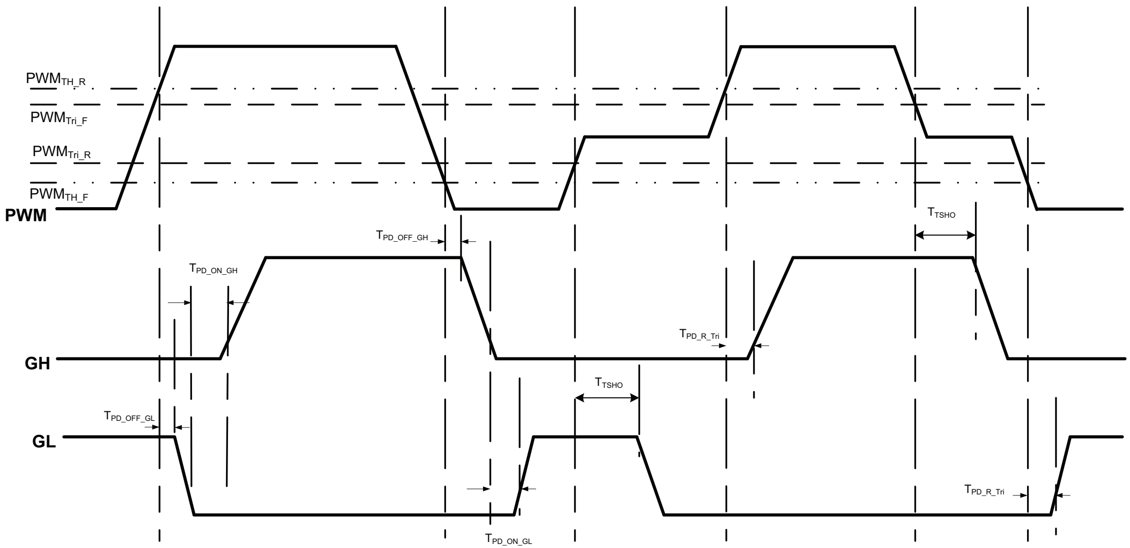

Figure 4: Definition of PWM Logic and Tri-state

SMOD OPERATION DIAGRAM

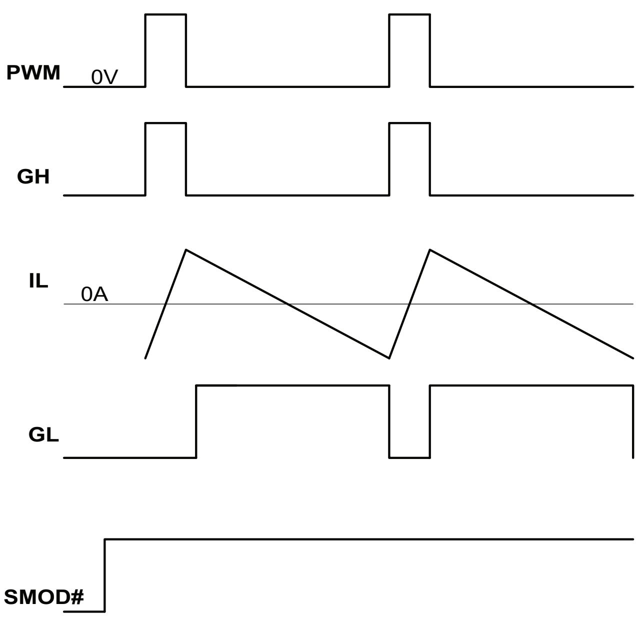

Figure 5: CCM Operation with SMOD# = HIGH

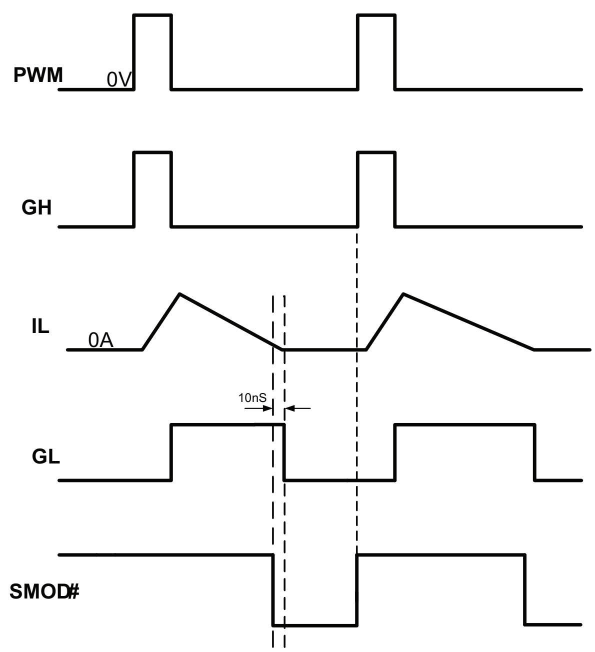

Figure 6: DCM Operation with SMOD# = Active Toggle

For technical questions, contact: powerictechsupport@vishay.com
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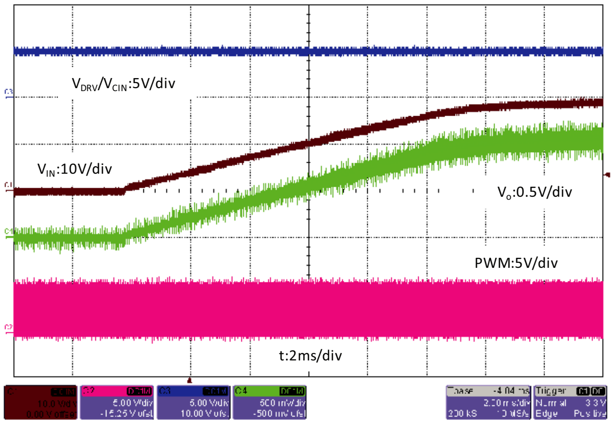
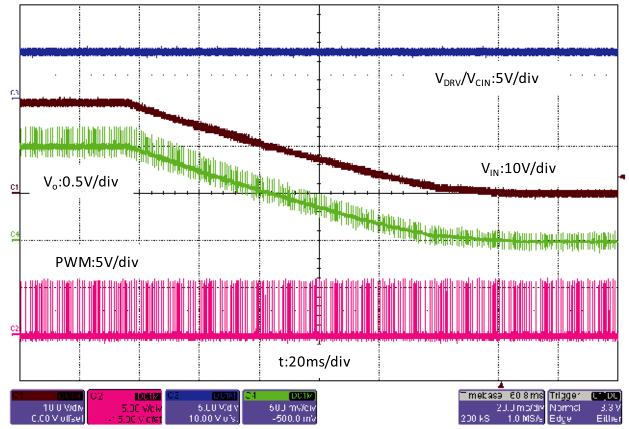
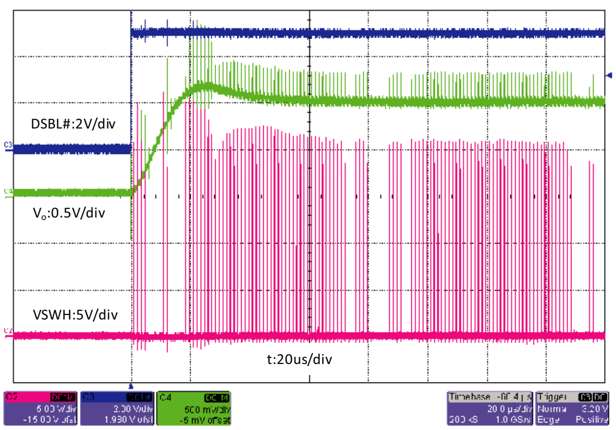
ELECTRICAL CHARACTERISTICS



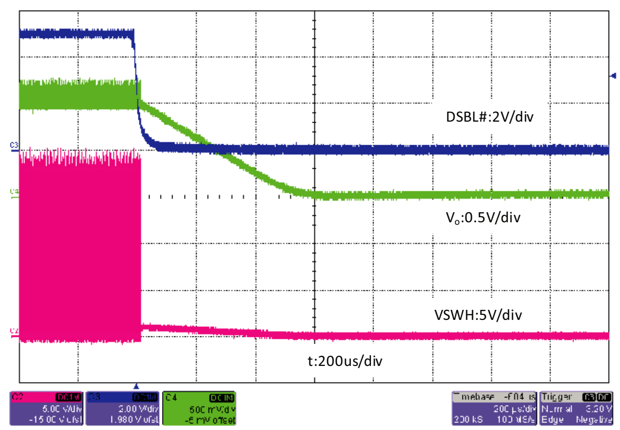
Start-up with V_{IN} Ramping Up
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 0 A



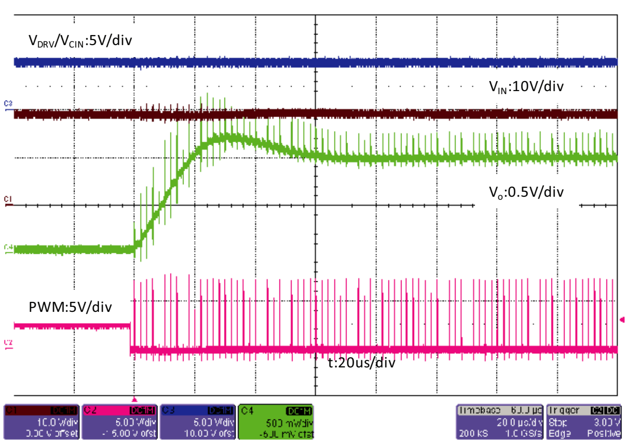
Power Off with V_{IN} Ramping Down
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A



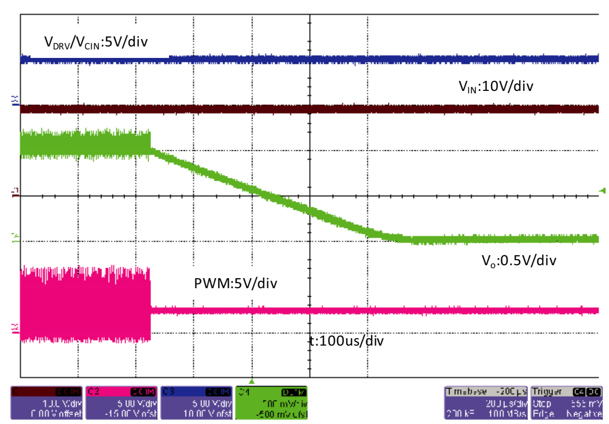
Enable with V_{IN} = 19 V,
V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A



Disable with V_{IN} = 19 V,
V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A

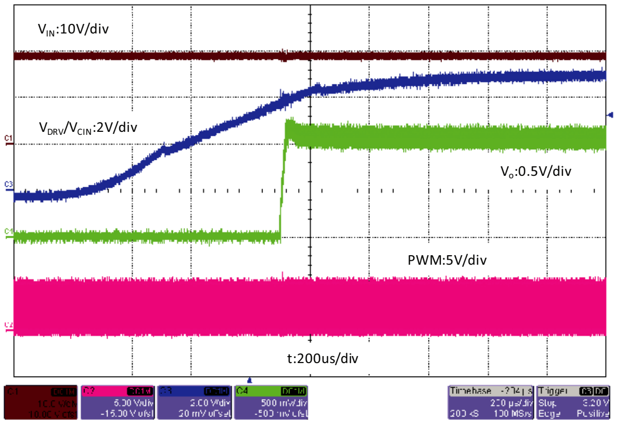


PWM Start with V_{IN} = 19 V,
V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A

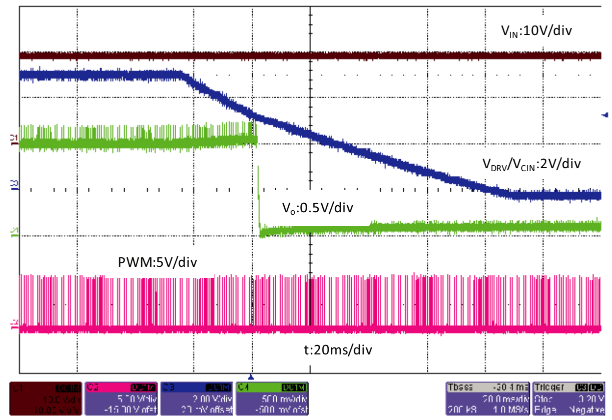


PWM Turn-off with V_{IN} = 19 V,
V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A

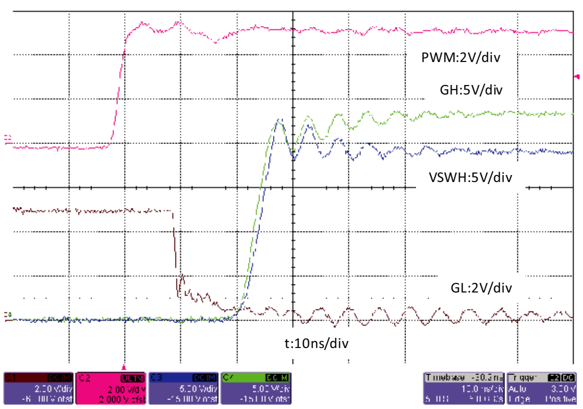
ELECTRICAL CHARACTERISTICS



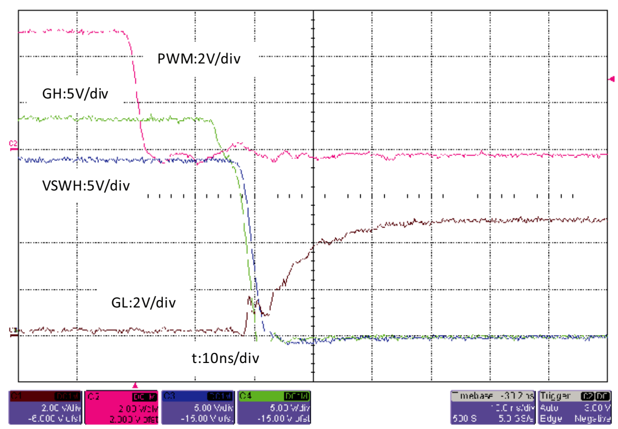
Start-up with V_{DRV}/V_{CIN} Ramping Up
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 0 A



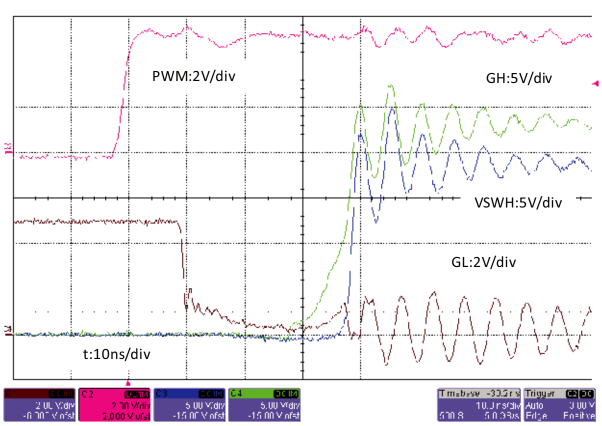
Power off with V_{DRV}/V_{CIN} Ramping Down
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A



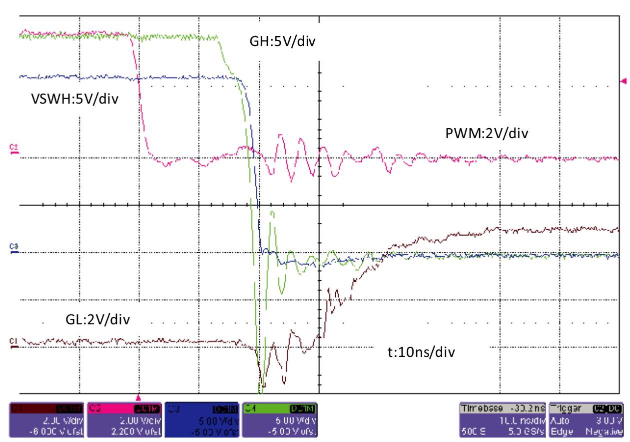
Switching Waveform at PWM Rising Edge
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 0 A



Switching Waveform at PWM Falling Edge
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 0 A

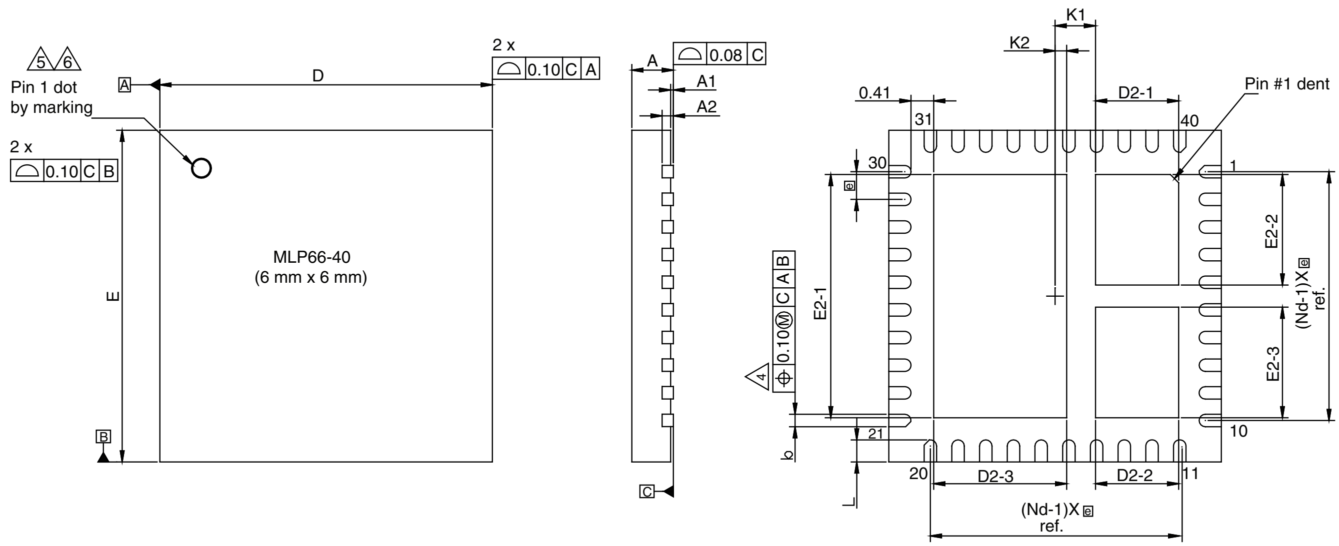


Switching Waveform at PWM Rising Edge
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 30 A



Switching Waveform at PWM Falling Edge
V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 30 A

PACKAGE DIMENSIONS



Top View Side View Bottom View

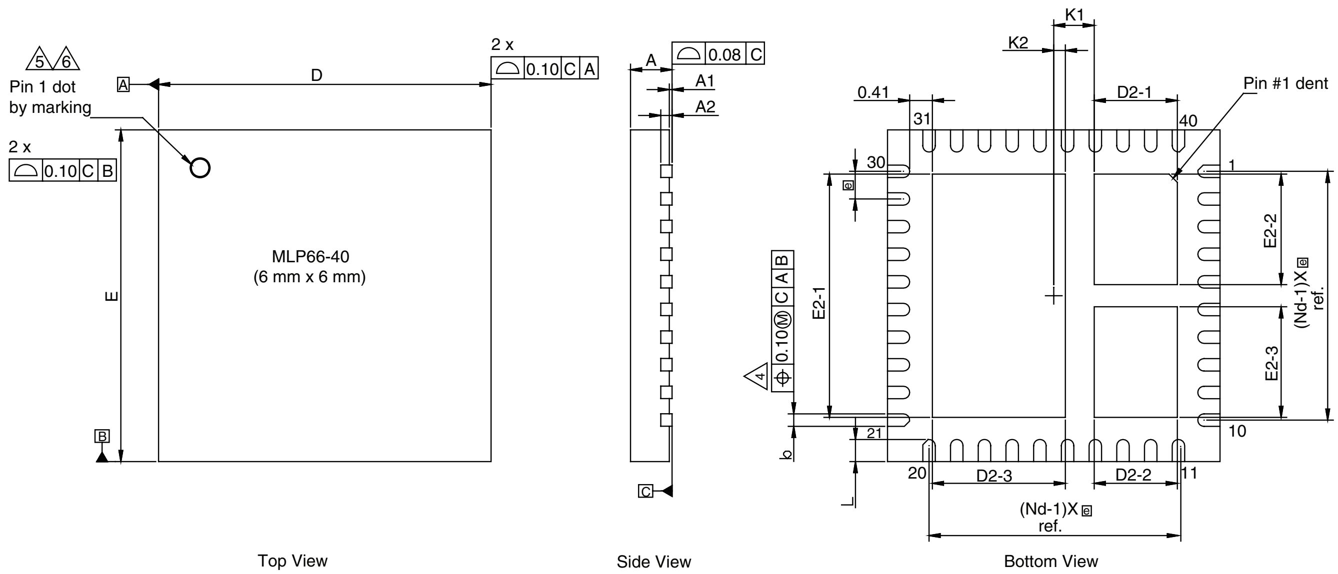
DIM	MILLIMETERS			INCHES		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A(8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b(4)	0.20	0.25	0.30	0.078	0.098	0.011
D	6.00 BSC			0.236 BSC		
e	0.50 BSC			0.019 BSC		
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N(3)	40			40		
Nd(3)	10			10		
Ne(3)	10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC			0.008 BSC		

Notes:

1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5M-1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction .
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body .
6. Exact shape and size of this feature is optional.
7. Package warpage max. 0.08 mm.
8. Applied only for terminals.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63822.

PowerPAK® MLP66-40 CASE OUTLINE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (4)	0.20	0.25	0.30	0.078	0.098	0.011
D		6.00 BSC			0.236 BSC	
e		0.50 BSC			0.019 BSC	
E		6.00 BSC			0.236 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)		40			40	
Nd (3)		10			10	
Ne (3)		10			10	
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1		0.73 BSC			0.028 BSC	
K2		0.21 BSC			0.008 BSC	
ECN: T09-0195-Rev. A, 04-May-09 DWG: 5986						

Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

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OCEAN CHIPS

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Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

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- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

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