

General Description

MIC4420, MIC4429 and MIC429 MOSFET drivers are tough, efficient, and easy to use. The MIC4429 and MIC429 are inverting drivers, while the MIC4420 is a non-inverting driver.

They are capable of 6A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4420/4429/429 accepts any logic input from 2.4V to V_S without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

MIC4420/4429/429 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern BiCMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability insures adequate gate voltage to the MOSFET during power up/down sequencing.

Note: See MIC4120/4129 for high power and narrow pulse applications.

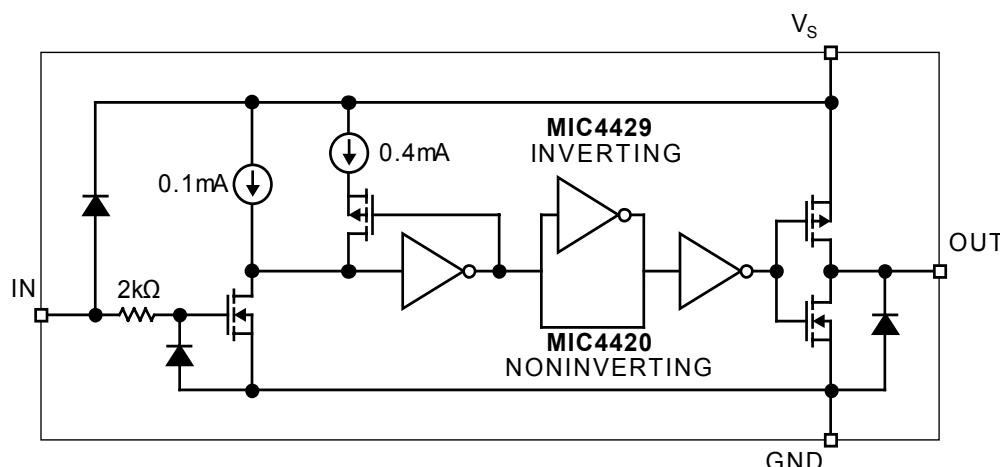
Features

- CMOS Construction
- Latch-Up Protected: Will Withstand >500mA Reverse Output Current
- Logic Input Withstands Negative Swing of Up to 5V
- Matched Rise and Fall Times 25ns
- High Peak Output Current 6A Peak
- Wide Operating Range 4.5V to 18V
- High Capacitive Load Drive 10,000pF
- Low Delay Time 55ns Typ
- Logic High Input for Any Voltage From 2.4V to V_S
- Low Equivalent Input Capacitance (typ) 6pF
- Low Supply Current 450 μ A With Logic 1 Input
- Low Output Impedance 2.5 Ω
- Output Voltage Swing Within 25mV of Ground or V_S

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class-D Switching Amplifiers

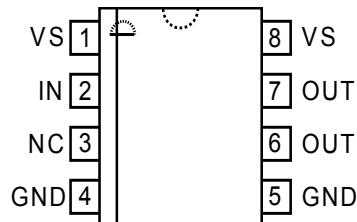
Functional Diagram



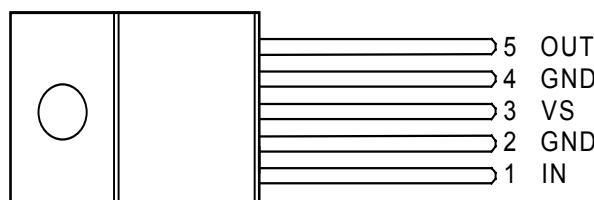
Ordering Information

Standard	Part No.	Pb-Free	Temperature Range	Package	Configuration
MIC4420CN		MIC4420ZN	0°C to +70°C	8-Pin PDIP	Non-Inverting
MIC4420BN		MIC4420YN	-40°C to +85°C	8-Pin PDIP	Non-Inverting
MIC4420CM		MIC4420ZM	0°C to +70°C	8-Pin SOIC	Non-Inverting
MIC4420BM		MIC4420YM	-40°C to +85°C	8-Pin SOIC	Non-Inverting
MIC4420BMM		MIC4420YMM	-40°C to +85°C	8-Pin MSOP	Non-Inverting
MIC4420CT		MIC4420ZT	0°C to +70°C	5-Pin TO-220	Non-Inverting
MIC4429CN		MIC4429ZN	0°C to +70°C	8-Pin PDIP	Inverting
MIC4429BN		MIC4429YN	-40°C to +85°C	8-Pin PDIP	Inverting
MIC4429CM		MIC4429ZM	0°C to +70°C	8-Pin SOIC	Inverting
MIC4429BM		MIC4429YM	-40°C to +85°C	8-Pin SOIC	Inverting
MIC4429BMM		MIC4429YMM	-40°C to +85°C	8-Pin MSOP	Inverting
MIC4429CT		MIC4429ZT	0°C to +70°C	5-Pin TO-220	Inverting

Pin Configurations



Plastic DIP (N)
SOIC (M)
MSOP (MM)



TO-220-5 (T)

Pin Description

Pin Number TO-220-5	Pin Number DIP, SOIC, MSOP	Pin Name	Pin Function
1	2	IN	Control Input
2, 4	4, 5	GND	Ground: Duplicate pins must be externally connected together.
3, TAB	1, 8	V _S	Supply Input: Duplicate pins must be externally connected together.
5	6, 7	OUT	Output: Duplicate pins must be externally connected together.
	3	NC	Not connected.

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage	20V
Input Voltage	$V_S + 0.3V$ to GND – 5V
Input Current ($V_{IN} > V_S$)	50mA
Power Dissipation, $T_A \leq 25^\circ C$	
PDIP	960W
SOIC	1040mW
5-Pin TO-220	2W
Power Dissipation, $T_C \leq 25^\circ C$	
5-Pin TO-220	12.5W
Derating Factors (to Ambient)	
PDIP	7.7mW/ $^\circ C$
SOIC	8.3mW/ $^\circ C$
5-Pin TO-220	17mW/ $^\circ C$
Storage Temperature	-65 $^\circ C$ to +150 $^\circ C$
Lead Temperature (10 sec.)	300 $^\circ C$

Operating Ratings

Supply Voltage	4.5V to 18V
Junction Temperature	150 $^\circ C$
Ambient Temperature	
C Version	0 $^\circ C$ to +70 $^\circ C$
B Version	-40 $^\circ C$ to +85 $^\circ C$
Package Thermal Resistance	
5-pin TO-220 (θ_{JC})	10 $^\circ C/W$
8-pin MSOP (θ_{JA})	250 $^\circ C/W$

Electrical Characteristics: ($T_A = 25^\circ C$ with 4.5V $\leq V_S \leq 18V$ unless otherwise specified. Note 4.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.4		V
V_{IL}	Logic 0 Input Voltage			1.1	0.8	V
V_{IN}	Input Voltage Range		-5		$V_S + 0.3$	V
I_{IN}	Input Current	$0 V \leq V_{IN} \leq V_S$	-10		10	μA
OUTPUT						
V_{OH}	High Output Voltage	See Figure 1	$V_S - 0.025$			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output Low	$I_{OUT} = 10 \text{ mA}, V_S = 18 \text{ V}$		1.7	2.8	Ω
R_O	Output Resistance, Output High	$I_{OUT} = 10 \text{ mA}, V_S = 18 \text{ V}$		1.5	2.5	Ω
I_{PK}	Peak Output Current	$V_S = 18 \text{ V}$ (See Figure 6)		6		A
I_R	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME (Note 3)						
t_R	Rise Time	Test Figure 1, $C_L = 2500 \text{ pF}$		12	35	ns
t_F	Fall Time	Test Figure 1, $C_L = 2500 \text{ pF}$		13	35	ns
t_{D1}	Delay Time	Test Figure 1		18	75	ns
t_{D2}	Delay Time	Test Figure 1		48	75	ns
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3 \text{ V}$ $V_{IN} = 0 \text{ V}$		0.45 90	1.5 150	mA μA
V_S	Operating Input Voltage		4.5		18	V

Electrical Characteristics: ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ with $4.5\text{V} \leq V_S \leq 18\text{V}$ unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
V_{IN}	Input Voltage Range		-5		$V_S + 0.3$	V
I_{IN}	Input Current	$0\text{V} \leq V_{IN} \leq V_S$	-10		10	μA
OUTPUT						
V_{OH}	High Output Voltage	Figure 1	$V_S - 0.025$			V
V_{OL}	Low Output Voltage	Figure 1			0.025	V
R_O	Output Resistance, Output Low	$I_{OUT} = 10\text{mA}$, $V_S = 18\text{V}$		3	5	Ω
R_O	Output Resistance, Output High	$I_{OUT} = 10\text{mA}$, $V_S = 18\text{V}$		2.3	5	Ω
SWITCHING TIME (Note 3)						
t_R	Rise Time	Figure 1, $C_L = 2500\text{pF}$		32	60	ns
t_F	Fall Time	Figure 1, $C_L = 2500\text{pF}$		34	60	ns
t_{D1}	Delay Time	Figure 1		50	100	ns
t_{D2}	Delay Time	Figure 1		65	100	ns
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3\text{V}$ $V_{IN} = 0\text{V}$		0.45 0.06	3.0 0.4	mA
V_S	Operating Input Voltage		4.5		18	V

Note 1: Functional operation above the absolute maximum stress ratings is not implied.

Note 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.

Note 3: Switching times guaranteed by design.

Note 4: Specification for packaged product only.

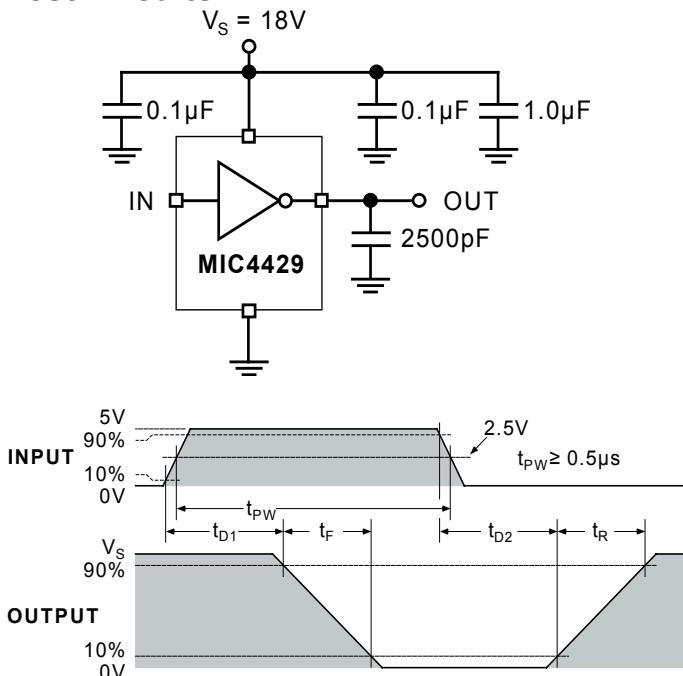
Test Circuits

Figure 1. Inverting Driver Switching Time

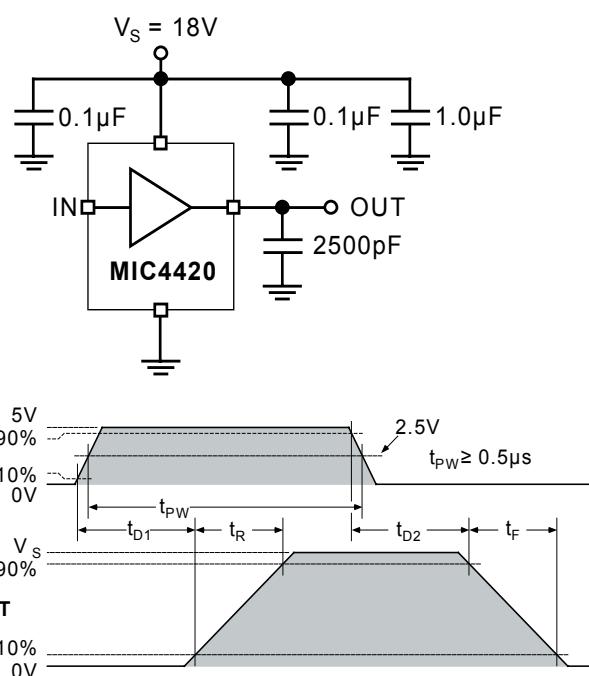
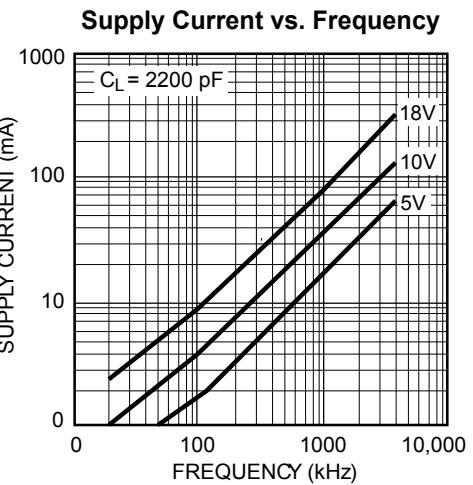
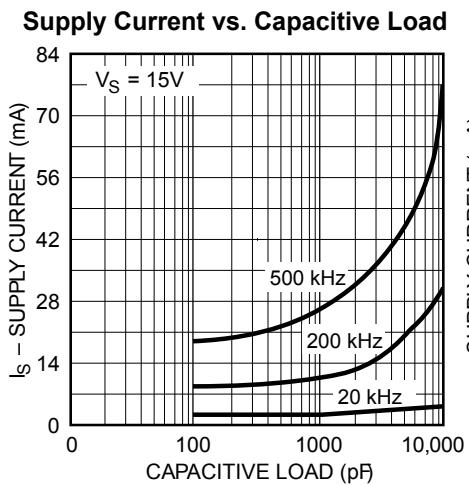
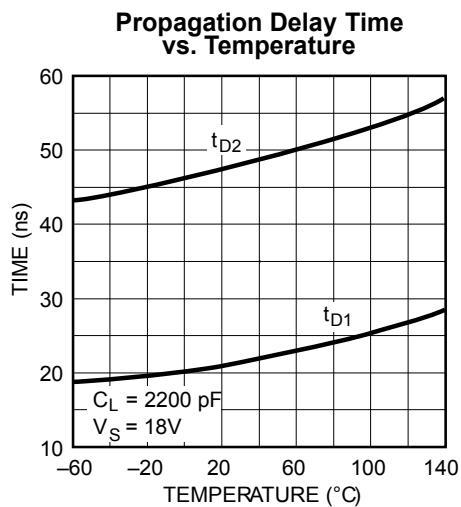
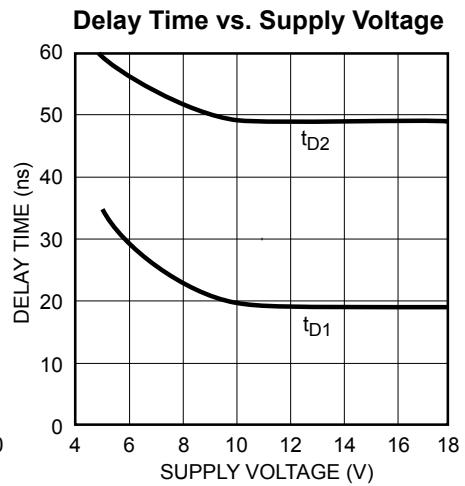
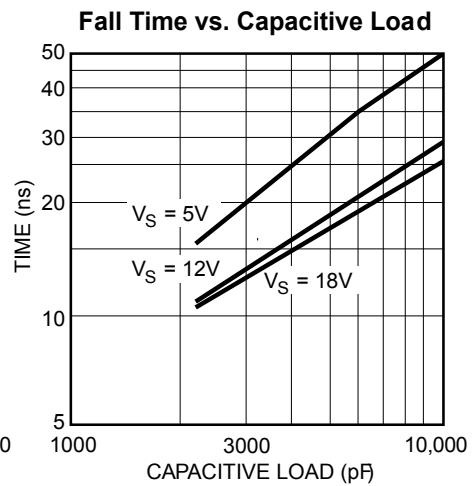
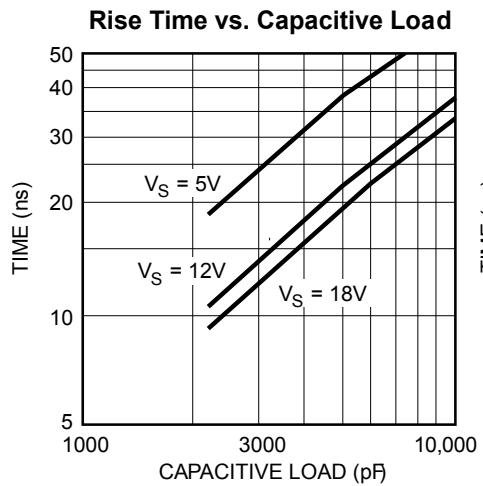
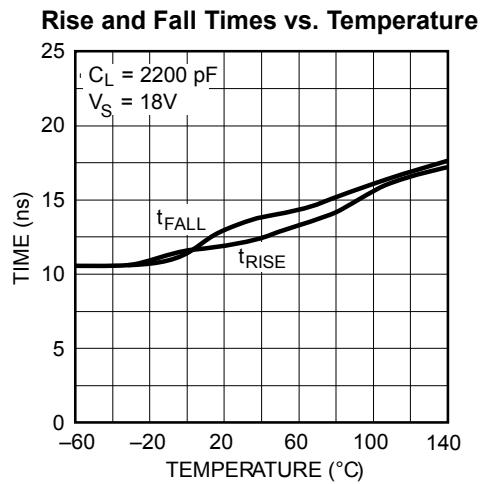
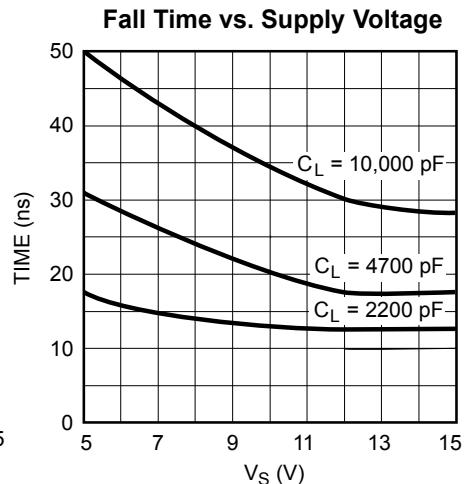
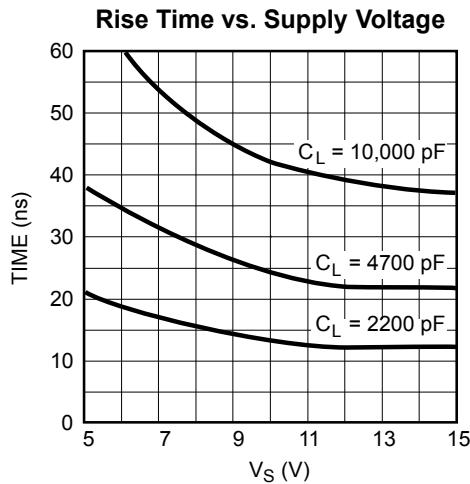
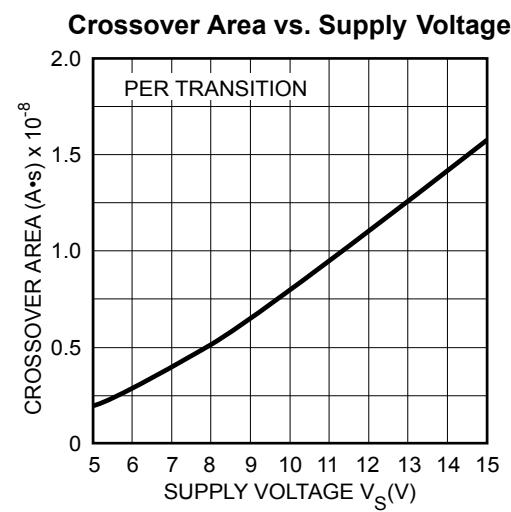
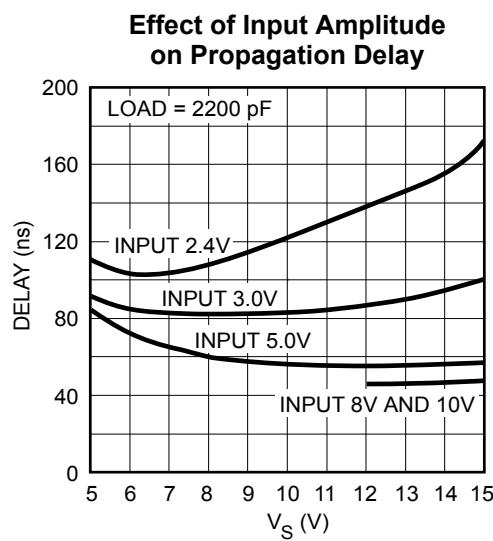
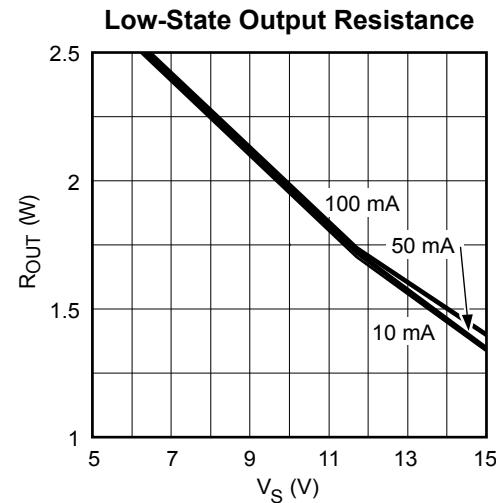
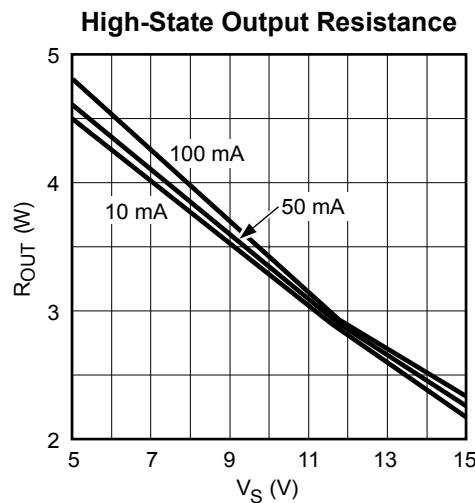
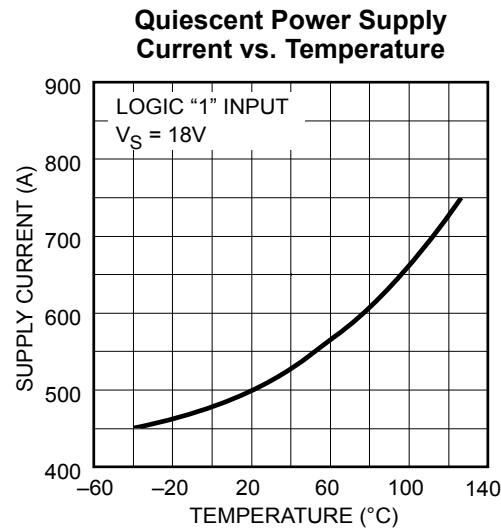
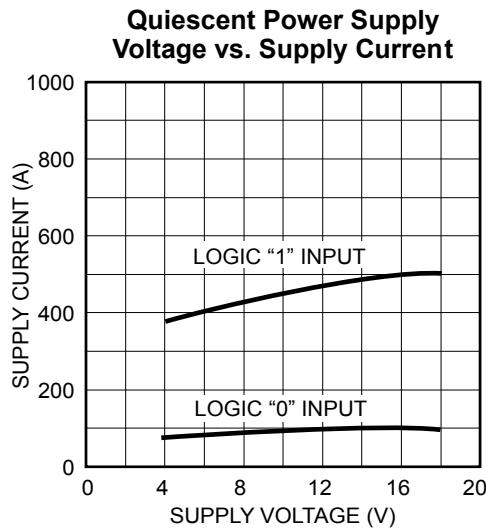


Figure 2. Noninverting Driver Switching Time

Typical Characteristic Curves



Typical Characteristic Curves (Cont.)



Applications Information

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500pF load to 18V in 25ns requires a 1.8 A current from the device power supply.

The MIC4420/4429 has double bonding on the supply pins, the ground pins and output pins. This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 1 μ F low ESR film capacitor in parallel with two 0.1 μ F low ESR ceramic capacitors, (such as AVX RAM GUARD[®]), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high current capability of the MIC4420/4429 demands careful PC board layout for best performance. Since the MIC4429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4429 input structure includes 300mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 3 shows the feedback effect in detail. As the MIC4429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To insure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4429 GND pins should, however, still be connected to power ground.

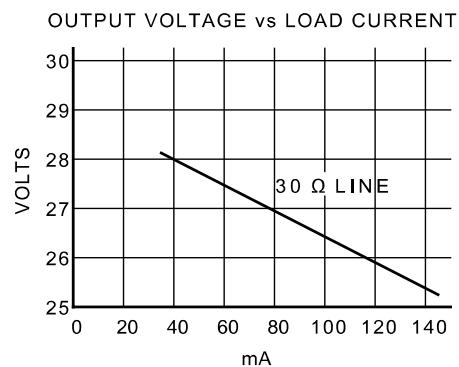
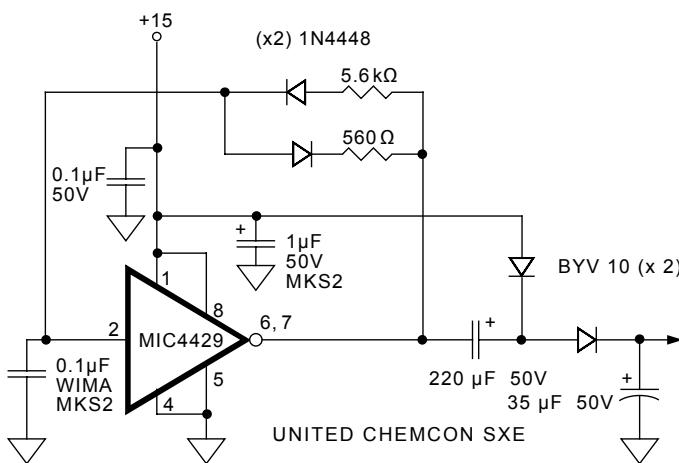


Figure 3. Self-Contained Voltage Doubler

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2 C V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage on the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = f C (V_S)^2$$

where:

f = Operating Frequency

C = Load Capacitance

V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I V_D (1-D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q , as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of $\leq 0.2\text{mA}$; a logic high will result in a current drain of $\leq 2.0\text{mA}$. Quiescent power can therefore be found from:

$$P_Q = V_S [D I_H + (1-D) I_L]$$

where:

I_H = quiescent current with input high

I_L = quiescent current with input low

D = fraction of time input is high (duty cycle)

V_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

$$P_T = 2 f V_S (\text{A}\cdot\text{s})$$

where ($\text{A}\cdot\text{s}$) is a time-current factor derived from the typical characteristic curves.

Total power (P_D) then, as previously described is:

$$P_D = P_L + P_Q + P_T$$

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is shown by the "Typical Characteristic Curve : Crossover Area vs. Supply Voltage and is in ampere-seconds. This figure must be multiplied by the number of repetitions per second (frequency) to find Watts.

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

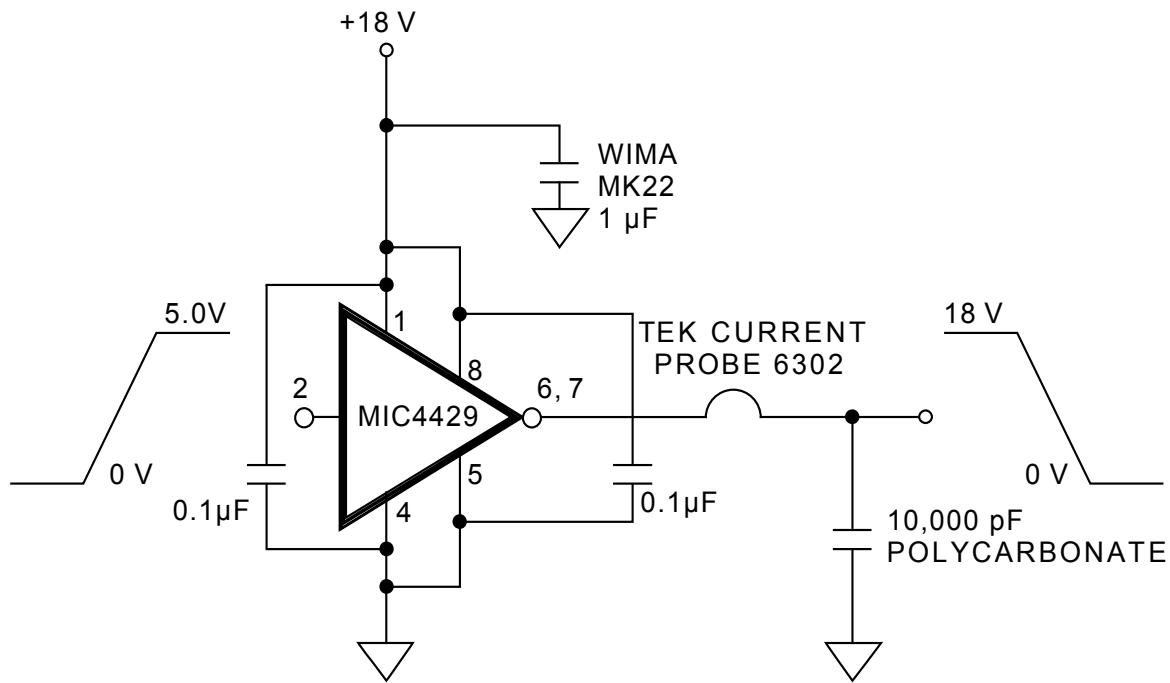
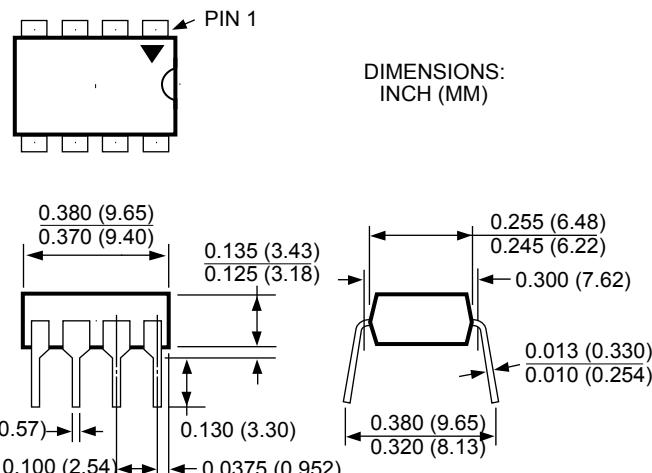
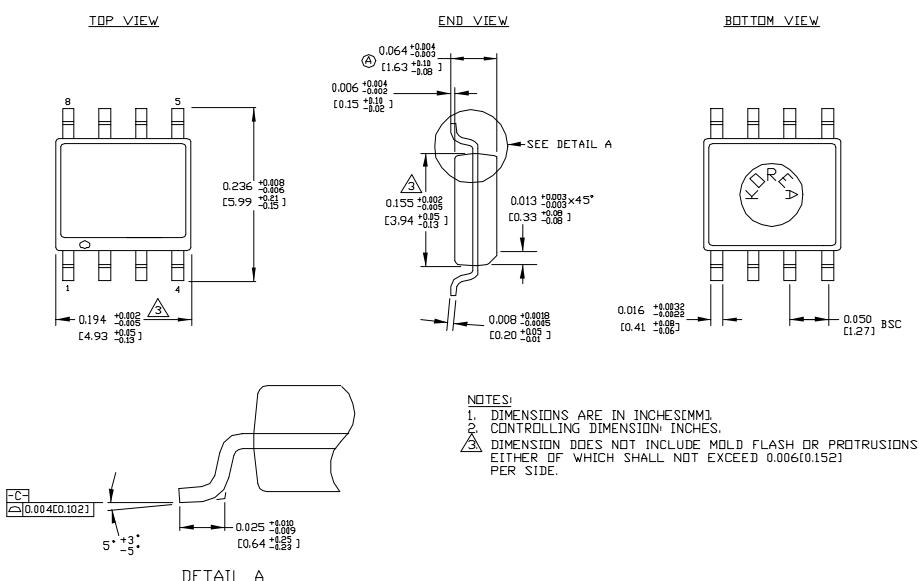


Figure 5. Peak Output Current Test Circuit

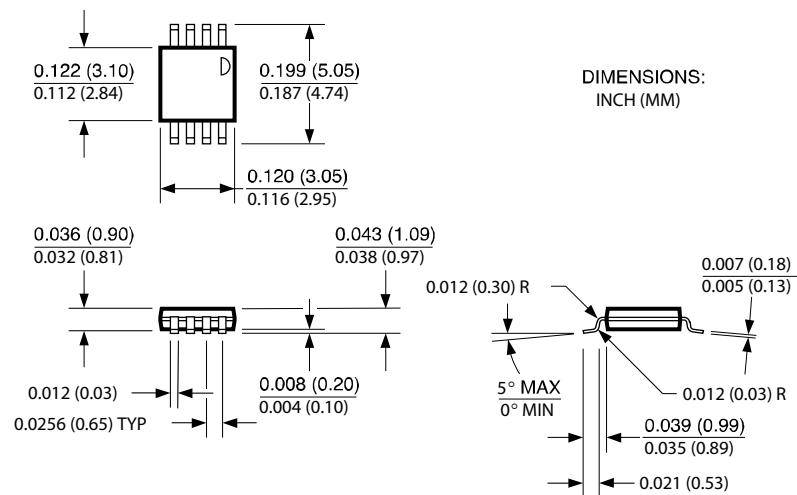
Package Information



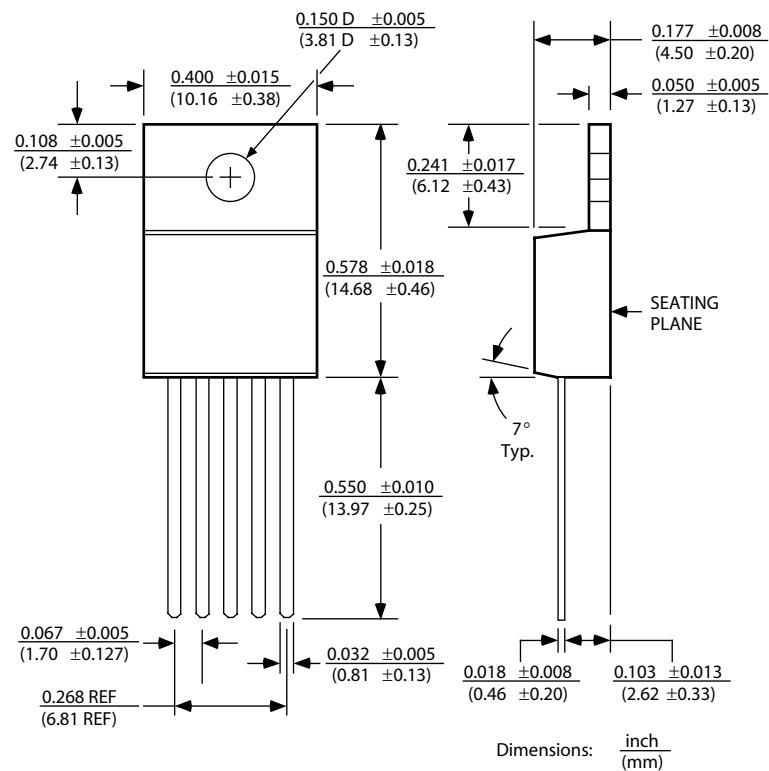
8-Pin Plastic DIP (N)



8-Pin SOIC (M)



8-Pin MSOP (MM)



5-Lead TO-220 (T)

MICREL INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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Телефон: 8 (812) 309-75-97 (многоканальный)

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Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А