Future Technology Devices International Ltd.

Morph-IC-II

Datasheet

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Morph-IC-II is a compact, yet powerful FPGA module which is capable of synthesising LSI (Large Scale Integration) designs using the embedded Altera Cyclone-II FPGA. Communication between the FPGA and a PC is carried out via the FTDI FT2232H, a USB 2.0 Hi-Speed (480Mbit/s) USB bridge. Sub-100ms FPGA programming/re-programming makes Morph-IC-II ideal for applications which require users to reconfigure hardware functionality 'on-the-fly' by downloading new software over USB : "morphing" the hardware.

Morph-IC-II has increased in capability and processing power from a previous FTDI FPGA module called MorphIC-1K.

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1 Introduction

Morph-IC-II is a compact and powerful FPGA module which is capable of implementing LSI (Large Scale Integration) designs or entry level VLSI (Very Large Scale Integration) designs. Designs can be synthesised through utilising up to 4,608 Logic Elements of Morph-IC-II's on board FPGA.

The Morph-IC-II platform combines an Altera Cyclone®-II FPGA with high-performance USB 2.0 capabilities that facilitate Hi-speed communications with ultra-fast, sub-100ms FPGA programming/re-programming. This makes Morph-IC-II ideal for applications which require users to reconfigure hardware functionality 'on-the-fly' by downloading new software over USB : "morphing" the hardware.

Communication between the FPGA and the PC is done through a USB 2.0 connection to the FTDI FT2232H USB 2.0 Hi-Speed (480Mbit/s) USB bridge. Morph-IC-II is an easy to use module which allows users to program and interact with the FPGA using a free software package produced by Altera called Quartus II.

This datasheet describes the following:

- Features and applications of Morph-IC-II

- The pin configuration

- Mechanical details

- User guide

- Schematic details

- EEPROM default setting

Morph-IC-II is fully backward compatible with the MorphIC-1K module (the predecessor of Morph-IC-II). The MorphIC-1K is an FPGA/USB module used in medium scale production as an alternative to producing an ASIC and prototyping. Morph-IC-II is an upgraded version of the MorphIC-1K with increased capacity and increased speed. Morph-IC-II is a plug in replacement for the MorphIC-1K, but Morph-IC-II has additional I/Os. For new applications, it is recommended to design any application board for the Morph-IC-II header configuration to utilize the additional 40 I/Os and the JTAG signal ports of the header.

Although Morph-IC-II is fully backward compatible with MorphIC-1K, there are some differences. For example, Morph-IC-II uses Port A for the FIFO interface rather than Port B. Morph-IC-II has some additional features over MorphIC-1K such as being able to operate some I/Os at various logic voltage levels. For example the I/O can be operated at 1.5V/1.8V/2.5V/3.3V. This provides added flexibility to the designer.

Morph-IC-II is shown in Fig. 1. The module has 4 connectors giving access to all the FPGA I/Os plus a JTAG header, that can be used to interface to Morph-IC-II with *SignalTap Analyser* (a function included in the Quartus-II package). SignalTap can be used to display the waveform of every pin of the FPGA. Morph-IC-II interfaces to a PC through a USB Type B connector. Two LEDs indicate when the board is powered and when the FPGA is programmed.

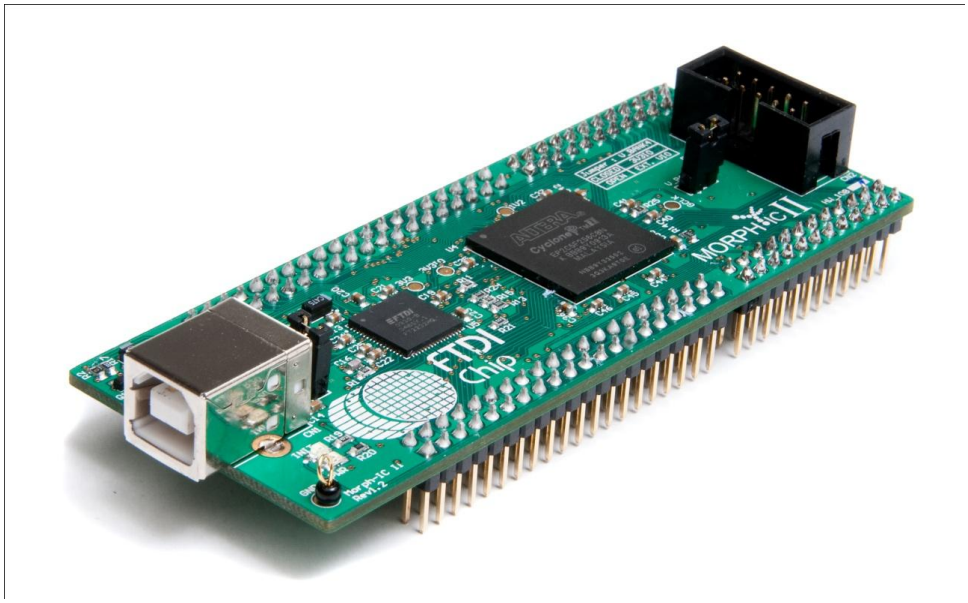

Fig. 1 – The Morph-IC-II

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1.1 Applications

Possible applications:

- ASIC prototyping using USB connectivity to FPGA.
- Providing a fast and easy alternative to ASIC solutions for low to medium volumes of product.
- Academic FPGA design exercise – ideal for learning and experimenting with HDL (Hardware Design Language)
- Digital signal processing
- Audio/Video
- Cryptography

2 Features

Morph-IC-II has the following features:

- FT2232HQ Dual, Hi-Speed USB UART/FIFO IC used for USB communications
- Altera Cyclone 2 - EP2C5F256C8N FPGA capable of synthesizing large scale integrated circuits
- Ultra fast FPGA configuration/reconfiguration over USB (under 0.1 sec)
- 4,608 Embedded FPGA Logic Elements (about 80,000 Gates typically)
- 26 Embedded Logic RAM Elements (119Kbits)
- FPGA-PC USB Data Transfer at up to 40M Byte/sec
- Onboard 93LC56B configuration EEPROM
- MOSFET switched 5V and 3.3V power outputs for powering external logic
- Onboard 12MHz crystal and essential support components for FT2232HQ
- 80 dedicated external I/O pins
- Onboard 50MHz oscillator as FPGA primary clock – also available for external use.
- JTAG interface for testing the I/Os and registers of the FPGA
- 1 dedicated external clock input
- Powered from USB bus or external PSU
- Standard 0.1 inch pitch format connector pins, ideal for rapid prototyping or small-medium size production runs
- FTDI's VCP and D2XX USB Windows and Linux USB drivers (provided) eliminate the need for driver development in most cases
- FPGA loader interface DLL (for Windows only not including CE) supplied including interface examples in VB, VC++ and Delphi
- Stand-alone FPGA loader programs provided for Windows and Linux
- VHDL programming examples (I/O over USB) provided
- Delphi application software examples including source code provided
- Free Altera Quartus II Software Starter Suite development software available from the Altera Website
- Backward compatible with the existing MorphIC-I
- Supports 1.5/1.8/2.5/3.3-V LVTTL/LVCMOS signals, IOBANK1-3 restricted to 3.3V.

2.1 Driver Support

Morph-IC-II uses the FTDI Ft2232H USB bridge chip. This chip requires USB drivers which can be downloaded free of charge from http://www.ftdichip.com/FTDrivers.htm.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 2000, Server 2003, XP Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows 7
- Windows XP Embedded
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Mac OS-X
- Linux (2.6.9 or later)

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 2000, Server 2003, Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows 7
- Windows XP Embedded
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Linux (2.4 or later) and Linux x86_64

The utilities included Morph-IC-II package can run on Windows 2000, ME, XP, Vista and 7.

The recommend design utility for Morph-IC-II is Quartus-II. This free software can be downloaded from the Altera website: **http://www.altera.com**.

3 Functional Description

3.1 Morph-IC-II Block Diagram

A block diagram of the Morph-IC-II is given in Fig. 2. Morph-IC-II module can be USB powered or self powered. The power mode is selected using the "VBUS" jumper - as indicated on the diagram below. The FPGA can be programmed from a PC via the USB interface and the FT2232H USB bridge.

FT2232H requires a 12MHz crystal and an external EEPROM which is used to configure FT2232H.

The Altera FPGA is powered from a +3.3V regulator supply with the exception of its internal PLLs which are powered by a +1.2V regulated supply. The power supply to the FPGA is disabled, using the MOSFET switch, when FT2232H is in power save mode.

The I/Os of the FPGA are partitioned into 4 I/O banks. These banks each have their own power connection. The voltage of the power connection to each bank defines the voltage level of the signals of that bank.

The power supply to I/O bank 4 is configured differently to add more flexibility. The I/O bank 4 power can be supplied from an external supply to the V_Bank 4 pins on J2 or from the 3V3IO net connected to the on board regulator. This feature allows signals of different voltage levels to be used in an application and is explained with more detail in Section 3.2.

Morph-IC-II uses a 50MHz oscillator which provides the clock source to the FPGA. Alternatively the FPGA can be synchronised to an external clock using the CLKIN pin on connector J2.

The four connectors J1, J2, J3 and J4 provide I/O connectivity between Morph-IC-II and any application board. The connector give a total of 80 signal lines, a FIFO interface capability, power supply pins, an external clock line and an external reset line. The JTAG interface can be accessed through the JTAG port or J3 and J4 connectors, using an Altera Byte Blaster (or equivalent) cable and *SignalTap Analyser* which is an application of Quartus II the signals of all the I/Os of the FPGA can be displayed on a PC monitor.

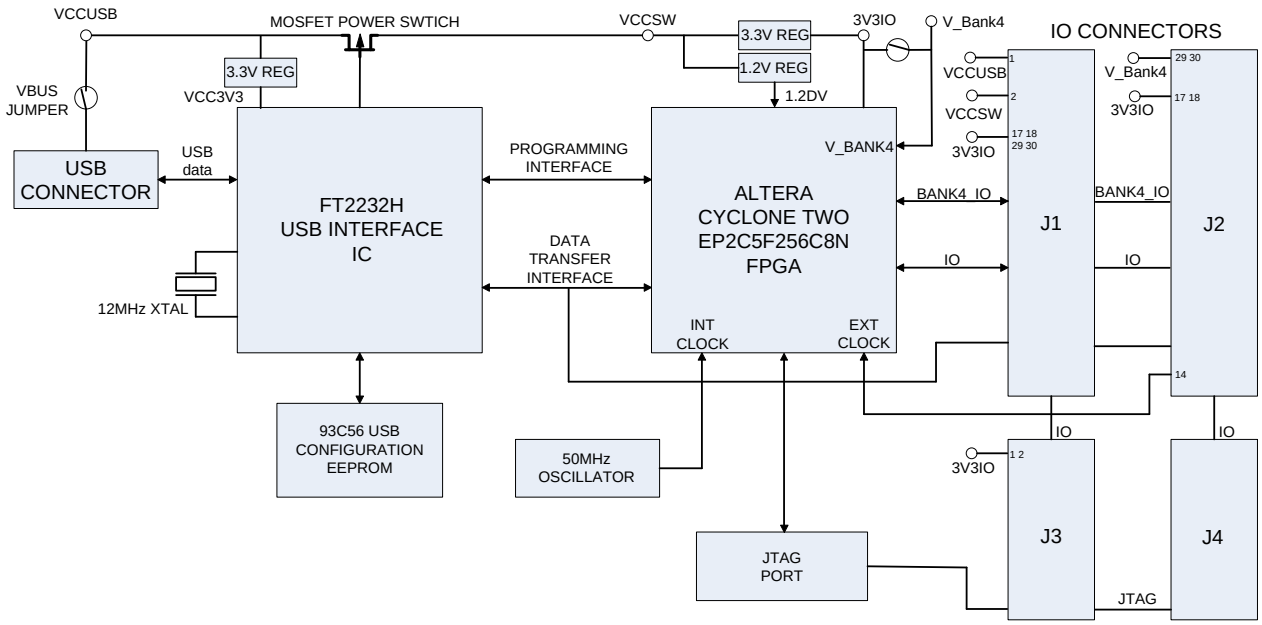

Fig. 2 – Hardware Representation of the Morph-IC-II

3.2 Getting Started

3.2.1 Configuring the Jumper settings

Morph-IC-II module has two jumpers labelled VBUS and V_BANK4.

1) **Jumper VBUS connects USB connector pin 1 to J1-1.**

   A) When jumper VBUS is closed, the Morph-IC-II module is powered from the USB bus. This connects the VBUS power from the USB host PC to the voltage regulator input of Morph-IC-II. This voltage regulator provides power to the following: VCC3V3, VPLL and VUSB all of which power the FT2232H chip. This mode is known as "bus powered mode".

   B) When jumper VBUS is open, the Morph-IC-II module requires an external voltage supply of 5 Volts DC applied to J1-1. This mode is known as "self powered mode".

2) **Jumper V_BANK4 connects 3V3IO to the power supply pins of Bank 4.**

   A) When jumper V_BANK4 is closed, a short is formed between 3V3IO and V_BANK4. This connection provides 3.3 volts to I/O Bank 4 of the FPGA.

   NOTE: When this jumper is closed J2-29 and J2-30 must be unconnected or connected to a 3V3 supply (this is the case for typical MorphIC-1K application boards).

   B) When jumper V_BANK4 is open, an external voltage supply must be applied to J2-29 and J2-30 to power the I/O Bank 4. The voltage level supplied should match the voltage level of the input signals.

A summary of the jumper functions is given in Table 1.

Jumper Name	State	Description
VBUS	CLOSED	Powered from the USB Bus
VBUS	OPEN	An external supply needs to be applied via J1-1
V_BANK4	CLOSED	3.3V supplied to I/O Bank 4
V_BANK4	OPEN	An external voltage of either 1.5V, 1.8V, 2.5V or 3.3V needs to be applied to I/O Bank 4 via J2-29 and J2-30

Table 1 – Jumper Description

NOTE: When using V_BANK4, care must be taken regarding this jumper; if there is a large enough discrepancy between the voltage that powers an IO Bank and the logic high voltage of the signals processed by the bank damage can occur.

3.2.2 Configuring the FPGA

The Morph-IC-II package includes a *.RBF loader programme called "MorphLd". This programme is used to load RBF files into the FPGA of Morph-IC-II via the USB to Passive Serial interface. These *.RBF are synthesised HDL (VHDL or Verilog) code with additional settings for the FPGA specified by the Quartus-II options. These files are generated when a HDL project is compiled using (suitably configured) Quartus-II or a similar HDL compiler. Using this utility along with Quartus-II the HDL code of an application can be compiled and exported to Morph-IC-II.

(See AN_141_MorphIO-II and MorphLd Utilities for Morph-IC-II)

3.3 Morph-IC-II Signal Levels Supported.

Morph-IC-II provides a flexible method to process signals of different voltage levels. This method allows a voltage of either 3.3V, 2.5V, 1.8V or 1.5V to be applied to I/O Bank 4 by adjusting the externally supplied power supply to bank 4 and reconfiguring the pin-map. This means Morph-IC-II supports the different voltage levels on different banks as shown in Fig. 3.

As illustrated in Fig. 3 I/O Banks 1 – 3 can only process 3.3V TTL and CMOS signals. Other voltage levels are not supported on these I/O banks since signal lines between FT2232H and FPGA are connected to these I/Os. Therefore a 3.3V power supply is hardwired to the voltage supplies of I/O Bank 1-3.

A step by step example of how to modify the I/O signal levels of I/O Bank 4 is given in a separate applications note "AN_141_MorphIO-II and MorphLd Utilities for Morphic-II". This can be downloaded from the FTDI website.

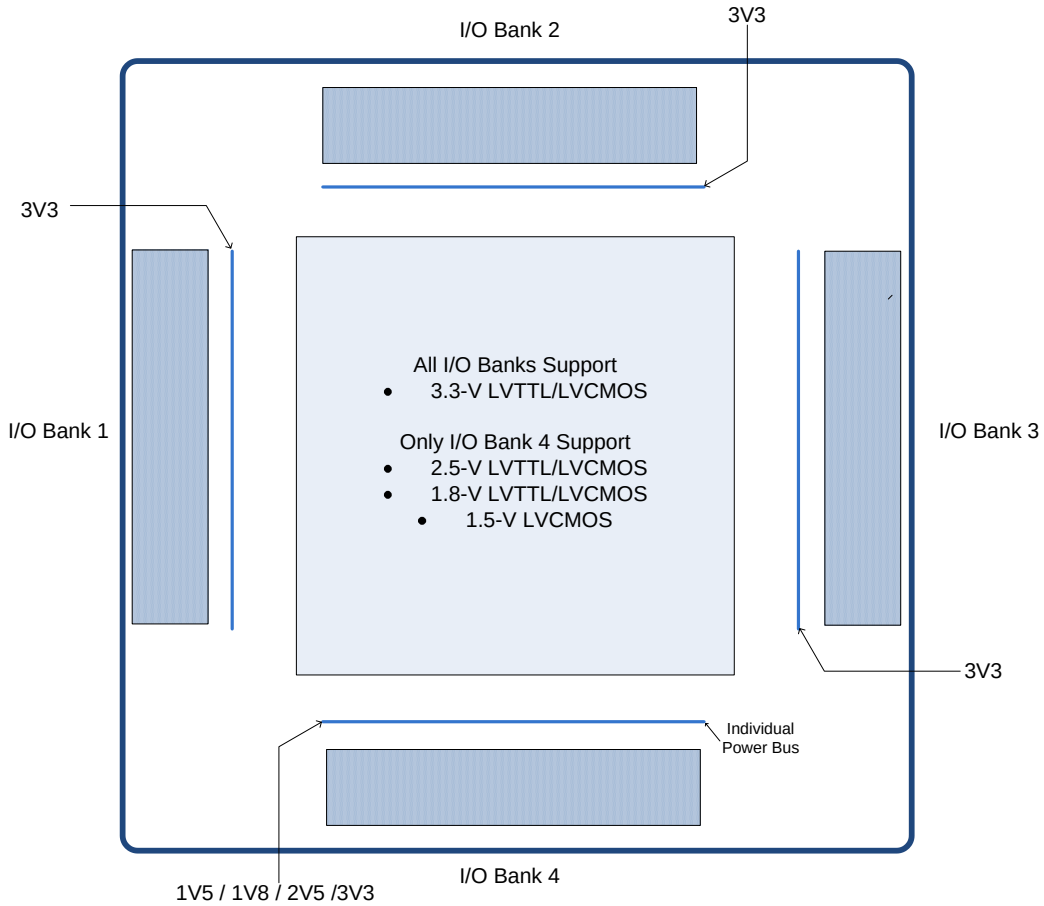

Fig. 3 – I/O Bank *Logic Voltage Levels*

3.4 Morph-IC-II Header Connections.

Morph-IC-II's FPGA is connected to five connectors: J1-J4 and the JTAG Port.

J1 to J4 are used for the following functions: connecting I/Os, "self-powered" power supply, specific bank supply voltages and clock connections.

The JTAG connector is used to scan the I/O and registers of the FPGA.

Reference Designator	Name	Description
J1	-	40 Pin Header
J2	-	40 Pin Header
J3	-	24 Pin Header
J4	-	24 Pin Header
CN1	-	USB Connector
CN2	JTAG Port	JTAG Port, used to scan I/Os and registers of the FPGA, this feature makes it possible to probe of the signals of a FPGA.

Table 2 – Connector Description

A description for each Morph-IC-II connector is given in Table 2.

The pin description of J1, J2, J3 and J4 connectors are given in Table 3, Table 4, Table 5 and Table 6.

Pin labels for these headers are also illustrated in Fig 4 and Fig 5.

Connector Pin	Name	Description		Connector Pin	Name	Description
J1-1	VCCUSB	When Jumper VBUS is closed J1-1 outputs the USB Bus Voltage, When Jumper VBUS is open J1-1 is an input for and external power supply to the board.		J1-21	IOR3	General Input/output
J1-2	VCCSW	5V Power pin, turned off during USB suspend		J1-22	IOL3	General Input/output
J1-3	AD4	Data Transfer Interface		J1-23	GND	0V Power pin
J1-4	AD5	Data Transfer Interface		J1-24	GND	0V Power pin
J1-5	AD6	Data Transfer Interface		J1-25	IOL4	General Input/output
J1-6	AD7	Data Transfer Interface		J1-26	IOM4	General Input/output
J1-7	TXE#	Data Transfer Interface (Active Low)		J1-27	IOP4	General Input/output
J1-8	RXF#	Data Transfer Interface (Active Low)		J1-28	IOK4	General Input/Output
J1-9	WR#	Data Transfer Interface (Active Low)		J1-29	3V3IO	3.3V Power pin, turned off during USB suspend
J1-10	RD#	Data Transfer Interface (Active Low)		J1-30	3V3IO	3.3V Power pin, turned off during USB suspend
J1-11	GND	0V Power pin		J1-31	IOP5	General Input/Output
J1-12	GND	0V Power pin		J1-32	IOK5	General Input/Output
J1-13	IOK1	General Input/Output		J1-33	IOR7	General Input/Output
J1-14	RESETIN#	Reset Input (Active Low)		J1-34	ION8	General Input/Output
J1-15	IOP11	General Input/Output		J1-35	GND	0V Power pin
J1-16	IOC1	General Input/Output		J1-36	GND	0V Power pin
J1-17	3V3IO	3.3V Power pin, turned off during USB suspend		J1-37	NC	No Connection
J1-18	3V3IO	3.3V Power pin, turned off during USB suspend		J1-38	IOR8	General Input/Output
J1-19	IOT4	General Input/Output		J1-39	IOL9	General Input/Output
J1-20	IOT7	General Input/Output		J1-40	IOM11	General Input/Output

Table 3 – Pin out of Connection J1

Connector Pin	Name	Description		Connector Pin	Name	Description
J2-1	AD3	Data Transfer Interface		J2-21	IOA6	General Input/Output
J2-2	AD2	Data Transfer Interface		J2-22	IOB7	General Input/Output
J2-3	AD0	Data Transfer Interface		J2-23	GND	0V Power pin
J2-4	AD1	Data Transfer Interface		J2-24	GND	0V Power pin
J2-5	NC	No Connection		J2-25	IOG7	General Input/Output
J2-6	NC	No Connection		J2-26	IOA9	General Input/Output
J2-7	IOE4	General Input/Output		J2-27	IOG6	General Input/Output
J2-8	IOE3	General Input/Output		J2-28	IOF6	General Input/Output
J2-9	IOE5	General Input/Output		J2-29	V_BANK4	3.3V Power pin/V-Bank 4 power supply
J2-10	IOD4	General Input/Output		J2-30	V_BANK4	3.3V Power pin/V-Bank 4 power supply
J2-11	GND	0V Power pin		J2-31	IOD5	General Input/Output
J2-12	GND	0V Power pin		J2-32	IOC5	General Input/Output
J2-13	IOA7	General Input/Output		J2-33	IOE6	General Input/Output
J2-14	CLKIN	Secondary input clock source		J2-34	IOD8	General Input/Output
J2-15	IOA3	General Input/Output		J2-35	GND	0V Power pin
J2-16	GND	General Input/Output		J2-36	GND	0V Power pin
J2-17	3V3IO	3.3V Power pin, turned off during USB suspend		J2-37	IOF9	General Input/Output
J2-18	3V3IO	3.3V Power pin, turned off during USB suspend		J2-38	IOC11	General Input/Output
J2-19	IOA5	General Input/Output		J2-39	IOC12	General Input/Output
J2-20	IOD6	General Input/Output		J2-40	IOC13	General Input/Output

Table 4 – Pin out of Connection J2

Connector Pin	Name	Description		Connector Pin	Name	Description
J3-1	3V3IO	3.3V Power pin, turned off during USB suspend		J3-13	IOR14	General Input/Output
J3-2	3V3IO	3.3V Power pin, turned off during USB suspend		J3-14	ION14	General Input/Output
J3-3	ION11	General Input/Output		J3-15	IOP16	General Input/Output
J3-4	IOP13	General Input/Output		J3-16	IOP15	General Input/Output
J3-5	IOL12	General Input/Output		J3-17	ION16	General Input/Output
J3-6	IOT9	General Input/Output		J3-18	IOM14	General Input/Output
J3-7	IOR9	General Input/Output		J3-19	IOL16	General Input/Output
J3-8	IOT10	General Input/Output		J3-20	IOL15	General Input/Output
J3-9	IOR11	General Input/Output		J3-21	IOK16	General Input/Output
J3-10	IOT13	General Input/Output		J3-22	IOF16	General Input/Output
J3-11	IOR13	General Input/Output		J3-23	JTAG_TDI	JTAG Interface
J3-12	IOT14	General Input/Output		J3-24	JTAG_TMS	JTAG Interface

Table 5 – Pin out of Connection J3

Connector Pin	Name	Description		Connector Pin	Name	Description
J4-1	IOF15	General Input/Output		J4-13	IOB13	General Input/Output
J4-2	IOD13	General Input/Output		J3-14	IOA13	General Input/Output
J4-3	IOH13	General Input/Output		J4-15	IOB14	General Input/Output
J4-4	IOD14	General Input/Output		J4-16	IOA14	General Input/Output
J4-5	IOG12	General Input/Output		J4-17	IOD15	General Input/Output
J4-6	IOG13	General Input/Output		J4-18	IOD16	General Input/Output
J4-7	IOJ11	General Input/Output		J4-19	IOE14	General Input/Output
J4-8	IOC14	General Input/Output		J4-20	IOE16	General Input/Output
J4-9	IOJ12	General Input/Output		J4-21	GND	0V Power pin
J4-10	IOG16	General Input/Output		J4-22	GND	0V Power pin
J4-11	IOB12	General Input/Output		J4-23	JTAG_TDO	JTAG Interface
J4-12	IOA12	General Input/Output		J4-24	JTAG_TCK	JTAG Interface

Table 6 – Pin out of Connection J4

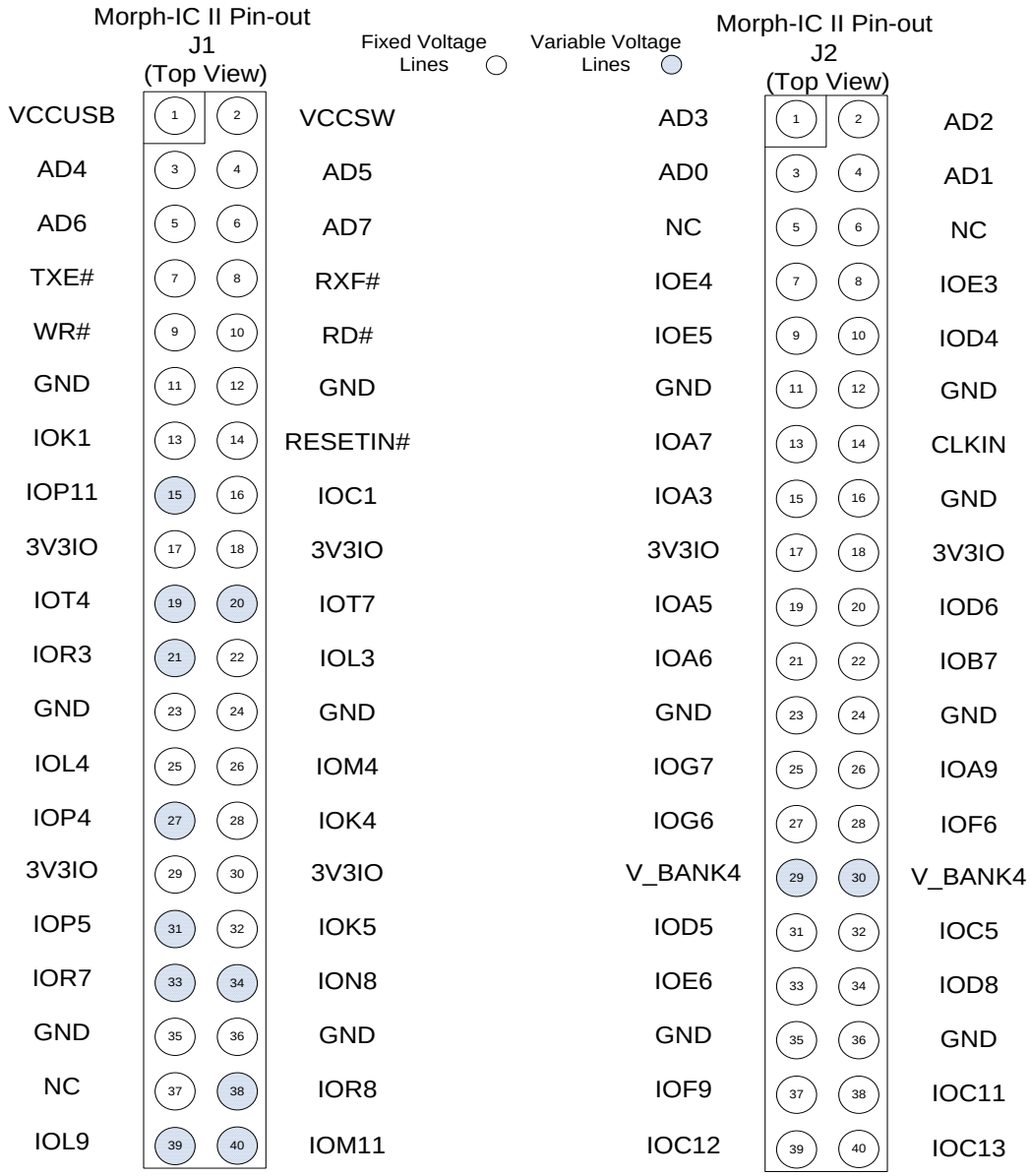

Fig. 4 – Pin outs of J1 & J2

= Active Low

The signal names of J1 and J2 are illustrated in Fig. 4. The pins are colour coded to indicate whether or not the pin is associated with I/O BANK4. Likewise Fig. 5 defines the pins associated with the variable voltage level tolerant I/O BANK4. Fig 5 also details labelling of J3 and J4 signals.

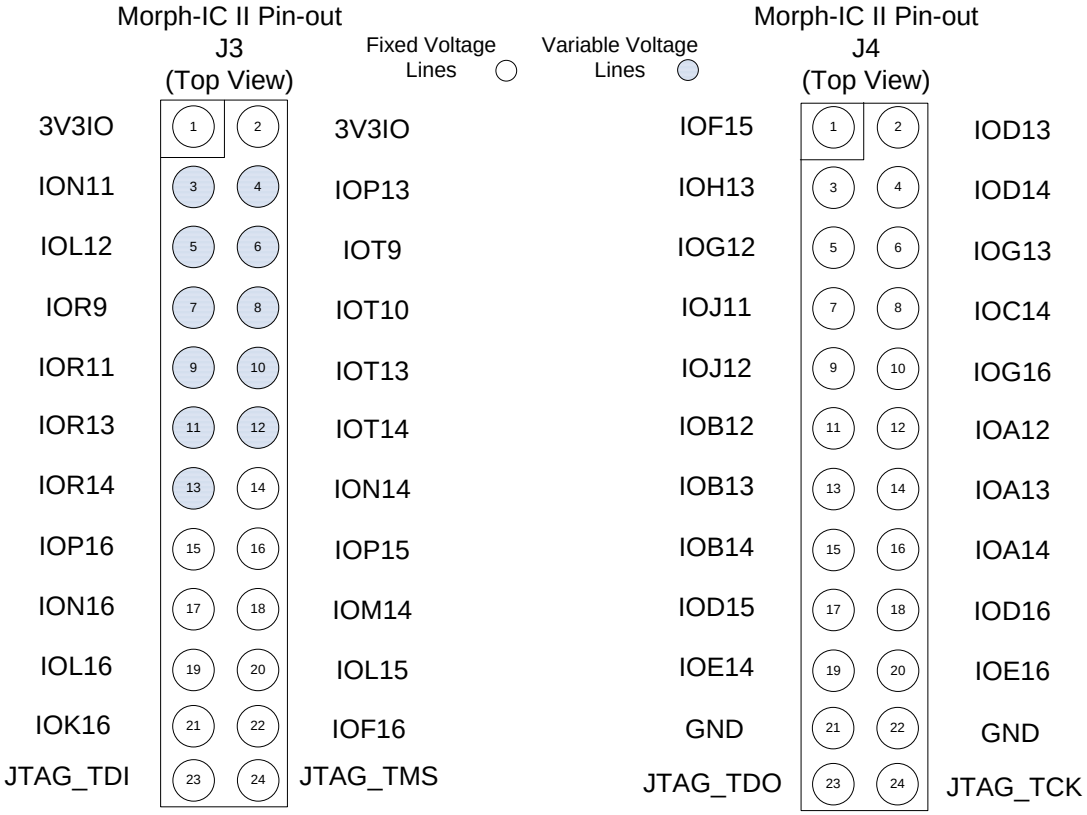

Fig. 5 – Pin outs of J3 & J4

3.5 Morph-IC-II Hardware Configuration

3.5.1 Communications and Programming Interfaces of Morph-IC-II

Morph-IC-II communicates with a PC via USB. To allow USB communications between a PC and the FPGA, Morph-IC-II uses an FT2232H USB device to create a communications bridge between the PC USB interface and the FPGA. This communications bridge splits into two channels: a programming interface channel and a parallel 245 FIFO communications interface channel. The programming interface uses channel B of the FT2232H to configure the FPGA using Altera's *Passive Serial* interface. The 245 communications interface uses channel A of the FT2232H to transfer data, either synchronously or asynchronously, over the 245 FIFO interface to and from the FPGA. The connections of the programming interface are illustrated in Fig. 6 and the connections of the 245 FIFO data interface are illustrated in Fig. 7.

For synchronous 245 FIFO mode two extra data lines are required; these are CLKOUT and OE# (Output Enable). These two additional signals provide the synchronous clock and control line for the synchronous 245 mode. This mode can transmit data at higher rates than asynchronous 245 FIFO. These signals are only available on channel A of the FT2232H chip therefore; Morph-IC-II uses channel A for the FIFO interface as opposed to MorphIC-1K which has the FIFO interface in channel B. This leaves channel B available on Morph-IC-II to be used to program the FPGA. This difference does not affect backward compatibility with MorphIC-1K hardware, but this change needs to be considered when upgrading a MorphIC-1K application to a Morph-IC-II application.

Morph-IC-II utilises the functionality of the Multi-Protocol Synchronous Serial Engine (MPSSE) architecture in channel B of the FT2232H chip to adapt to the Altera's *Passive Serial* interface. MPSSE is an FTDI function that allows different synchronous protocols to be configured on any available data channel. Once the FPGA has been configured, channel B of FT2232H can be reconfigured, using MPSSE, to operate as general purpose IO pins (see Section 3.5.2 for details on GPIO).

The FPGA can be configured and reconfigured in less than 0.1 of a second. This provides flexibility for any application to be reconfigured on-the-fly. The FPGA configuration file (*.RBF or Raw Binary File) is output by Altera Quartus II software. These configuration files can then be downloaded to the FPGA using a *.RBF loading utility called the MorphLd which is included in the Morph-IC-II package.

Alternatively, for on-the–fly programming, application software can be used to load *.RBFs using commands driven by FTDI's DLL library. An example of where a software programme executed a load *.RBF file command is the MorphIO-II utility where the utility is set to run an *.RBF containing the HDL code designed for this programme is loaded to the FPGA More information and instructions on how to use these utilities are given in application note AN_141_MorphIO-II and MorphLd Utilities for Morph-IC-II.

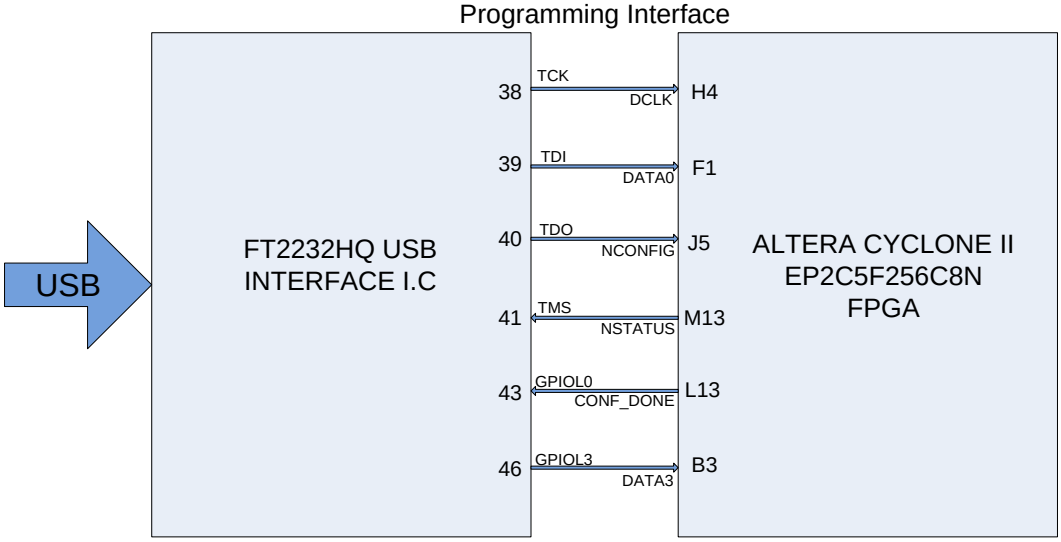

Fig. 6 – The Passive Serial Programming Interface

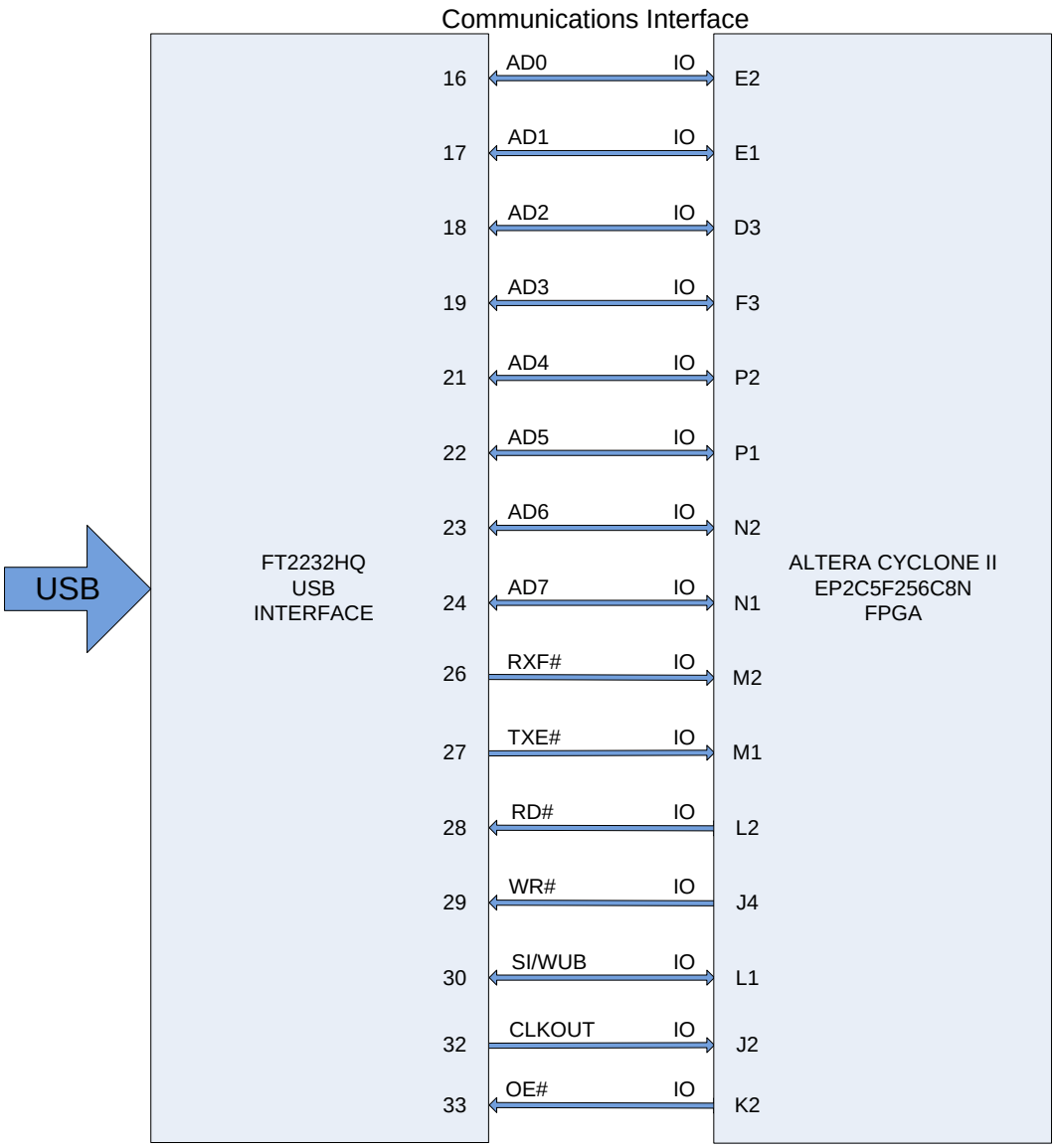

Fig. 7 – The 245 Communication Interface

3.5.2 GPIO Connections

The programming interface used by channel B of FT2232H is outlined at the beginning of section 3.5. Once the FPGA has been programmed, channel B of FT2232H can be redefined to utilise the six GPIO connections to the FPGA. These GPIO connections are illustrated in Fig. 8.

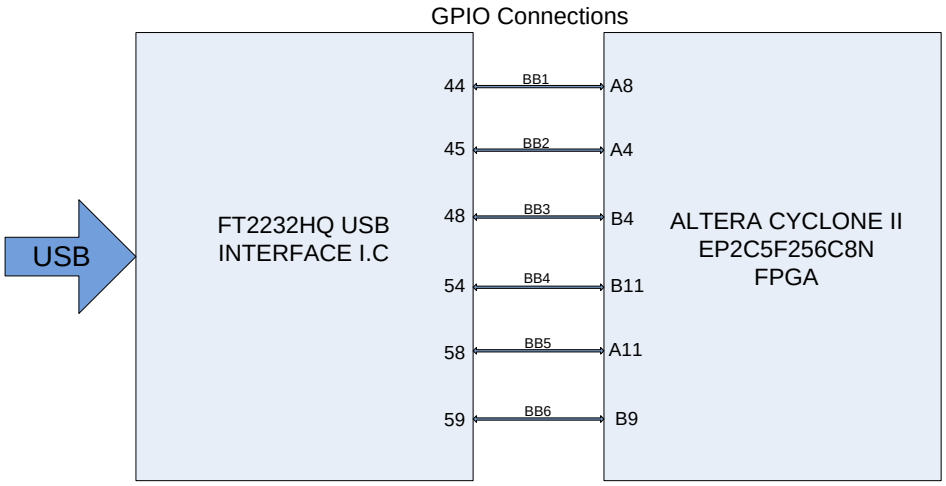

Fig. 8 – GPIO Connections

3.5.3 Morph-IC-II JTAG Connections

The interface between a JTAG programmer and Morph-IC-II's JTAG interface is illustrated in Fig. 9. The block on the left represents a programmer that will interface with the Morph-IC-II. The block on the right represents the Morph-IC-II FPGA module.

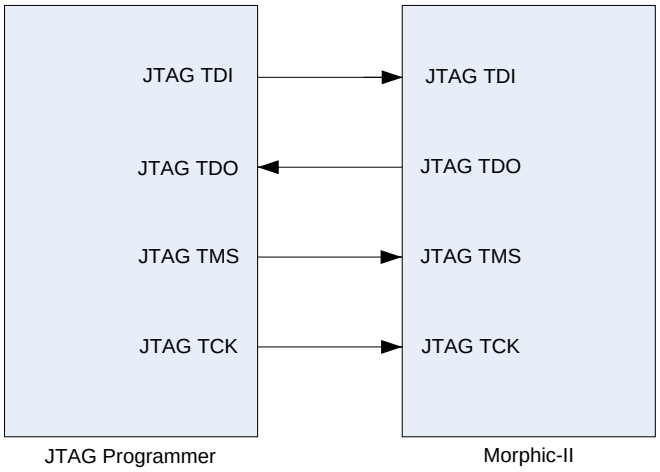

Fig. 9 – JTAG Programmer Interface

3.5.4 Pin-Map Configuration

The Cyclone-II FPGA of the Morph-IC-II can be configured from an *.RBF file. These *.RBF files can be generated using the free software package called Quartus II. An *.RBF file generated by Quartus II contains the *.RTL code which synthesises the circuit, the signals of each pin (which are defined in the top level entity of the *.RTL) and the settings of each pin (which includes current draw and logic level standards). The pin map editor included in Quartus-II is used to specify the signal assignments and the setting of each pin.

Along with making pin assignment to each port of the top-level entity, the voltage and current can be defined for each port. However there are restrictions, every signal in an I/O Bank needs to operate at the same *logic voltage level* and the I/O Bank needs to be powered with the same voltage as the *logic voltage level* of the signals. Morph-IC-II's I/O Banks 1 to 3 are connected directly to the FT2232H chip and all these signals are fixed to 3.3V-TTL/CMOS. I/O Bank 4 is the only bank that can have signals operating at voltages other than 3.3V-TTL/CMOS. Again all signals need to be at the same *logic voltage level*, to supply power with a voltage other than 3.3V, remove V_BANK4 jumper and apply DC power regulated to the same voltage level as the *logic voltage level* of I/O Bank4 to (at least one of) the header nodes labelled V_BANK4. More information and an example for pin-map editing are given in the application note: AN_141_MorphIO-II and MorphLd Utilities for Morph-IC-II

4 MorphIO-II – An Application Software

MorphIO-II is an easy to use utility used for displaying and setting the binary levels and port direction of all Morph-IC-II's 80 I/Os. A screen shot demonstrating how the IO are set is given in Fig. 10. This diagram shows MorphIO-II with some voltage levels set to different values. An illustration of J1-19 being set to low and J1-15 being set to high is also shown here. It is also illustrated that only these two pins are set as outputs the remaining pins are set as inputs. To set the level of a pin it is required to be defined as an output.

The defined settings for a pin are illustrated in MorphIO-II's GUI using a check box. These check boxes are located in one of the following columns I, O, H and L.

Check boxes in the I columns set a pin to be an input. Check boxes in the O columns set a pin to be an output. Check boxes in the H columns set output pins to be high. Check boxes in the L columns set output pins to be low.

It is also demonstrated in Fig. 11 pin J1-19 being set to a logic low thus inducing a logic low reading on this pin, all other levels read are logic highs. This is indicated by a green and red "light" around the level select check box which is used to display a logic level read of the pin, a green light indicates a low and red light indicates a high. In this demonstration J1-15 is set to output logic high, and it reads back logic high, while all other pins except pin J1-19 are reading logic high and are set to be inputs. All input pins are reading a logic high by default, this is because the I/Os of the Cyclone-II have a weak pull-up embedded in the FPGA.

A screen shot of the entire MorphIO-II is illustrated in Fig. 11, all 80 I/O controls and clock enables are controlled through this GUI. A load and save configuration control is also displayed in this diagram; these controls are for controlling the feature used to save and load the settings all the controls of the MorphIO-II.

MorphIO-II can also be used to apply a clock signal to the dedicated clock pins of the FPGA, these dedicated clock pins are displayed on MorphIO-II's GUI with a clock button next to the IO control panel. The frequency of the applied clock signal can range from 12.3KHz to 50MHz. An illustration of how to set the clock frequency is given in Fig. 12. The frequency is selected by navigating through the Setup tab, selecting the pin being toggled and selecting the required clock frequency.

In MorphIO-II's GUI, the I/O control blocks of I/O Bank 4 are colour coded dark gray to indicate that these I/Os can transfer signals with *logic voltage levels* other than 3.3V. In order to process these signals, two changes are necessary.

The first change is to set the Quartus-II files used to configure MorphIO-II's application to deal with these new I/O settings which are intended to be processed on I/O Bank4. This task is carried out by changing the I/O Standards specified in the I/O pin map for all ports in I/O Bank4 to be set to the IO Standard of the intended signal being processed via I/O Bank4. Then compile the new design and paste the newly generated *.RBF file to the directory of MorphIO-II making sure the name is "morphio50m_Mii" (MorphIO-II is hardcoded to read a *.RBF file with the name "morphio50m_Mii" from its stored directory).

The second change is to reconfigure the hardware to supply the correct voltage to I/O Bank4, this is done by opening jumper VBank4 to remove the short to 3.3V, and then applying power with the voltage set to the same voltage as logic high of the used logic standard.

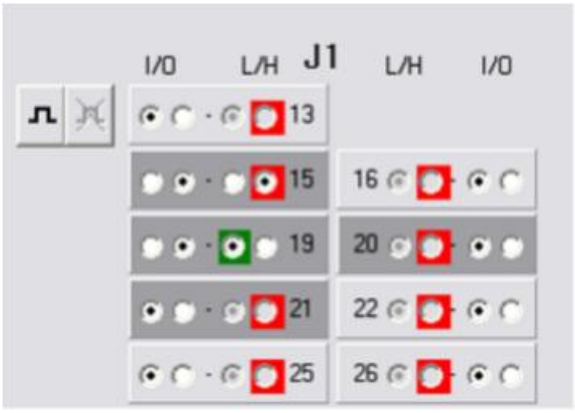

Fig. 10 – MorphIO-II Settings

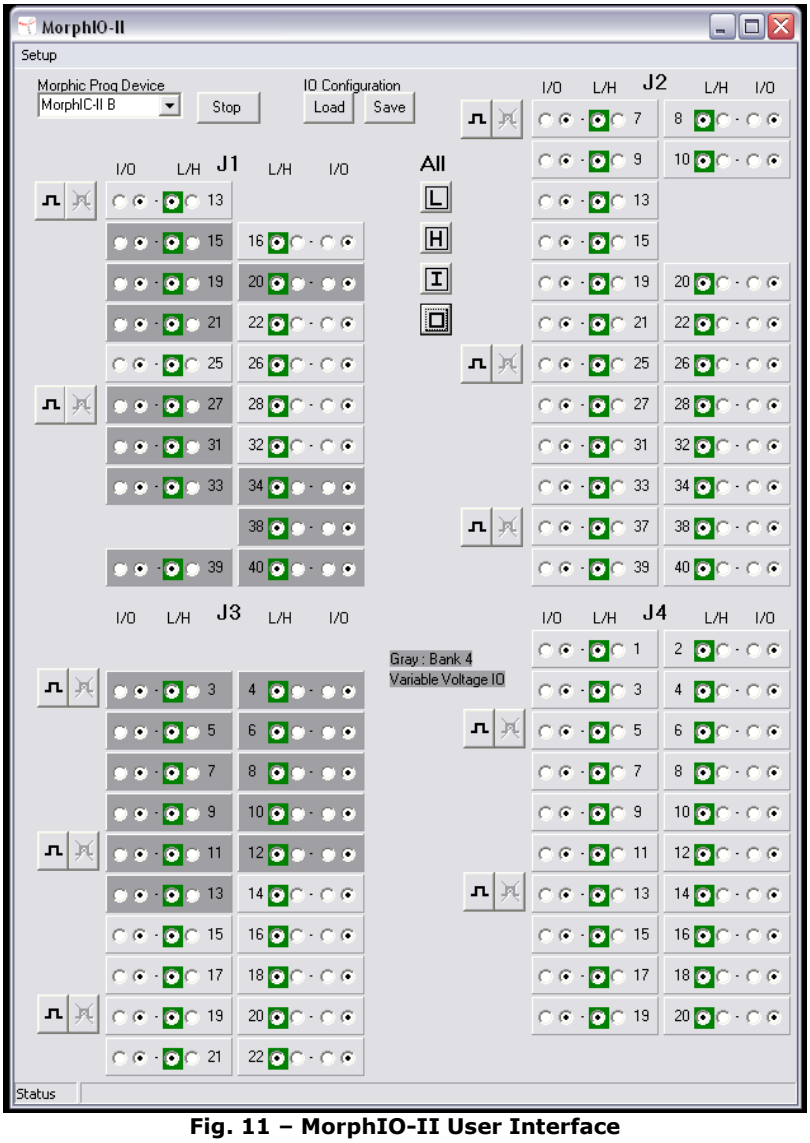

Fig. 11 – MorphIO-II User Interface

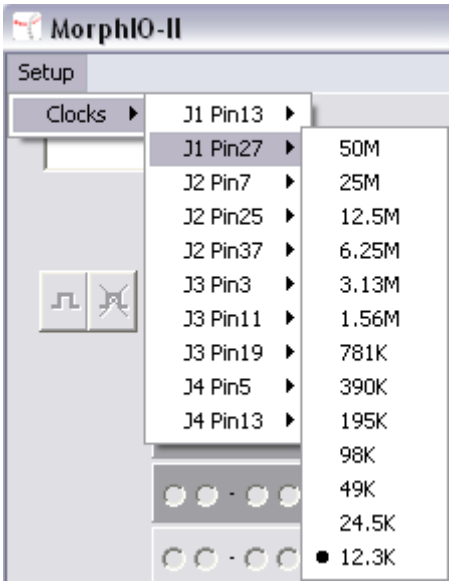

Fig. 12 – Set Clock Frequency

5 Electrical Details

5.1 Absolute Maximum Ratings

The absolute maximum ratings of Morph-IC-II are as follows. Exceeding these values may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Ambient Operating Temperature (Power Applied)	0°C to 85°C	Degrees C
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V
DC Input Voltage – All Other Inputs such as PWREN#, SUSPEND#, RESET#, EECS, EECLK, EEDATA	-0.5 to + (VCC3V3 +0.5)	V
DC Input Voltage	-0.3 to +4.6	V
DC Output Current – Outputs from the FT2232H	16	mA
DC Output Current – Outputs from the FPGA	-25 to 40	mA
VCCUSB – Self Powered Source	-0.3 to 12	V
EXT. VIO	-0.5 to 4.6	V

Table 5.1 – Absolute Maximum Ratings

5.2 Recommended Opperating Conditions

Parameter	Value	Unit
EXT. VIO - Supply voltage for output buffers, 3.3-V operation	3.135 to 3.465	V
EXT. VIO - Supply voltage for output buffers, 2.5-V operation	2.375 to 2.625	V
EXT. VIO - Supply voltage for output buffers, 1.8-V operation	1.71 to 1.89	V
EXT. VIO - Supply voltage for output buffers, 1.5-V operation	1.425 to 1.575	V

Table 5.2 – Recommended Operating Conditions

Description	V_{IL} MAX	V_{IH} MIN	V_{OL} MAX	V_{OH} MIN	Unit
3.3V LVTTL and CMOS	0.8	1.7	0.4 (LVTTL) 0.2 (LVCMOS)	2.4 (LVTTL) EXT. VIO - 0.2 (LVCMOS)	V
2.5V LVTTL and CMOS	0.7	1.7	0.4	2.0	V
1.8V LVTTL and CMOS	0.35 x EXT. VIO	0.65 x EXT. VIO	0.45	EXT. VIO - 0.45	V
1.5V LVTTL and CMOS	0.35 x EXT. VIO	0.65 x EXT. VIO	0.25 x EXT. VIO	0.75 x EXT. VIO	V

Table 5.3 – Recommended Operating Conditions

The I/O pins are +3.3v cells, which are +5V tolerant.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vil	Input low Switching Threshold		-	0.80	V	LVTTL
Vih	Input High Switching Threshold	2.00	-		V	LVTTL
Vt	Switching Threshold		1.50		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage	0.80	1.10	-	V	
Vt+	Schmitt trigger positive going threshold voltage		1.60	2.00	V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
R_{CONT}	Value of I/O pin pull-up resistor of FPGA before and during configuration	10	25	50	KΩ	V_{CCIO} = 3.3V

Table 5.4 – I/O Pin Characteristics VCCIO = +3.3V

Detailed electrical characteristics of the FT2232H can be found in its datasheet at http://www.ftdichip.com/Documents/DataSheets.htm#ICs.

Detailed electrical characteristics and ratings of the FPGA can be found in the Cyclone II handbook. This handbook can be found at http://www.altera.com/products/devices/cyclone2/cy2-index.jsp.

6 Mechanical Details

The mechanical details of Morph-IC-II are illustrated in Fig. 13.

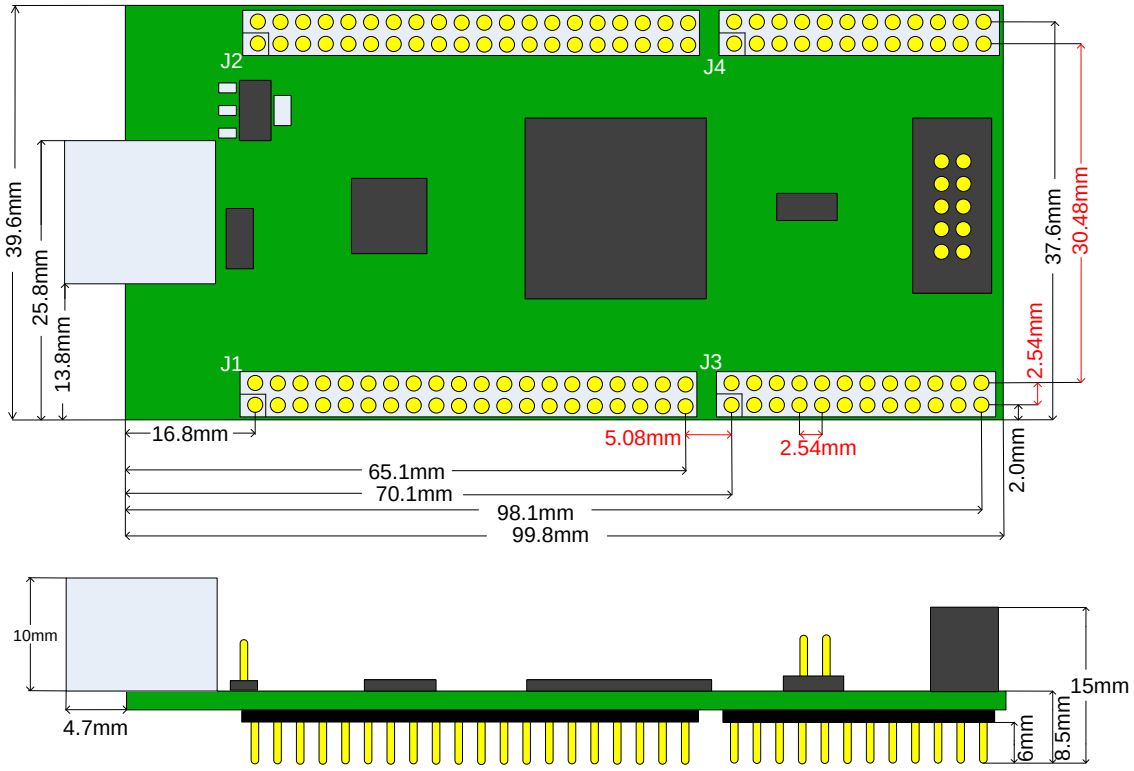

Fig. 13 – Morph-IC-II Dimensions (Top and Side View)

All dimensions shown in millimetres with a tolerance of ±0.1mm.

The headers J1, J2, J3 and J4 are mounted on the bottom of the PCB. The overall height (top of USB connector to bottom of pins) of the module is 18.5mm.

The cross section of each pin is 0.64 mm square.

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Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – FT2232H EEPROM Configuration

The Morph-IC-II utilises an EEPROM which contains the USB configuration descriptors for the FT2232H. When this module is plugged into a PC or a USB reset is performed, the PC will read these descriptors. The default values stored into the EEPROM are defined in Table 5.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6010h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the EEPROM during device final test.
Pull down I/O Pins in USB Suspend	Disabled	I/O pins on the FT2232H are pulled high during USB Suspend (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	Morph-IC-II	
Max Bus Power Current	500mA	
Power Source	Bus Powered	
USB Version	0200	Hi-Speed USB
Remote Wake Up	Disabled	Remote Wake Up is disabled
Load VCP Driver	Disabled	The Morph-IC-II will only load the D2XX device driver. The loading of VCP ports is suppressed.

Table 5 - Default Internal EEPROM Configuration

The EEPROM on the Morph-IC-II can be re-programmed over USB using the utility program MPROG or FT_PROG. Both can be downloaded from the **www.ftdichip.com**. MPROG Version 3.5 or later is required for the FT2232H chip. Users who do not have their own USB Vendor ID but would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact FTDI support for this service.

Appendix B – Revision History

Draft	First draft	28th October 2009
Rev 1.0	First release	9th August 2010
Rev 1.01	Minor text corrections	20th August 2010
Rev 1.02	Updated max speed to 40Mbytes/s due to new driver	26th August 2010
Rev 1.03	Added a note on the MORPHPROG.dll not being supported by Windows CE	31th January 2011
Rev 1.04	Added dimention to mechanical drawing and upgraded schematic drawing with higher resolution images	25th Febuary 2011

Appendix C – Schematic Drawings

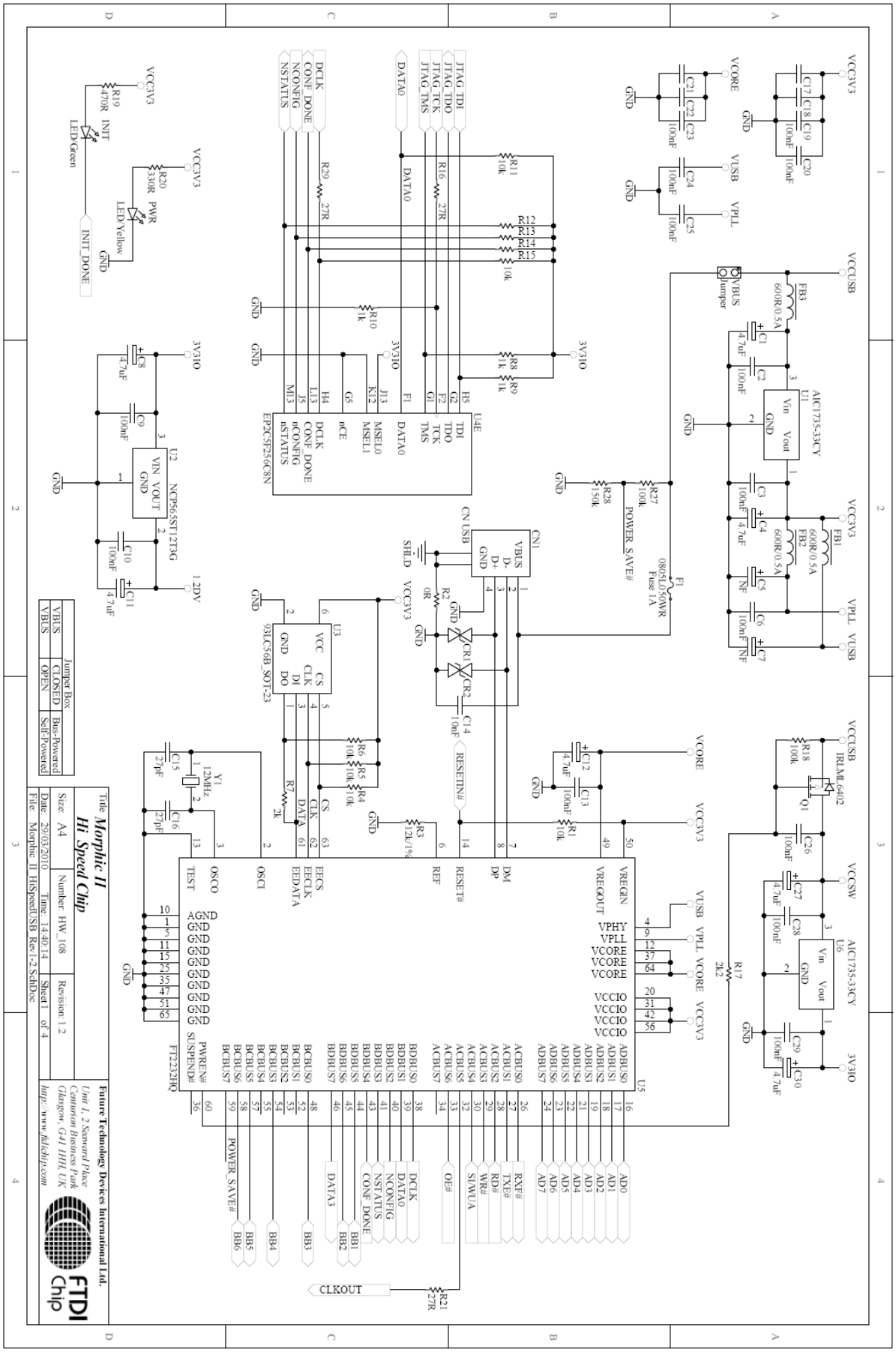

Fig. 14 – A Schematic of the USB Interface

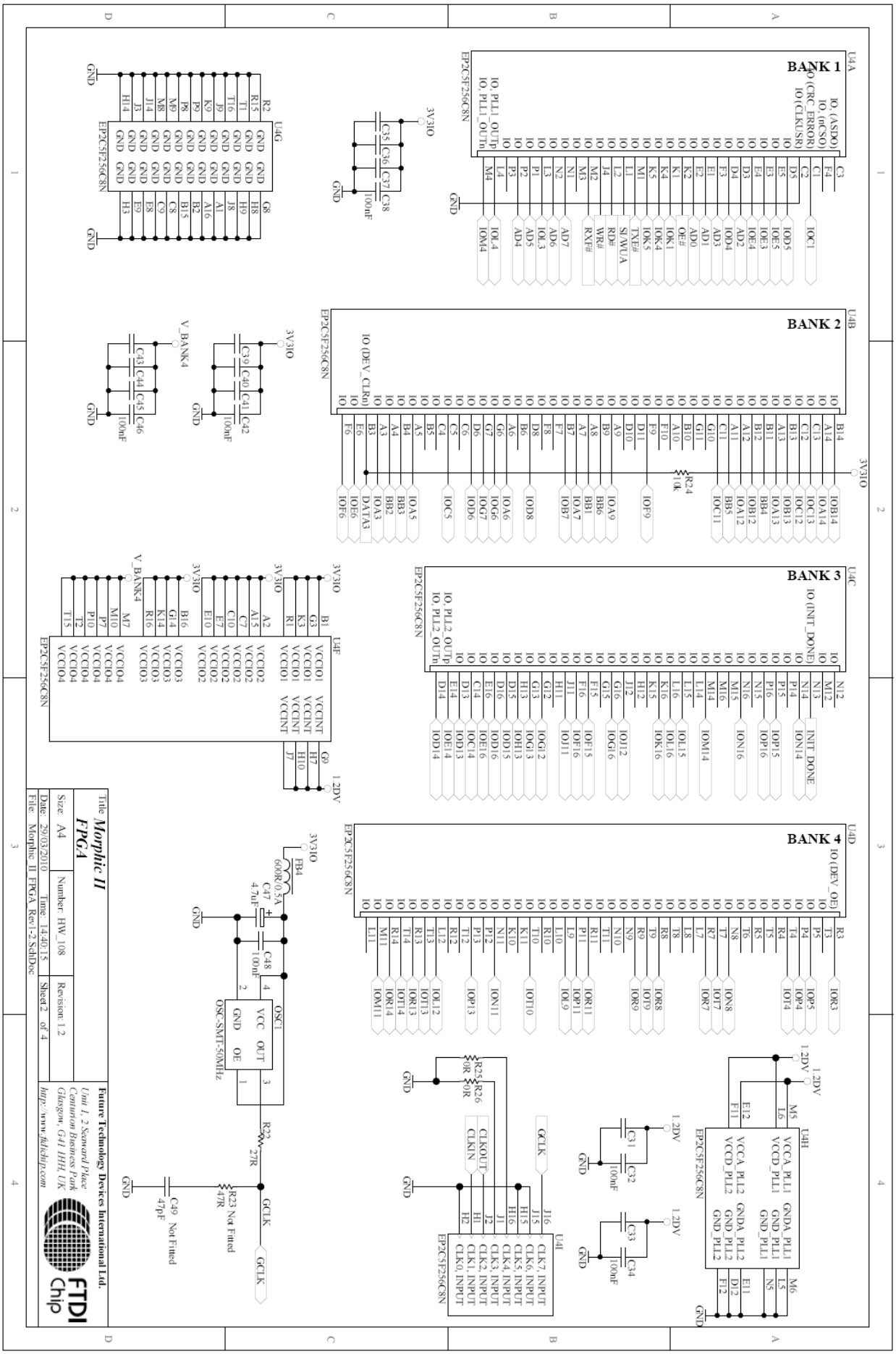

Fig. 15 – A Schematic of the FPGA

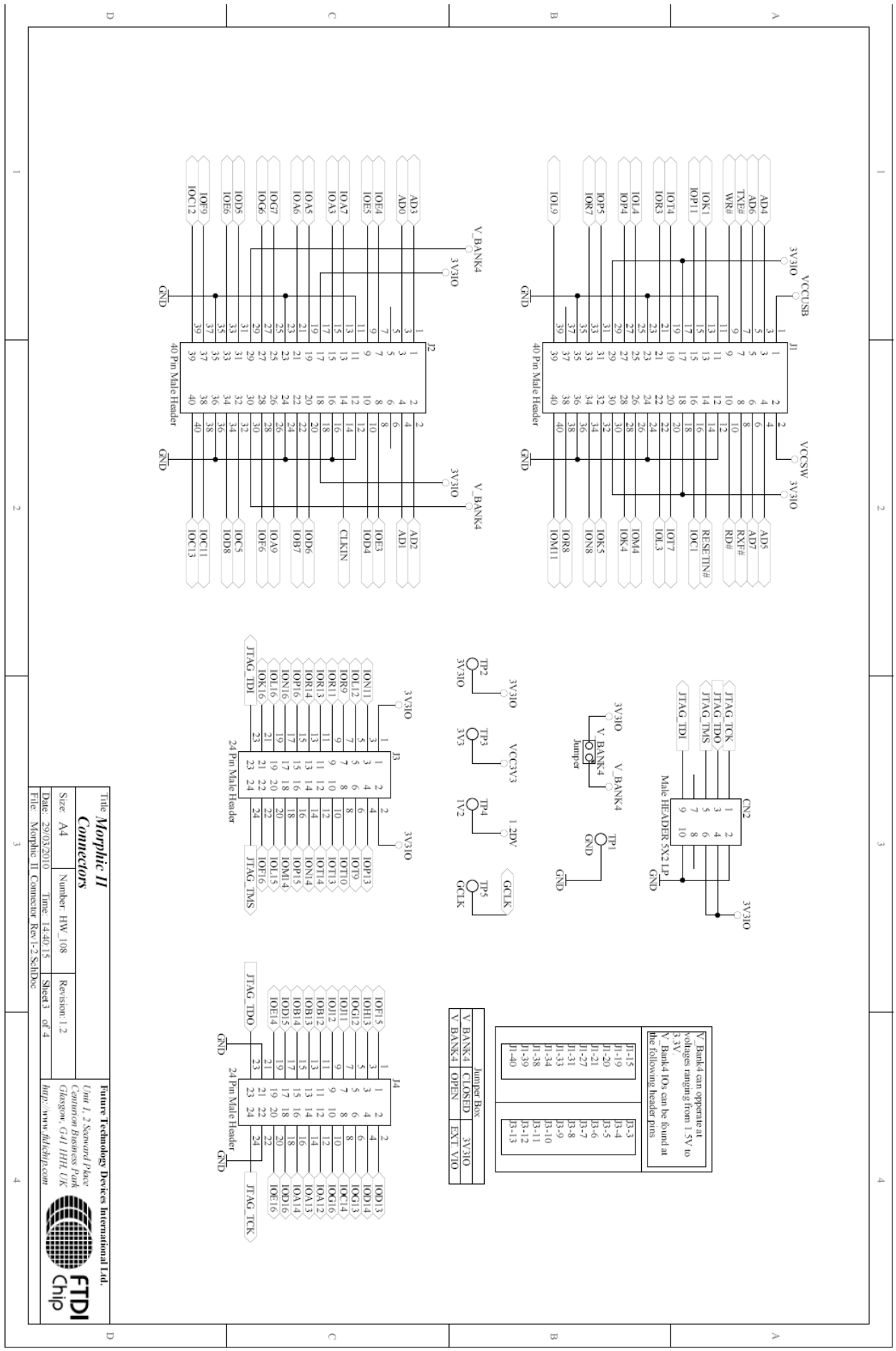

Fig. 16 – A Schematic of the I/O Pin

Appendix D - Assembly Drawings

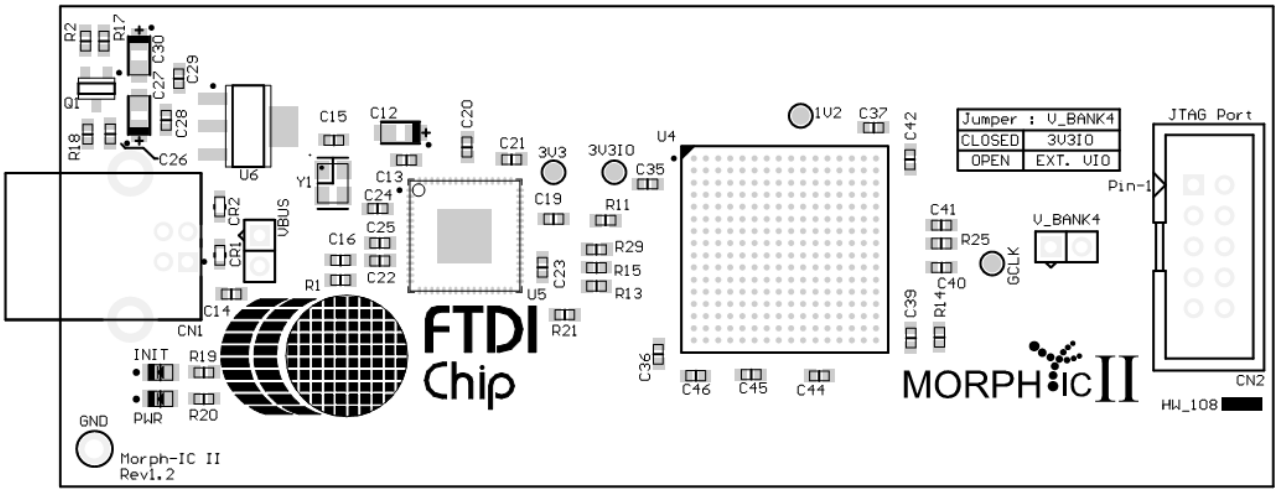

Fig. 17 – Component Layout Top View

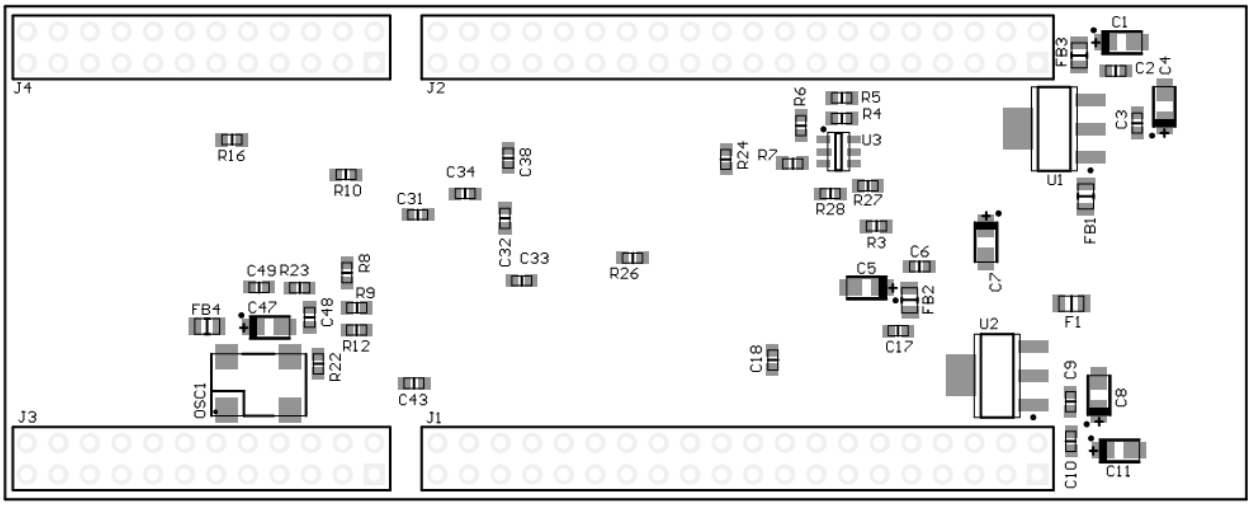

Fig. 18 – Component Layout Bottom View

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