

## Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

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Kind regards,

Team Nexperia

# PEMD48; PUMD48

NPN/PNP resistor-equipped transistors;  
R1 = 47 k $\Omega$ , R2 = 47 k $\Omega$  and R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

Rev. 6 — 24 January 2012

Product data sheet

## 1. Product profile

### 1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in small Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		Package configuration
	NXP	JEITA	
PEMD48	SOT666	-	ultra small and flat lead
PUMD48	SOT363	SC-88	very small

### 1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

### 1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

### 1.4 Quick reference data

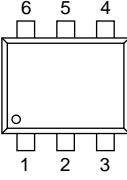
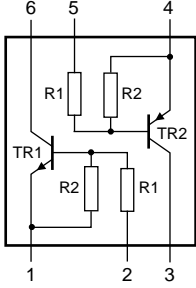
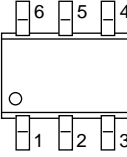
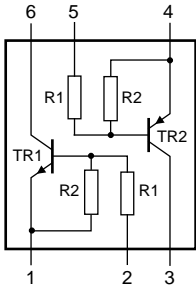
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
I <sub>O</sub>	output current		-	-	100	mA
<b>Transistor TR1 (NPN)</b>						
R1	bias resistor 1 (input)		33	47	61	k $\Omega$
R2/R1	bias resistor ratio		0.8	1.0	1.2	
<b>Transistor TR2 (PNP)</b>						
R1	bias resistor 1 (input)		1.54	2.20	2.86	k $\Omega$
R2/R1	bias resistor ratio		17	21	26	



## 2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>PEMD48 (SOT666)</b>			
1	GND (emitter) TR1		 <p style="text-align: right;">006aaa143</p>
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		
<b>PUMD48 (SOT363)</b>			
1	GND (emitter) TR1		 <p style="text-align: right;">006aaa143</p>
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

## 3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PEMD48	-	plastic surface-mounted package; 6 leads	SOT666
PUMD48	SC-88	plastic surface-mounted package; 6 leads	SOT363

## 4. Marking

Table 5. Marking codes

Type number	Marking code <sup>[1]</sup>
PEMD48	48
PUMD48	4*8

[1] \* = placeholder for manufacturing site code.

**5. Limiting values**

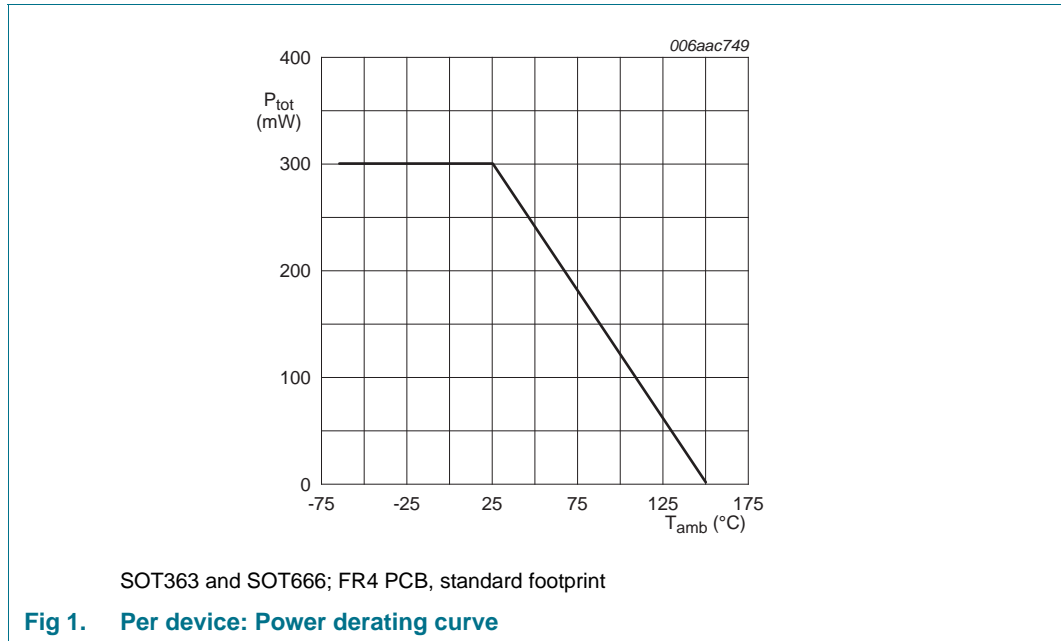
**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

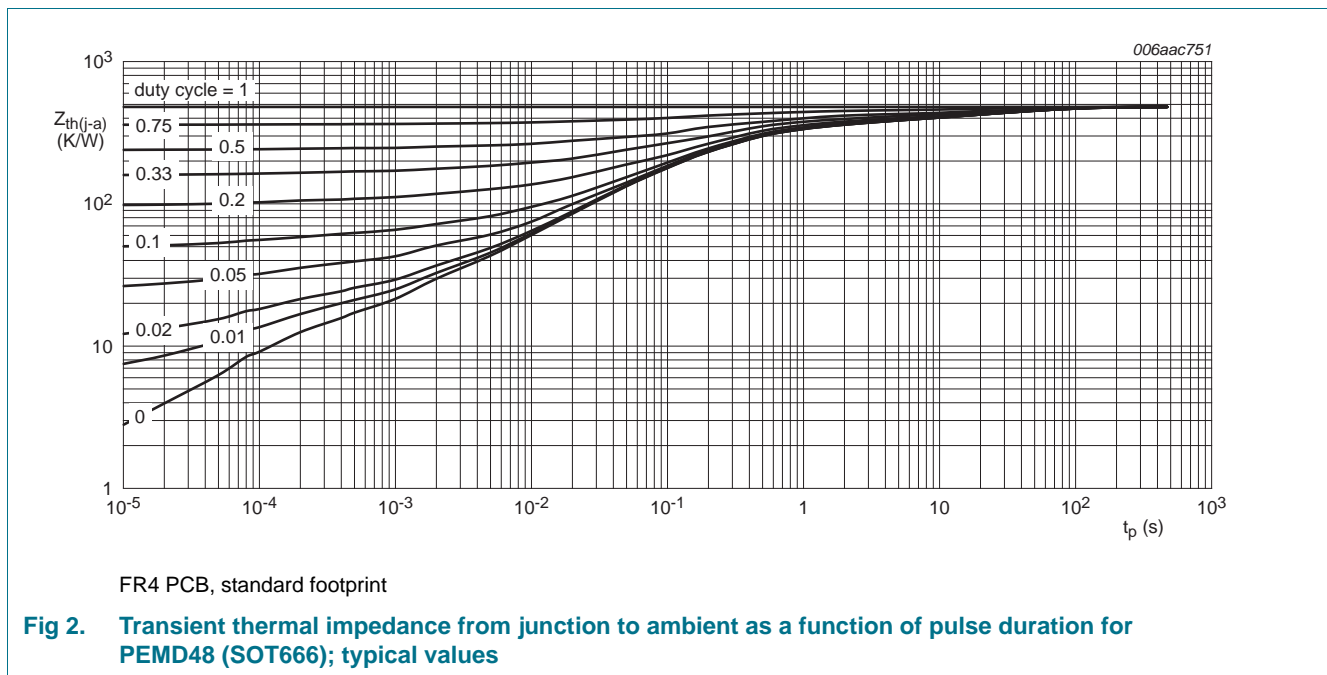
Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$V_{CBO}$	collector-base voltage	open emitter	-	50	V	
$V_{CEO}$	collector-emitter voltage	open base	-	50	V	
$V_{EBO}$	emitter-base voltage	open collector				
	TR1 (NPN)		-	10	V	
	TR2 (PNP)		-	-5	V	
$V_I$	input voltage TR1					
	positive		-	+40	V	
	negative		-	-10	V	
	input voltage TR2					
	positive		-	+5	V	
	negative		-	-12	V	
$I_O$	output current		-	100	mA	
$I_{CM}$	peak collector current		-	100	mA	
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$				
	PEMD48 (SOT666)		[1][2]	-	200	mW
	PUMD48 (SOT363)		[1]	-	200	mW
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$				
	PEMD48 (SOT666)		[1][2]	-	300	mW
	PUMD48 (SOT363)		[1]	-	300	mW
$T_j$	junction temperature		-	150	°C	
$T_{amb}$	ambient temperature		-65	+150	°C	
$T_{stg}$	storage temperature		-65	+150	°C	

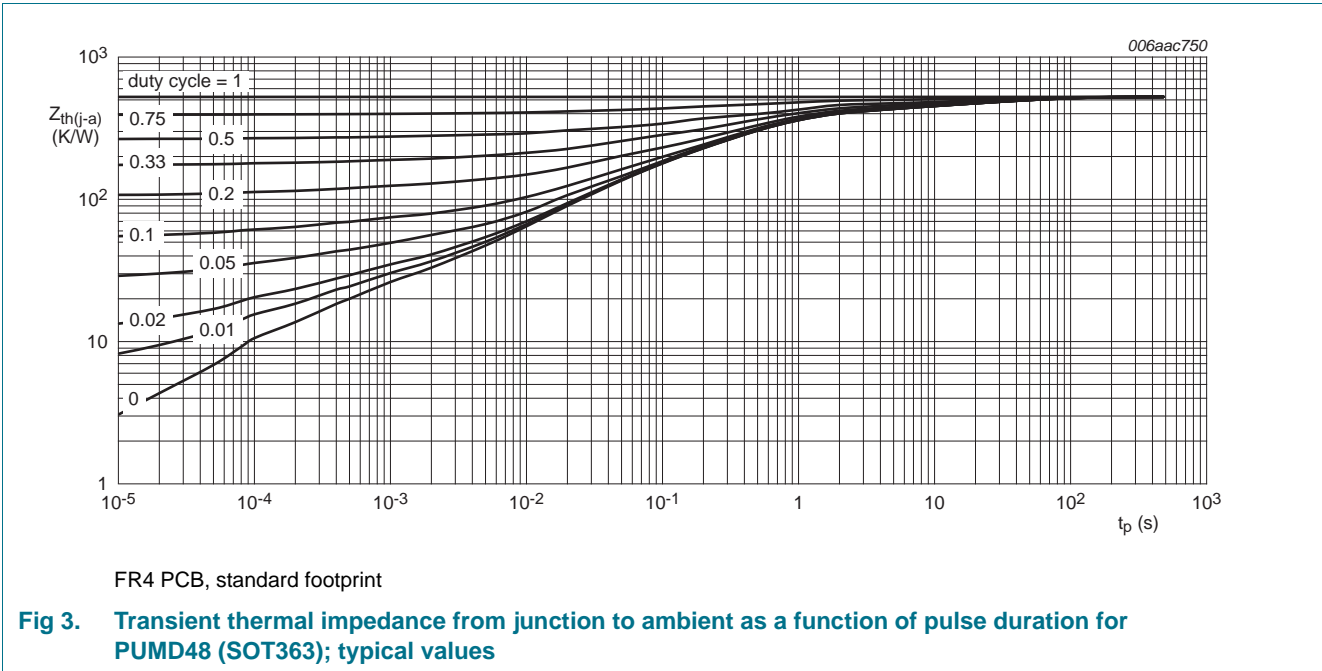
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



## 6. Thermal characteristics





**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\text{ °C}$				
	PEMD48 (SOT666)		[1][2]	-	625	K/W
	PUMD48 (SOT363)		[1]	-	625	K/W
<b>Per device</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\text{ °C}$				
	PEMD48 (SOT666)		[1][2]	-	417	K/W
	PUMD48 (SOT363)		[1]	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

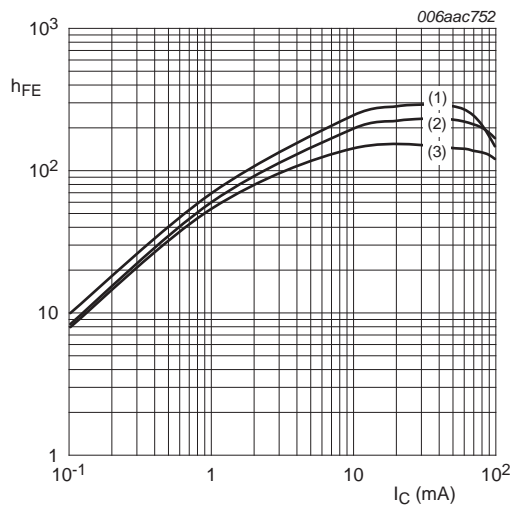
## 7. Characteristics

**Table 8. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

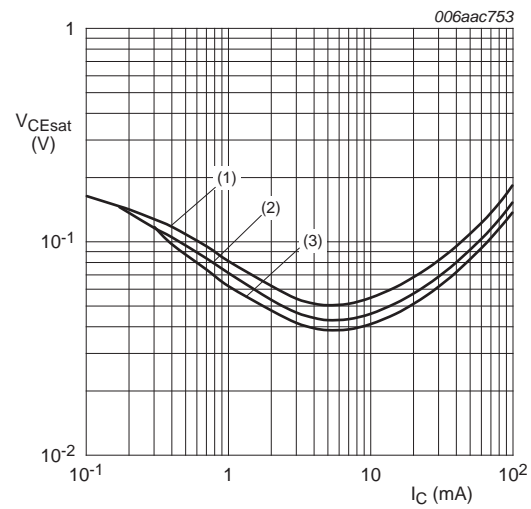
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor; for the PNP transistor with negative polarity</b>							
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA	
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	$\mu\text{A}$	
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	5	$\mu\text{A}$	
<b>Transistor TR1 (NPN)</b>							
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	90	$\mu\text{A}$	
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$	80	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}$	-	1.2	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 2\text{ mA}$	3	1.6	-	V	
R1	bias resistor 1 (input)		33	47	61	k $\Omega$	
R2/R1	bias resistor ratio		0.8	1.0	1.2		
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	2.5	pF	
$f_T$	transition frequency	$V_{CB} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}$	[1]	-	230	-	MHz
<b>Transistor TR2 (PNP)</b>							
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-180	$\mu\text{A}$	
$h_{FE}$	DC current gain	$V_{CE} = -5\text{ V}; I_C = -10\text{ mA}$	100	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -5\text{ mA}; I_B = -0.25\text{ mA}$	-	-	-100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\text{ V}; I_C = -100\text{ }\mu\text{A}$	-	-0.6	-0.5	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\text{ V}; I_C = -5\text{ mA}$	-1.1	-0.75	-	V	
R1	bias resistor 1 (input)		1.54	2.20	2.86	k $\Omega$	
R2/R1	bias resistor ratio		17	21	26		
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	3	pF	
$f_T$	transition frequency	$V_{CB} = -5\text{ V}; I_C = -10\text{ mA}; f = 100\text{ MHz}$	[1]	-	180	-	MHz

[1] Characteristics of built-in transistor.



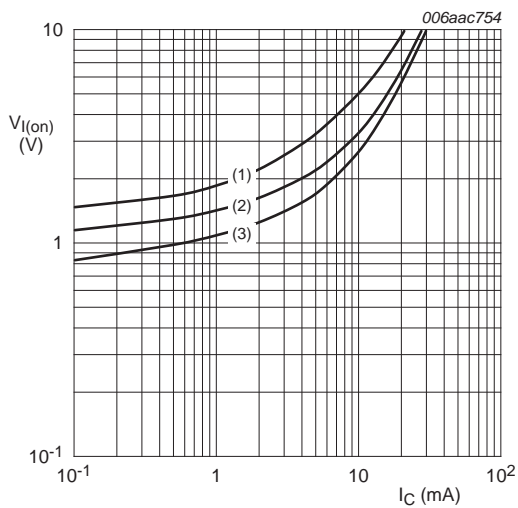
- $V_{CE} = 5\text{ V}$
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig 4. TR1 (NPN): DC current gain as a function of collector current; typical values**



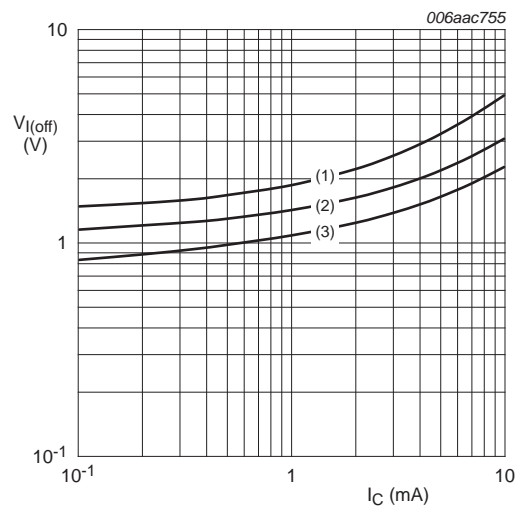
- $I_C/I_B = 20$
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



- $V_{CE} = 0.3\text{ V}$
- (1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

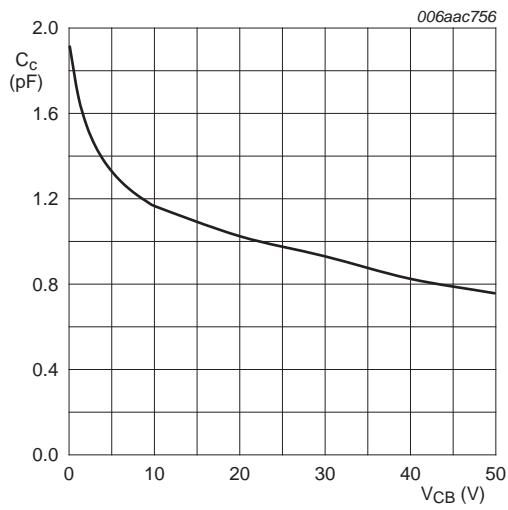
**Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values**



- $V_{CE} = 5\text{ V}$
- (1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

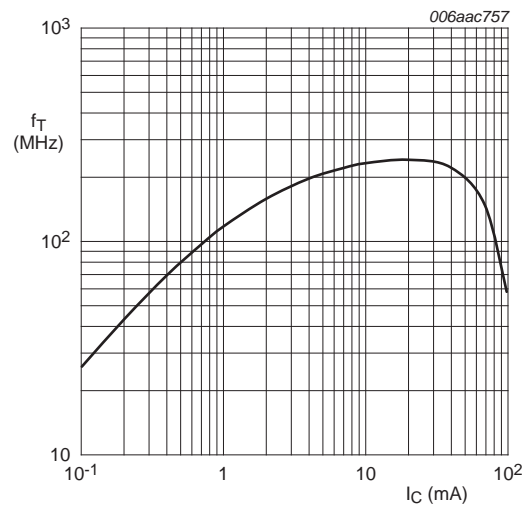
**Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values**





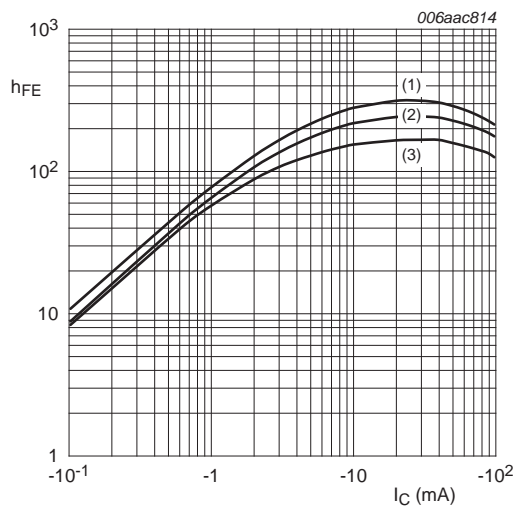
$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values**



$V_{CE} = 5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

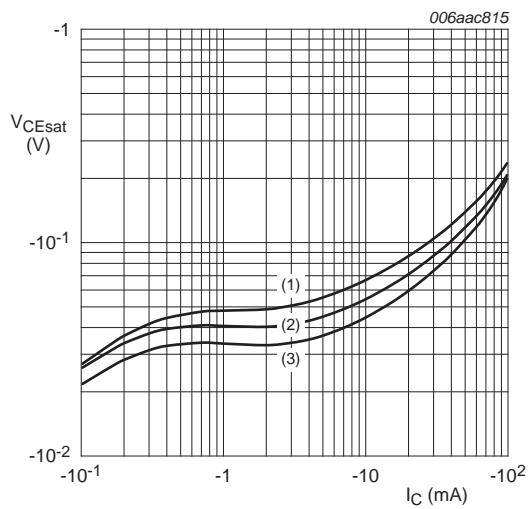
**Fig 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor**



$V_{CE} = -5 \text{ V}$

- (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$
- (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$
- (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

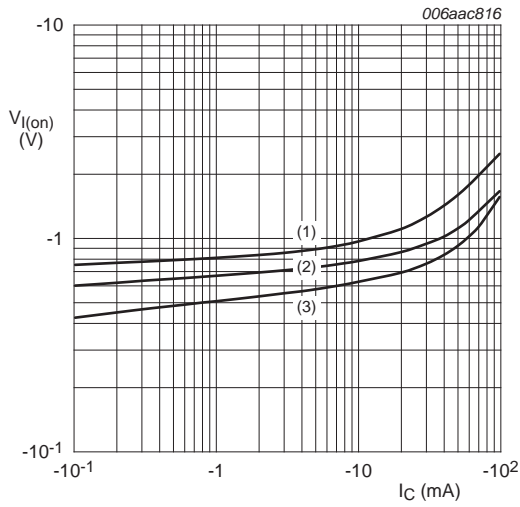
**Fig 10. TR2 (PNP): DC current gain as a function of collector current; typical values**



$I_C/I_B = 20$

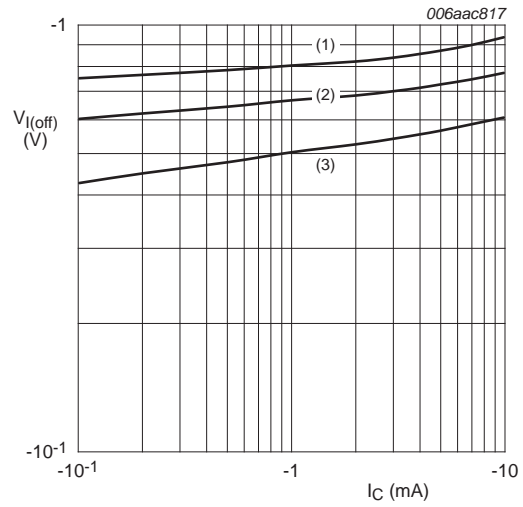
- (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$
- (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$
- (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

**Fig 11. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



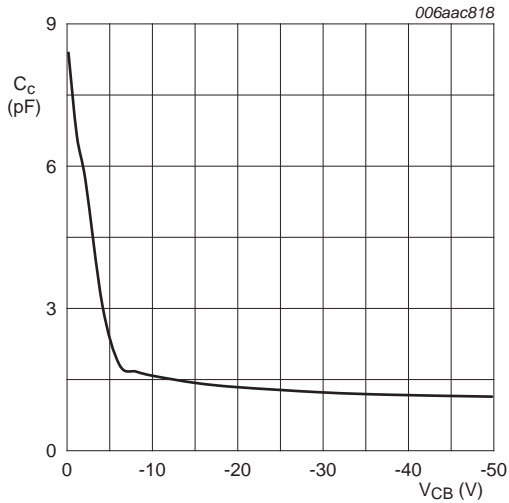
$V_{CE} = -0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 12. TR2 (PNP): On-state input voltage as a function of collector current; typical values**



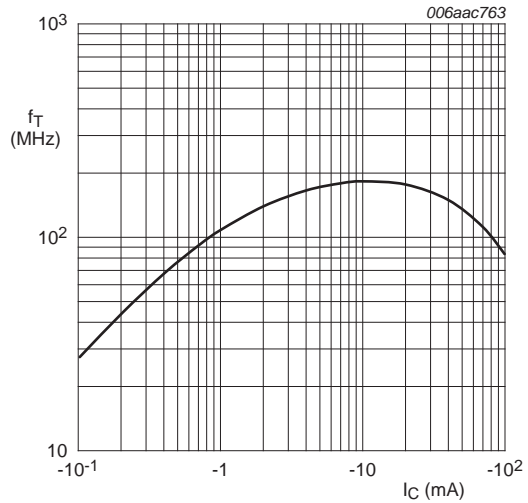
$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 13. TR2 (PNP): Off-state input voltage as a function of collector current; typical values**



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 14. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values**



$V_{CE} = -5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

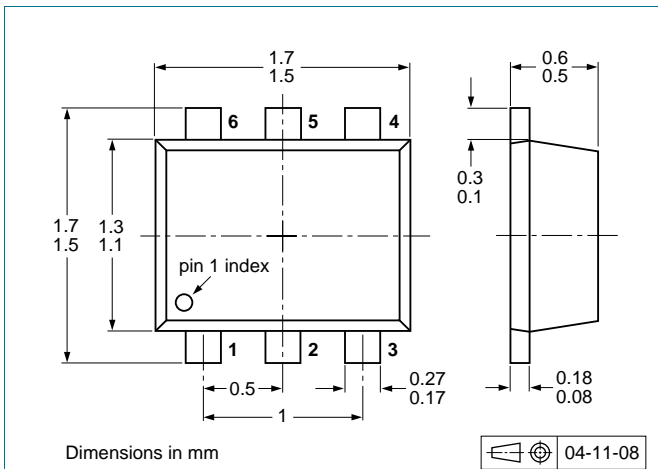
**Fig 15. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor**

**8. Test information**

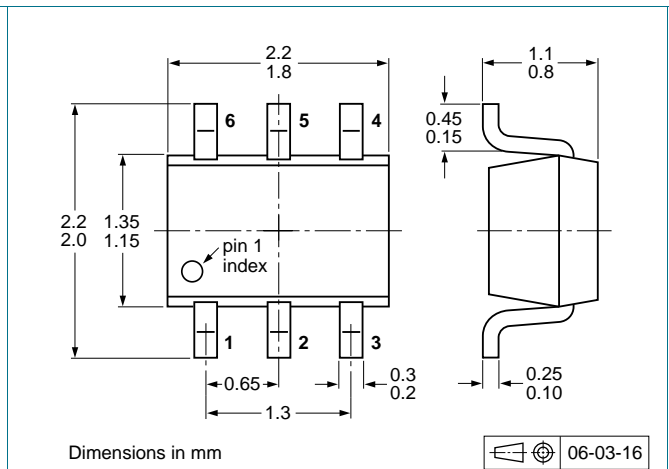
**8.1 Quality information**

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

**9. Package outline**



**Fig 16. Package outline PEMD48 (SOT666)**



**Fig 17. Package outline PUMD48 (SOT363/SC-88)**

## 10. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

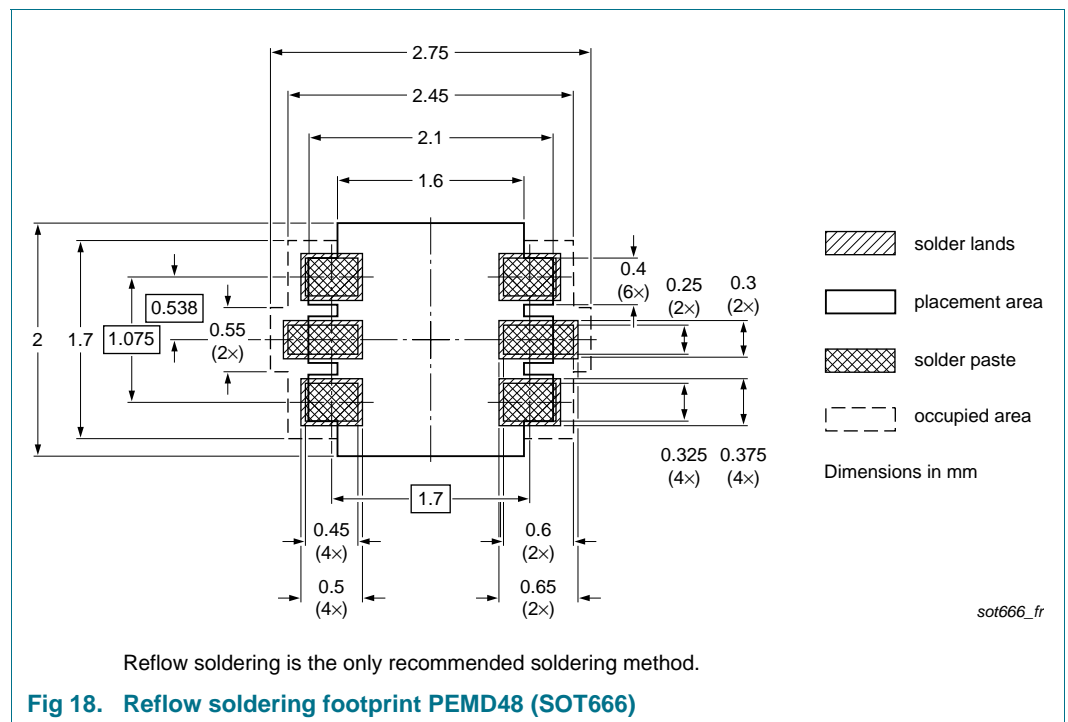
Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMD48	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMD48	SOT363	4 mm pitch, 8 mm tape and reel; T1 <sup>[2]</sup>	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 <sup>[3]</sup>	-125	-	-	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

## 11. Soldering



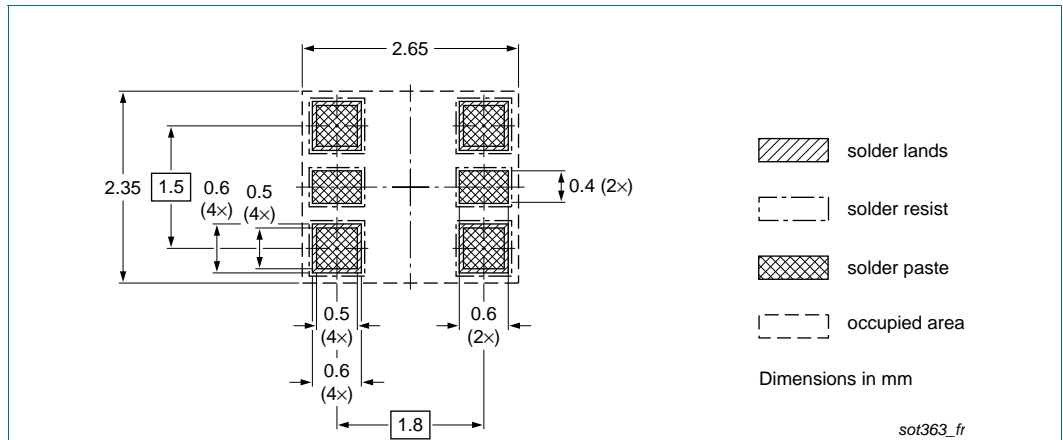


Fig 19. Reflow soldering footprint PUMD48 (SOT363/SC-88)

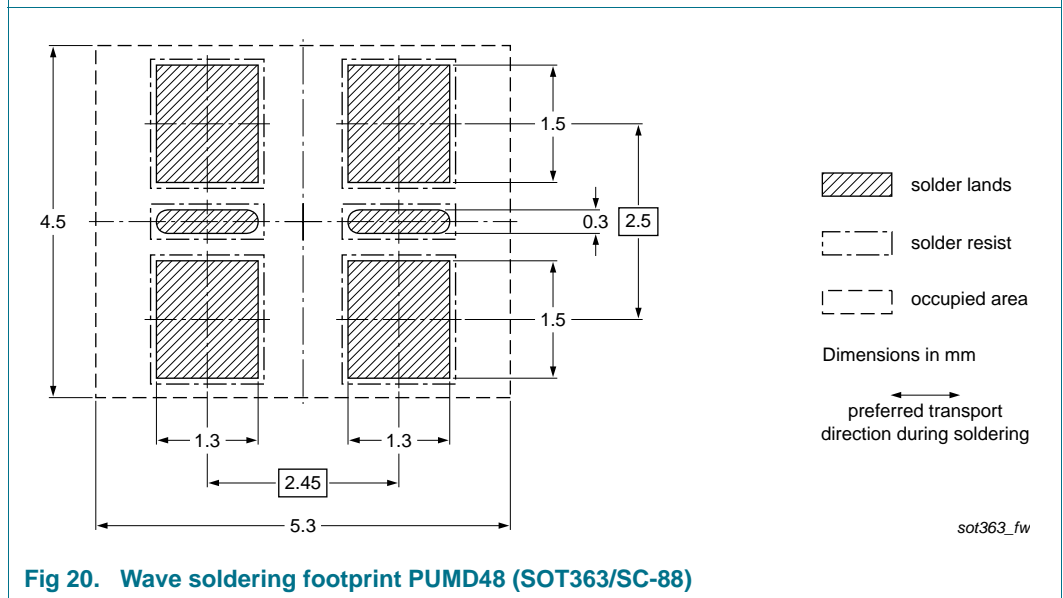


Fig 20. Wave soldering footprint PUMD48 (SOT363/SC-88)

## 12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD48_PUMD48 v.6	20120124	Product data sheet	-	PEMD48_PUMD48 v.5
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1 “Product profile”</a>: updated</li> <li>• <a href="#">Section 4 “Marking”</a>: updated</li> <li>• <a href="#">Table 7 “Thermal characteristics”</a>: updated according to the latest measurements</li> <li>• <a href="#">Table 6 “Limiting values”</a>: updated according to the latest measurements</li> <li>• <a href="#">Table 8 “Characteristics”</a>: I<sub>CEO</sub> updated according to the latest measurements, f<sub>T</sub> added</li> <li>• <a href="#">Figure 1</a> to <a href="#">3</a>, <a href="#">8</a>, <a href="#">9</a>, <a href="#">14</a> and <a href="#">15</a>: added</li> <li>• <a href="#">Figure 4</a> to <a href="#">7</a> and <a href="#">Figure 10</a> to <a href="#">13</a>: updated</li> <li>• <a href="#">Section 8 “Test information”</a>: added</li> <li>• <a href="#">Section 11 “Soldering”</a>: added</li> <li>• <a href="#">Section 13 “Legal information”</a>: updated</li> </ul>			
PEMD48_PUMD48 v.5	20100413	Product data sheet	-	PEMD48_PUMD48 v.4
PEMD48_PUMD48 v.4	20040624	Product specification	-	PEMD48_PUMD48 v.3
PEMD48_PUMD48 v.3	20040602	Product specification	-	PEMD48 v.2 PUMD48 v.2
PUMD48 v.2	20010201	Product specification	-	PUMD48 v.1
PUMD48 v.1	19990422	Product specification	-	-
PEMD48 v.2	20011107	Product specification	-	PEMD48 v.1
PEMD48 v.1	20010924	Preliminary specification	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 13.2 Definitions

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**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

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## 14. Contact information

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