



General Description

The MAX8632 integrates a synchronous-buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT, and a 10mA reference output buffer to generate VTTR. The buck controller drives two external n-channel MOSFETs to generate output voltages down to 0.7V from a 2V to 28V input with output currents up to 15A. The LDO can sink or source up to 1.5A continuous and 3A peak current. Both the LDO output and the 10mA reference buffer output can be made to track the REFIN voltage. These features make the MAX8632 ideally suited for DDR memory applications in desktops, notebooks, and graphic cards.

The PWM controller in the MAX8632 utilizes Maxim's proprietary Quick-PWM™ architecture with programmable switching frequencies of up to 600kHz. This control scheme handles wide input/output voltage ratios with ease and provides 100ns response to load transients while maintaining high efficiency and a relatively constant switching frequency. The MAX8632 offers fully programmable UVP/OVP and skip-mode options ideal in portable applications. Skip mode allows for improved efficiency at lighter loads.

The VTT and VTTR outputs track to within 1% of VREFIN / 2. The high bandwidth of this LDO regulator allows excellent transient response without the need for bulk capacitors, thus reducing cost and size.

The buck controller and LDO regulators are provided with independent current limits. Adjustable lossless foldback current limit for the buck regulator is achieved by monitoring the drain-to-source voltage drop of the low-side MOSFET. Additionally, overvoltage and undervoltage protection mechanisms are built in. Once the overcurrent condition is removed, the regulator is allowed to enter soft-start again. This helps minimize power dissipation during a short-circuit condition. The MAX8632 allows flexible sequencing and standby power management using the SHDN and STBY inputs, which support all DDR operating states.

The MAX8632 is available in a small 5mm × 5mm, 28pin thin QFN package.

Applications

DDR I and DDR II Memory Power Supplies **Desktop Computers** Notebooks and Desknotes **Graphic Cards** Game Consoles **RAID** Networking

Features

Buck Controller

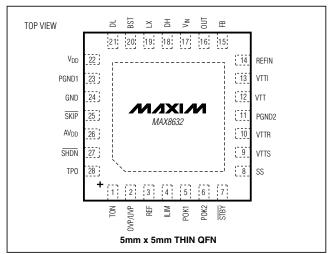
- ♦ Quick-PWM with 100ns Load-Step Response
- ♦ Up to 95% Efficiency
- ♦ 2V to 28V Input Voltage Range
- ♦ 1.8V/2.5V Fixed or 0.7V to 5.5V Adjustable Output
- ♦ Up to 600kHz Selectable Switching Frequency
- ♦ Programmable Current Limit with Foldback Capability
- ♦ 1.7ms Digital Soft-Start
- ♦ Independent Shutdown and Standby Controls
- ♦ Overvoltage-/Undervoltage-Protection Option
- **Power-Good Window Comparator LDO Section**
- **♦** Fully Integrated VTT and VTTR Capability
- ♦ VTT Has ±3A Sourcing/Sinking Capability
- ♦ Only 20µF Ceramic Capacitance Required for VTT
- ♦ VTT and VTTR Outputs Track V_{REFIN} / 2
- **♦** All-Ceramic Output-Capacitor Designs
- ♦ 1.0V to 2.8V Input Voltage Range
- **♦ Power-Good Window Comparator**

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|----------------|---------------------------|
| MAX8632ETI+ | -40°C to +85°C | 28 Thin QFN-EP* 5mm × 5mm |

- + Denotes lead-free packaging.
- * EP = Exposed pad.

Pin Configuration



Typical Operating Circuit appears at end of data sheet. Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

| V _{IN} to GND | | VTTS to GND | () |
|--|------------------------------------|--|----------------|
| V _{DD} , AV _{DD} , VTTI to GND | | PGND1, PGND2, TP0 to GND | |
| SHDN, REFIN to GND | 0.3V to +6V | REF Short Circuit to GND | Continuous |
| SS, POK1, POK2, SKIP, ILIM, FB | | Continuous Power Dissipation (T _A = +70 |)°C) |
| STBY, TON, REF, UVP/OVP to GN | D0.3V to (AV _{DD} + 0.3V) | 28-Pin 5mm x 5mm Thin QFN (derate | 35.7mW/°C |
| OUT, VTTR to GND | 0.3V to (AV _{DD} + 0.3V) | above +70°C) | 2.86W |
| DL to PGND1 | 0.3V to (V _{DD} + 0.3V) | Operating Temperature Range | 40°C to +85°C |
| DH to LX | 0.3V to (V _{BST} + 0.3V) | Junction Temperature | +150°C |
| LX to BST | 6V to +0.3V | Storage Temperature Range | 65°C to +150°C |
| LX to GND | 2V to +30V | Lead Temperature (soldering, 10s) | +300°C |
| VTT to GND | 0.3V to (V _{VTTI} + 0.3V) | | |
| | | | |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{IN} = +15V, V_{DD} = AV_{DD} = V_{\overline{SHDN}} = \overline{STBY} = V_{BST} = V_{ILIM} = 5V, V_{OUT} = V_{REFIN} = V_{VTTI} = 2.5V, UVP/OVP = TP0 = FB = \overline{SKIP} = GND, PGND1 = PGND2 = LX = GND, TON = OPEN, V_{VTTS} = V_{VTT}, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

| PARAMETER | SYMBOL | cc | ONDITIONS | MIN | TYP | MAX | UNITS | |
|---|------------------------------------|---|---------------------------|-------|------|-------|-------|--|
| MAIN PWM CONTROLLER | | | | | | | | |
| Innut Veltage Denge | VIN | | | 2 | | 28 | V | |
| Input Voltage Range | V _{DD} , AV _{DD} | | | 4.5 | | 5.5 | V | |
| Output Adjust Range | Vout | | | 0.7 | | 5.5 | V | |
| | | FB = OUT | | 0.693 | 0.7 | 0.707 | | |
| Output Voltage Accuracy (Note 2) | | FB = GND | | 2.47 | 2.5 | 2.53 | V | |
| (Note 2) | | FB = V _{DD} | | 1.78 | 1.8 | 1.82 | | |
| Soft-Start Ramp Time | tss | Rising edge of SF | IDN to full current limit | | 1.7 | | ms | |
| | | V _{IN} = 15V, V _{OUT} = 1.5V (Note 3) | TON = GND (600kHz) | 170 | 194 | 219 | | |
| On-Time | | | TON = REF (450kHz) | 213 | 243 | 273 | ns | |
| On-Time | ton | | TON = open (300kHz) | 316 | 352 | 389 | | |
| | | | $TON = AV_{DD} (200kHz)$ | 461 | 516 | 571 | | |
| Minimum Off-Time | toff_min | (Note 3) | | 200 | 300 | 450 | ns | |
| V _{IN} Quiescent Supply Current | I _{IN} | | | | 25 | 40 | μΑ | |
| V _{IN} Shutdown Supply Current | | SHDN = GND | | | 1 | 5 | μΑ | |
| AV Outles sent Comple Comment | | All on (PWM, VTT, and VTTR on) | | | 2.5 | 5 | | |
| AV _{DD} Quiescent Supply Current | IAVDD | STBY = GND (only VTTR and PWM on) | | | 1 | 2 | mA | |
| AV _{DD} + V _{DD} Shutdown Supply Current | | SHDN = GND | | | | 20 | μA | |
| AV _{DD} Undervoltage-Lockout | | Rising edge of VIN | V | 4.05 | 4.25 | 4.40 | V | |
| Threshold | | Hysteresis | | | 50 | | mV | |
| V _{DD} Quiescent Supply Current | I _{VDD} | Set V _{FB} = 0.8V | | | 1 | 5 | μΑ | |

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN} = +15V, V_{DD} = AV_{DD} = V_{\overline{SHDN}} = \overline{STBY} = V_{BST} = V_{ILIM} = 5V, V_{OUT} = V_{REFIN} = V_{VTTI} = 2.5V, UVP/OVP = TP0 = FB = \overline{SKIP} = GND, PGND1 = PGND2 = LX = GND, TON = OPEN, V_{VTTS} = V_{VTT}, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|--|-------|------|-------|-------|
| REFERENCE | 1. | | | | | I. |
| Reference Voltage | V _{REF} | AV _{DD} = 4.5V to 5.5V; I _{REF} = 0 | 1.98 | 2 | 2.02 | V |
| Reference Load Regulation | | I _{REF} = 0 to 50μA | | | 0.01 | V |
| DEE Undervoltege Leekeuit | | V _{REF} rising | | 1.93 | | V |
| REF Undervoltage Lockout | | Hysteresis | | 300 | | mV |
| FAULT DETECTION | | | | | | |
| OVP Trip Threshold (Referred to Nominal V _{OUT}) | | UVP/OVP = AV _{DD} | 112 | 116 | 120 | % |
| UVP Trip Threshold (Referred to Nominal V _{OUT}) | | | 65 | 70 | 75 | % |
| POK1 Trip Threshold | | Lower level, falling edge, 1% hysteresis | 87 | 90 | 93 | 0/ |
| (Referred to Nominal V _{OUT}) | | Upper level, rising edge, 1% hysteresis | 107 | 110 | 113 | % |
| POK2 Trip Threshold (Referred to Nominal V _{VTTS} | | Lower level, falling edge, 1% hysteresis | 87.5 | 90 | 92.5 | % |
| and V _{VTTR}) | | Upper level, rising edge, 1% hysteresis | 107.5 | 110 | 112.5 | 70 |
| POK2 Disable Threshold (Measured at REFIN) | | V _{REFIN} rising (hysteresis = 75mV typ) | 0.7 | | 0.9 | V |
| UVP Blanking Time | | From rising edge of SHDN | 10 | 20 | 40 | ms |
| OVP, UVP, POK_ Propagation Delay | | | | 10 | | μs |
| POK_ Output Low Voltage | | ISINK = 4mA | | | 0.3 | V |
| POK_ Leakage Current | | V _{POK} _ = 5.5V, V _{FB} = 0.8V, V _{VTTS} = 1.3V | | | 1 | μΑ |
| ILIM Adjustment Range | V _{ILIM} | | 0.25 | | 2.00 | V |
| ILIM Input Leakage Current | | | | | 0.1 | μΑ |
| Current-Limit Threshold (Fixed) PGND1 to LX | | | 45 | 50 | 55 | mV |
| Current-Limit Threshold (Adjustable) PGND1 to LX | | V _{ILIM} = 2V | 170 | 200 | 235 | mV |
| Current-Limit Threshold (Fixed, Negative Direction) PGND1 to LX | | $\overline{\text{SKIP}} = \text{AV}_{\text{DD}}$ | -75 | -60 | -45 | mV |
| Current-Limit Threshold (Adjustable, Negative Direction) PGND1 to LX | | $\overline{\text{SKIP}} = \text{AV}_{\text{DD}}, \text{V}_{\text{ILIM}} = 2\text{V}$ | | -250 | | mV |
| Zero-Crossing Detection Threshold PGND1 to LX | | | | 3 | | mV |
| Thermal-Shutdown Threshold | | | | +160 | | °C |
| Thermal-Shutdown Hysteresis | | | | 15 | | °C |
| I nermal-Shutdown Hysteresis | | | | 15 | | |



ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN} = +15V, V_{DD} = AV_{DD} = V_{\overline{SHDN}} = \overline{STBY} = V_{BST} = V_{ILIM} = 5V, V_{OUT} = V_{REFIN} = V_{VTTI} = 2.5V, UVP/OVP = TP0 = FB = \overline{SKIP} = GND, PGND1 = PGND2 = LX = GND, TON = OPEN, V_{VTTS} = V_{VTT}, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | | |
|--|--------|-------------------------|------------------------|-----|------|-------|--|--|
| MOSFET DRIVERS | • | | • | | | • | | |
| DH Gate-Driver On-Resistance | | $V_{BST} - V_{LX} = 5V$ | | 1 | 4 | Ω | | |
| DL Gate-Driver On-Resistance in High State | | | | 1 | 4 | Ω | | |
| DL Gate-Driver On-Resistance in Low State | | | | 0.5 | 3 | Ω | | |
| Dead Time (Additional to | | DH falling to DL rising | | 30 | | | | |
| Adaptive Delay) | | DL falling to DH rising | | 50 | | ns | | |
| INPUTS AND OUTPUTS | | | | | | | | |
| Logic Input Threshold | | Rising edge | 1.20 | 1.7 | 2.20 | V | | |
| (SHDN, STBY, SKIP) | | Hysteresis | | 225 | | mV | | |
| Logic Input Current (SHDN, STBY, SKIP) | | | -1 | | +1 | μΑ | | |
| Dual-Mode™ Input Logic | | Low (2.5V output) | | | 0.05 | V | | |
| Levels (FB) | | High (1.8V output) | 2.1 | | | 7 V | | |
| Input Bias Current (FB) | | | -0.1 | | +0.1 | μΑ | | |
| | | High | AV _{DD} - 0.4 | | | | | |
| Four-Level Input Logic Levels (TON, OVP/UVP) | | Floating | 3.15 | | 3.85 | V | | |
| (1014, 041 / 041) | | REF | 1.65 | | 2.35 | | | |
| | | Low | | | 0.5 | | | |
| Logic Input Current (TON, OVP/UVP) | | | -3 | | +3 | μΑ | | |
| | | FB = GND | 90 | 175 | 350 | | | |
| OUT Input Resistance | | $FB = AV_{DD}$ | 70 | 135 | 270 | kΩ | | |
| | | FB adjustable mode | 400 | 800 | 1600 | | | |
| OUT Discharge-Mode On-Resistance | | | | 10 | 25 | Ω | | |
| DL Turn-On Level During Discharge Mode (Measured at OUT) | | | 0.01 | 0.1 | 0.20 | V | | |

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

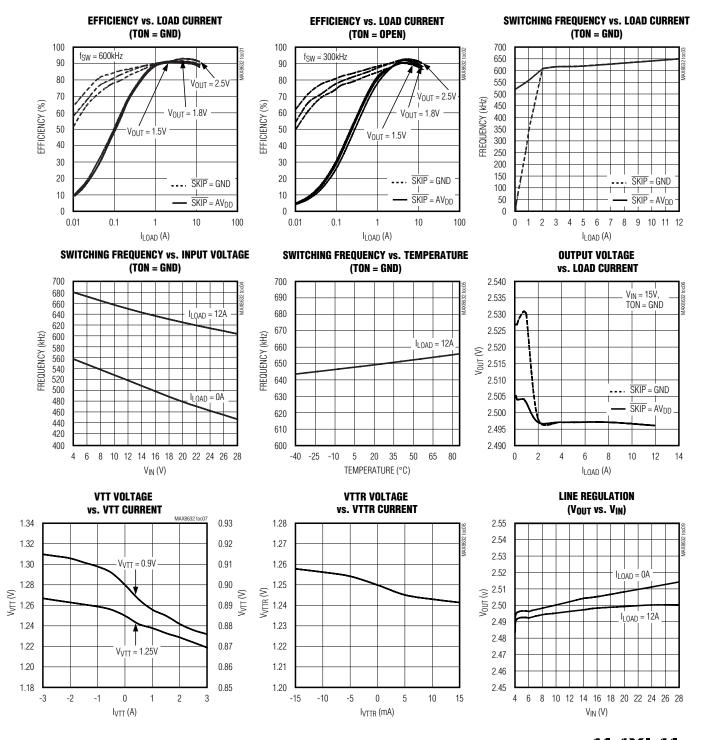
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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------|--|------|------|------|-------|
| LINEAR REGULATORS (VTTR A | ND VTT) | | | | | |
| VTTI Input Voltage Range | V _{VTTI} | V _{VTTI} | | | 2.8 | V |
| VTTI Supply Current | Ivtti | I _{VTT} = I _{VTTR} = 0 | | <0.1 | 1 | mA |
| VTTI Shutdown Current | | SHDN = GND | | | 10 | μΑ |
| REFIN Input Impedance | | V _{REFIN} = 2.5V | 12 | 20 | 30 | kΩ |
| REFIN Range | V _{REFIN} | | 1 | | 2.8 | V |
| VTT, VTTR UVLO Threshold (Measured at OUT) | | | 0.01 | 0.1 | 0.20 | V |
| Soft-Start Charge Current | ISS | V _{SS} = 0 | | 4 | | μΑ |
| VTT Internal MOSFET High-Side On-Resistance | | $I_{VTT} = -100$ mA, $V_{VTTI} = 1.5$ V, $AV_{DD} = 4.5$ V | | | 0.3 | Ω |
| VTT Internal MOSFET Low-Side On-Resistance | | I _{VTT} = 100mA, AV _{DD} = 4.5V | | | 0.3 | Ω |
| VTT Output Accuracy (Referred to V _{REFIN} / 2) | | V _{REFIN} = 1.5V or 2.5V, I _{VTT} = 1mA | -1 | | +1 | % |
| VTT Load Degulation | | $V_{REFIN} = 2.5V$, $I_{VTT} = 0$ to $\pm 1.5A$ | | 1.3 | | - % |
| VTT Load Regulation | | $V_{REFIN} = 1.5V$, $I_{VTT} = 0$ to $\pm 1A$ | | 1.3 | | 70 |
| VTT Current Limit | | VTT = 0 or VTTI | ±3 | ±5 | ±6.5 | А |
| VTTS Input Current | Ivtts | V _{VTTS} = 1.5V, VTT open | | 0.1 | 1 | μΑ |
| VTTR Output Error (Referred to V _{REFIN} / 2) | | V _{REFIN} = 1.5V or 2.5V, I _{VTTR} = 0 | -1 | | +1 | % |
| VTTR Current Limit | | V _{VTTR} = 0 or V _{VTTI} | ±18 | ±32 | ±50 | mA |
| VTTR Bias Current | | VREFIN = VVTTI = 0 | | 0.6 | 4 | μΑ |

- **Note 1:** Specifications to -40°C are guaranteed by design, not production tested.
- Note 2: When the inductor is in continuous conduction, the output voltage has a DC regulation level higher than the error-comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage has a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.
- Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, V_{BST} = 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times may differ due to MOSFET switching speeds.

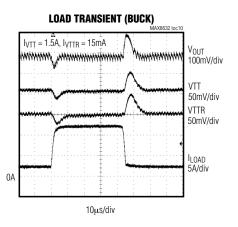
Typical Operating Characteristics

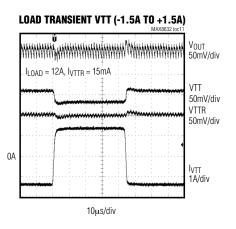
 $(V_{VIN} = 12V, V_{OUT} = 2.5V, TON = GND, \overline{SKIP} = AV_{DD}, circuit of Figure 8, T_A = +25°C, unless otherwise noted.)$

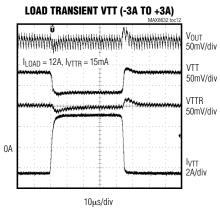


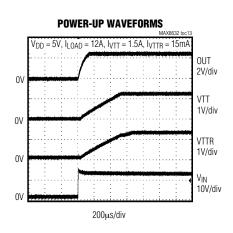
Typical Operating Characteristics (continued)

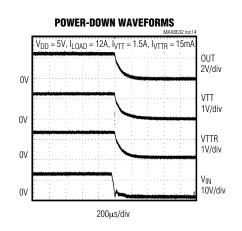
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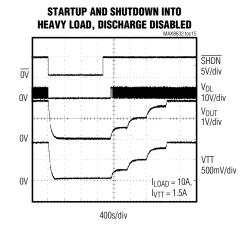


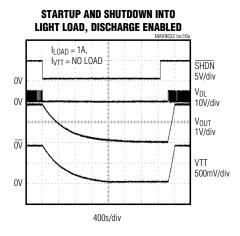


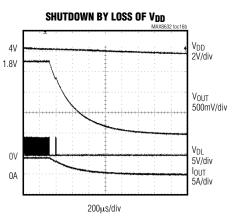


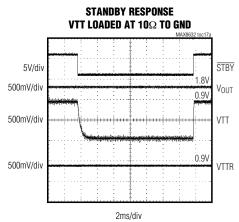






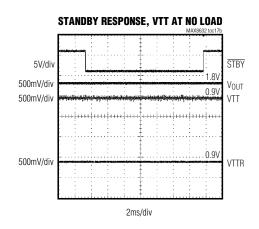


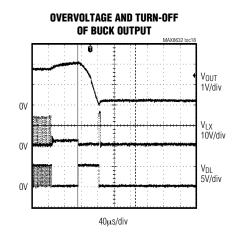


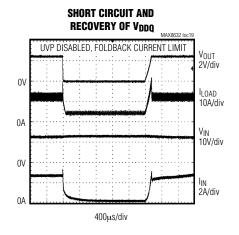


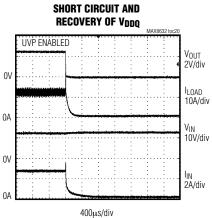
Typical Operating Characteristics (continued)

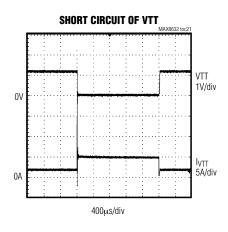
(V_{VIN} = 12V, V_{OUT} = 2.5V, TON = GND, $\overline{\text{SKIP}}$ = AV_{DD}, circuit of Figure 8, T_A = +25°C, unless otherwise noted.)











Pin Description

| PIN | NAME | FUNCTION |
|-----|-------------|---|
| 1 | TON | On-Time Selection-Control Input. This four-level logic input sets the nominal DH on-time. Connect to GND, REF, AV _{DD} , or leave TON unconnected to select the following nominal switching frequencies: TON = AV _{DD} (200kHz) TON = open (300kHz) TON = REF (450kHz) TON = GND (600kHz) |
| 2 | OVP/ UVP | Overvoltage-/Undervoltage-Protection Control Input. This four-level logic input enables or disables the overvoltage and/or undervoltage protection. The overvoltage limit is 116% of the nominal output voltage. The undervoltage limit is 70% of the nominal output voltage. Discharge mode is enabled when OVP is also enabled. Connect the OVP/UVP pin to the following pins for the desired function: OVP/UVP = AVDD (Enable OVP and discharge mode, enable UVP.) OVP/UVP = open (Enable OVP and discharge mode, disable UVP.) OVP/UVP = GND (Disable OVP and discharge mode, disable UVP.) |
| 3 | REF | +2.0V Reference Voltage Output. Bypass to GND with a 0.1μF (min) capacitor. REF can supply 50μA for external loads. Can be used for setting voltage for ILIM. REF turns off when SHDN is low and OUT < 0.1V. |
| 4 | ILIM | Valley Current-Limit Threshold Adjustment for Buck Regulator. The current-limit threshold across PGND and LX is 0.1 times the voltage at ILIM. Connect ILIM to a resistive divider, typically from REF to GND, to set the current-limit threshold between 25mV and 200mV. This corresponds to a 0.25V to 2V range at ILIM. Connect ILIM to AV _{DD} to select the 50mV default current-limit threshold. See the <i>Setting the Current Limit (Buck)</i> section. |
| 5 | POK1 | Buck Power-Good Open-Drain Output. POK1 is low when the buck output voltage is more than 10% above or below the normal regulation point or during soft-start. POK1 is high impedance when the output is in regulation and the soft-start circuit has terminated. POK1 is low in shutdown. |
| 6 | POK2 | LDO Power-Good Open-Drain Output. In normal mode, POK2 is low when either VTTR or VTTS is more than 10% above or below the normal regulation point, which is typically REFIN / 2. In standby mode, POK2 responds only to the VTTR input. POK2 is low in shutdown, and when VREFIN is less than 0.8V. |
| 7 | STBY | Standby. Connect to GND for low-quiescent mode where the VTT output is open circuit. POK2 takes input from only VTTR in this mode. PWM output can be on or off, depending on the state of SHDN. |
| 8 | SS | Soft-Start Control for VTT. Connect a capacitor (C9 in Figure 8) from SS to ground. Leave SS open to disable soft-start. SS discharges to ground when VTT is off. See the <i>POR</i> , <i>UVLO</i> , and <i>Soft-Start</i> section. |
| 9 | VTTS | Sensing Pin for Termination Supply Output. Normally connected to VTT pin to allow accurate regulation to half the REFIN voltage. Connected to a resistive divider from VTT to GND to regulate VTT to higher than half the REFIN voltage. |
| 10 | VTTR | Termination Reference Voltage. VTTR tracks V _{REFIN} / 2. |

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----|------------------|---|
| 11 | PGND2 | Power Ground for VTT and VTTR. Connect PGND2 externally to the underside of the exposed pad. |
| 12 | VTT | Termination Power-Supply Output. Connect VTT to VTTS to regulate to V _{REFIN} / 2. |
| 13 | VTTI | Power-Supply Input Voltage for VTT and VTTR. Normally connected to the output of the buck regulator for DDR application. |
| 14 | REFIN | External Reference Input. This is used to regulate the VTT and VTTR outputs to V _{REFIN} / 2. |
| 15 | FB | Feedback Input for Buck Output. Connect to AV _{DD} for a +1.8V fixed output or to GND for a +2.5V fixed output. For an adjustable output (0.7V to 5.5V), connect FB to a resistive divider from the output voltage. FB regulates to +0.7V. |
| 16 | OUT | Output-Voltage Sense Connection. Connect to the positive terminal of the buck output filter capacitor. OUT senses the output voltage to determine the on-time for the high-side switching MOSFET (Q1 in Figure 8). OUT also serves as the buck output's feedback input in fixed-output modes. When discharge mode is enabled by OVP/UVP, the output capacitor is discharged through an internal 10Ω resistor connected between OUT and GND. OUT also acts as the input to the VTT and VTTR UVLO detector. |
| 17 | VIN | Input-Voltage Sense Connection. Connect to input power source. V _{IN} is used only to set the PWM's ontime one-shot timer. IN voltage range is from 2V to 28V. |
| 18 | DH | High-Side Gate-Driver Output. Swings from LX to BST. DH is low when in shutdown or UVLO. |
| 19 | LX | External Inductor Connection. Connect LX to the input side of the inductor. LX is used for both current limit and the return supply of the DH driver. |
| 20 | BST | Boost Flying-Capacitor Connection. Connect to an external capacitor and diode according to Figure 8. See the <i>Boost-Supply Diode and Capacitor Selection (Buck)</i> section. |
| 21 | DL | Synchronous-Rectifier Gate-Driver Output. Swings from PGND to V _{DD} . |
| 22 | V _{DD} | Supply Input for the DL Gate Drive. Connect to the +4.5V to +5.5V system supply voltage. Bypass to PGND1 with a 1µF (min) ceramic capacitor. |
| 23 | PGND1 | Power Ground for Buck Controller. Connect PGND1 externally to the low-side FET's source. |
| 24 | GND | Analog Ground for Both Buck and LDO. Connect GND externally to the underside of the exposed pad. |
| 25 | SKIP | Pulse-Skipping Control Input. Connect to AV _{DD} for low-noise, forced-PWM mode. Connect to GND to enable pulse-skipping operation. |
| 26 | AV _{DD} | Analog Supply Input for Both Buck and LDO. Connect to the +4.5V to +5.5V system supply voltage with a series 10Ω resistor. Bypass to GND with a 1μF or greater ceramic capacitor. |
| 27 | SHDN | Shutdown Control Input. Use to control buck output. A rising edge on SHDN clears the overvoltage-and undervoltage-protection fault latches (see Tables 2 and 3). Connect to AV _{DD} for normal operation. |
| 28 | TP0 | This is a test pin. Must connect to GND externally. |
| _ | EP | Exposed pad. The exposed pad must be star-connected to GND and PGND2. See <i>Special Layout Considerations for LDO Section</i> for more details. |

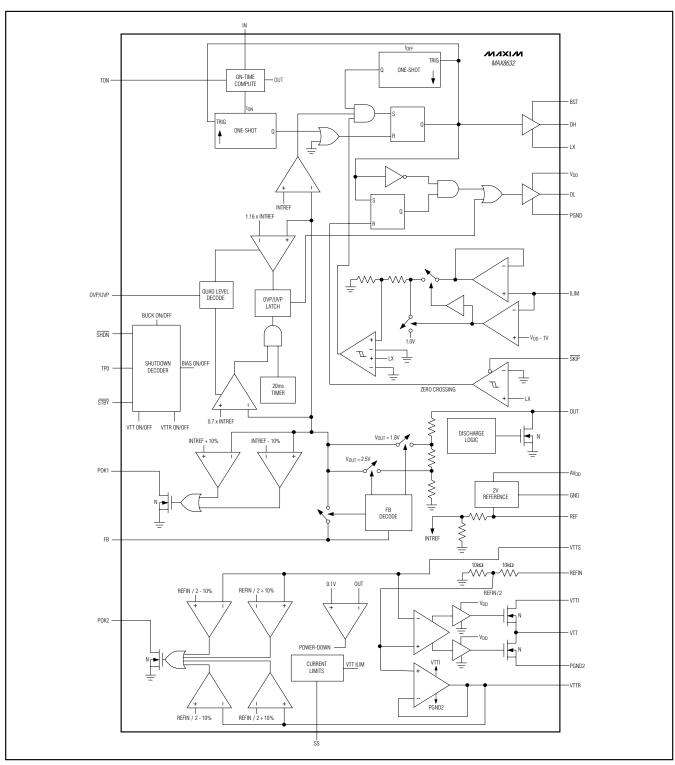


Figure 1. Functional Diagram

Detailed Description

The MAX8632 combines a synchronous-buck PWM controller, an LDO linear regulator, and a 10mA reference output buffer. The buck controller drives two external n-channel MOSFETs to deliver load currents up to 15A and generate voltages down to 0.7V from a +2V to +28V input. The LDO linear regulator can sink and source up to 1.5A continuous and 3A peak current with relatively fast response. These features make the MAX8632 ideally suited for DDR memory applications.

The MAX8632 buck regulator is equipped with a fixed switching frequency of up to 600kHz using Maxim's proprietary constant on-time Quick-PWM architecture. This control scheme handles wide input/output voltage ratios with ease, and provides 100ns "instant-on" response to load transients, while maintaining high efficiency with relatively constant switching frequency.

The buck controller, LDO, and a reference output buffer are provided with independent current limits. Lossless foldback current limit in the buck regulator is achieved by monitoring the drain-to-source voltage drop of the low-side FET. The ILIM input is used to adjust this current limit. Overvoltage protection, if selected, is achieved by latching the low-side synchronous FET on and the high-side FET off when the output voltage is over 116% of its set output. It also features an optional undervoltage protection by latching the MOSFET drivers to the OFF state during an overcurrent condition, when the output voltage is lower than 70% of the regulated output. This helps minimize power dissipation during a short-circuit condition.

The current limit in the LDO and buffered reference output buffer is $\pm 5A$ and $\pm 32mA$, respectively, and neither have the over- or undervoltage protection. When the current limit in either output is reached, the output no longer regulates the voltage, but regulates the current to the value of the current limit.

+5V Bias Supply (VDD and AVDD)

The MAX8632 requires an external +5V bias supply in addition to the input voltage (V_{IN}). Keeping the bias supply external to the IC improves the efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and the gate drivers. If stand-alone capability is needed, then the +5V supply can be generated with an external linear regulator such as the MAX1615. V_{DD}, AV_{DD}, and IN can be connected together if the input source is a fixed +4.5V to +5.5V supply.

 V_{DD} is the supply input for the buck regulator's MOSFET drivers, and AVDD supplies the power for the rest of

the IC. The current from the AVDD and VDD power supply must supply the current for the IC and the gate drive for the MOSFETs. This maximum current can be estimated as:

$$I_{BIAS} = I_{VDD} + I_{AVDD} + f_{SW} \times (Q_{G1} + Q_{G2})$$

where I_{VDD} + I_{AVDD} are the quiescent supply currents into V_{DD} and AV_{DD}, Q_{G1} and Q_{G2} are the total gate charges of MOSFETs Q1 and Q2 (at V_{GS} = 5V) in Figure 8, and f_{SW} is the switching frequency.

Free-Running Constant-On-Time PWM

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward (Figure 1). This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to the output voltage. Another one-shot sets a minimum off-time of 300ns (typ). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to input and output voltages. The high-side switch on-time is inversely proportional to the input voltage (VIN) and is proportional to the output voltage:

$$t_{ON} = K \times \frac{\left(V_{OUT} + I_{LOAD} \times R_{DS(ON)Q2}\right)}{V_{IN}}$$

where K (the switching period) is set by the TON input connection (Table 1) and RDS(ON)Q2 is the on-resistance of the synchronous rectifier (Q2) in Figure 8. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold:

- 1) The frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band.
- The inductor ripple-current operating point remains relatively constant, resulting in an easy design methodology and predictable output voltage ripple.

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* table (approximately ±12.5% at 600kHz and 450kHz, and ±10% at 200kHz and 300kHz). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range. For example, the 600kHz setting typically runs approximately 10% slower with inputs much greater than 5V due to the very short on-times required.

The constant on-time translates only roughly to a constant switching frequency. The on-times guaranteed in the *Electrical Characteristics* table are influenced by resistive losses and by switching delays in the highside MOSFET. Resistive losses, which include the inductor, both MOSFETs, the output capacitor's ESR, and any PC board copper losses in the output and ground, tend to raise the switching frequency as the load increases. The dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times are added to the effective ontime. The dead time occurs only in PWM mode (\overline{SKIP} = V_{DD}) and during dynamic output-voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including the synchronous rectifier, the inductor, and any PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, including the high-side switch (Q1 in Figure 8), the inductor, and any PC board resistances, and t_{ON} is the one-shot on-time (see the *On-Time One-Shot (TON)* section.

Automatic Pulse-Sk<u>ipping</u> Mode (SKIP = GND)

In skip mode (SKIP = GND), an inherent automatic switchover to PFM takes place at light loads (Figure 2). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator differentially senses the inductor current across the synchronous-rectifier MOSFET (Q2 in Figure 8). Once VPGND - VLX drops below 5% of the current-limit threshold (2.5mV for the default 50mV current-limit threshold),

the comparator forces DL low (Figure 1). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load-current level at which PFM/PWM crossover occurs, ILOAD(SKIP), is equal to half the peak-to-peak ripple current, which is a function of the inductor value (Figure 2). This threshold is relatively constant, with only a minor dependence on the input voltage (VIN):

$$I_{LOAD(SKIP)} = \left(\frac{V_{OUT} \times K}{2L}\right) \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

where K is the on-time scale factor (see Table 1). For example, in Figure 8 (K = 1.7 μ s, V_{OUT} = 2.5V, V_{IN} = 12V, and L = 1 μ H), the pulse-skipping switchover occurs at:

$$\left(\frac{2.5V \times 1.7\mu s}{2 \times 1\mu H}\right) \left(\frac{12V - 2.5V}{12V}\right) = 1.68A$$

The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used. The switching waveforms can appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance

Table 1. Approximate K-Factor Errors

| TON SETTING | TYPICAL K-FACTOR (μs) | K-FACTOR ERROR (%) | MINIMUM V _{IN} AT V _{OUT} = 2.5V (h = 1.5; SEE THE DROPOUT PERFORMANCE (BUCK) SECTION) |
|----------------------------------|-----------------------------|--------------------------|---|
| 200 (TON = AV _{DD}) | 5.0 | ±10 | 3.15 |
| 300 (TON = open) | 3.3 | ±10 | 3.47 |
| 450 (TON = REF) | 2.2 | ±12.5 | 4.13 |
| 600 (TON = GND) | 1.7 | ±12.5 | 5.61 |

remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input-voltage levels.

DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX8632 regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ($\overline{SKIP} = GND$ and $I_{LOAD} < I_{LOAD}(\overline{SKIP})$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Forced-PWM Mode ($\overline{SKIP} = AV_{DD}$)

The low-noise forced-PWM mode (SKIP = AVDD) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of VOUT / VIN. Forced-PWM mode keeps the switching frequency fairly constant. However, forced-PWM operation comes at a cost where the no-load VDD bias current remains between 2mA and 20mA due to the external MOSFET's gate charge and switching frequency. Forced-PWM mode is most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output-voltage adjustment.

Current-Limit Buck Regulator (ILIM) Valley Current Limit

The current-limit circuit for the buck regulator portion of the MAX8632 employs a unique "valley" current-sensing algorithm that senses the voltage drop across LX and PGND1 and uses the on-resistance of the rectifying MOSFET (Q2 in Figure 8) as the current-sensing element. If the magnitude of the current-sense signal is above the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle (Figure 4). With valley current-limit sensing, the actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor current ripple. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and input voltage. When combined with the undervoltage-protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX8632 also implements a negative current limit to prevent excessive reverse inductor currents when the buck regulator output is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when $V_{\rm ILIM}$ is adjusted. The current-limit threshold is adjusted with an external resistor-divider at ILIM. A 2 μ A to 20 μ A divider current is recommended for accuracy and noise immunity.

The current-limit threshold adjustment range is from 25mV to 200mV. In the adjustable mode, the current-limit threshold voltage (from PGND1 to LX) is precisely 1/10th the voltage seen at ILIM. The threshold defaults to 50mV when ILIM is connected to AVDD. The logic threshold for switchover to the 50mV default value is approximately AVDD - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen between LX and GND.

POR, UVLO, and Soft-Start

Internal power-on reset (POR) occurs when AV_{DD} rises above approximately 2V, resetting the fault latch and the soft-start counter, powering up the reference, and preparing the buck regulator for operation. Until AV_{DD} reaches 4.25V (typ), AV_{DD} undervoltage-lockout (UVLO) circuitry inhibits switching. The controller inhibits switching by pulling DH low and holding DL low

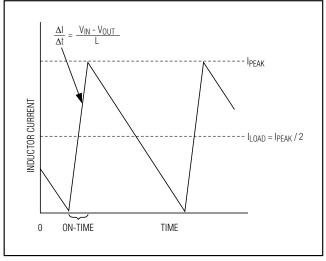


Figure 2. Pulse-Skipping/Discontinuous Crossover Point

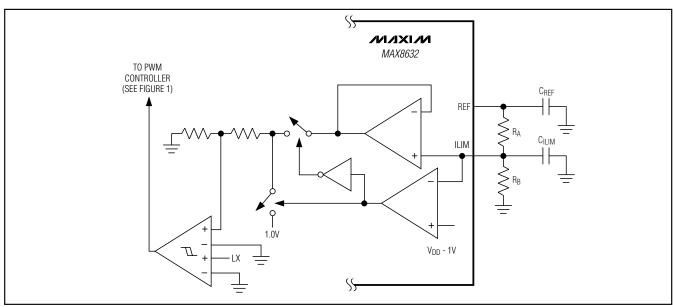


Figure 3. Adjustable Current-Limit Threshold

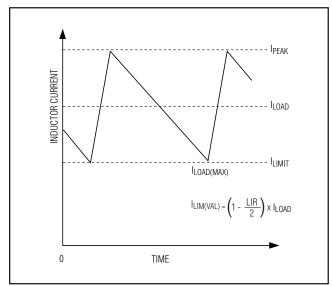


Figure 4. Valley Current-Limit Threshold

when OVP and shutdown discharge are disabled (OVP/UVP = REF or GND) or forcing DL high when OVP and shutdown discharge are enabled (OVP/UVP = AV_{DD} or OPEN). See Table 3 for a detailed truth table for OVP/UVP and shutdown settings. When AV_{DD} rises above 4.25V, the controller activates the buck regulator and initializes the internal soft-start.

The buck regulator's internal soft-start allows a gradual increase of the current-limit level during startup to

reduce the input surge currents. The MAX8632 divides the soft-start period into five phases. During the first phase, the controller limits the current limit to only 20% of the full current limit. If the output does not reach regulation within 425µs, soft-start enters the second phase, and the current limit is increased by another 20%. This process repeats until the maximum current limit is reached, after 1.7ms, or when the output reaches the nominal regulation voltage, whichever occurs first. Adding a capacitor in parallel with the external ILIM resistors creates a continuously adjustable analog soft-start function for the buck regulator's output.

Soft-start in the LDO section can be realized by connecting a capacitor between the SS pin and ground. When VTT is turned off or placed in standby mode, or during thermal shutdown of the LDOs, the SS capacitor is discharged. When VTT is turned on or when the thermal limit is removed, an internal 4µA (typ) current charges the SS capacitor. The resulting ramp voltage on SS linearly increases the current-limit comparator threshold to the VTT output, until full current limit is attained when SS reaches approximately 1.6V. This lowering of the current limit during startup limits the initial inrush current peaks, particularly when driving capacitors. Choose the value of the SS capacitor appropriately to set the soft-start time window. Leave SS floating to disable the soft-start feature.

Power-OK (POK1)

POK1 is an open-drain output for a window comparator that continuously monitors VOUT. POK1 is actively held

low when \overline{SHDN} is low and during the buck regulator output's soft-start. After the digital soft-start terminates, POK1 becomes high impedance as long as the output voltage is within $\pm 10\%$ of the nominal regulation voltage set by FB. When Vout drops 10% below or rises 10% above the nominal regulation voltage, the MAX8632 pulls POK1 low. Any fault condition forces POK1 low until the fault latch is cleared by toggling \overline{SHDN} or cycling AVDD power below 1V. For logic-level output voltages, connect an external pullup resistor between POK1 and AVDD. A $100k\Omega$ resistor works well in most applications. Note that the POK1 window detector is completely independent of the overvoltage- and undervoltage-protection fault detectors and the state of VTTS and VTTR.

SHDN and **Output** Discharge

The SHDN input corresponds to the buck regulator and places the buck regulator's portion of the IC in a low-power mode (see the *Electrical Characteristics* table). SHDN is also used to reset a fault signal such as an overvoltage or undervoltage fault.

When output discharge is enabled, (OVP/UVP = AVDD or open) and \overline{SHDN} is pulled low, or if UVP is enabled (OVP/UVP = AVDD) and VOUT falls to 70% of its regulation set point, the MAX8632 discharges the buck regulator output (through the OUT input) through an internal 10Ω switch to ground. While the output is discharging, DL is forced low and the PWM controller is disabled but the reference remains active to provide an accurate threshold. Once the output voltage drops below 0.1V, the MAX8632 shuts down the reference and DL remains low.

When output discharge is disabled (OVP/UVP = REF or GND), the controller does not actively discharge the buck output and the DL driver remains low. Under these conditions, the buck output discharge rate is determinedby the load current and its output capacitance. The buck regulator detects and latches the dischargemode state set by the OVP/UVP setting on startup.

When OUT is discharging, both VTT and VTTR outputs remain alive and continue to track REFIN until OUT drops to 0.1V.

STBY

The STBY input is an active-low input that is used to shut down only the VTT output. When STBY is low, VTT is high impedance.

Power-OK (POK2)

POK2 is the open-drain output for a window comparator that continuously monitors the VTTS input and VTTR output. POK2 is pulled low when REFIN is less than 0.8V. POK2 is high impedance as long as the output voltage is within $\pm 10\%$ of the nominal regulation voltage as set by REFIN. When VvTTs or VvTTR rises 10% above or 10% below its nominal regulation voltage, the MAX8632 pulls POK2 low. For logic-level output voltages, connect an external pullup resistor between POK2 and AVDD. A 100k Ω resistor works well in most applications.

Current Limit (LDO for VTT and VTTR Buffer)

The VTT output is a linear regulator that regulates the input (VTTI) to half the V_{REFIN} voltage. The feedback point for VTT is at the VTTS input (Figure 1). VTT is capable of sinking and sourcing at least 1.5A of continuous current and 3A peak current. The current limit for VTT and VTTR is typically $\pm 5A$ and $\pm 32mA$, respectively. When the current limit for either output is reached, the outputs regulate the current, not the voltage.

Fault Protection

The MAX8632 provides overvoltage/undervoltage fault protection in the buck controller. Select OVP/UVP to enable and disable fault protection as shown in Table 3. Once activated, the controller continuously monitors the output for undervoltage and overvoltage fault conditions.

Table 2. Shutdown and Standby Control Logic

| SHDN | STBY | BUCK OUTPUT (V _{DDQ}) | VTT | VTTR |
|---------------------|--------------------|---------------------------------|--------------------------|--------------------------|
| AV _{DD} * | AV _{DD} * | ON | ON | ON |
| AV _{DD} ** | GND** | ON | OFF (high impedance) | ON |
| GND*** | X | OFF | OFF (tracking 0.5 REFIN) | OFF (tracking 0.5 REFIN) |

^{*}For DDR application, this is referred as S0 state, where all outputs are on.

^{**}For DDR application, this is referred as S3 state, where $V_{
m DDQ}$ and VTTR are kept on, but VTT is turned off (high impedance).

^{***}For DDR application, this is referred as S4/S5 states, where all outputs are off. Discharge mode should be selected (OVP/UVP = AV_{DD} or OPEN, see Table 3) to discharge the outputs.

Overvoltage Protection (OVP)

When the output voltage rises above 116% of the nominal regulation voltage and OVP is enabled (OVP/UVP = AV_{DD} or open), the OVP circuit sets the fault latch, shuts down the PWM controller, and immediately pulls DH low and forces DL high. This turns on the synchronous-rectifier MOSFET (Q2 in Figure 8) with a 100% duty cycle, rapidly discharging the output capacitor and clamping the output to ground. Once the output reaches 0.1V, DL is switched off, preventing the possibility of a negative voltage on the output. Toggle \overline{SHDN} or cycle \overline{AVDD} below 1V to clear the fault latch and restart the controller. OVP is disabled when OVP/UVP is connected to REF or GND (see Table 3). OVP only applies to the buck output. The VTT and VTTR outputs do not have overvoltage protection.

Undervoltage Protection (UVP)

When the output voltage drops below 70% of its regulation voltage while UVP is enabled, the controller sets the fault latch and begins the discharge mode (see the SHDN and Output Discharge section). UVP is ignored for at least 10ms (min) after startup or after a rising edge on SHDN. Toggle SHDN or cycle AVDD power below 1V to clear the fault latch and restart the controller. UVP is disabled when OVP/UVP is left open or connected to GND (see Table 3). UVP only applies to the buck output. The VTT and VTTR outputs do not have undervoltage protection.

Thermal Fault Protection

The MAX8632 features two thermal-fault-protection circuits. One monitors the buck-regulator portion of the IC and the other monitors the linear regulator (VTT) and the reference buffer output (VTTR). When the junction

temperature of the buck-regulator portion of the MAX8632 rises above +160°C, a thermal sensor activates the fault latch, pulls POK1 low, and shuts down the buck-controller output using discharge mode regardless of the OVP/UVP setting. Toggle SHDN or cycle AVDD below 1V to reactivate the controller after the junction temperature cools by 15°C. If the VTT and VTTR regulator portion of the IC has its die temperature rise above +160°C, then VTT and VTTR shut off, go high impedance, and restart after the die portion of the IC cools by 15°C. Both thermal faults are independent. For example, if the VTT output is overloaded to the point that it triggers its thermal fault, the buck regulator continues to function.

Design Procedure

Firmly establish the input voltage range (V_{IN}) and maximum load current (I_{LOAD}) in the buck regulator before choosing a switching frequency and inductor operating point (ripple current ratio or LIR). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- Input Voltage Range. The maximum value (VIN(MAX))
 must accommodate the worst-case voltage. The minimum value (VIN(MIN)) must account for the lowest
 voltage after drops due to connectors and fuses. If
 there is a choice, lower input voltages result in better
 efficiency.
- Maximum Load Current. There are two values to consider. The peak load current (IPEAK) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the

Table 3. OVP/UVP Fault Protection

| OVP/UVP | DISCHARGE | UVP PROTECTION | OVP PROTECTION |
|------------------|--|----------------|----------------|
| AV _{DD} | Yes. Output is discharged through an internal 10Ω resistance. | Enabled | Enabled |
| OPEN | Yes. Output is discharged through an internal 10Ω resistance. | Disabled | Enabled |
| REF | No. DL forced low when SHDN is low. | Enabled | Disabled |
| GND | No. DL forced low when SHDN is low. | Disabled | Disabled |

current-limit circuit. The continuous load current (ILOAD) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

- Switching Frequency. This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses proportional to frequency and V_{IN}². The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- Inductor Operating Point. This choice provides trade-offs: size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping (SKIP = low at light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Setting the Output Voltage (Buck)

Preset Output Voltages

The MAX8632 dual-mode operation allows the selection of common voltages without requiring external components (Figure 5). Connect FB to GND for a fixed 2.5V output, to AVDD for a fixed 1.8V output, or connect FB directly to OUT for a fixed 0.7V output.

Setting the Buck Regulator Output (V_{OUT}) with a Resistive Voltage-Divider at FB

The buck-regulator output voltage can be adjusted from 0.7V to 5.5V using a resistive voltage-divider (Figure 6). The MAX8632 regulates FB to a fixed reference voltage (0.7V). The adjusted output voltage is:

$$V_{OUT} = V_{FB} \left(1 + \frac{R_C}{R_D} \right) + \frac{V_{RIPPLE}}{2}$$

where V_{FB} is 0.7V, R_{C} and R_{D} are shown in Figure 6, and V_{RIPPLE} is:

$$V_{RIPPLE} = LIR \times I_{LOAD(MAX)} \times R_{ESR}$$

Setting the VTT and VTTR Voltages (LDO)

The termination power-supply output (VTT) can be set by two different methods. First, the VTT output can be connected directly to the VTTS input to force VTT to regulate to VREFIN / 2. Secondly, VTT can be forced to regulate higher than VREFIN / 2 by connecting a resistive divider from VTT to VTTS. The maximum value for VTT is VVTTI - VDROPOUT where VDROPOUT = IVTT × 0.3 Ω (max) at TA = +85°C.

The termination reference voltage (VTTR) tracks $0.5 \times VREFIN$.

Inductor Selection (Buck)

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT} (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

For example: ILOAD(MAX) = 12A, V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 600kHz, 30% ripple current or LIR = 0.3:

$$L \ = \ \frac{2.5 \text{V } (12 \text{V - 2.5V})}{12 \text{V} \times 600 \text{kHz} \times 12 \text{A} \times 0.3} \approx 1 \mu \text{H}$$

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at frequencies up

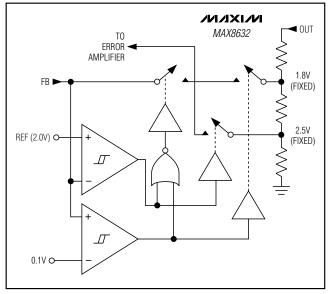


Figure 5. Dual-Mode Feedback Decoder

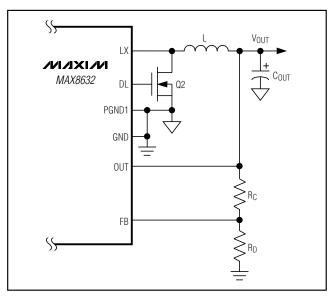


Figure 6. Setting VOUT with a Resistive Voltage-Divider

to 200kHz. The core must be large enough not to saturate at the peak inductor current (IPEAK):

$$I_{PEAK} = I_{LOAD(MAX)} \left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Input Capacitor Selection (Buck)

The input capacitor must meet the ripple current requirement (IRMS) imposed by the switching currents:

$$I_{RMS} = I_{LOAD} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

IRMS has a maximum value of I_{LOAD} / 2 when V_{IN} = $2 \times V_{OUT}$. For most applications, nontantalum capacitors (ceramic, aluminum, POS, or OSCON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX8632 is operated as the second stage of a two-stage power conversion system, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than 10° C

temperature rise at the RMS input current for optimal reliability and lifetime.

Output Capacitor Selection (Buck)

The output filter capacitor must have low enough equivalent series resistance (RESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor core voltage converters and other applications in which the output is subject to violent load transients, the output capacitor's size depends on how much RESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much RESR is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a stepdown controller is approximately equal to the total inductor ripple current multiplied by the output capacitor's RESR. Therefore, the maximum RESR required to meet ripple specifications is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{I_{LOAD(MAX)} \times LIR}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OSCONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent VSAG and VSOAR from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the VSAG and VSOAR equations in the *Transient Response (Buck)* section). However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability (see the *Stability Requirements* section).

Stability Requirements

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \leq \frac{f_{SW}}{\pi}$$
 where:
$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

If Cout consists of multiple same-value capacitors, as in Figure 8, the fest remains the same as that of a single capacitor.

For a typical 600kHz application, the ESR zero frequency must be well below 190kHz, preferably below 100kHz. Two 150 μ F/4V Sanyo POS capacitors are used to provide 12m Ω (max) of RESR. This results in a zero at 42kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and fast-feed-back loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired.

Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped but can cause the output voltage to rise above or fall below the tolerance limits. The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

VTT Output Capacitor Selection (LDO)

A minimum value of 20µF is needed to stabilize the VTT output. This value of capacitance limits the regulator's unity-gain bandwidth frequency to approximately 1.8MHz (typ) to allow adequate phase margin for stability. To keep the capacitor acting as a capacitor within the regulator's bandwidth, it is important that ceramic caps with low ESR and ESL be used.

Since the gain bandwidth is also determined by the transconductance of the output FETs, which increases with load current, the output capacitor may need to be greater than 20µF if the load current exceeds 1.5A, but can be smaller than 20µF if the maximum load current is less than 1.5A. As a guideline, choose the minimum capacitance and maximum ESR for the output capacitor using the following:

$$C_{OUT_MIN} = 20\mu F \times \sqrt{\frac{I_{LOAD}}{1.5A}}$$

 $R_{ESR_MAX} = 5m\Omega \times \sqrt{\frac{1.5A}{I_{LOAD}}}$

RESR value is measured at the unity-gain-bandwidth frequency given by approximately:

$$f_{GBW} = \frac{36}{C_{OUT}} \times \sqrt{\frac{I_{LOAD}}{1.5A}}$$

Once these conditions for stability are met, additional capacitors, including those of electrolytic and tantalum types, can be connected in parallel to the ceramic capacitor (if desired) to further suppress noise or voltage ripple at the output.

VTTR Output Capacitor Selection (LDO)

The VTTR buffer is a scaled-down version of the VTT regulator, with much smaller output transconductance. Its compensation cap can therefore be smaller, and its ESR larger, than what is required for its larger counterpart. For typical applications requiring load current up to $\pm 15 \text{mA}$, a ceramic cap with a minimum value of $1 \mu \text{F}$ is recommended (RESR < 0.3 Ω). Connect this cap between VTTR and the analog ground plane.

VTTI Input Capacitor Selection (LDO)

Both the VTT and VTTR output stages are powered from the same VTTI input. Their output voltages are referenced to the same REFIN input. The value of the VTTI bypass capacitor is chosen to limit the amount of ripple/noise at VTTI, or the amount of voltage dip during a load transient. Typically VTTI is connected to the output of the buck regulator, which already has a large bulk

capacitor. Nevertheless, a ceramic capacitor of at least 10µF must be used and must be added and placed as close as possible to the VTTI pin. This value must be increased with larger load current, or if the trace from the VTTI pin to the power source is long and has significant impedance. Furthermore, to prevent undesirable VTTI bounce from coupling back to the REFIN input and possibly causing instability in the loop, the REFIN pin should ideally tap its signal from a separate low-impedance DC source rather than directly from the VTTI input. If the latter is unavoidable, increase the amount of bypass capacitance at the VTTI input and add additional bypass at the REFIN pin.

MOSFET Selection (Buck)

The MAX8632 drives external, logic-level, n-channel MOSFETs as the circuit-switch elements. The key selection parameters:

On-resistance (RDS(ON)): the lower, the better.

Maximum drain-to-source voltage (VDSS): should be at least 20% higher than input supply rail at the high-side MOSFET's drain.

Gate charges (QG, QGD, QGS): the lower the better.

Choose MOSFETs with rated $R_{DS(ON)}$ at $V_{GS}=4.5V$. For a good compromise between efficiency and cost, choose the high-side MOSFET that has a conduction loss equal to its switching loss at nominal input voltage and maximum output current (see below). For the low-side MOSFET, make sure that it does not spuriously turn on because of dV/dt caused by the high-side MOSFET turning on, as this results in shoot-through current degrading efficiency. MOSFETs with a lower QGD to QGS ratio have higher immunity to dV/dt.

For proper thermal-management design, calculate the power dissipation at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage. For the low-side MOSFET, the worst case is at VIN(MAX). For the high-side MOSFET, the worst case could be at either VIN(MIN) or VIN(MAX). The high-side MOSFET and low-side MOSFET have different loss components due to the circuit operation. The low-side MOSFET operates as a zero-voltage switch; therefore, major losses are:

- The channel-conduction loss (PLSCC)
- The body-diode conduction loss (PLSDC)
- The gate-drive loss (PLSDR):

$$P_{LSCC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use RDS(ON) at TJ(MAX):

$$P_{LSDC} = 2I_{LOAD} \times V_F \times t_{DT} \times f_{SW}$$

where VF is the body-diode forward-voltage drop, tDT is the dead time (\approx 30ns), and fSW is the switching frequency. Because of the zero-voltage switch operation, the low-side MOSFET gate-drive loss occurs as a result of charging and discharging the input capacitance, (CISS). This loss is distributed among the average DL gate-driver's pullup and pulldown resistance, RDL (\approx 1 Ω), and the internal gate resistance (RGATE) of the MOSFET (\approx 2 Ω). The drive power dissipated is given by:

$$P_{LSDR} = C_{ISS} \times V_{GS}^2 \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{DL}}$$

The high-side MOSFET operates as a duty-cycle control switch and has the following major losses:

- The channel-conduction loss (PHSCC)
- The VI overlapping switching loss (PHSSW)
- The drive loss (PHSDR)

(The high-side MOSFET does not have body-diode conduction loss because the diode never conducts current):

$$P_{HSCC} = \frac{V_{OUT}}{V_{IN}} \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use RDS(ON) at TJ(MAX):

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times f_{SW} \times \frac{Q_{GS} + Q_{GD}}{I_{GATE}}$$

where IGATE is the average DH-driver output current determined by:

$$I_{GATE(ON)} = \frac{2.5V}{R_{DH} + R_{GATE}}$$

where RDH is the high-side MOSFET driver's on-resistance (1 Ω typ) and RGATE is the internal gate resistance of the MOSFET ($\approx 2\Omega$):

$$P_{HSDR} = Q_G \times V_{GS} \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{DH}}$$

where $V_{GS} = V_{DD} = 5V$. In addition to the losses above, allow about 20% more for additional losses because of MOSFET output capacitances and low-side MOSFET body-diode reverse-recovery charge dissipated in the high-side MOSFET that is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specifications to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above-calculated power dissipations. To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source, or add resistors in series with DH and DL to slow down the switching transitions. Adding series resistors increases the power dissipation of the MOSFET, so ensure that this does not overheat the MOSFET.

MOSFET Snubber Circuit (Buck)

Fast switching transitions cause ringing because of a resonating circuit formed by the parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, an optional series RC snubber circuit is added across each switch. Below is a simple procedure for selecting the value of the series RC of the snubber circuit:

- 1) Connect a scope probe to measure V_{LX} to PGND1, and observe the ringing frequency, f_R.
- 2) Estimate the circuit parasitic capacitance (CPAR) at LX by first finding a capacitor value, which, when connected from LX to PGND1, reduces the ringing frequency by half. CPAR can then be calculated as 1/3rd the value of the capacitor value found.
- 3) Estimate the circuit parasitic inductance (L_{PAR}) from the equation:

$$L_{PAR} = \frac{1}{(2\pi \times f_R)^2 \times C_{PAR}}$$

- 4) Calculate the resistor for critical dampening (R_{SNUB}) from the equation: R_{SNUB} = $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion.
- 5) The capacitor (C_{SNUB}) should be at least 2 to 4 times the value of C_{PAR} to be effective.

The power loss of the snubber circuit (PRSNUB) is dissipated in the resistor and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times V_{IN}^2 \times f_{SW}$$

where V_{IN} is the input voltage and f_{SW} is the switching frequency. Choose an R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Setting the Current Limit (Buck)

The current-sense method used in the MAX8632 makes use of the on-resistance (RDS(ON)) of the low-side MOSFET (Q2 in Figure 8). When calculating the current limit, use the worst-case maximum value for RDS(ON) from the MOSFET data sheet, and add some margin for the rise in RDS(ON) with temperature. A good general rule is to allow 0.5% additional resistance for each 1°C of temperature rise.

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at ILOAD(MAX) minus half the ripple current; therefore:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left(\frac{I_{LOAD(MAX)} \times LIR}{2}\right)$$

where I_{LIM(VAL)} equals the minimum valley current-limit threshold voltage divided by the on-resistance of Q2 (R_{DS(ON)Q2}). For the 50mV default setting, connect ILIM to AV_{DD}. In adjustable mode, the valley current-limit threshold is precisely 1/10th* the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to GND with ILIM connected to the center tap. The external 250mV to 2V adjustment range corresponds to a 25mV to 200mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10µA to prevent significant inaccuracy in the valley current-limit tolerance.

Foldback Current Limit

Alternately, foldback current limit can be implemented if the UVP latch option is not available. Foldback current limit reduces the power dissipation of external components so they can withstand indefinite overload and short circuit, with automatic recovery after the overload or short circuit is removed. To implement foldback current limit, connect a resistor from Vout to ILIM (R6 in Figures 7 and 8), in addition to the resistor-divider

^{*}In the negative direction, the adjustable current limit is typically -1/8th the voltage seen at ILIM.

network (R4 and R5) used for setting the adjustable current limit as shown in Figure 7.

The following is a procedure for calculating the value of R4, R5, and R6:

1) Calculate the voltage, VILIM(NOM), required at ILIM when the output voltage is at nominal:

$$V_{\text{ILIM(NOM)}} = 10 \times I_{\text{LOAD(MAX)}} \times \left(1 - \frac{\text{LIR}}{2}\right)$$

 $\times R_{\text{DS(ON)Q2}}$

- Pick a percentage of foldback, PFB, from 15% to 40%.
- 3) Calculate the voltage, V_{ILIM(OV)}, when the output is shorted (OV):

$$V_{ILIM(OV)} = P_{FB} \times V_{ILIM(NOM)}$$

4) The value for R4 can be calculated as:

$$R4 = \frac{2V - V_{ILIM(0V)}}{10\mu A}$$

5) The parallel combination of R5 and R6, denoted R56, is calculated as:

$$R56 = \left(\frac{2V}{10\mu A}\right) - R4$$

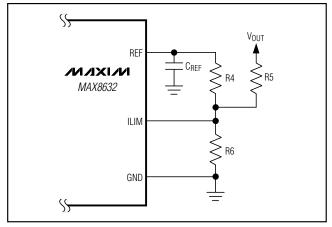


Figure 7. Foldback Current Limit

6) Then R6 can be calculated as:

$$R6 = \frac{V_{OUT} \times R4 \times R56}{\left[\left(V_{OUT} - \left(V_{ILIM(NOM)} - V_{ILIM(0V)}\right)\right) \times R4 - \left[\left(\left(V_{ILIM(NOM)} - V_{ILIM(0V)}\right) \times R56\right)\right]}$$

7) Then R5 is calculated as:

$$R5 = \frac{R6 \times R56}{R6 - R56}$$

Boost-Supply Diode and Capacitor Selection (Buck)

A low-current Schottky diode, such as the CMDSH-3 from Central Semiconductor, works well for most applications. Do not use large-power diodes, because higher junction capacitance can charge up the voltage at BST to the LX voltage and this exceeds the absolute maximum rating of 6V. The boost capacitor should be 0.1µF to 4.7µF, depending on the input and output voltages, external components, and PC board layout. The boost capacitance should be as large as possible to prevent it from charging to excessive voltage, but small enough to adequately charge during the minimum lowside MOSFET conduction time, which happens at maximum operating duty cycle (this occurs at minimum input voltage). In addition, ensure that the boost capacitor does not discharge to below the minimum gate-tosource voltage required to keep the high-side MOSFET fully enhanced for lowest on-resistance. This minimum gate-to-source voltage (VGS(MIN)) is determined by:

$$V_{GS(MIN)} = V_{DD} \times \frac{Q_G}{C_{BOOST}}$$

where V_{DD} is 5V, Q_{G} is the total gate charge of the high-side MOSFET, and C_{BOOST} is the boost-capacitor value where C_{BOOST} is C7 in Figure 8.

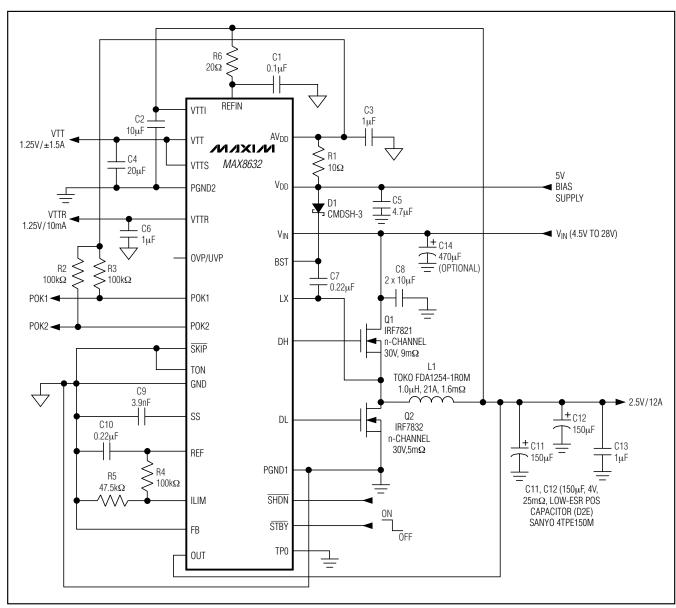


Figure 8. Typical Application Circuit

Transient Response (Buck)

The inductor ripple current also affects transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{L \times \Delta I_{LOAD(MAX)}^{2} \left[\frac{V_{OUT} \times K}{V_{IN}} + t_{OFF(MIN)} \right]}{2C_{OUT} \times V_{OUT} \left[\frac{\left(V_{IN} - V_{OUT}\right) \times K}{V_{IN}} + t_{OFF(MIN)} \right]}$$

where toff(MIN) is the minimum off-time (see the *Electrical Characteristics*) and K is from Table 1.

The overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{\Delta I_{LOAD(MAX)}^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

Applications Information

Dropout Performance (Buck)

The output-voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (see Table 1). Also, keep in mind that transient-response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the VSAG equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio h = ΔI_{UP} / ΔI_{DOWN} indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and VSAG greatly increases, unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between VSAG, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{\text{IN(MIN)}} = \left[\frac{V_{\text{OUT}} + V_{\text{DROP1}}}{1 - \left(\frac{h \times t_{\text{OFF(MIN)}}}{K}\right)} \right] + V_{\text{DROP2}} - V_{\text{DROP1}}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see the On-Time One-Shot (TON) section), $t_{OFF(MIN)}$ is from the Electrical Characteristics, and K is taken from Table 1. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then the operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG} . If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

A dropout design example follows:

VOUT = 2.5V

fsw = 600kHz

 $K = 1.7 \mu s$

tOFF(MIN) = 450ns

 $V_{DROP1} = V_{DROP2} = 100 \text{mV}$

h = 1.5

$$V_{IN(MIN)} = \left[\frac{2.5V + 0.1V}{1 - \left(\frac{1.5 \times 450ns}{1.7\mu s} \right)} \right] + 0.1V - 0.1V = 4.3V$$

Voltage Positioning (Buck)

In applications where fast-load transients occur, the output voltage changes instantly by Resr × Cout × Δl_{LOAD} . Voltage positioning allows the use of fewer output capacitors for such applications, and maximizes the output-voltage AC and DC tolerance window in tight-tolerance applications.

Figure 9 shows the connection of OUT and FB in a voltage-positioned circuit. In nonvoltage-positioned circuits, the MAX8632 regulates at the output capacitor. In voltage-positioned circuits, the MAX8632 regulates on the inductor side of the voltage-positioning resistor. VOUT is reduced to:

$$V_{OUT(VPS)} = V_{OUT(NO_LOAD)} - R_{POS} \times I_{LOAD}$$

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short.
 This practice is essential for high efficiency. Using

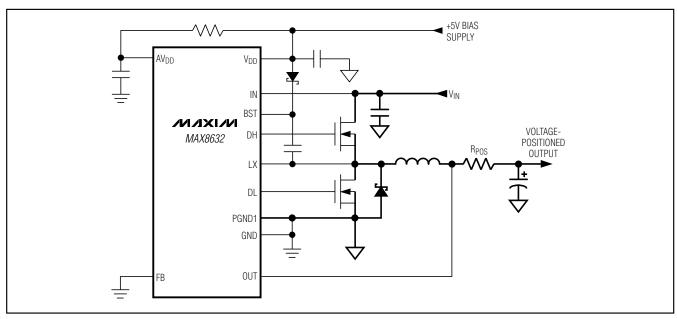


Figure 9. Voltage-Positioned Output

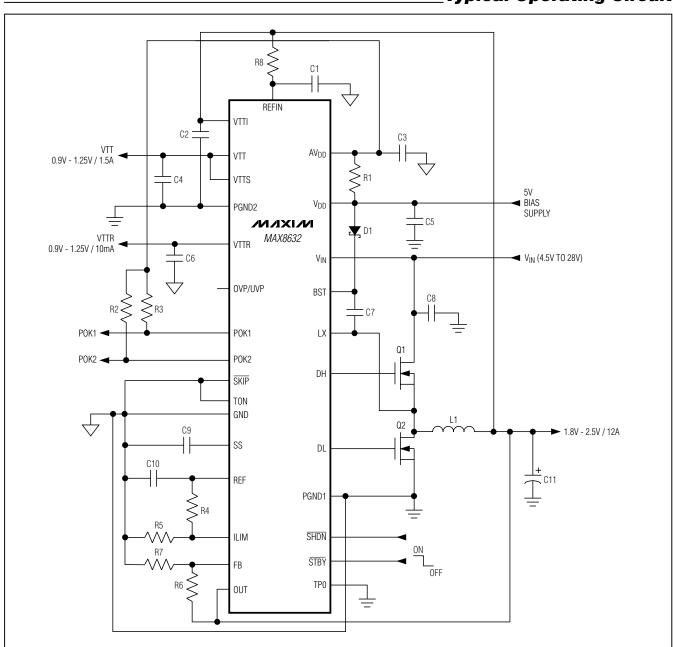
thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single $m\Omega$ of excess trace resistance causes a measurable efficiency penalty.

- The LX and PGND1 connections to the low-side MOSFET for current sensing must be made using Kelvin-sense connections.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor-charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the lowside MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (REF, FB, and ILIM).
- Input ceramic capacitors must be placed as close as possible to the high-side MOSFET drain and the low-side MOSFET source. Position the MOSFETs so the impedance between the input capacitor terminals and the MOSFETs is as low as possible.

Special Layout Considerations for LDO Section

The capacitor (or capacitors) at VTT should be placed as close to VTT and PGND2 (pins 12 and 11) as possible to minimize the series resistance/inductance of the trace. The PGND2 side of the capacitor must be short with a low-impedance path to the exposed pad underneath the IC. The exposed pad must be star-connected to GND (pin 24) and PGND2 (pin 11). Connect PGND1 (pin 23) separately to the nearby PGND plane at the source of the low-side MOSFET. Do not connect this pin directly to the exposed pad as this can inject undesirable switching noise into the clean analog GND. Instead, PGND1 (pin 23) is connected to PGND2 (pin 11) by the large PGND plane. A narrower trace can be used to connect the output voltage on the VTT side of the capacitor back to VTTS (pin 9). For best performance, the VTTI bypass capacitor must be placed as close to VTTI (pin 13) as possible. REFIN (pin 14) should be separately routed with a clean trace and adequately bypassed to GND. Refer to the MAX8632 evaluation kit data sheet for PC board guidelines.

Typical Operating Circuit

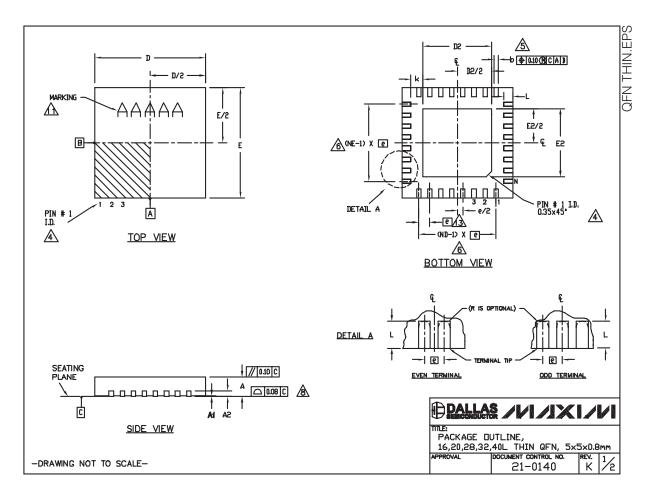


_Chip Information

TRANSISTOR COUNT: 5100 PROCESS: BICMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

| | COMMON DIMENSIONS | | | | | | | | | | | | | | |
|--------|-------------------|-------------|------|-----------|-------|-----------|------|-----------|------|------|-----------|------|------|---------|------|
| PKG. | 10 | 6L 5 | 5x5 | 2 | 0L : | 5×5 | 2 | :8L | 5x5 | 3 | 2L | 5×5 | 4 | 40L 5x5 | |
| SYMBOL | MIN. | NDM. | MAX. | MIN. | NOM. | MAX. | MIN. | NDM. | MAX. | MIN. | NOM. | MAX. | MIN. | NDM. | MAX. |
| Α | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.2 | 20 RE | F. | 0.2 | 20 RE | F. | 0.2 | 20 RE | F. | 0.2 | 20 RE | F. | 0.2 | 20 RE | F. |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| Ε | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| e | 0. | 80 B | SC. | 0.65 BSC. | | 0.50 BSC. | | 0.50 BSC. | | SC. | 0.40 BSC. | | sc. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | ı | - | 0.25 | 1 | - |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | | 16 | | | 20 | | | 28 | | 32 | | | 40 | | |
| ND | | 4 | | | 5 | | | 7 | | | 8 | | 10 | | |
| NE | | 4 | | | 5 | | | 7 | | 8 | | 10 | | | |
| JEDEC | _ \ | VHHB | | | WHHC | | \ \ | /HHD- | -1 | / | /HHD- | 2 | | | |

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- ⚠ DIMENSION 6 APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
 - ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS VELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
- VARPAGE SHALL NOT EXCEED 0.10 mm.
- MARKING IS FOR PACKAGE DRIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

-DRAWING NOT TO SCALE-

| EXPOSED PAD VARIATIONS | | | | | | | | |
|------------------------|------|------|------|------|------|------|--|--|
| PKG. | DS | | | E2 | | | | |
| CODES | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. | | |
| T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T1655N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| T2055M-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | | |
| T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | | |
| T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | | |
| T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| T2855N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| 13255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T3255M-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 | | |
| T4055-2 | 3,40 | 3,50 | 3.60 | 3.40 | 3.50 | 3.60 | | |



PACKAGE DUTLINE,

16,20,28,32,40L THIN QFN, 5x5x0.8mm DOCUMENT CONTROL NO.

21-0140

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Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

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ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

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