

Programmable power line communication modem System on Chip

Datasheet - production data



Features

- Programmable power line communication (PLC) modem System on Chip
- Integrated differential PLC analog front-end
 - PGA with automatic gain control and ADC
 - DAC with transmission pre-driver
 - Digital transmission level control
 - Zero crossing comparator
 - Up to 500 kHz PLC signal bandwidth
- High performance, fully programmable real-time engine dedicated to PLC PHY and real-time MAC protocol management (400 MHz max. frequency)
 - Dedicated code and data SRAM memories
- Standard ARM® 32-bit Cortex®-M4F fully programmable core for protocol upper layers and peripherals management
 - 200 MHz maximum frequency
 - 256 kB of embedded SRAM for code and data
 - 96 kB of embedded SRAM for data
 - 8 kB of embedded shared RAM
 - Bootloader ROM memory
 - One Time Programmable (OTP) memory with dedicated areas available for secure keys and user information storage
 - Serial wire and JTAG interfaces
 - 24 multiplexed GPIOs
 - 4 general purpose timers

- 1 flexible CRC calculation unit
- 2 USART, 1 UART, 3 SPI, 1 I²C
- Cryptographic engine
 - AES 128/192/256 engine
 - True random number generator
 - Pseudo random number generator
- Clock management:
 - 25 MHz external crystal for system clock
 - Integrated 25 MHz oscillator (XOSC) with frequency synthesizer (FS) and pre-scaler units to generate internal clock signals
- Power management
 - 3.3 V external supply voltage for I/O and analog
 - 2.5 V internal linear regulator for analog
 - 1.1 V external supply voltage for digital
 - Normal, Slow, Doze and low power modes
- Available in QFN56 package
- -40 °C to +105 °C temperature range

Applications

- Smart metering, smart grid and Internet of Things applications
- Suitable for application design compliant with CENELEC, FCC and ARIB regulations

Table 1. Device summary

| Order code | Package | Packing |
|------------|---------|---------------|
| ST8500 | QFN56 | Tray |
| ST8500TR | | Tape and reel |

Contents

| | | |
|----------|--|----------|
| 1 | Description | 4 |
| 2 | Device architecture | 5 |
| 2.1 | Power line communication (PLC) subsystem | 6 |
| 2.1.1 | Digital front-end (DFE) | 7 |
| 2.1.2 | Analog front-end (AFE) | 7 |
| 2.1.3 | Real-time engine (RTE) | 7 |
| 2.2 | Protocol core subsystem | 8 |
| 2.2.1 | ARM® Cortex™-M4F core | 8 |
| 2.2.2 | Multi-AHB bus matrix | 8 |
| 2.2.3 | Debug with serial wire JTAG debug port (SWJ-DP) | 9 |
| 2.2.4 | Floating point unit (FPU) | 9 |
| 2.2.5 | Nested vectored interrupt controller (NVIC) | 9 |
| 2.2.6 | General-purpose input/outputs (GPIOs) | 11 |
| 2.2.7 | General-purpose timer (GPT) | 11 |
| 2.2.8 | Window Watchdog (WWDG) | 11 |
| 2.2.9 | SysTick timer | 11 |
| 2.2.10 | Universal synchronous/asynchronous receiver transmitters (USART) | 11 |
| 2.2.11 | Serial peripheral interface (SPI) | 12 |
| 2.2.12 | Inter-integrated circuit interface (I ² C) | 12 |
| 2.2.13 | AES engine | 12 |
| 2.2.14 | True random number generator (TRNG) | 12 |
| 2.2.15 | Pseudo random number generator (PRNG) | 13 |
| 2.2.16 | CRC (cyclic redundancy check) calculation unit | 13 |
| 2.3 | Inter-processor communication (IPC) | 13 |
| 2.4 | Cortex™ memories | 13 |
| 2.4.1 | Embedded SRAM (instruction and data) | 13 |
| 2.4.2 | Embedded SRAM (data only) | 13 |
| 2.4.3 | Embedded ROM | 13 |
| 2.4.4 | One Time Programmable (OTP) section | 14 |
| 2.5 | Clock and reset management (CRM) | 15 |
| 2.5.1 | Clock management | 15 |
| 2.5.2 | Reset management | 16 |

| | | |
|----------|--|-----------|
| 2.6 | Power management | 16 |
| 2.6.1 | External power supply dimensioning | 17 |
| 2.6.2 | System power modes and low-power mode | 18 |
| 2.7 | Boot modes and system programmability | 19 |
| 3 | Pinout and pin description | 21 |
| 3.1 | Pin definition | 21 |
| 3.2 | GPIOs multiplexing scheme | 24 |
| 4 | Memory map | 25 |
| 5 | Electrical characteristics | 26 |
| 5.1 | Absolute maximum ratings | 26 |
| 5.2 | Thermal characteristics | 26 |
| 5.3 | Operating conditions | 27 |
| | Power supply characteristics | 27 |
| 5.4 | PLC analog front-end (AFE) characteristics | 30 |
| 5.4.1 | Transmission path characteristics | 30 |
| 5.4.2 | Reception path characteristics | 31 |
| 5.4.3 | Zero crossing comparator characteristics | 32 |
| 5.5 | Other characteristics | 32 |
| 6 | Package information | 34 |
| 6.1 | QFN56 (7 x 7 x 1 mm) package information | 34 |
| 7 | Revision history | 36 |

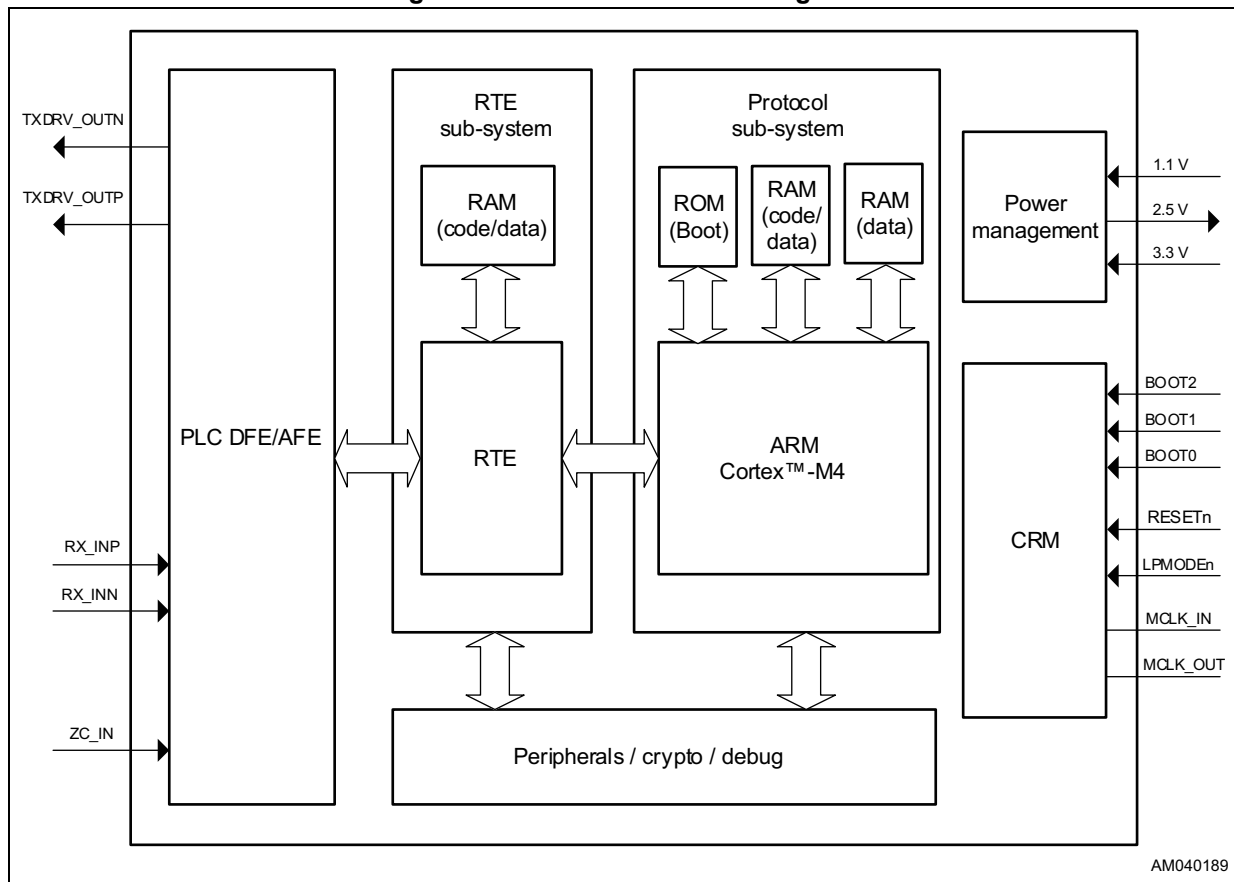
1 Description

The ST8500 is a fully programmable power line communication (PLC) modem System on Chip (SoC), able to run any PLC protocol in the frequency band up to 500 kHz.

The device architecture has been designed to target CENELEC EN50065, FCC and ARIB compliant applications supporting all major PLC protocol standards such as ITU G.9904 (PRIME), ITU G.9903 (G3-PLC[®]) and many other possible PLC protocol specifications and evolutions.

The ST8500 basic block diagram is shown in [Figure 1](#).

Figure 1. ST8500 basic block diagram



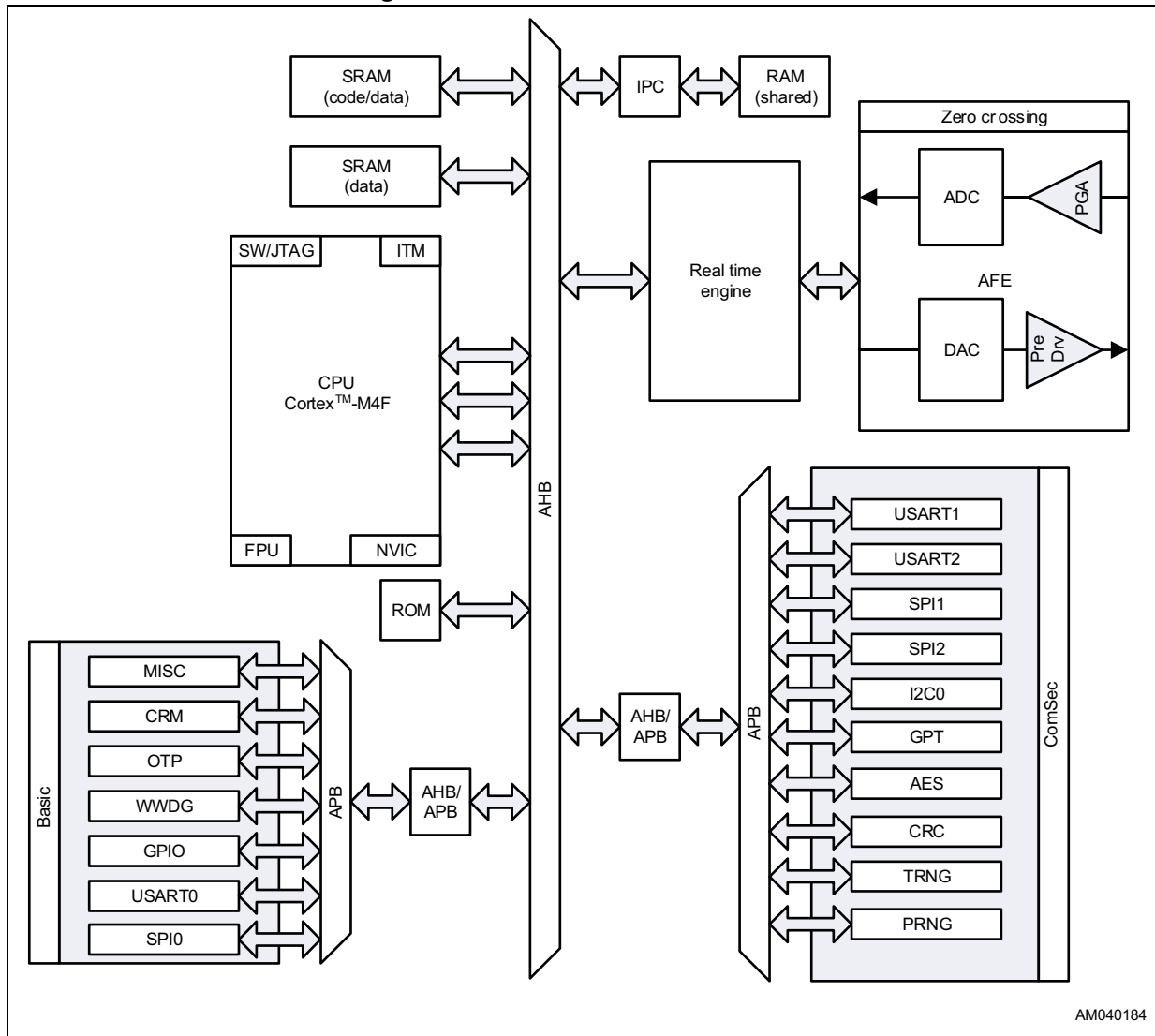
2 Device architecture

The ST8500 architecture is composed of the following parts:

1. PLC front-end including digital front-end (DFE) and analog front-end (AFE)
2. Real-time engine: the digital core running the lower layers of the PLC protocol stack and implementing modulation, demodulation and advanced forward error corrections (FEC) algorithms
3. Protocol engine: the digital core running the upper layers of the PLC protocol stack and managing the interface with external microcontrollers.
4. Peripherals, crypto, debug section
5. Clock and reset section
6. Power management section

The ST8500 detailed architecture is shown in [Figure 2](#).

Figure 2. ST8500 detailed architecture



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2.1 Power line communication (PLC) subsystem

The ST8500 device embeds a fully programmable power line communication subsystem, comprising the RTE, DFE and AFE.

The AFE has been designed for a differential power line interface; however, the single-ended operation is possible for simpler hardware application development.

The DC to 500 kHz signal bandwidth is supported, targeting a number of possible PLC solutions.

2.1.1 Digital front-end (DFE)

Transmission and reception filter chains

The DFE includes programmable transmission/reception digital filter chains to fit the signal bandwidth in different PLC modulation cases. The ADC and DAC clock frequencies are controlled by the DFE to get the right sample rate fitting the filter chain configuration.

Automatic gain control (AGC)

The DFE implements the automatic gain control (AGC) block for the PGA, whose purpose is to adapt the signal to the ADC dynamic range.

2.1.2 Analog front-end (AFE)

Reception chain

The ST8500 AFE features a programmable gain amplifier (PGA) and a dedicated analog-to-digital converter (ADC) to achieve high RX sensitivity and a wide input range.

Transmission chain

The transmitted signal, generated in the digital domain, is fed into a dedicated digital-to-analog converter (DAC).

The DAC output is then fed into a pre-driver for buffering and applying an additional gain.

Zero crossing comparator

The mains line zero crossing can be detected by providing a mains synchronous bipolar (AC) signal at the input of this comparator.

The zero crossing comparator provides positive and negative event information (rising/falling edge or high/low level).

Zero crossing information can also trigger an event for the GPT0 timer in order to capture the zero crossing timestamp for the application purpose.

Line driver thermal sense

The AFE also includes the thermal sense (TS) block to detect the temperature of the line driver.

Line driver current sense

The AFE also includes the current sense (CS) block to detect the output current of the line driver.

2.1.3 Real-time engine (RTE)

To effectively and flexibly target the performance required by different PLC standards, the ST8500 embeds a dedicated high performance fully programmable real-time engine (RTE). It is able to address specific real-time PLC functionalities such as modulation and demodulation according to different modulation schemes, advanced correction coding algorithms (Viterbi, Convolutional, Reed-Solomon, etc.) and several other time-constrained communication services.

2.2 Protocol core subsystem

2.2.1 ARM® Cortex™-M4F core

The Cortex™-M4F processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high end processing the hardware including IEEE754-compliant single precision (32-bit) floating point computation, a range of a single cycle and SIMD multiplication and multiply with accumulate capabilities, saturating arithmetic and dedicated hardware division.

To facilitate the design of cost-sensitive devices, the Cortex™-M4F processor implements tightly coupled system components that reduce the processor area while significantly improving interrupt handling and system debug capabilities. The Cortex™-M4F processor implements a version of the Thumb® instruction set based on the Thumb®-2 technology, ensuring high code density and reduced program memory requirements. The Cortex™-M4F instruction set provides the exceptional performance expected by a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

The Cortex™-M4F processor provides multiple interfaces using the AMBA™ technology to provide high-speed, low latency memory accesses. It supports unaligned data accesses and implements atomic bit manipulation that enables faster peripheral controls, system spinlocks and thread-safe Boolean data handling.

Table 2. Cortex™-M4F core configuration

| Component | Presence | Comment |
|-------------|----------|--|
| MPU_PRESENT | No | Memory protection unit (MPU) is not present |
| NUM_IRQ | N/A | Number of interrupts: 32 |
| LVL_WIDTH | N/A | Interrupt priority width: 3 |
| DEBUG_LVL | N/A | Minimum debug. 2 breakpoints, 1 watchpoint, no Flash patch |
| JTAG | Yes | JTAG-DP is included. The SW-DP is always included. |
| ITM | Yes | Instrumentation Trace Macrocell™ |
| DWT | Yes | Data watchpoint and trace |
| WIC | No | Wake-up interrupt controller (WIC) is not present |
| BB | No | Bit banding region is not present |
| FPU | Yes | Floating point unit present (single precision) |

2.2.2 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (Cortex™-M4F and RTE) and the slaves (RAM, AHB and APB peripherals and real-time engine) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

2.2.3 Debug with serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

2.2.4 Floating point unit (FPU)

The FPU fully supports single precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between the fixed point and floating point data formats, and floating point constant instructions.

The FPU provides floating point operations that are compliant with the NSI/IEEE Std 754-2008 A, IEEE Standard for Binary Floating-point Arithmetic[®], referred to as the IEEE 754 Standard.

The FPU contains 32 single precision extension registers, which can also be accessible as 16 double word registers for load, store, and move operations.

2.2.5 Nested vectored interrupt controller (NVIC)

The ST8500 embeds a NVIC closely integrated with the ARM Cortex™-M4F core. The NVIC is able to handle 32 maskable interrupts. The software priority level is configurable in the range of 0 - 31 for each interrupt. A higher level corresponds to a lower priority, so the level 0 is the highest interrupt priority. In case two or more interrupt lines share the same software priority level, the hardware priority level is used. Interrupt descriptions and hardware priorities are shown in [Table 3](#).

Table 3. Interrupt definition and position

| Position | Hardware priority | Acronym | Description | Offset from VTOR |
|----------|-------------------|------------------|---|------------------|
| - | -3 | Reset | Reset | 0x00000004 |
| - | -2 | NMI | Non maskable interrupt - system error | 0x00000008 |
| - | -1 | HardFault | All class of fault | 0x0000000C |
| - | 0 | MemManage | MPU mismatch | 0x00000010 |
| - | 1 | BusFault | Prefetch fault, memory access fault | 0x00000014 |
| - | 2 | UsageFault | Undefined instruction or illegal state | 0x00000018 |
| - | - | - | Not present | 0x0000001C |
| - | - | - | Not present | 0x00000020 |
| - | - | - | Not present | 0x00000024 |
| - | - | - | Not present | 0x00000028 |
| - | 3 | SVCall | System service call via SWI instruction | 0x0000002C |
| - | 4 | Debug Monitor | Debug monitor | 0x00000030 |
| - | - | - | Not present | 0x00000034 |
| - | 5 | PendSV | Pendable request for system service | 0x00000038 |
| - | 6 | Systick | System tick timer | 0x0000003C |
| 0 | 7 | lpmode_entry_irq | CRM low power mode enter interrupt | 0x00000040 |
| 1 | 8 | lpmode_exit_irq | CRM low power mode exit interrupt | 0x00000044 |

Table 3. Interrupt definition and position (continued)

| Position | Hardware priority | Acronym | Description | Offset from VTOR |
|----------|-------------------|---------------|--|------------------|
| 2 | 9 | crm_error_irq | CRM error interrupt | 0x00000048 |
| 3 | 10 | WWDG | Window watchdog - global interrupt | 0x0000004C |
| 4 | 11 | GPT0 | GPT0 - global interrupt | 0x00000050 |
| 5 | 12 | GPT1 | GPT1 - global interrupt | 0x00000054 |
| 6 | 13 | GPT2 | GPT2 - global interrupt | 0x00000058 |
| 7 | 14 | GPT3 | GPT3 - global interrupt | 0x0000005C |
| 8 | 15 | SPI0 | SPI0 - global interrupt | 0x00000060 |
| 9 | 16 | SPI1 | SPI1 - global interrupt | 0x00000064 |
| 10 | 17 | SPI2 | SPI2 - global interrupt | 0x00000068 |
| 11 | 18 | USART0 | USART0 - global interrupt | 0x0000006C |
| 12 | 19 | USART1 | USART1 - global interrupt | 0x00000070 |
| 13 | 20 | USART2 | USART2 - global interrupt | 0x00000074 |
| 14 | 21 | IPC_mailbox | IPC - mailbox interrupt | 0x00000078 |
| 15 | 22 | IPC_queues | IPC - queues interrupt | 0x0000007C |
| 16 | 23 | IPC_mem | IPC - shared memory Interrupt | 0x00000080 |
| 17 | 24 | I2C_event | I2C0 - global event interrupt | 0x00000084 |
| 18 | 25 | I2C_error | I2C0 - global error interrupt | 0x00000088 |
| 19 | 26 | AES | AES - global interrupt | 0x0000008C |
| 20 | 27 | OTP_error | OTP - global error interrupt | 0x00000090 |
| 21 | 28 | OTP_eoo | OTP - end of operation interrupt | 0x00000094 |
| 22 | 29 | GPIO00 | GPIO00 - global interrupt | 0x00000098 |
| 23 | 30 | GPIO01 | GPIO01 - global interrupt | 0x0000009C |
| 24 | 31 | - | Reserved | 0x000000A0 |
| 25 | 32 | GPIO03 | GPIO03 - global interrupt | 0x000000A4 |
| 26 | 33 | - | Reserved | 0x000000A8 |
| 27 | 34 | - | Reserved | 0x000000AC |
| 28 | 35 | - | Reserved | 0x000000B0 |
| 29 | 36 | FPU | Floating point unit - global interrupt | 0x000000B4 |
| 30 | 37 | - | Reserved | 0x000000B8 |
| 31 | 38 | - | Reserved | 0x000000BC |

2.2.6 General-purpose input/outputs (GPIOs)

The ST8500 device has 3 GPIOs ports named GPIO00, GPIO01 and GPIO03. Each port can control 8 pins. Each GPIO pin can be individually configured by software as output (push-pull or open drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate functions (with or without pull-up or pull-down).

The GPIO03 port exports system defined functionalities such as boot mode selection and JTAG that the running code can overwrite after the bootloader has left the control to it. The final system design must take care of this special configuration.

External interrupt

Each GPIOs port can generate interrupts depending on a level (low and high), or a transactional value of the pin (rising or falling edge). For each port, one interrupt line is dedicated. The pins of one port share the same interrupt line.

2.2.7 General-purpose timer (GPT)

There are 4 general-purpose timers (GPT0 to GPT3) embedded in the ST8500.

GPTs have a 32-bit auto-reload up/downcounter and a 32-bit pre-scaler. The counters can be frozen in debug mode.

The GPT0 timer is also connected to the zero crossing comparator so it is able to record the timestamp of the ZC event.

2.2.8 Window Watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.2.9 SysTick timer

The Cortex™-M4F has a 24-bit system timer, SysTick, which counts down from the programmable reload value to zero. It supports the auto-reload and can generate a maskable system interrupt when the counter reaches zero.

2.2.10 Universal synchronous/asynchronous receiver transmitters (USART)

The ST8500 device has two embedded universal synchronous/asynchronous receiver transmitters (USART0 to USART1) and one embedded universal asynchronous receiver transmitter (USART2).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode; they have the LIN Master/Slave capability, Smart card mode (ISO 7816 compliant) and SPI-like communication capability.

They provide hardware management of the CTS and RTS signals and the RS485 driver enable. The maximum communication speed is up to 1 Mbit/s.

All USARTs have a clock domain (ICLK) independent from the Cortex™ clock (PCLK).

2.2.11 Serial peripheral interface (SPI)

Three SPI interfaces (SPI0 to SPI2) allow communication up to 50 Mbit/s in master and up to 24 Mbit/s slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit pre-scaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

2.2.12 Inter-integrated circuit interface (I²C)

The ST8500 device embeds one I²C. The I²C bus interface handles communications between the device and the serial I²C bus. It controls all I²C bus-specific sequencing, protocol, arbitration and timing. In addition to receiving and transmitting data, this interface converts it from the serial to the parallel format and vice versa. The interrupts are enabled or disabled by software. The interface is connected to the I²C bus by a data pin (SDA) and by a clock pin (SCL).

The I²C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
 - Slave and master modes, multimaster capability
 - Standard-mode (Sm), with a bitrate up to 100 kbit/s
 - Fast-mode (Fm), with a bitrate up to 400 kbit/s
 - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
 - Programmable setup and hold times
 - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
 - Hardware PEC (packet error checking) generation and verification with ACK control
 - Address resolution protocol (ARP) support
 - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock (ICLK): a choice of independent clock sources allowing the I²C communication speed to be independent from the PCLK clock reprogramming.
- Programmable analog and digital noise filters

2.2.13 AES engine

The ST8500 embeds a hardware AES peripheral that implements an advanced standard cryptographic algorithm according to the NIST FIPS 197. The block processes 128-bit data blocks using a key with the following possible sizes: 128, 192, 256 bits. The peripheral also supports the following modes: “Electronic Code Book” (ECB), “Cipher Block Chaining” (CBC), “Counter mode” (CTR), “Galois/Counter Mode” (GCM), GMAC and CCM modes.

The peripheral is able to encrypt and decrypt data. Interrupt can be generated when one operation is finished.

2.2.14 True random number generator (TRNG)

The ST8500 embeds a TRNG processor based on a continuous analog noise that provides a random 16-bit value. To avoid pseudo random sequences, two consecutive accesses have to be performed when the ready bit in the status register is set to 1.

2.2.15 Pseudo random number generator (PRNG)

The ST8500 embeds a PRNG processor that provides a pseudo random 32-bit value. Initial seed can be configured by software.

2.2.16 CRC (cyclic redundancy check) calculation unit

The cyclic redundancy check (CRC) is a widely used method for detecting errors. The CRC calculation unit is used to get a CRC code in a flexible way using a configurable polynomial. The output data size can be selected between 8, 16, 24 or 32 bits.

The input data size can be configured between 1, 8, 16, 24 or 32 bits with selectable bit and byte endianness.

The CRC unit allows the specification of the initial value (all zero, all one, or a generic value) and the possibility to select an automatic XOR with all one when reading the data output.

2.3 Inter-processor communication (IPC)

The Cortex™-M4 core and the real-time engine (RTE) communicate by means of an additional 8-kByte shared static RAM. This memory can be accessed by the two cores through an interprocessor communication block that guarantees coherent and consistent read and modify operations, to provide several functionalities to the system, among the others:

- Configuration of real-time engine modes and functionalities during the normal working operations
- Data and information exchange between the Cortex™-M4 and real-time engine in both directions.

2.4 Cortex™ memories

2.4.1 Embedded SRAM (instruction and data)

The ST8500 device embeds 256 kByte of the SRAM for a fast code execution. This SRAM can be used also to store data with penalties in the concurrent instruction and data access. The data SRAM start address is 0x00050000, the end address is 0x0008FFFF.

2.4.2 Embedded SRAM (data only)

The ST8500 device embeds 96 kBytes of the SRAM for data management. The Cortex™-M4 can perform byte, half word (16 bits) or full word (32 bits) access to the SRAM at maximum speed, with zero wait states for both read and write operations. The data SRAM start address is 0x00090000, the end address is 0x000A7FFF.

2.4.3 Embedded ROM

The ST8500 device embeds a ROM memory used to store the bootloader program written during the device production phase.

2.4.4 One Time Programmable (OTP) section

The ST8500 device embeds an OTP area that stores device sensitive information, security control bits and additional user specific bytes. The OTP section has two different HW protection methods, ECC or HW redundancy, as indicated in [Table 4](#).

Table 4. OTP section

| Word | Word size | Protection | Description |
|------|-----------|---------------|--|
| 0 | 16 bits | HW redundancy | User security bits: b0: Cortex™-M4F images in clear text enabled b1: Cortex™-M4F JTAG enabled b2: user OTP write locked b3: Cortex™-M4F key read locked b4-15: reserved |
| 1 | 32 bits | ECC | Cortex™-M4F image decryption key word0 |
| 2 | 32 bits | ECC | Cortex™-M4F image decryption key word1 |
| 3 | 32 bits | ECC | Cortex™-M4F image decryption key word2 |
| 4 | 32 bits | ECC | Cortex™-M4F image decryption key word3 |
| 5 | 32 bits | ECC | Cortex™-M4F image decryption key word4 |
| 6 | 32 bits | ECC | Cortex™-M4F image decryption key word5 |
| 7 | 32 bits | ECC | Cortex™-M4F image decryption key word6 |
| 8 | 32 bits | ECC | Cortex™-M4F image decryption key word7 |
| 9 | 32 bits | ECC | User specific word 0 |
| 10 | 32 bits | ECC | User specific word 1 |
| 11 | 32 bits | ECC | User specific word 2 |
| 12 | 32 bits | ECC | User specific word 3 |

The ECC calculation unit improves robustness of data storage. This ECC block encodes and decodes each 32-bits words in programming and reading operations. The user must program all the ECC protected words in one shot, no modification is possible afterward.

The HW redundancy is a more flexible protection mechanism but limits the size of each word to 16-bits. The user can write words in multiple shots but respecting this rule: the word value can be changed only making '0's becoming '1's (in no case single bits can be written back at 0).

2.5 Clock and reset management (CRM)

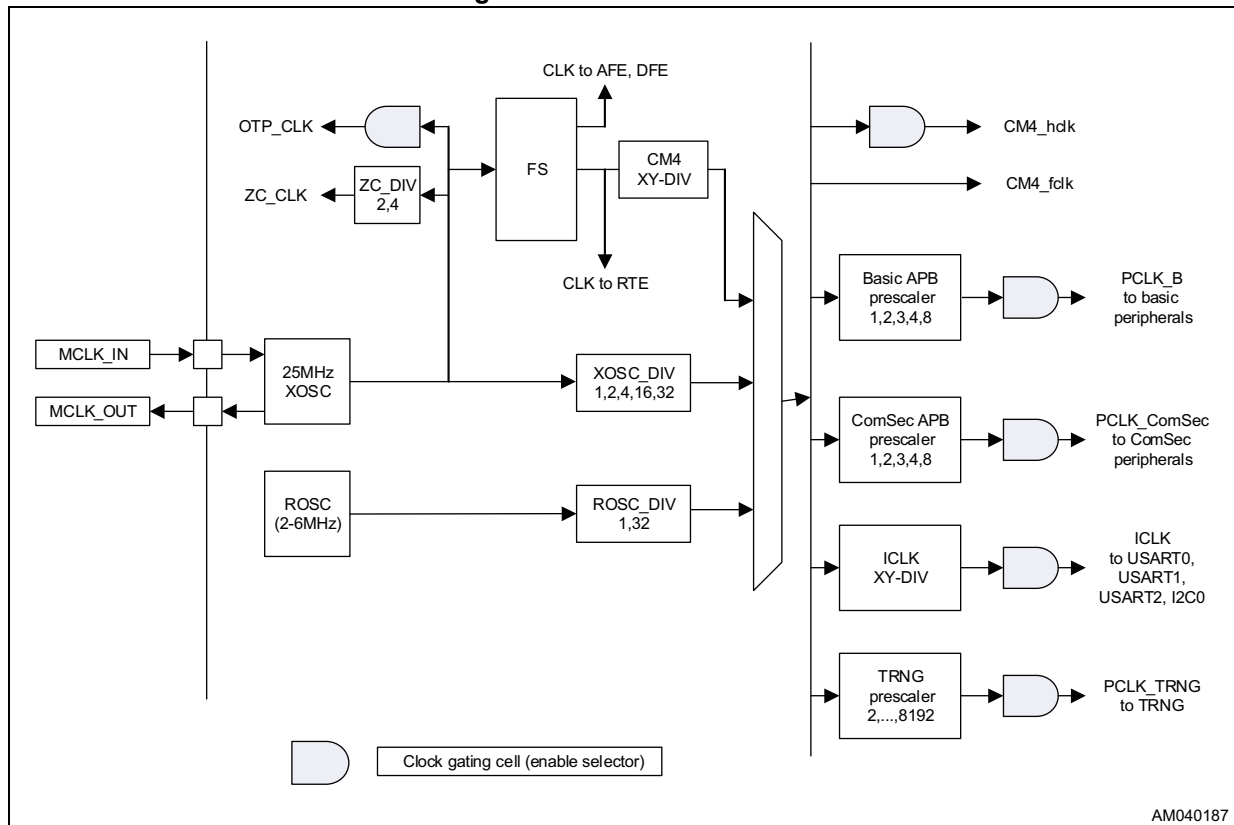
2.5.1 Clock management

ST8500 internal clock signals can be generated from two different clock sources:

1. An external 25 MHz that must be provided through a crystal connected to MCLK_IN and MCLK_OUT pins. If this source is not present the device does not start in order to respect the security requirements.
2. An internal ring oscillator with 4 MHz nominal frequency.

The clock strategy and distribution is depicted in [Figure 3](#).

Figure 3. ST8500 clock tree



At the power-on the Cortex™-M4F directly uses the XOSC clock with the SLOW mode. The internal frequency synthesizer (FS) and pre-scaler units generate all the needed internal clock signals. The frequency synthesizer generates a fixed frequency at a nominal frequency of 400 MHz (VCO). This frequency is pre-scaled at boot time to provide the proper clock for DFE, AFE and RTE subsystems.

The application code can select the clock source for the Cortex™-M4 subsystem between:

1. The VCO output of FS by means of a programmable pre-scaler. The application core must properly configure it to provide the clock in the range from 1.5 MHz to 200 MHz.
2. The 25 MHz oscillator by means of a programmable pre-scaler at a nominal frequency ranging from 0.8 MHz up to 25 MHz.
3. The internal ring oscillator, either directly (at a nominal frequency 4 MHz) or by means of a fixed pre-scaler (at a nominal frequency of 0.125 MHz).

Each APB bus can be fed at an integer fraction of the Cortex™-M4F clock with a prescaling factor up to 8. The application core must configure the APB clock to respect the maximum limit of 100 MHz. USART and I²C peripherals have an independent clock divider to generate the proper baudrate and clock on the line.

It is also possible to apply clock gating to each bus in case of low power mode or unused peripherals. Clock gating can be applied to clock signals as indicated in [Figure 3](#).

2.5.2 Reset management

The power-on-reset (POR) is conditioned by the level of the required supply voltages (3.3 V, 2.5 V and 1.1 V, see [Section 2.6](#)). At the power-on, the whole ST8500 is kept under reset until the supply voltages are above the respective turn-on thresholds, while the device is turned off as soon as one of the supply voltages fall below the respective turn-off thresholds.

The system reset is generated by:

- The RESETn pin (active low)
- The Cortex™-M4F core that can assert a system software reset
- The window watchdog (see [Section 2.2.8 on page 11](#))

The software reset to single peripherals can be forced through CRM registers.

2.6 Power management

The ST8500 shall be powered by at least two external supply voltages:

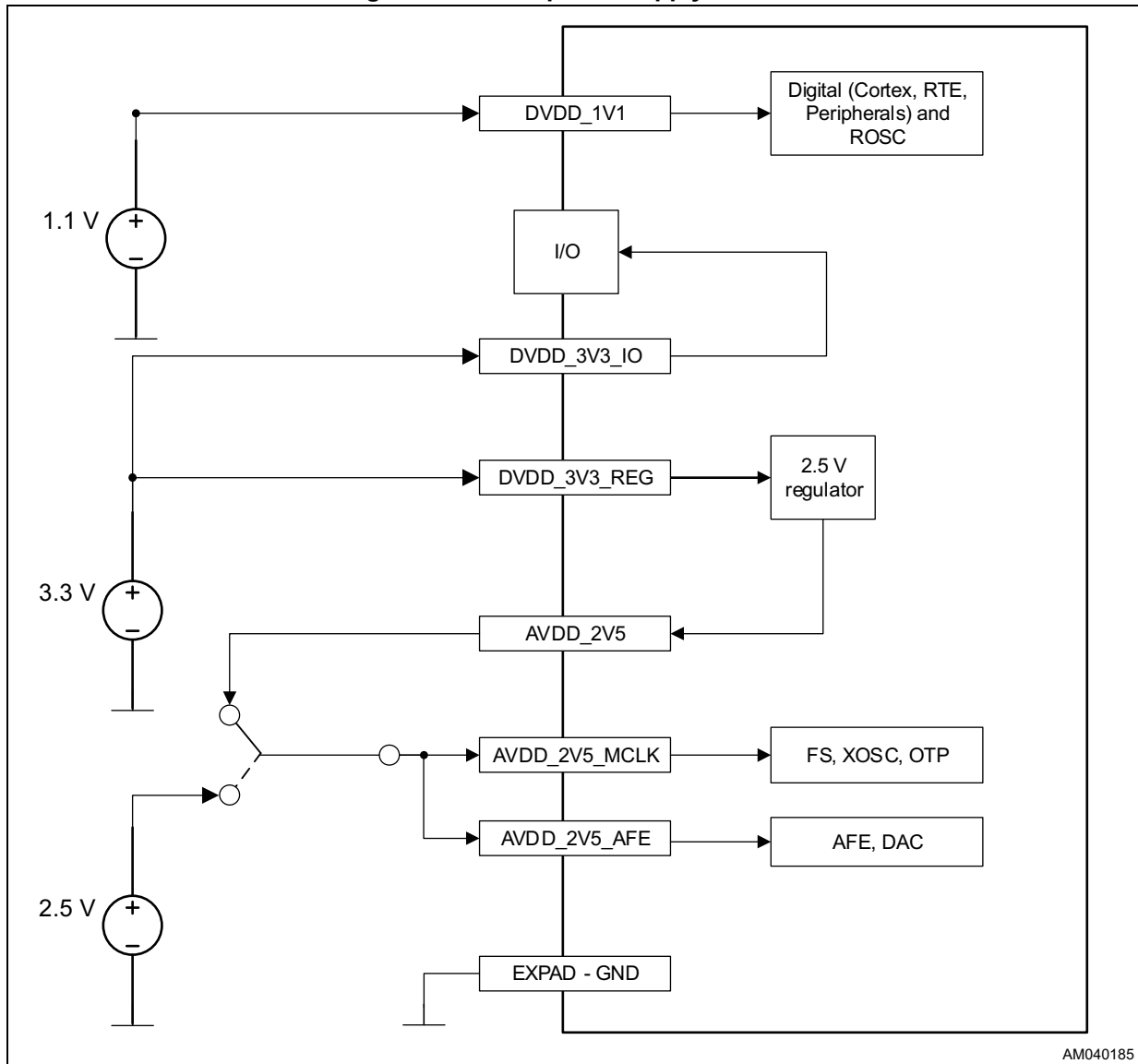
- 3.3 V for I/Os and TX driver
- 1.1 V for the digital part and memories

The device needs also an analog 2.5 V supply that can be either internally generated through an LDO from the 3.3 V supply, or externally supplied.

The internal regulator connected to AVDD_2V5 is not designed to supply external circuitry; its output is externally accessible for filtering the purpose only.

The only ground reference of the device is the exposed pad (EXPAD-GND). It has to be properly soldered to a ground pad on the application PCB.

Figure 4. ST8500 power supply scheme



2.6.1 External power supply dimensioning

To cover all possible corner cases, the external power supply peak capability should take into account the values provided in [Table 5](#).

Table 5. Power supply peak consumption

| Power supply rails | Conditions | Value | Unit |
|--------------------|---|-------|------|
| 1.1 V supply rail | Full temperature range, maximum clock frequencies | 420 | mW |
| 3.3 V supply rail | | 320 | mW |

2.6.2 System power modes and low-power mode

In order to fine-tune the power consumption, the ST8500 device supports different power modes. Based on the selected clock source (see [Section 2.5](#)) the Cortex™-M4 can select the system power mode between:

- NORMAL mode: the system is clocked by the VCO output frequency of the FS (with prescaling factor)
- SLOW mode: the system is clocked directly by the XOSC frequency
- DOZE mode: the system is clocked by the ROSC oscillator
- LOW-POWER mode: the system is clocked by the ROSC oscillator and additional power saving strategies can be applied.

In NORMAL mode, the Cortex™-M4 is able to run at its maximum frequency but, in case lower speed is sufficient to meet the application requirements, its clock frequency can be scaled down to reduce power consumption, while AFE, DFE and RTE frequencies are always internally selected to meet the running PLC protocol requirements. In case PLC connectivity is temporarily not required, the Cortex™-M4 can be put in SLOW (depending on the computational power and power consumption required) turning off the frequency synthesizer (and all the derived clock signals). When in DOZE mode also the XOSC block can be turned off.

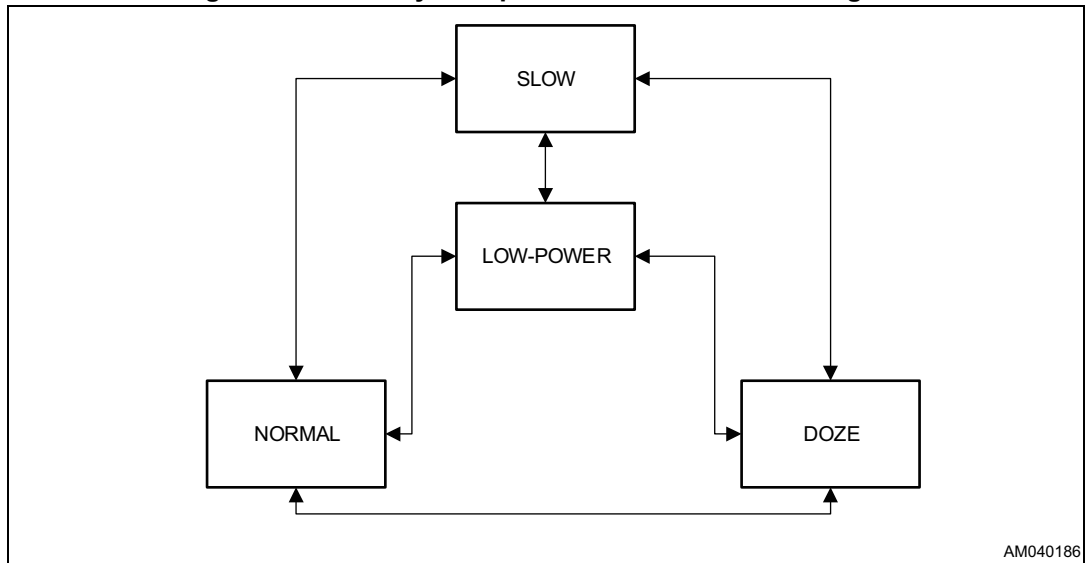
An additional LOW-POWER mode is present. In this mode it is possible to define which power reduction strategies are put in place by the means of a software selectable mask which can:

- Disable the AFE analog blocks
- Disable the external clock sources (XOSC and FS)
- Apply clock gating to all the digital blocks including the CPU
- Power down the SRAM memories

The LOW-POWER can be selected by the Cortex™-M4F or by an external controller with a dedicated pin (LPMODEn, active low). The exit from LOW-POWER mode is controlled by the Cortex™-M4, by LPMODEn pin, by internal GPT0 timer tick. During LOW-POWER mode the content of SRAM memories is still valid and accessible by cores if not put in power-down.

[Figure 5](#) shows the possible transitions between power system modes.

Figure 5. ST8500 system power modes transition diagram



AM040186

Clock gating is available in any modes for peripherals and clock sources in order to save all the dynamic power contributions related to the resources not used by the application.

2.7 Boot modes and system programmability

ST8500 boot mode is defined by the status of the three pins GPIO3_0/BOOT0, GPIO3_1/BOOT1, GPIO3_2/BOOT2 when the device awakes from a reset condition (either power-on, hardware or software reset), the correspondence between the value of BOOTx pins and the boot mode is shown in [Table 6](#).

Table 6. Boot modes selection

| Boot pins | | | Boot mode |
|-----------|-------|-------|--|
| BOOT2 | BOOT1 | BOOT0 | |
| 0 | 0 | 0 | Boot from UART host interface |
| 0 | 0 | 1 | Boot from SPI host interface |
| 0 | 1 | 0 | Boot from SPI external Flash (large configuration) |
| 0 | 1 | 1 | Boot from SPI external Flash (small configuration) |
| 1 | 0 | 0 | Reserved1 |
| 1 | 0 | 1 | Reserved1 |
| 1 | 1 | 0 | Reserved1 |
| 1 | 1 | 1 | Reserved2 |

The application and RTE codes can be either downloaded by the external host (through SPI or UART interface) or written as binary images on one external SPI Flash (either up to 4 Mbit for the small configuration or from 8 Mbit for the large configuration). The internal bootloader takes the responsibility to load the codes in the proper cores and to start running them. If “Reserved2” mode is selected an endless loop is performed. If one of the

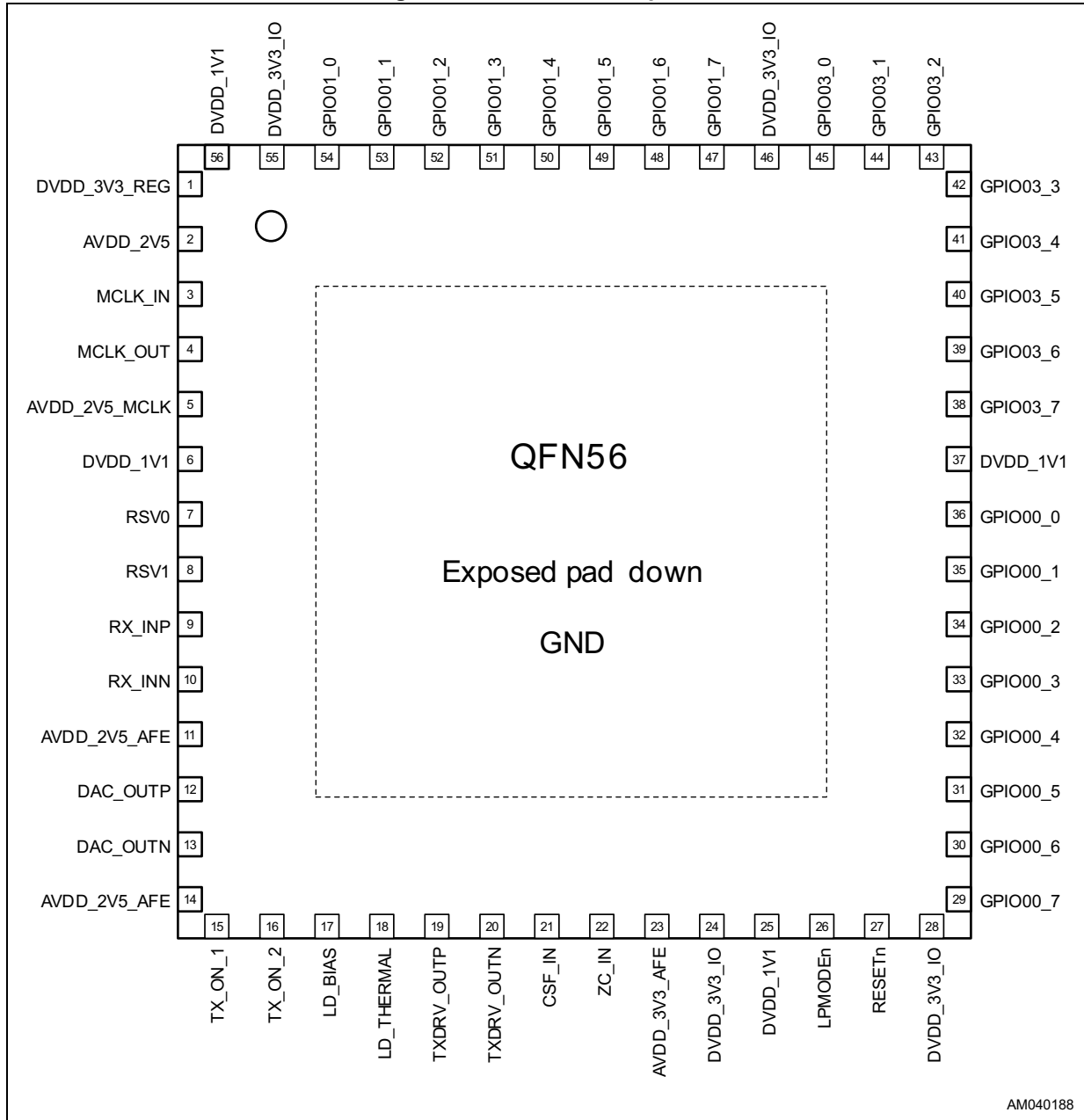
“Reserved1” modes is selected the bootloader automatically jumps to the RAM code starting address. In this case, the user can access to the device through the JTAG if not locked.

The system JTAG is not accessible during the execution of the bootloader procedure. At the end of the bootloader, it becomes accessible. It is also possible by means of an appropriate user security bit in the OTP memory (see [Section 2.4.4 on page 14](#)), to keep the JTAG port locked even after the boot procedure, to avoid unwanted accesses to the core and memories.

3 Pinout and pin description

3.1 Pin definition

Figure 6. ST8500 QFN56 pinout



AM040188

Table 7. Pin description

| QFN56 pin | Pin name | Type | RS | Description |
|-----------|---------------|------|------|--|
| 1 | DVDD_3V3_REG | S | - | 3.3 V input for the 2.5 V regulator |
| 2 | AVDD_2V5 | S | - | 2.5 V regulator output |
| 3 | MCLK_IN | A | - | 25 MHz oscillator input |
| 4 | MCLK_OUT | A | - | 25 MHz oscillator output |
| 5 | AVDD_2V5_MCLK | S | - | FS and oscillator 2.5 V supply |
| 6 | DVDD_1V1 | S | - | Digital block (FS and oscillator) 1.1 V supply |
| 7 | RSV0 | - | - | Connect to GND |
| 8 | RSV1 | - | - | Connect to GND |
| 9 | RX_INP | A | I | PGA positive input |
| 10 | RX_INN | A | I | PGA negative input |
| 11 | AVDD_2V5_AFE | S | - | AFE (PGA) 2.5 V supply |
| 12 | DAC_OUTP | A | O | Transmission DAC positive output |
| 13 | DAC_OUTN | A | O | Transmission DAC negative output |
| 14 | AVDD_2V5_AFE | S | - | AFE (DAC) 2.5 V supply |
| 15 | TX_ON_1 | A | O | TX enable power amplifier 1 |
| 16 | TX_ON_2 | A | O | TX enable power amplifier 2 |
| 17 | LD_BIAS | A | O | Line driver bias current |
| 18 | LD_THERMAL | A | I | Line driver temperature sense |
| 19 | TXDRV_OUTP | A | O | Transmission pre-driver positive output |
| 20 | TXDRV_OUTN | A | O | Transmission pre-driver negative output |
| 21 | CSF_IN | A | I | Line driver current sense feedback input |
| 22 | ZC_IN | A | I | Zero crossing comparator input |
| 23 | AVDD_3V3_AFE | S | - | Transmission pre-driver 3.3 V supply |
| 24 | DVDD_3V3_IO | S | - | I/O 3.3 V supply |
| 25 | DVDD_1V1 | S | - | Digital block 1.1 V supply |
| 26 | LPMODEn | D | I PU | LOW-POWER mode enable (active low) |
| 27 | RESETn | D | I PU | Reset (active low) |
| 28 | DVDD_3V3_IO | S | - | I/O 3.3 V supply |
| 29 | GPIO00_7 | D | I PU | General purpose I/O |
| 30 | GPIO00_6 | D | I PU | General purpose I/O |
| 31 | GPIO00_5 | D | I PU | General purpose I/O |
| 32 | GPIO00_4 | D | I PD | General purpose I/O |
| 33 | GPIO00_3 | D | I PU | General purpose I/O |
| 34 | GPIO00_2 | D | I PD | General purpose I/O |
| 35 | GPIO00_1 | D | I PU | General purpose I/O |

Table 7. Pin description (continued)

| QFN56 pin | Pin name | Type | RS | Description |
|-----------|-------------|--------|------|----------------------------|
| 36 | GPIO00_0 | D | I PU | General purpose I/O |
| 37 | DVDD_1V1 | S | - | Digital block 1.1 V supply |
| 38 | GPIO03_7 | D | I PU | General purpose I/O (JTAG) |
| 39 | GPIO03_6 | D | I PU | General purpose I/O (JTAG) |
| 40 | GPIO03_5 | D | I PU | General purpose I/O (JTAG) |
| 41 | GPIO03_4 | D | I PD | General purpose I/O (JTAG) |
| 42 | GPIO03_3 | D | I PU | General purpose I/O (JTAG) |
| 43 | GPIO03_2 | D | I PD | General purpose I/O (Boot) |
| 44 | GPIO03_1 | D | I PD | General purpose I/O (Boot) |
| 45 | GPIO03_0 | D | I PD | General purpose I/O (Boot) |
| 46 | DVDD_3V3_IO | S | - | I/O 3.3 V supply |
| 47 | GPIO01_7 | D(I2C) | I PU | General purpose I/O |
| 48 | GPIO01_6 | D(I2C) | I PU | General purpose I/O |
| 49 | GPIO01_5 | D | I PD | General purpose I/O |
| 50 | GPIO01_4 | D | I PD | General purpose I/O |
| 51 | GPIO01_3 | D | I PU | General purpose I/O |
| 52 | GPIO01_2 | D | I PU | General purpose I/O |
| 53 | GPIO01_1 | D | I PU | General purpose I/O |
| 54 | GPIO01_0 | D | I PD | General purpose I/O |
| 55 | DVDD_3V3_IO | S | - | I/O 3.3 V supply |
| 56 | DVDD_1V1 | S | - | Digital block 1.1 V supply |
| 57 | EXPAD-GND | S | - | Exposed pad - GND |

3.2 GPIOs multiplexing scheme

In the ST8500 device, peripherals are connected to I/Os through a multiplexer. At a given time, each I/O can be controlled by only one single peripheral. In this way, there is no conflict between peripherals sharing the same I/O pins.

Thanks to a set of configuration registers, the user can select one of the three possible alternate functions for each pin as described in [Table 8](#).

Table 8. GPIOs multiplexing scheme

| Pin name | Selection: 11 | Selection: 00 | Selection: 01 | Selection: 10 |
|----------|---------------|------------------------|----------------------|---------------|
| GPIO00_0 | Input/output | USART1_RX | SPI2_SCLK | RESERVED |
| GPIO00_1 | Input/output | USART1_TX | SPI2_MOSI | RESERVED |
| GPIO00_2 | Input/output | USART1_RTS | SPI2_SS _n | RESERVED |
| GPIO00_3 | Input/output | USART1_CTS | SPI2_MISO | RESERVED |
| GPIO00_4 | Input/output | USART0_RX | SPI0_SCLK | RESERVED |
| GPIO00_5 | Input/output | USART0_TX | SPI0_MOSI | RESERVED |
| GPIO00_6 | Input/output | USART0_RTS | SPI0_SS _n | RESERVED |
| GPIO00_7 | Input/output | USART0_CTS | SPI0_MISO | RESERVED |
| GPIO01_0 | Input/output | SPI1_SCLK | - | RESERVED |
| GPIO01_1 | Input/output | SPI1_MOSI | - | RESERVED |
| GPIO01_2 | Input/output | SPI1_SS _n | USART0_SCLK | RESERVED |
| GPIO01_3 | Input/output | SPI1_MISO | - | RESERVED |
| GPIO01_4 | Input/output | USART2_RX | I2C0_SMBA | RESERVED |
| GPIO01_5 | Input/output | USART2_TX | USART1_SCLK | RESERVED |
| GPIO01_6 | Input/output | USART2_RTS | I2C0_SDA | RESERVED |
| GPIO01_7 | Input/output | USART2_CTS | I2C0_SCL | RESERVED |
| GPIO03_0 | Input/output | BOOT0 | - | RESERVED |
| GPIO03_1 | Input/output | BOOT1 | - | RESERVED |
| GPIO03_2 | Input/output | BOOT2 | - | RESERVED |
| GPIO03_3 | Input/output | JTAG_TMS/SWIO | - | RESERVED |
| GPIO03_4 | Input/output | JTAG_TCK/SWCLK | - | RESERVED |
| GPIO03_5 | Input/output | JTAG_TDO/SWV | - | RESERVED |
| GPIO03_6 | Input/output | JTAG_TRST _n | - | RESERVED |
| GPIO03_7 | Input/output | JTAG_TDI | - | RESERVED |

4 Memory map

Figure 7. ST8500 memory map

| | | |
|------------|----------------------|----------|
| 0x4001C000 | ComSec | PRNG |
| 0x4001B000 | | TRNG |
| 0x4001A000 | | AES |
| 0x40019000 | | CRC |
| 0x40018000 | | GPT3 |
| 0x40017000 | | GPT2 |
| 0x40016000 | | GPT1 |
| 0x40015000 | | GPT0 |
| 0x40014000 | | I2C0 |
| 0x40013000 | | USART2 |
| 0x40012000 | | USART1 |
| 0x40011000 | | SPI2 |
| 0x40010000 | | SPI1 |
| 0x4000A000 | Reserved | |
| 0x40009000 | Basic | GPIO03 |
| 0x40008000 | | Reserved |
| 0x40007000 | | GPIO01 |
| 0x40006000 | | GPIO00 |
| 0x40005000 | | OTP |
| 0x40004000 | | MISC |
| 0x40003000 | | CRM |
| 0x40002000 | | WWDG |
| 0x40001000 | | USART0 |
| 0x40000000 | | SPIO |
| 0x20023000 | Reserved | |
| 0x20022FFF | IPC | |
| 0x20022000 | SRAM (IPC) | |
| 0x20021FFF | SRAM (IPC) | |
| 0x20020000 | SRAM (IPC) | |
| | Reserved | |
| 0x000A7FFF | SRAM (data) | |
| 0x00090000 | SRAM (data) | |
| 0x0008FFFF | SRAM (code and data) | |
| 0x00050000 | SRAM (code and data) | |
| 0x0004FFFF | SRAM (code and data) | |
| 0x00000000 | Reserved | |

5 Electrical characteristics

5.1 Absolute maximum ratings

Table 9. Absolute maximum ratings - voltage

| Symbol | Parameter | Min. | Max. | Unit |
|---|--|-----------|---------------------------------|------|
| AVDD_2V5 | 2.5 V internal regulator voltage range | GND - 0.3 | 3.9 | V |
| AVDD_2V5_AFE | 2.5 V PLC AFE supply voltage range | GND - 0.3 | 3.9 | V |
| AVDD_3V3_AFE | 3.3 V PLC AFE supply voltage range | GND - 0.3 | 3.9 | V |
| DVDD_3V3_IO | 3.3 V I/O supply voltage range | GND - 0.3 | 3.9 | V |
| AVDD_2V5_MCLK | 2.5 V MCLK supply voltage range | GND - 0.3 | 3.9 | V |
| DVDD_1V1 | 1.1 V digital block supply voltage | GND - 0.3 | 1.5 | V |
| V(DIG_IN) | Digital pin input voltage range | GND - 0.3 | Min. (3.9, DVDD_3V3_IO+0.3) | V |
| V(MCLK) | 25 MHz oscillator pins voltage range | GND - 0.3 | Min. (3.9, DVDD_3V3_IO + 0.3) | V |
| RX_IN | RX_IN pins voltage range | -2.5 | 5 | V |
| DAC_OUT | DAC output pins voltage range | GND - 0.3 | Min. (3.9, AVDD_2.5V_AFE + 0.3) | V |
| ZC_IN | ZC_IN pin voltage range | -3.3 | Min. (3.9, AVDD_3V3_AFE + 0.3) | V |
| CSF_IN, TX_ON, LD_BIAS, LD_THERMAL, TXDRV_OUT | All other analog pins voltage range | GND - 0.3 | Min. (3.9, AVDD_3V3_AFE + 0.3) | V |
| V(ESD) | Maximum withstanding voltage range test condition: ANSI-ESDA-JEDEC JS-001 "human body model" acceptance criteria: "normal performance" | -2 | +2 | kV |

5.2 Thermal characteristics

Table 10. Thermal characteristics

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|--------|-------------------------------|------------|------|------|------|
| T(J) | Junction temperature | - | | 125 | °C |
| T(AMB) | Operating ambient temperature | - | -40 | 105 | °C |
| T(STG) | Storage temperature | - | -50 | 150 | °C |

5.3 Operating conditions

T(AMB) = -40 to +105 °C, T(J) < 125 °C unless otherwise specified.

Power supply characteristics

Table 11. Analog supply characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|--|------|------|------|------|
| V(AVDD_2V5) | 2.5 V regulator output | - | 2.3 | 2.5 | 2.75 | V |
| V(DVDD_3V3_REG) | 2.5 V regulator input voltage | - | 3 | 3.3 | 3.6 | V |
| I(DVDD_3V3_REG) | 2.5 V regulator quiescent current | - | - | - | 1.5 | mA |
| V(AVDD_2V5_AFE)_TH | 2.5 V PLC AFE supply voltage turn-on threshold | - | - | 2.1 | 2.25 | V |
| V(AVDD_2V5_AFE)_TL | 2.5 V PLC AFE supply voltage turn-off threshold | - | 1.8 | 1.9 | - | V |
| V(AVDD_2V5_AFE)_HYST | 2.5 V PLC AFE supply voltage hysteresis | - | - | 200 | - | mV |
| I(AVDD_2V5_AFE)_RX | 2.5 V PLC AFE supply current in Rx mode | - | - | 6.5 | 7.5 | mA |
| I(AVDD_2V5_AFE)_TX | 2.5 V PLC AFE (PGA and DAC) supply current in Tx mode | DAC full scale current = 10 mA Fclk: 20 MHz | - | 10 | - | mA |
| I(AVDD_3V3_AFE)_RX | 3.3 V PLC AFE supply current in Rx mode | - | - | 0.03 | 0.1 | mA |
| I(AVDD_3V3_AFE)_TX | 3.3 V PLC AFE supply current in Tx mode | TXDRV_OUT pins with no load | - | 3 | 5 | mA |
| V(DVDD_3V3_IO) | Digital I/O supply voltage | - | 3.0 | 3.3 | 3.6 | V |
| V(DVDD_3V3_IO)_TH | Digital I/O supply voltage turn-on threshold | - | - | 2.7 | 2.85 | V |
| V(DVDD_3V3_IO)_TL | Digital I/O supply voltage turn-off threshold | - | 2.4 | 2.5 | - | V |
| V(DVDD_3V3_IO)_HYST | Digital I/O supply voltage hysteresis | - | - | 200 | - | mV |
| V(DVDD_1V1) | 1.1 digital block supply | - | 1.05 | 1.1 | 1.21 | V |
| V(DVDD_1V1)_TH | 1.1 supply voltage turn-on threshold | - | - | 0.93 | 1.03 | V |
| V(DVDD_1V1)_TL | 1.1 supply voltage turn-off threshold | - | 0.65 | 0.73 | - | V |
| V(DVDD_1V1)_HYST | 1.1 supply voltage hysteresis | - | - | 200 | - | mV |

Table 12. Digital supply characteristics - RTE

| Symbol | Parameter | Conditions ⁽¹⁾ | Min. | Typ. | Max. | Unit |
|-------------|------------------------------|---------------------------|------|------|------|------|
| I(DVDD_1V1) | 1.1 V digital supply current | RTE frequency = 50 MHz | - | 3 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | RTE frequency = 120 MHz | - | 36 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | RTE frequency = 250 MHz | - | 60 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | RTE frequency = 400 MHz | - | 128 | - | mA |

1. The tests are performed with the following enabled blocks: 1 x GPT, 1 x SPI, 1 x USART, IPC, AES, TRNG, ROSC. Cortex™ frequency equals to 100 MHz. The value is calculated by measuring the difference in the supply current with and without RTE enabled and running.

Table 13. Digital supply characteristics - Cortex™-M4

| Symbol | Parameter | Conditions ⁽¹⁾ | Min. | Typ. | Max. | Unit |
|-------------|------------------------------|-----------------------------|------|------|------|------|
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ frequency = 50 MHz | - | 20 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ frequency = 100 MHz | - | 32 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ frequency = 200 MHz | - | 38 | - | mA |

1. The tests are performed with the following enabled blocks: 1 x GPT, 1 x SPI, 1 x USART, IPC, AES, TRNG, ROSC.

Table 14. Digital supply characteristics - low power modes

| Symbol | Parameter | Conditions ⁽¹⁾ | Min. | Typ. | Max. | Unit |
|-------------|------------------------------|---|------|------|------|------|
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ in SLOW, clock fed by 25 MHz XOSC | - | 9 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ in DOZE or LOW-POWER, clock fed by ROSC | - | 7.5 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ in LOW-POWER mode, clock fed by ROSC, AFE disabled | - | 7.5 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ in LOW-POWER mode, clock fed by ROSC, external clock sources disabled | - | 7.5 | - | mA |
| I(DVDD_1V1) | 1.1 V digital supply current | Cortex™ in LOW-POWER mode, clock fed by ROSC, all digital blocks disabled but Cortex™ | - | 7.5 | - | mA |

1. The tests are performed with the following enabled blocks: 1 x GPT, 1 x SPI, 1 x USART, IPC, AES, TRNG, ROSC.

Table 15. Supply characteristics - oscillator and clock

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------|--|-----------------------|------|------|------|------|
| I(DVDD_2V5_MCLK) | FS current consumption from 2.5 V power supply | Master clock - 25 MHz | - | 1.8 | 2.5 | mA |
| I(DVDD_1V1) | FS current consumption from 1.1 V power supply | Master clock - 25 MHz | - | 3.5 | 5 | mA |
| I(DVDD_2V5_MCLK) | XOSC current consumption from 2.5 V power supply | Master clock - 25 MHz | - | 0.5 | 1 | mA |
| I(DVDD_1V1) | ROSC current consumption from 1V1 power supply | Master clock - 25 MHz | - | 0.15 | 1.5 | mA |

Table 16. Digital supply characteristics - I/O

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------|--|--|------|------|------|------|
| I(DVDD_3V3_IO) | 3.3 V digital supply current consumption | 8 GPIO toggling at 0.5 MHz with $C_{ext} \cong 50$ pF see ⁽¹⁾ | - | 2.8 | 6 | mA |
| I(DVDD_3V3_IO) | 3.3 V digital supply current consumption | 8 GPIO toggling at 1 MHz with $C_{ext} \cong 50$ pF see ⁽¹⁾ | - | 5.5 | 11 | mA |
| I(DVDD_3V3_IO) | 3.3 V digital supply current consumption | 8 GPIO toggling at 8 MHz with $C_{ext} \cong 50$ pF see ⁽¹⁾ | - | 33 | 76 | mA |

1. The tests are performed with the following enabled blocks: 1 x GPT, 1 x SPI, 1 x USART, IPC, AES, TRNG, ROSC. Cortex™ frequency equals to 100 MHz.

Table 17. Digital supply characteristics - OTP

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------|---|------------------------|------|------|------|------|
| I(DVDD_2V5) | 2.5 V digital supply current consumption ⁽¹⁾ | OTP static consumption | - | 20 | - | nA |
| I(DVDD_1V1) | 1.1 V digital supply current consumption ⁽¹⁾ | OTP read operation | - | - | 0.4 | mA |

1. Guaranteed by design, not tested in production.

5.4 PLC analog front-end (AFE) characteristics

5.4.1 Transmission path characteristics

Table 18. DAC and pre-driver characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------|---|--|------|----------------|------|------|
| I(DAC_OUT) FS | DAC output full-scale current | Tx mode, current measured on both outputs | - | 10 | - | mA |
| V(DAC_OUT) | Tx mode, differential | Rload = 50 Ω ± 1%, FS = 10 mA | - | 1 | - | Vpp |
| V(TX_OUT) BIAS | Transmitter output bias voltage | Rx mode | - | AVDD_3V3_AFE/2 | - | V |
| - | Pre-driver load impedance ⁽¹⁾ | - | 1 | - | - | kΩ |
| V(TX_OUT) HD2 | Transmitter output 2 nd harmonic distortion - see ⁽²⁾ | V(TX_OUT) = 4.6 V pk-pk, no load, Fout = 100 KHz, single-ended T(AMB) = 25 °C | - | -66 | - | dBc |
| V(TX_OUT) HD3 | Transmitter output 3 rd harmonic distortion see ⁽²⁾ | | - | -75 | - | dBc |
| V(TX_OUT) THD | Transmitter output total harmonic distortion see ⁽²⁾ | | - | -65 | - | dB |
| V(TX_OUT) HD2 | Transmitter output 2 nd harmonic distortion | V(TX_OUT) = 4.6 V pk-pk, no load, Fout = 100 KHz, differential T(AMB) = 25 °C | - | -69 | - | dBc |
| V(TX_OUT) HD3 | Transmitter output 3 rd harmonic distortion | | - | -75 | - | dBc |
| V(TX_OUT) THD | Transmitter output total harmonic distortion | | - | -67 | -60 | dB |
| V(TX_OUT) HD2 | Transmitter output 2 nd harmonic distortion - see ⁽²⁾ | V(TX_OUT) = 4.6 V pk-pk, no load, Fout = 500 KHz, single-ended T(AMB) = 25 °C | - | -61 | - | dBc |
| V(TX_OUT) HD3 | Transmitter output 3 rd harmonic distortion see ⁽²⁾ | | - | -73 | - | dBc |
| V(TX_OUT) THD | Transmitter output total harmonic distortion see ⁽²⁾ | | - | -60 | - | dB |
| V(TX_OUT) HD2 | Transmitter output 2 nd harmonic distortion | V(TX_OUT) = 4.6 V pk-pk, no load, Fout = 500 KHz, differential T(AMB) = 25 °C | - | -72 | - | dBc |
| V(TX_OUT) HD3 | Transmitter output 3 rd harmonic distortion | | - | -75 | - | dBc |
| V(TX_OUT) THD | Transmitter output total harmonic distortion | | - | -69 | -60 | dB |

1. Guaranteed by design, not tested in production.

2. Based on characterization, not tested in production.

5.4.2 Reception path characteristics

Table 19. Receiver input referred noise

| Symbol | Parameter ⁽¹⁾ | Conditions | Min. | Typ. | Max. | Unit |
|--------------------|-------------------------------|----------------------------------|------|------|------|------------|
| V(RX_INP - RX_INN) | Receiver input referred noise | CENELEC-A (35 kHz to 95 kHz) | - | 17 | - | dB μ V |
| | | CENELEC -B (95 kHz to 125 kHz) | - | 14 | - | dB μ V |
| | | CENELEC -C (125 kHz to 140 kHz) | - | 11 | - | dB μ V |
| | | CENELEC -D (140 kHz to 148 kHz) | - | 8 | - | dB μ V |
| | | ARIB STD-T84 (35 kHz to 400 kHz) | - | 24 | - | dB μ V |
| | | FCC-LOW (35 kHz to 125 kHz) | - | 19 | - | dB μ V |
| | | G3-FCC (150 kHz to 490 kHz) | - | 24 | - | dB μ V |

1. Guaranteed by design, not tested in production.

Table 20. PGA characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------------|--------------------------------|-------------------|------|------------------------|------|------------|
| V(RX_INP), V(RX_INN) | Receiver input maximum voltage | Single-ended mode | - | 7.5 | - | V p-p |
| V(RX_INP -RX_INN) | Receiver input maximum voltage | Differential mode | - | 15 | - | V p-p |
| V(RX_INP), V(RX_INN) | Receiver input bias voltage | - | - | (AVDD_2V5 AFE) * 0.475 | - | V |
| Z(RX_INP), Z(RX_INN) | Receiver input impedance | Single-ended | - | 5 | - | k Ω |
| GPGA | PLC PGA minimum gain | - | - | -18 | - | dB |
| | PLC PGA maximum gain | - | - | 54 | - | dB |
| GPGA Step | PLC PGA gain step | - | - | 3 | - | dB |

Table 21. ADC characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|-----------|-------------------|------|------|------|-------|
| ADC input range | - | Differential mode | - | 1.8 | - | V p-p |
| Resolution | - | - | - | 11 | - | bit |

5.4.3 Zero crossing comparator characteristics

Table 22. Zero crossing characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------|--|------------|------|------|--------------|------|
| V(ZC_IN)MAX | Zero crossing Detection input Voltage range | - | -3.3 | - | AVDD_3V3_AFE | V |
| V(ZC_IN)TL | Zero crossing Detection input Low threshold | - | - | -6 | - | mV |
| V(ZC_IN)TH | Zero crossing Detection input High threshold | - | - | +6 | - | mV |
| ZC_INd.c. | Zero crossing Input duty cycle | - | - | 50 | - | % |

5.5 Other characteristics

Table 23. I/O characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|--|----------------------|-------------------|------|-------------------|------|
| I(I/O) | Output current sunk by any I/Os and control pin | - | - | - | 8 | mA |
| | Output current sourced by any I/Os and control pin | - | - | - | 8 | mA |
| R_PU | Pull-up resistor | No load | 38 | 50 | 68 | kΩ |
| R_PD | Pull-down resistor | No load | 38 | 50 | 68 | kΩ |
| VIH | High level input voltage | - | DVDD_3V3_IO * 0.7 | - | - | V |
| VIL | Low level input voltage | - | - | - | DVDD_3V3_IO * 0.3 | V |
| VOH | High level output voltage | 8 mA sourced current | 2.8 | - | - | V |
| VOL | Low level output voltage | 8 mA sunk current | - | - | 0.4 | V |

Table 24. 25 MHz oscillator characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------|---|--------------------|------|------|------|------|
| f(MCLK) | Crystal oscillator frequency | - | - | 25 | - | MHz |
| C0 | External quartz crystal shunt capacitance | - | - | - | 2.6 | pF |
| ESR | External quartz crystal ESR value | See ⁽¹⁾ | - | - | 20 | Ω |
| CL | MCLK_IN, MCLK_OUT load capacitance | See ⁽¹⁾ | - | 18 | - | pF |

1. Guaranteed by design, not tested in production.

Table 25. Low-power RC oscillator (ROSC) characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------|----------------------------------|------------|------|------|------|------|
| f(ICLK) | Internal RC oscillator frequency | - | 3.1 | 4.2 | 5.5 | MHz |

Table 26. QFN56 (7 x 7 x 1 mm) package mechanical data

| Symbol | Dimension (millimeters) | | |
|--------|-------------------------|------|------|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0 | - | 0.05 |
| A2 | - | 0.65 | - |
| A3 | - | 0.20 | - |
| b | 0.16 | 0.21 | 0.26 |
| D | - | 7.00 | - |
| D2 | 4.50 | 4.60 | 4.70 |
| e | - | 0.40 | - |
| E | - | 7.00 | - |
| E2 | 4.50 | 4.60 | 4.70 |
| L | 0.35 | 0.40 | 0.45 |
| k | 0.70 | - | - |
| N | - | 56 | - |

Table 27. QFN56 (7 x 7 x 1 mm) package tolerance of form and position

| Symbol | Millimeters |
|--------|-------------|
| aaa | 0.10 |
| bbb | 0.07 |
| ccc | 0.10 |
| ddd | 0.05 |
| eee | 0.08 |

7 Revision history

Table 28. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 25-Oct-2017 | 1 | Initial release. |
| 08-Nov-2017 | 2 | Minor updates in Features and Description. |
| 19-Jun-2018 | 3 | Updated Table 1 on page 1 (added ST8500TR and Tray). |

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А