# Dual and Quad Precision Rail-to-Rail Input and Output Op Amps

## FEATURES

- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- **Low Input Offset Voltage: 150µV**
- High Common Mode Rejection Ratio: 90dB
- High $A_{VOL}$: >1V/µV Driving 10k Load
- Low Input Bias Current: 10nA
- Wide Supply Range: 1.8V to ±15V
- Low Supply Current: 375µA per Amplifier
- High Output Drive: 30mA
- 400kHz Gain-Bandwidth Product
- Slew Rate: 0.13V/µs
- Stable for Capacitive Loads Up to 1000pF

## APPLICATIONS

- Rail-to-Rail Buffer Amplifiers
- Low Voltage Signal Processing
- Supply Current Sensing at Either Rail
- Driving A/D Converters

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## DESCRIPTION

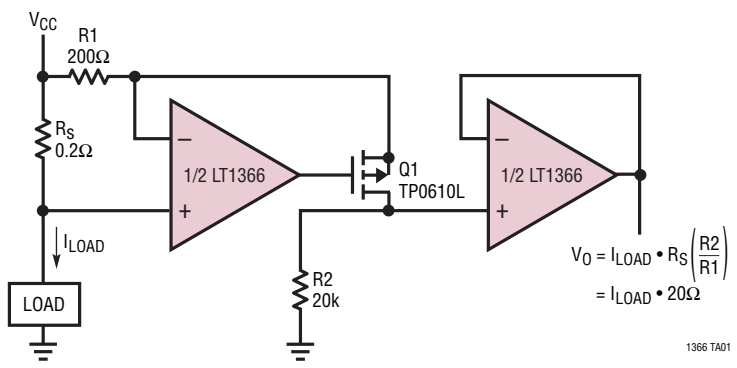
The LT®1366/LT1367/LT1368/LT1369 are dual and quad bipolar op amps which combine rail-to-rail input and output operation with precision specifications. These op amps maintain their characteristics over a supply range of 1.8V to 36V. Operation is specified for 3V, 5V and ±15V supplies. Input offset voltage is typically 150µV, with an open-loop gain $A_{VOL}$ of 1 million while driving a 10k load. Common mode rejection is typically 90dB over the full rail-to-rail input range, and supply rejection is 110dB.

The LT1366/LT1367 have conventional compensation which assures stability for capacitive loads of 1000pF or less. The LT1368/LT1369 have compensation that requires a 0.1µF output capacitor, which improves the amplifier's supply rejection and reduces output impedance at high frequencies. The output capacitor's filtering action reduces high frequency noise, which is beneficial when driving A/D converters.

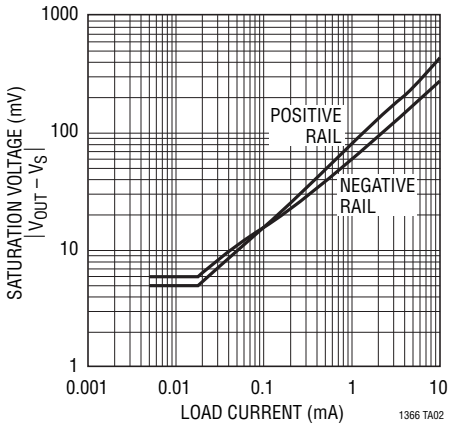
The LT1366/LT1368 are available in plastic 8-pin PDIP and 8-lead SO packages with the standard dual op amp pinout. The LT1367/LT1369 feature the standard quad pinout, which is available in a plastic 14-lead SO package. These devices can be used as plug-in replacements for many standard op amps to improve input/output range and precision.

## TYPICAL APPLICATION

**Positive Supply Rail Current Sense**




**Output Saturation Voltage vs Load Current**

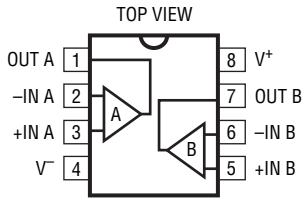


## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($V^+$ to $V^-$) ..... 36V
Input Current..... ±15mA
Output Short-Circuit Duration (Note 2)..... Continuous
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

## PIN CONFIGURATION

LT1366/LT1368

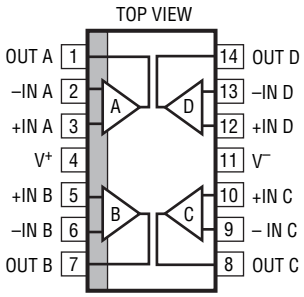



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 130°C/W (N8)
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 190°C/W (S8)

LT1367/LT1369




S PACKAGE
14-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 150°C/W

## AVAILABLE OPTIONS

| PRODUCT NUMBER | NUMBER OF OP AMPS | LOAD CAPACITANCE | MAX $V_{OS}$ (25°C) AT $V_S$ = 5V, 0V | ORDER PART NUMBER | |
|---|---|---|---|---|---|
| | | | | PLASTIC (N) | SURFACE MOUNT(S) |
| LT1366 | 2 | 0pF < $C_L$ < 1000pF | 475µV | LT1366CN8 | LT1366CS8 |
| LT1367 | 4 | 0pF < $C_L$ < 1000pF | 800µV | | LT1367CS |
| LT1368 | 2 | $C_L$ = 0.1µF | 475µV | LT1368CN8 | LT1368CS8 |
| LT1369 | 4 | $C_L$ = 0.1µF | 800µV | | LT1369CS |

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|---|
| LT1366CN8#PBF | LT1366CN8#TRPBF | 1366 | 8-Lead PDIP | 0°C to 70°C |
| LT1366CS8#PBF | LT1366CS8#TRPBF | 1366 | 8-Lead Plastic SO | 0°C to 70°C |
| LT1367CS#PBF | LT1367CS#TRPBF | LT1367CS | 14-Lead Plastic SO | 0°C to 70°C |
| LT1368CN8#PBF | LT1368CN8#TRPBF | 1368 | 8-Lead PDIP | 0°C to 70°C |
| LT1368CS8#PBF | LT1368CS8#TRPBF | 1368 | 8-Lead Plastic SO | 0°C to 70°C |
| LT1369CS#PBF | LT1369CS#TRPBF | LT1369CS | 14-Lead Plastic SO | 0°C to 70°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C; $V_S$ = 5V, 0V; $V_{CM}$ = 2.5V; $V_O$ = 2.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (LT1366/LT1368) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 150<br>150 | 475<br>475 | µV<br>µV |
| | Input Offset Voltage (LT1367/LT1369) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 150<br>150 | 800<br>700 | µV<br>µV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift (LT1366/LT1368)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | | 150<br>250 | 400<br>700 | µV<br>µV |
| | Input Offset Voltage Shift (LT1367/LT1369)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | | 150<br>250 | 650<br>1600 | µV<br>µV |
| $I_B$ | Input Bias Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | 0<br>–35 | 10<br>–10 | 35<br>0 | nA<br>nA |
| $\Delta I_B$ | Input Bias Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | | 20 | 70 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 1<br>0.3 | 12<br>12 | nA<br>nA |
| $\Delta I_{OS}$ | Input Offset Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | | 1 | 12 | nA |
| | Input Bias Current Match (Channel to Channel) | $V_{CM} = V_{CC}$ (Note 4)<br>$V_{CM} = V_{EE}$ (Note 4) | 0<br>0 | 1<br>1 | 12<br>12 | nA<br>nA |
| $e_n$ | Input Noise Voltage Density | f = 1kHz | | 29 | | nV/√Hz |
| $i_n$ | Input Noise Current Density | f = 1kHz | | 0.07 | | pA/√Hz |
| $C_{IN}$ | Input Capacitance | | | 12 | | pF |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_O$ = 50mV to 4.8V, $R_L$ = 10k | 250 | 2000 | | V/mV |
| CMRR | Common Mode Rejection Ratio (LT1366/LT1368)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | 81<br>75 | 90<br>90 | | dB<br>dB |
| | Common Mode Rejection Ratio (LT1367/LT1369)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | 77<br>71 | 90<br>90 | | dB<br>dB |
| PSRR | Power Supply Rejection Ratio<br>PSRR Match (Channel to Channel) (Note 4) | $V_S$ = 2.0V to 12V, $V_{CM} = V_O$ = 0.5V<br>$V_S$ = 2.0V to 12V, $V_{CM} = V_O$ = 0.5V | 90<br>84 | 105<br>100 | | dB<br>dB |
| $V_{OL}$ | Output Voltage Swing Low | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 2.5mA | | 6<br>40<br>110 | 12<br>70<br>200 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 2.5mA | $V_{CC}$ – 0.012<br>$V_{CC}$ – 0.100<br>$V_{CC}$ – 0.250 | $V_{CC}$ – 0.004<br>$V_{CC}$ – 0.050<br>$V_{CC}$ – 0.150 | | V<br>V<br>V |
| $I_{SC}$ | Short-Circuit Current | (Note 2) | ±15 | ±30 | | mA |
| $I_S$ | Supply Current per Amplifier | | | 340 | 520 | µA |
| GBW | Gain-Bandwidth Product (LT1366/LT1367)<br>Gain-Bandwidth Product (LT1368/LT1369) | $A_V$ = 1000<br>$A_V$ = 1000 | | 0.4<br>0.16 | | MHz<br>MHz |
| $t_S$ | Settling Time (LT1366/LT1367) | $A_V$ = 1, $V_{STEP}$ = 4V to 0.1% | | 30 | | µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified temperature range of 0°C < $T_A$ < 70°C. $V_S$ = 5V, 0V; $V_{CM}$ = 2.5V, $V_O$ = 2.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (LT1366/LT1368) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 200<br>200 | 575<br>575 | µV<br>µV |
| | Input Offset Voltage (LT1367/LT1369) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 200<br>200 | 950<br>900 | µV<br>µV |
| $V_{OS}$ TC | Input Offset Voltage Drift | (Note 3) | ● | | 2 | 6 | µV/°C |
| $\Delta V_{OS}$ | Input Offset Voltage Shift (LT1366/LT1368)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | ●<br>● | | 200<br>250 | 425<br>900 | µV<br>µV |
| | Input Offset Voltage Shift (LT1367/LT1369)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | ●<br>● | | 200<br>250 | 675<br>1900 | µV<br>µV |
| $I_B$ | Input Bias Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | 0<br>–45 | 15<br>–10 | 45<br>0 | nA<br>nA |
| $\Delta I_B$ | Input Bias Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | ● | | 25 | 90 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 2<br>1 | 15<br>15 | nA<br>nA |
| $\Delta I_{OS}$ | Input Offset Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | ● | | 2 | 15 | nA |
| | Input Bias Current Match (Channel to Channel) | $V_{CM} = V_{CC}$ (Note 4)<br>$V_{CM} = V_{EE}$ (Note 4) | ●<br>● | 0<br>0 | 2<br>1 | 15<br>15 | nA<br>nA |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_O$ = 50mV to 4.8V, $R_L$ = 10k | ● | 250 | 2000 | | V/mV |
| CMRR | Common Mode Rejection Ratio (LT1366/LT1368)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | ●<br>● | 80<br>74 | 87<br>87 | | dB<br>dB |
| | Common Mode Rejection Ratio (LT1367/LT1369)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | ●<br>● | 77<br>71 | 87<br>87 | | dB<br>dB |
| PSRR | Power Supply Rejection Ratio<br>PSRR Match (Channel to Channel) (Note 4) | $V_S$ = 2.3V to 12V, $V_{CM} = V_O$ = 0.5V<br>$V_S$ = 2.3V to 12V, $V_{CM} = V_O$ = 0.5V | ●<br>● | 88<br>82 | 105<br>100 | | dB<br>dB |
| $V_{OL}$ | Output Voltage Swing Low | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 2.5mA | ●<br>●<br>● | | 9<br>45<br>120 | 14<br>80<br>230 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High | No Load<br>$I_{SOURCE}$ = 0.5mA<br>$I_{SOURCE}$ = 2.5mA | ●<br>●<br>● | $V_{CC}$ – 0.014<br>$V_{CC}$ – 0.110<br>$V_{CC}$ – 0.300 | $V_{CC}$ – 0.005<br>$V_{CC}$ – 0.055<br>$V_{CC}$ – 0.180 | | V<br>V<br>V |
| $I_{SC}$ | Short-Circuit Current | (Note 2) | ● | ±12.5 | | | mA |
| $I_S$ | Supply Current per Amplifier | | ● | | 385 | 540 | µA |

**$T_A$ = 25°C; $V_S$ = 3V, 0V; $V_{CM}$ = 1.5V; $V_O$ = 1.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (LT1366/LT1368) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 150<br>150 | 475<br>475 | µV<br>µV |
| | Input Offset Voltage (LT1367/LT1369) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 150<br>150 | 850<br>750 | µV<br>µV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift (LT1366/LT1368)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | | 150<br>250 | 400<br>700 | µV<br>µV |
| | Input Offset Voltage Shift (LT1367/LT1369)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | | 150<br>250 | 650<br>1700 | µV<br>µV |
| $I_B$ | Input Bias Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | 0<br>–35 | 10<br>–10 | 35<br>0 | nA<br>nA |
| $\Delta I_B$ | Input Bias Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | | 20 | 70 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 1.0<br>0.3 | 12<br>12 | nA<br>nA |

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C; $V_S$ = 3V, 0V; $V_{CM}$ = 1.5V; $V_O$ = 1.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $\Delta I_{OS}$ | Input Offset Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | | 1 | 12 | nA |
| | Input Bias Current Match (Channel to Channel) | $V_{CM} = V_{CC}$ (Note 4)<br>$V_{CM} = V_{EE}$ (Note 4) | 0<br>0 | 1<br>1 | 12<br>12 | nA<br>nA |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_O$ = 50mV to 2.8V, $R_L$ = 10k | 250 | 1500 | | V/mV |
| CMRR | Common Mode Rejection Ratio (LT1366/LT1368)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | 77<br>71 | 86<br>86 | | dB<br>dB |
| | Common Mode Rejection Ratio (LT1367/LT1369)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | 73<br>67 | 86<br>86 | | dB<br>dB |
| $V_{OL}$ | Output Voltage Swing Low | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 2.5mA | | 6<br>40<br>110 | 12<br>70<br>200 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 2.5mA | $V_{CC}$ – 0.012<br>$V_{CC}$ – 0.100<br>$V_{CC}$ – 0.250 | $V_{CC}$ – 0.004<br>$V_{CC}$ – 0.050<br>$V_{CC}$ – 0.150 | | V<br>V<br>V |
| $I_{SC}$ | Short-Circuit Current | (Note 2) | ±10 | ±20 | | mA |
| $I_S$ | Supply Current per Amplifier | | | 330 | 500 | µA |

**The ● denotes the specifications which apply over the specified temperature range of 0°C < $T_A$ < 70°C. $V_S$ = 3V, 0V; $V_{CM}$ = 1.5V, $V_O$ = 1.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (LT1366/LT1368) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 200<br>200 | 575<br>575 | µV<br>µV |
| | Input Offset Voltage (LT1367/LT1369) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 200<br>200 | 950<br>900 | µV<br>µV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift (LT1366/LT1368)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | ●<br>● | | 200<br>250 | 425<br>900 | µV<br>µV |
| | Input Offset Voltage Shift (LT1367/LT1369)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | ●<br>● | | 200<br>250 | 675<br>1900 | µV<br>µV |
| $V_{OS}$ TC | Input Offset Voltage Drift | (Note 3) | ● | | 2 | 6 | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | 0<br>–45 | 15<br>–10 | 45<br>0 | nA<br>nA |
| $\Delta I_B$ | Input Bias Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | ● | | 25 | 90 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 2<br>1 | 15<br>15 | nA<br>nA |
| $\Delta I_{OS}$ | Input Offset Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | ● | | 2 | 15 | nA |
| | Input Bias Current Match (Channel to Channel) | $V_{CM} = V_{CC}$ (Note 4)<br>$V_{CM} = V_{EE}$ (Note 4) | ●<br>● | 0<br>0 | 2<br>1 | 15<br>15 | nA<br>nA |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_O$ = 50mV to 2.8V, $R_L$ = 10k | ● | 150 | 1500 | | V/mV |
| CMRR | Common Mode Rejection Ratio (LT1366/LT1368)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | ●<br>● | 76<br>70 | 83<br>83 | | dB<br>dB |
| | Common Mode Rejection Ratio (LT1367/LT1369)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | ●<br>● | 72<br>66 | 83<br>83 | | dB<br>dB |
| $V_{OL}$ | Output Voltage Swing Low | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 2.5mA | ●<br>●<br>● | | 9<br>45<br>120 | 14<br>80<br>230 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing High | No Load<br>$I_{SOURCE}$ = 0.5mA<br>$I_{SOURCE}$ = 2.5mA | ●<br>●<br>● | $V_{CC}$ – 0.014<br>$V_{CC}$ – 0.110<br>$V_{CC}$ – 0.300 | $V_{CC}$ – 0.005<br>$V_{CC}$ – 0.055<br>$V_{CC}$ – 0.180 | | V<br>V<br>V |
| $I_{SC}$ | Short-Circuit Current | (Note 2) | ● | ±10 | | | mA |
| $I_S$ | Supply Current per Amplifier | | ● | | 375 | 520 | µA |

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C, $V_S$ = ±15V, $V_{CM}$ = 0V, $V_O$ = 0V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (LT1366/LT1368) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 200<br>200 | 700<br>700 | µV<br>µV |
| | Input Offset Voltage (LT1367/LT1369) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 200<br>200 | 1000<br>900 | µV<br>µV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift (LT1366/LT1368)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | | 150<br>300 | 500<br>1300 | µV<br>µV |
| | Input Offset Voltage Shift (LT1367/LT1369)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | | 150<br>300 | 650<br>2000 | µV<br>µV |
| $I_B$ | Input Bias Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | 0<br>–35 | 10<br>–10 | 35<br>0 | nA<br>nA |
| $\Delta I_B$ | Input Bias Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | | 20 | 70 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | | 1.0<br>0.3 | 12<br>12 | nA<br>nA |
| $\Delta I_{OS}$ | Input Offset Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | | 1 | 12 | nA |
| | Input Bias Current Match (Channel to Channel) | $V_{CM} = V_{CC}$ (Note 4)<br>$V_{CM} = V_{EE}$ (Note 4) | 0<br>0 | 1<br>1 | 12<br>12 | nA<br>nA |
| $C_{IN}$ | Input Capacitance | | | 7.1 | | pF |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_O$ = –14.7V to 14.7V, $R_L$ = 10k<br>$V_O$ = –10V to 10V, $R_L$ = 2k | 1000<br>500 | 10000<br>10000 | | V/mV<br>V/mV |
| | Channel Separation | $V_O$ = –10V to 10V, $R_L$ = 2k | 120 | 135 | | dB |
| SR | Slew Rate (LT1366/LT1367) | $A_V$ = –1, $R_L$ = Open, $V_O$ = ±10V,<br>Measured at $V_O$ = ±5V | | 0.13 | | V/µs |
| | Slew Rate (LT1368/LT1369) | $A_V$ = –1, $R_L$ = Open, $V_O$ = ±10V,<br>Measured at $V_O$ = ±5V | | 0.065 | | V/µs |
| CMRR | Common Mode Rejection Ratio (LT1366/LT1368)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | 95<br>89 | 106<br>106 | | dB<br>dB |
| | Common Mode Rejection Ratio (LT1367/LT1369)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | 93<br>87 | 106<br>106 | | dB<br>dB |
| PSRR | Power Supply Rejection Ratio<br>PSRR Match (Channel to Channel) | $V_S$ = ±5V to ±15V<br>$V_S$ = ±5V to ±15V (Note 4) | 90<br>84 | 110<br>105 | | dB<br>dB |
| $V_{OL}$ | Output Voltage Swing Low | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 10mA | | $V_{EE}$ + 0.006<br>$V_{EE}$ + 0.040<br>$V_{EE}$ + 0.240 | $V_{EE}$ + 0.012<br>$V_{EE}$ + 0.070<br>$V_{EE}$ + 0.500 | V<br>V<br>V |
| $V_{OH}$ | Output Voltage Swing High | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 2.5mA | $V_{CC}$ – 0.012<br>$V_{CC}$ – 0.100<br>$V_{CC}$ – 0.800 | $V_{CC}$ – 0.004<br>$V_{CC}$ – 0.050<br>$V_{CC}$ – 0.400 | | V<br>V<br>V |
| $I_{SC}$ | Short-Circuit Current | (Note 2) | ±30 | ±75 | | mA |
| $I_S$ | Supply Current per Amplifier | | | 370 | 550 | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified temperature range of 0°C < $T_A$ < 70°C. $V_S$ = ±15V, $V_{CM}$ = 0V, $V_O$ = 0V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (LT1366/LT1368) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 250<br>250 | 850<br>850 | µV<br>µV |
| | Input Offset Voltage (LT1367/LT1369) | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 250<br>250 | 1150<br>1000 | µV<br>µV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift (LT1366/LT1368)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | ●<br>● | | 200<br>300 | 525<br>1500 | µV<br>µV |
| | Input Offset Voltage Shift (LT1367/LT1369)<br>Input Offset Voltage Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$, $V_{CC}$ (Notes 4, 5) | ●<br>● | | 200<br>300 | 750<br>2300 | µV<br>µV |
| $V_{OS}$ TC | Input Offset Voltage Drift | (Note 3) | ● | | 2 | 8 | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | 0<br>–45 | 15<br>–10 | 45<br>0 | nA<br>nA |
| $\Delta I_B$ | Input Bias Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | ● | | 25 | 90 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM} = V_{CC}$<br>$V_{CM} = V_{EE}$ | ●<br>● | | 2<br>1 | 15<br>15 | nA<br>nA |
| $\Delta I_{OS}$ | Input Offset Current Shift | $V_{CM} = V_{EE}$ to $V_{CC}$ | ● | | 2 | 15 | nA |
| | Input Bias Current Match (Channel to Channel) | $V_{CM} = V_{CC}$ (Note 4)<br>$V_{CM} = V_{EE}$ (Note 4) | ●<br>● | 0<br>0 | 2<br>1 | 15<br>15 | nA<br>nA |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_O$ = –14.7V to 14.7V, $R_L$ = 10k<br>$V_O$ = –10V to 10V, $R_L$ = 2k | ●<br>● | 750<br>500 | 6000<br>6000 | | V/mV<br>V/mV |
| | Channel Separation | $V_O$ = –10V to 10V, $R_L$ = 2k | ● | 110 | 135 | | dB |
| CMRR | Common Mode Rejection Ratio (LT1366/LT1368)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | ●<br>● | 95<br>89 | 103<br>103 | | dB<br>dB |
| | Common Mode Rejection Ratio (LT1367/LT1369)<br>CMRR Match (Channel to Channel) | $V_{CM} = V_{EE}$ to $V_{CC}$<br>$V_{CM} = V_{EE}$ to $V_{CC}$ (Note 4) | ●<br>● | 92<br>86 | 103<br>103 | | dB<br>dB |
| PSRR | Power Supply Rejection Ratio<br>PSRR Match (Channel to Channel) | $V_S$ = ±5V to ±15V<br>$V_S$ = ±5V to ±15V (Note 4) | ●<br>● | 80<br>75 | 105<br>100 | | dB<br>dB |
| $V_{OL}$ | Output Voltage Swing Low | No Load<br>$I_{SINK}$ = 0.5mA<br>$I_{SINK}$ = 10mA | ●<br>●<br>● | | $V_{EE}$ + 0.009<br>$V_{EE}$ + 0.045<br>$V_{EE}$ + 0.300 | $V_{EE}$ + 0.014<br>$V_{EE}$ + 0.080<br>$V_{EE}$ + 0.600 | V<br>V<br>V |
| $V_{OH}$ | Output Voltage Swing High | No Load<br>$I_{SOURCE}$ = 0.5mA<br>$I_{SOURCE}$ = 10mA | ●<br>●<br>● | $V_{CC}$ – 0.014<br>$V_{CC}$ – 0.11<br>$V_{CC}$ – 0.95 | $V_{CC}$ – 0.005<br>$V_{CC}$ – 0.055<br>$V_{CC}$ – 0.500 | | V<br>V<br>V |
| $I_{SC}$ | Short-Circuit Current | (Note 2) | ● | ±30 | | | mA |
| $I_S$ | Supply Current per Amplifier | | ● | | 415 | 575 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Applies to short circuits to ground for all split supplies and for single supplies less than 20V. Short circuits to either supply for supplies greater than 20V total may permanently damage the part. A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 3:** This parameter is not 100% tested.

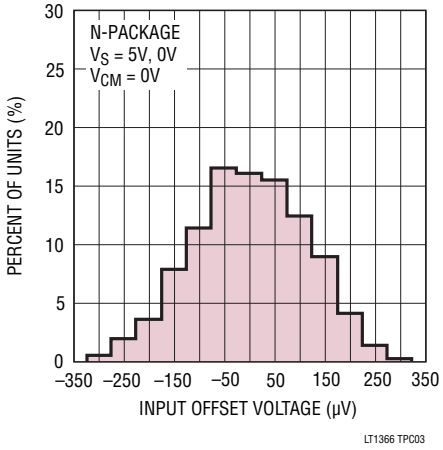
**Note 4:** Matching parameters are the difference between amplifiers A and D and between B and C on the LT1367/LT1369; between the two amplifiers on the LT1366/LT1368.

**Note 5:** Input offset voltage match is the difference in offset voltage between amplifiers measured at both $V_{CM} = V_{EE}$ and $V_{CM} = V_{CC}$.

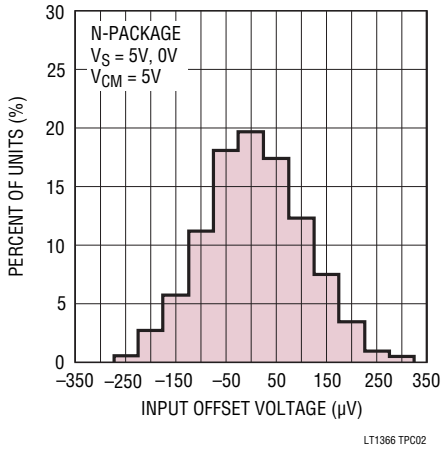
## TYPICAL PERFORMANCE CHARACTERISTICS

**(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)**

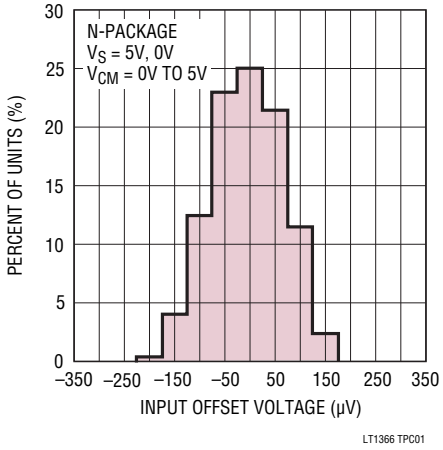
**PNP Stage $V_{OS}$ Distribution (LT1366/LT1368)**



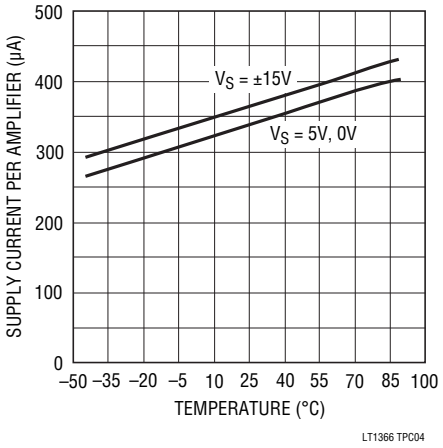

**NPN Stage $V_{OS}$ Distribution (LT1366/LT1368)**



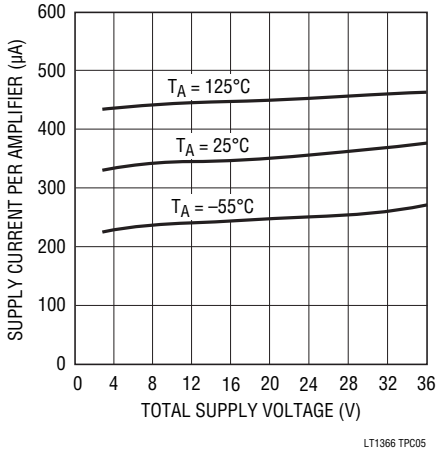

**$\Delta V_{OS}$-Shift Between PNP and NPN Stages (LT1366/LT1368)**



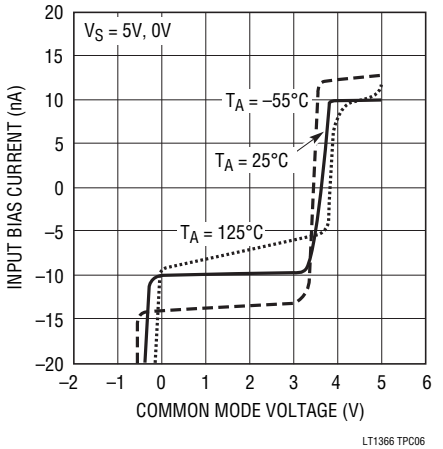

**Supply Current vs Temperature**



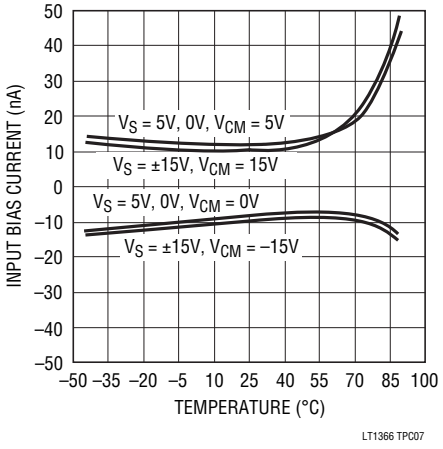

**Supply Current vs Supply Voltage**



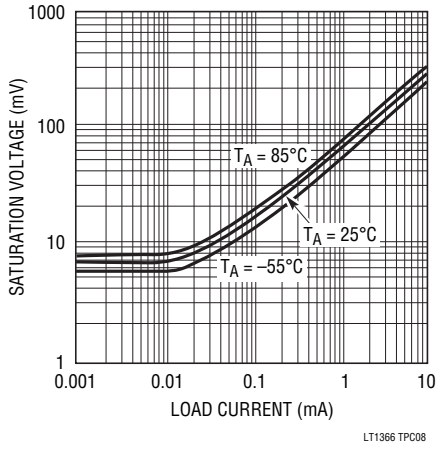

**Input Bias Current vs Common Mode Voltage**



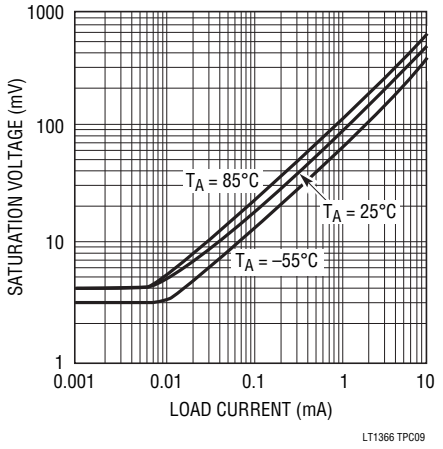

**Input Bias Current vs Temperature**




**Output Saturation Voltage vs Load Current (Output High)**



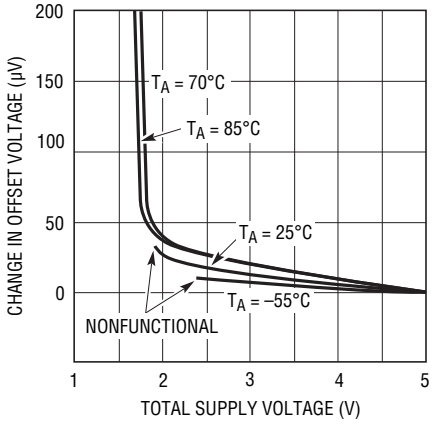

**Output Saturation Voltage vs Load Current (Output Low)**



# TYPICAL PERFORMANCE CHARACTERISTICS

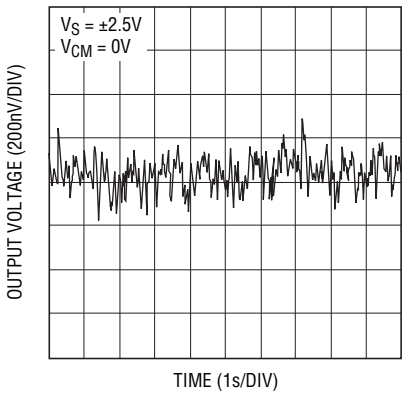
**(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)**

### Minimum Supply Voltage



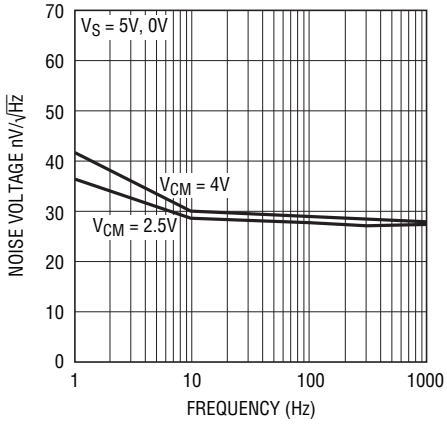

LT1366 TPC10

### 0.1Hz to 10Hz Output Voltage Noise



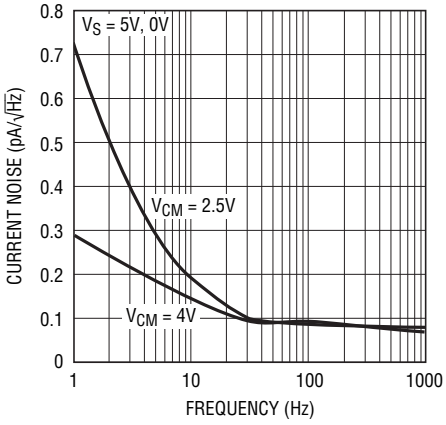

LT1366 TPC11

### Noise Voltage Spectrum



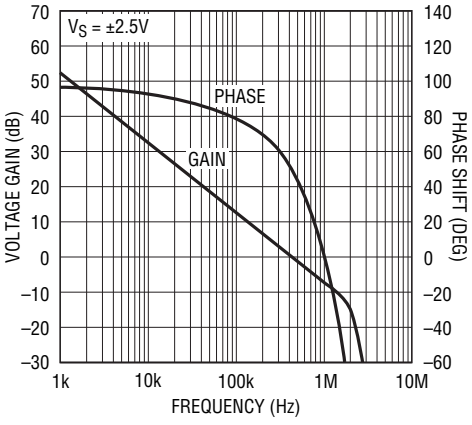

LT1366 TPC12

### Noise Current Spectrum



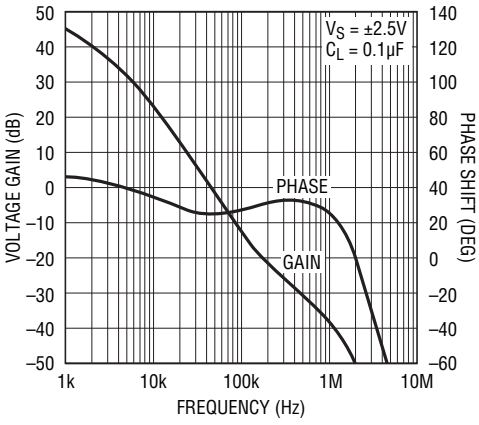

LT1366 TPC13

### Gain and Phase Shift vs Frequency (LT1366/LT1367)



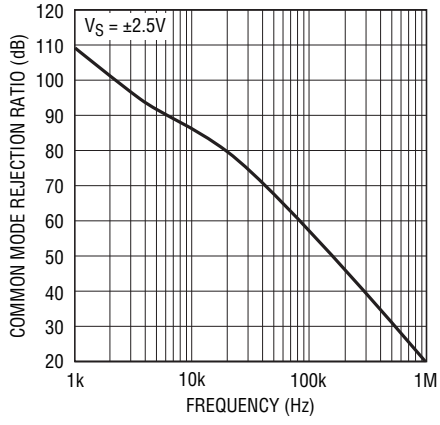

LT1366 TPC14

### Gain and Phase Shift vs Frequency (LT1368/LT1369)



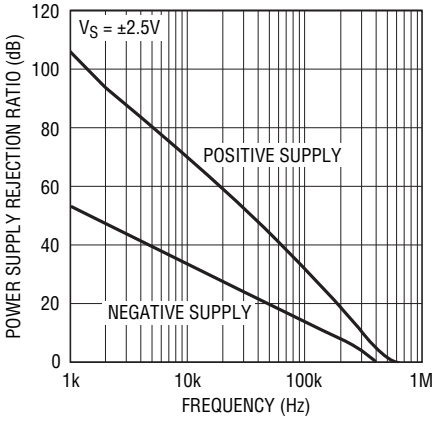

LT1366 TPC15

### CMRR vs Frequency (LT1366 and LT1367)



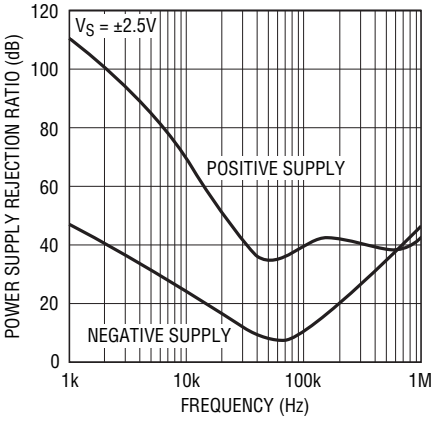

LT1366 TPC16

### PSRR vs Frequency (LT1366/LT1367)




LT1366 TPC17

### PSRR vs Frequency (LT1368/LT1369)

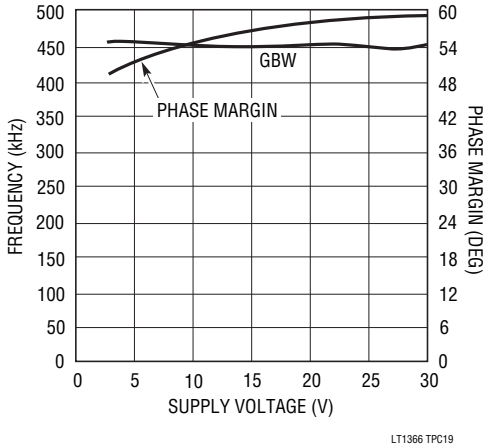



LT1366 TPC18

## TYPICAL PERFORMANCE CHARACTERISTICS

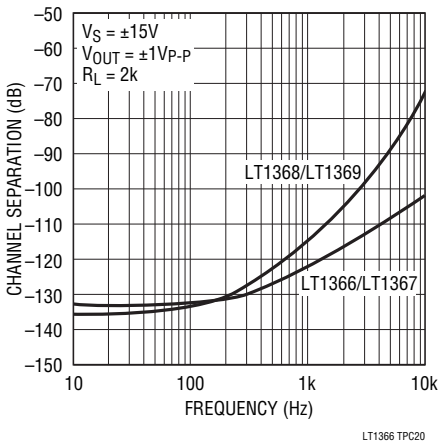
**(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)**

### Gain-Bandwidth and Phase Margin vs Supply Voltage (LT1366/LT1367)



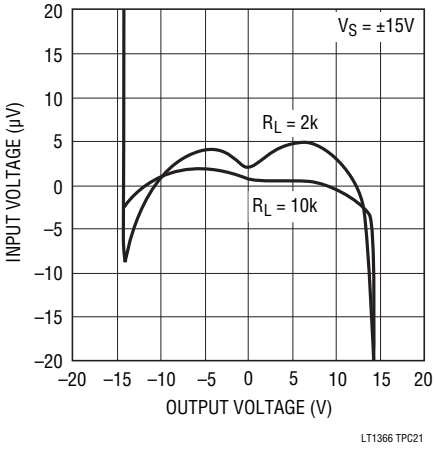

LT1366 TPC19

### Channel Separation vs Frequency



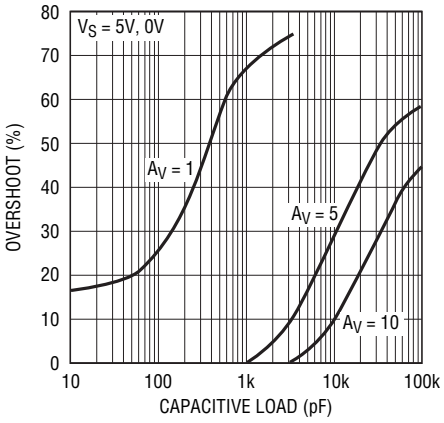

LT1366 TPC20

### Open-Loop Gain



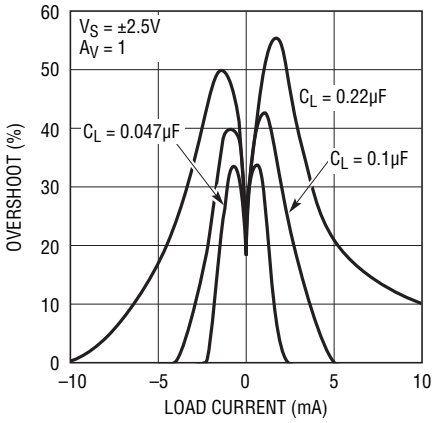

LT1366 TPC21

### Capacitive Load Handling (LT1366/LT1367)



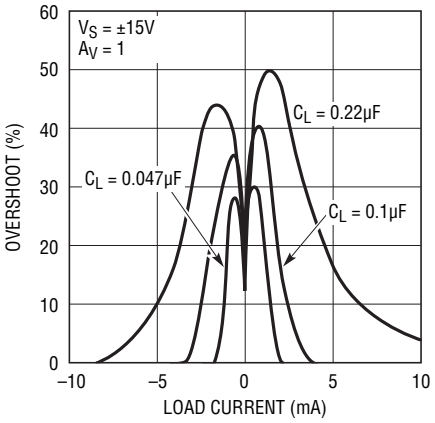

LT1366 TPC22

### Overshoot vs Load Current (LT1368/LT1369)



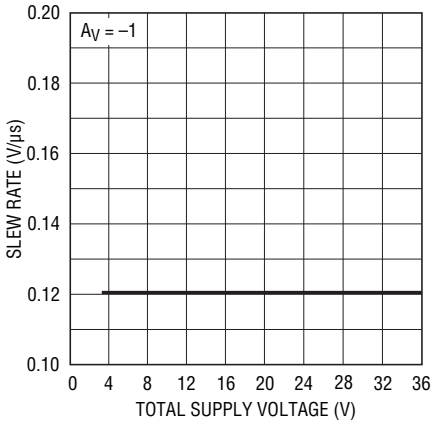

LT1366 TPC23

### Overshoot vs Load Current (LT1368/LT1369)



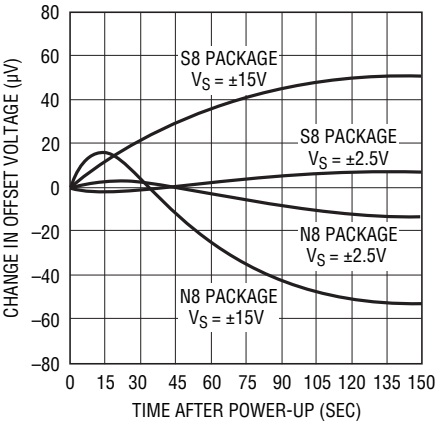

LT1366 TPC24

### Slew Rate vs Supply Voltage



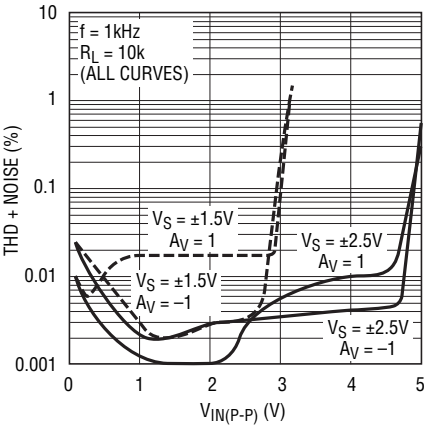

LT1366 TPC25

### Warm-Up Drift vs Time




LT1366 TPC26

### THD + Noise vs Peak-to-Peak Voltage

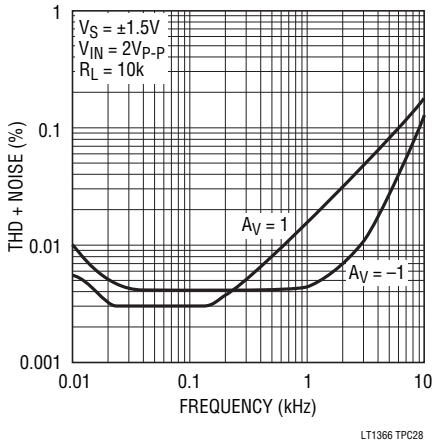



LT1366 TPC27

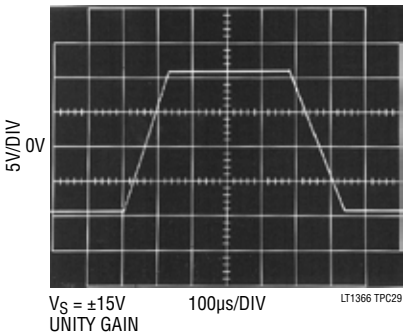
## TYPICAL PERFORMANCE CHARACTERISTICS

**(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)**

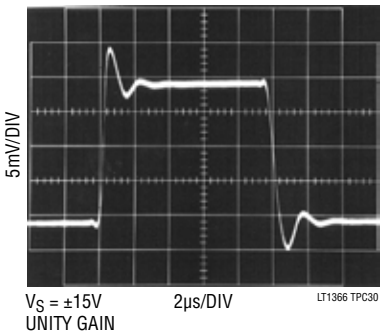
**THD + Noise vs Frequency**




**Large-Signal Response (LT1366/LT1367)**




**Small-Signal Response (LT1366/LT1367)**




## APPLICATIONS INFORMATION

### Rail-to-Rail Operation

The LT1366 family differs from conventional op amps in the design of both the input and output stages. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4, which are active over different portions of the input common mode range. Lateral devices are used in both input stages, eliminating the need for clamps across the input pins. Each input stage is trimmed for offset voltage. A complementary output configuration (Q23 through Q26) is employed to create an output stage with rail-to-rail swing. The amplifier is fabricated on Linear

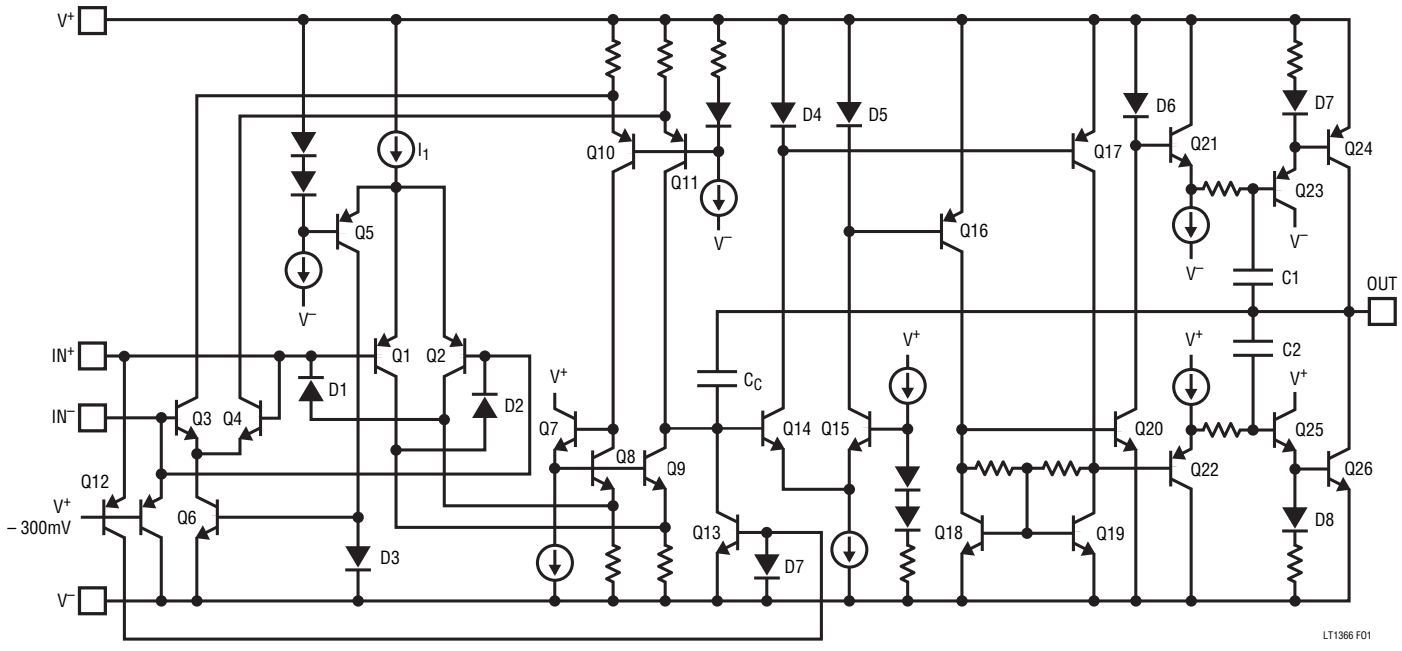



**Figure 1. LT1366 Simplified Schematic Diagram**

## APPLICATIONS INFORMATION

Technology's proprietary complementary bipolar process, which ensures very similar DC and AC characteristics for the output devices Q24 and Q26.

A simple comparator Q5 steers current from current source $I_1$ between the two input stages. When the input common mode voltage $V_{CM}$ is near the negative supply, Q5 is reverse biased, and $I_1$ becomes the tail current for the PNP differential pair Q1/Q2. At the other extreme, when $V_{CM}$ is within about 1.3V from the positive supply, Q5 diverts $I_1$ to the current mirror D3/Q6, which furnishes the tail current for the NPN differential pair Q3/Q4.

The collector currents of the two input pairs are combined in the second stage, consisting of Q7 through Q11. Most of the voltage gain in the amplifier is contained in this stage. Differential amplifier Q14/Q15 buffers the output of the second stage, converting the output voltage to differential currents. The differential currents pass through current mirrors D4/Q17 and D5/Q16, and are converted to differential voltages by Q18 and Q19. These voltages are also buffered and applied to the output Darlington pairs Q23/Q24 and Q25/Q26. Capacitors C1 and C2 form local feedback loops around the output devices, lowering the output impedance at high frequencies.

### Input Offset Voltage

Since the amplifier has two input stages, the input offset voltage changes depending upon which stage is active. The input offsets are random, but bounded voltages. When the amplifier switches between stages, offset voltages may go up, down, or remain flat; but will not exceed the guaranteed limits. This behavior is illustrated in three distribution plots of input offset voltage in the Typical Performance Characteristics section.

### Overdrive Protection

Two circuits prevent the output from reversing polarity when the input voltage exceeds the common mode range. When the noninverting input exceeds the positive supply by approximately 300mV, the clamp transistor Q12 (Figure 1) turns on, pulling the output of the second stage low, which forces the output high. For inputs below the negative supply, diodes D1 and D2 turn on, overcoming the saturation of the input pair Q1/Q2.

When overdriven, the amplifier draws input current that exceeds the normal input bias current. Figures 2 and 3 show some typical overdrive currents as a function of input voltage. The input current must be less than 1mA of positive overdrive or less than 7mA of negative overdrive, for the phase reversal protection to work properly. When the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current. In addition to overdrive protection, the amplifier is protected against ESD strokes up to 4kV on all pins.

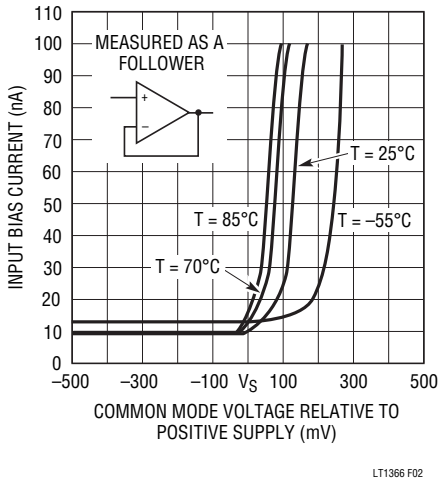



**Figure 2. Input Bias Current vs Common Mode Voltage**

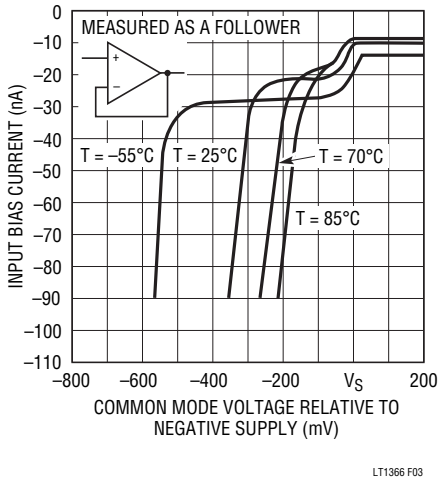



**Figure 3. Input Bias Current vs Common Mode Voltage**

# APPLICATIONS INFORMATION

### Improved Supply Rejection in the LT1368/LT1369

The LT1368/LT1369 are variations of the LT1366/LT1367 offering greater supply rejection and lower high frequency output impedance. The LT1368/LT1369 require a 0.1µF load capacitance for compensation. The output capacitance forms a filter, which reduces pickup from the supply and lowers the output impedance. This additional filtering is helpful in mixed analog/digital systems with common supplies, or systems employing switching supplies. Filtering also reduces high frequency noise, which may be beneficial when driving A/D converters.

Figure 4 shows the outputs of the LT1366/LT1368 perturbed by a 200mV$_{P-P}$ 50kHz square wave added to the positive supply. The LT1368's power supply rejection is about ten times greater than that of the LT1366 at 50kHz. Note the 5-to-1 scale change in the output voltage traces.

The tolerance of the external compensation capacitor is not critical. The plots of Overshoot vs Load Current in the Typical Performance Characteristics section illustrate the effect of a capacitive load.

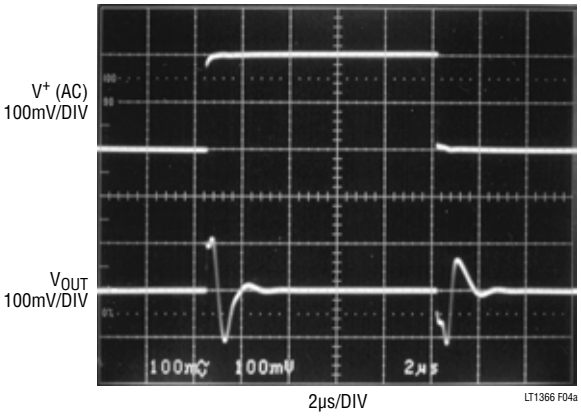



Figure 4a. LT1366 Power Supply Rejection Test

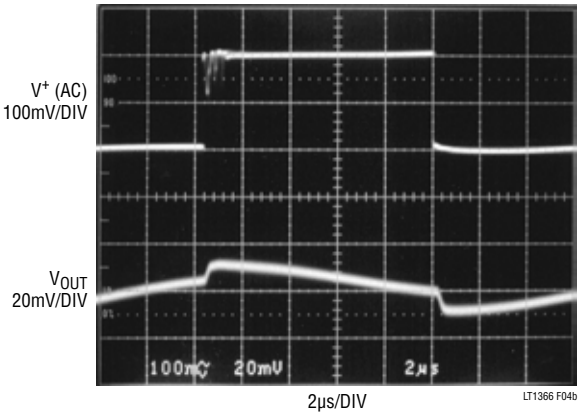



Figure 4b. LT1368 Power Supply Rejection Test

# TYPICAL APPLICATIONS

### Buffering A/D Converters

Figure 5 shows the LT1368 driving an LTC®1288 2-channel micropower A/D converter (ADC). The LTC1288 can accommodate voltage references and input signals equal to the supply rails. The sampling nature of this ADC eliminates the need for an external sample-and-hold, but may call for a drive amplifier because of the ADC's 12µs settling requirement. The LT1368's rail-to-rail operation and low input offset voltage make it well-suited for low power, low frequency A/D applications. Either the LT1366 or LT1368 could be used for this application. However, for low frequencies (f < 1kHz) the LT1368 provides better supply rejection.

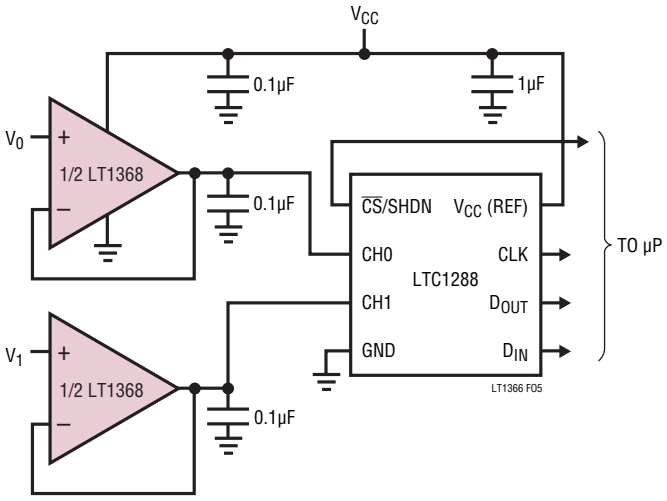



Figure 5. 2-Channel Low Power A/D Converter

## TYPICAL APPLICATIONS

### Precision Low Dropout Regulator

Microprocessors and complex digital circuits frequently specify tight control of power supply characteristics. The circuit shown in Figure 6 provides a precise 3.6V, 1A output from a minimum 3.8V input voltage. The circuit's nominal operating voltage is 4.75V ±5%. The voltage reference and resistor ratios determine output voltage accuracy, while the LT1366's high gain enforces 0.2% line and load regulation. Quiescent current is about 1mA and does not change appreciably with supply or load. All components are available in surface mount packages.

The regulator's main loop consists of A1 and a logic-level FET, Q1. The output is fed back to the op amp's positive input because of the phase inversion through Q1. The regulator's frequency response is limited by Q1's roll-off and the phase lead introduced by the output capacitor's effective series resistance (ESR). Two pole-zero networks compensate for these effects. The pole formed with R5 and C2 rolls off the gain set with the feedback network, while the pole formed with R7 and C3 rolls off A1's gain directly, which is the dominant influence on settling time. The zeros formed with R6 and C2, and R8 and C3 provide phase boost near the unity-gain crossover, which increases the regulator's phase margin. Although not directly part of the compensation, R9 decouples the op amp's output from Q1's large gate capacitance.

A second loop provides a foldback current limit. A2 compares the sense voltage across R1 with 50mV referenced to the positive rail. When the sense voltage exceeds the reference, A2's output drives Q1's gate positive via A1. In current limit, the output voltage collapses and the current limit LED (D1) turns on causing about 30mV to drop across R3. A2 regulates Q1's drain current so that the deficit between the 50mV reference and the voltage across R3 is made up across the sense resistor. The reduced sense voltage is 20mV, which sets the current limit to about 400mA. As the supply voltage increases, the voltage across R3 increases, and the current limit folds back to a lower level. The current limit loop deactivates when the load current drops below the regulated output current. When the supply turns on rapidly, C1 bypasses the fold back circuit allowing the regulator to start-up into a heavy load.

Q1 does not require a heat sink. When mounted on a type FR4 PC board, Q1 has a thermal resistance of 50°C/W. At 1.4W worst-case dissipation, Q1 can operate up to 80°C.

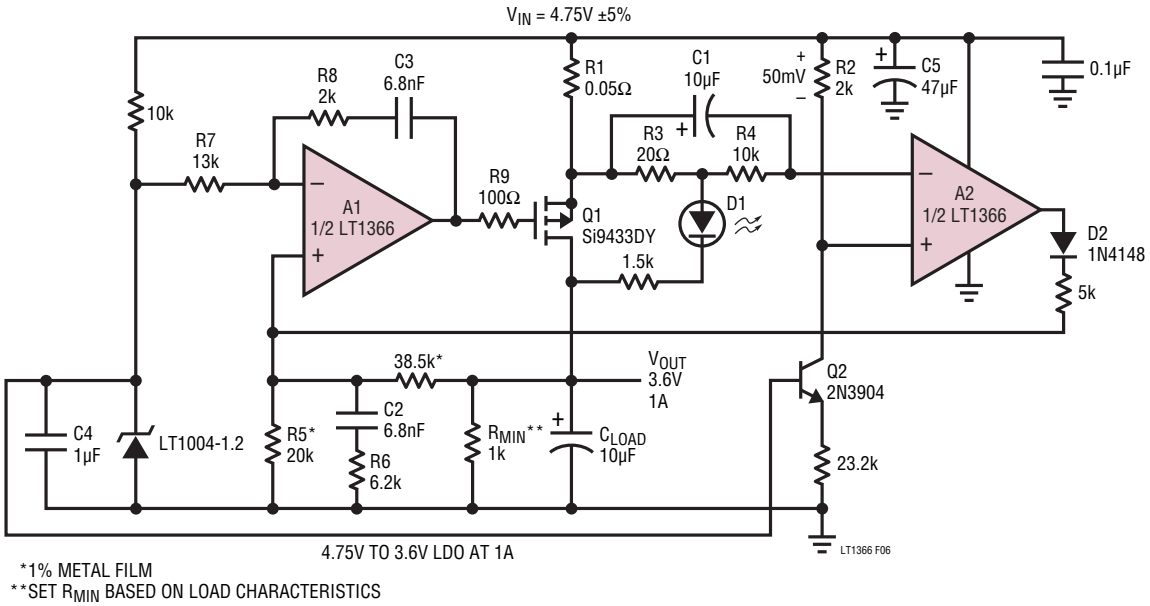



**Figure 6. Precision 3.6V, 1A Low Dropout Regulator**

# TYPICAL APPLICATIONS

### High Side Current Source

The wide compliance current source shown in Figure 7 takes advantage of the LT1366's ability to measure small signals near the positive supply rail. The LT1366 adjusts Q1's gate voltage to force the voltage across the sense resistor ($R_{SENSE}$) to equal the voltage from the supply to the potentiometer's wiper. A rail-to-rail op amp is needed because the voltage across the sense resistor must drop to zero when the divided reference voltage is set to zero. Q2 acts as a constant current sink to minimize error in the reference voltage when the supply voltage varies.

The circuit can operate over a wide supply range ($5V < V_{CC} < 30V$). At low input voltage, circuit operation is limited by the MOSFET's gate drive requirements. At high input voltage, circuit operation is limited by the LT1366's absolute maximum ratings and the output power requirements.

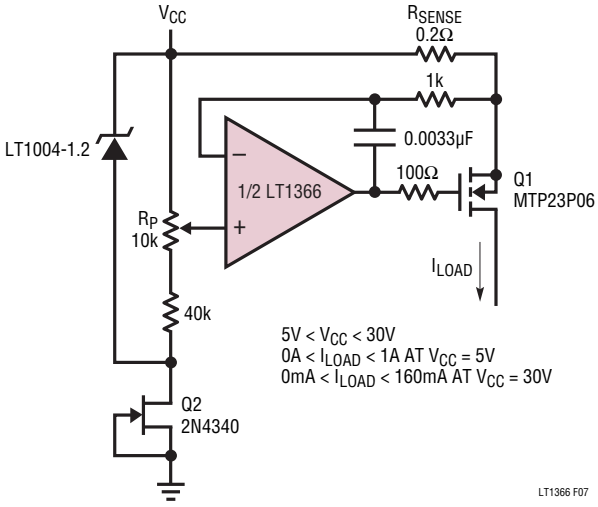



**Figure 7. High Side Current Source**

The circuit delivers 1A at 200mV of sense voltage. With a 5V input supply, the power dissipation is 5W. For operation at 70°C ambient temperature, the MOSFET's heat sink must have a thermal resistance of:

$$\theta_{HS} = \theta_{JA(SYSTEM)} - \theta_{JC(FET)}$$
$$= (125°C - 70°C)/5W - 1.25°C/W$$
$$= 11°C/W - 1.25°C/W$$
$$= 9.75°C/W$$

which is easily achievable with a small heat sink. Input voltages greater than 5V require the use of a larger heat sink or a reduction of the output current.

The circuit's supply regulation is about 0.03%/V. The output impedance is equal to the MOSFET's output impedance multiplied by the op amp's open-loop gain. Degradations in current-source compliance occur when the voltage across the MOSFET's on-resistance and the sense resistor drops below the voltage required to maintain the desired output current. This condition occurs when:

$$[V_{CC} - V_{OUT}] < [I_{LOAD} \bullet (R_{SENSE} + R_{ON})]$$

### Single Supply, 1kHz, 4th Order Butterworth Filter

An LT1367 is used in Figure 8 to form a 4th order Butterworth filter. The filter is a simplified state variable architecture consisting of two cascaded 2nd order sections. Each section uses the 360 degree phase shift around

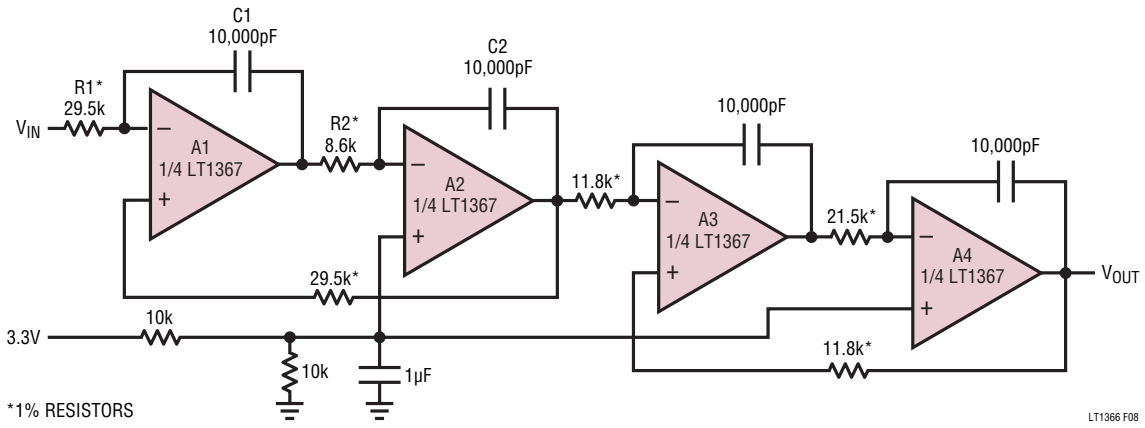



**Figure 8. 4-Pole 1kHz, 3.3V Single Supply, State Variable Filter Using the LT1367**

## TYPICAL APPLICATIONS

the 2 op amp loop to create a negative summing junction at A1's positive input[1]. The circuit has low sensitivities for center frequency and Q, which are set with the following equations:

$$\omega_0^2 = 1/(R1 \bullet C1 \bullet R2 \bullet C2)$$

where:

$$R1 = 1/(\omega_0 \bullet Q \bullet C1) \text{ and } R2 = Q/(\omega_0 \bullet C2).$$

The DC bias applied to A2 and A4, half supply, is not needed when split supplies are available. The circuit swings rail-to-rail in the passband making it an excellent anti-aliasing filter for ADCs. The amplitude response is flat to 1kHz then rolls off at 80dB/decade.

[1]James Hahn, "State Variable Filter Trims Predecessor's Component Count," Electronics, April 21, 1982.

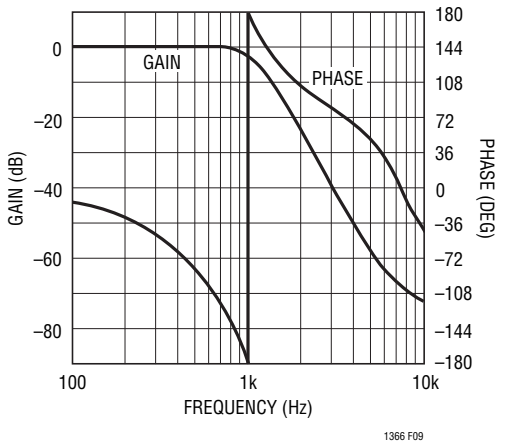



**Figure 9. Frequency Response of 4th Order Butterworth Filter**

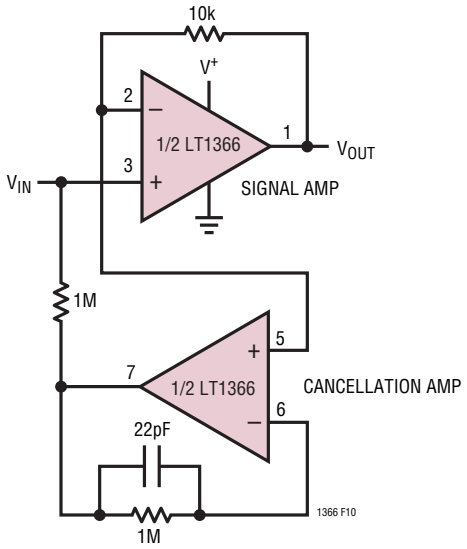



**Figure 10. Input Bias Current Cancellation**

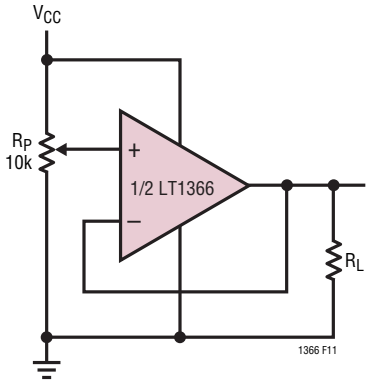
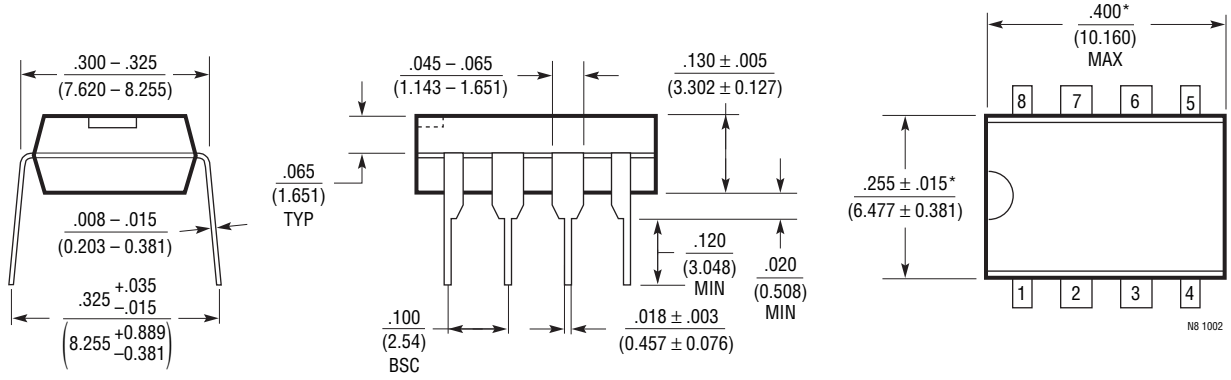



**Figure 11. Rail-to-Rail Potentiometer Buffer**

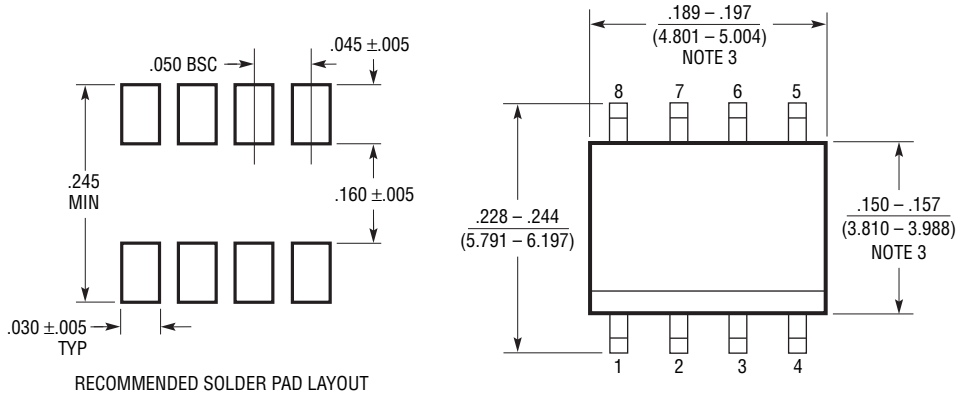
# PACKAGE DESCRIPTION

**N8 Package**
**8-Lead PDIP (Narrow .300 Inch)**
(Reference LTC DWG # 05-08-1510)




NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

**S8 Package**
**8-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610)

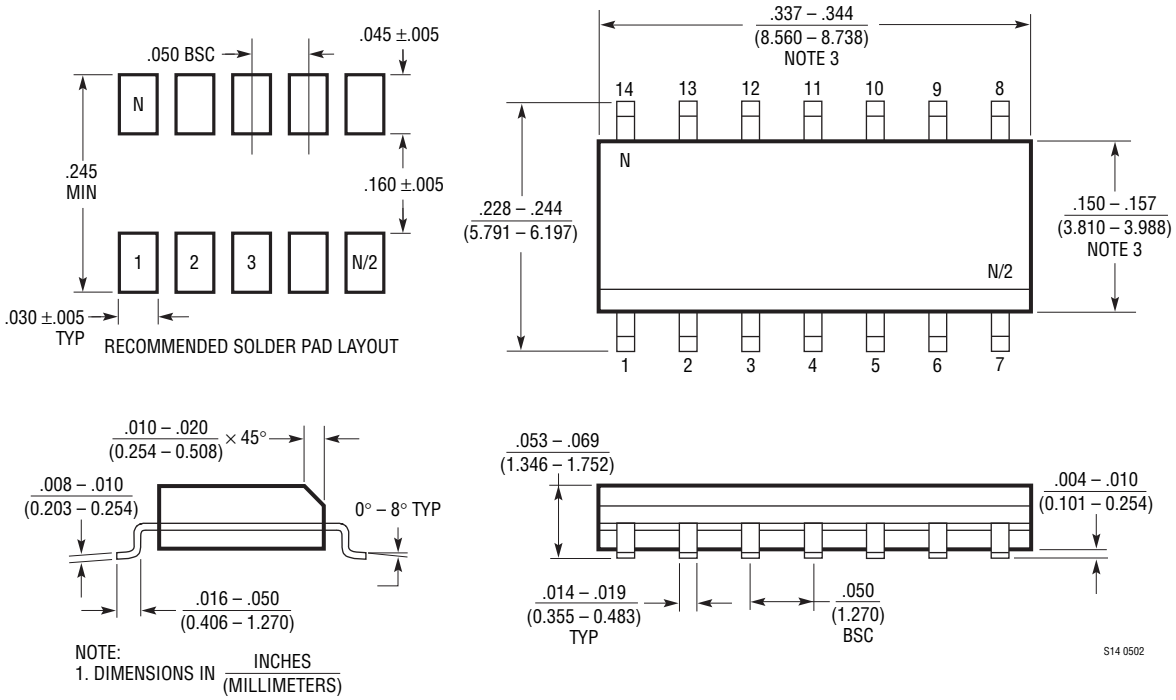



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

# PACKAGE DESCRIPTION

**S Package**
**14-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610)




NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

## REVISION HISTORY (Revision history begins at Rev B)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| B | 03/10 | Change to Absolute Maximum Ratings | 2 |
| | | Updated Format of Order Information Section | 2 |
| | | Change to Electrical Characteristics Note | 3, 4, 5, 6, 7 |



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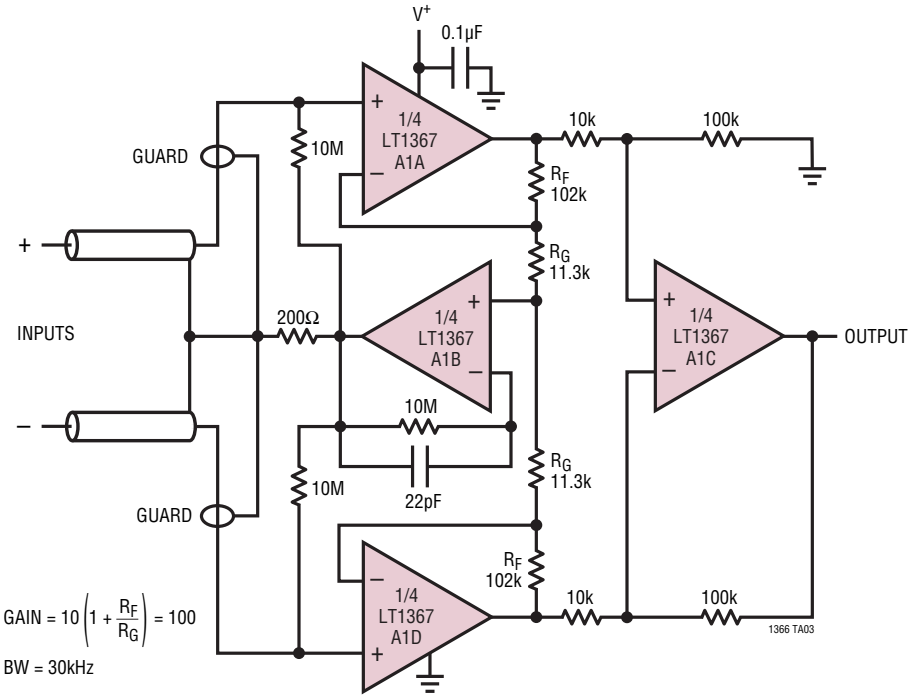
## TYPICAL APPLICATION

**Instrumentation Amplifier**




## RELATED PARTS

| PART | DESCRIPTION | COMMENTS |
|---|---|---|
| LT1078/LT1079 | Dual/Quad 55µA Max, Single Supply, Precision Op Amps | Input/Output Common Mode Includes Ground, 70µV $V_{OS(MAX)}$ and 2.5µV/°C Drift (Max), 200kHz GBW, 0.07V/µs Slew Rate |
| LTC1152 | Rail-to-Rail Input, Rail-to-Rail Output, Zero-Drift Amplifier | High DC Accuracy, 10µV $V_{OS(MAX)}$, 100nV/°C Drift, 1MHz GBW, 1V/µs Slew Rate, Supply Current 2.2mA (Max), Single Supply, Can Be Configured for C-Load™ Operation |
| LT1178/LT1179 | Dual/Quad 17µA Max, Single Supply, Precision Op Amps | Input/Output Common Mode Includes Ground, 70µV $V_{OS(MAX)}$ and 4µV/°C Drift (Max), 85kHz GBW, 0.04V/µs Slew Rate |
| LT1211/LT1212 | Dual/Quad 14MHz, 7V/µs, Single Supply, Precision Op Amps | Input Common Mode Includes Ground, 275µV $V_{OS(MAX)}$ and 6µV/°C Drift (Max), Supply Current 1.8mA per Op Amp (Max) |
| LT1495/LT1496 | 1.5µA, Rail-to-Rail Input/Output Dual/Quad | 375µV $V_{OS(MAX)}$, 2µV/°C Drift (Max), Over-The-Top® Input |

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