



MICROCHIP MCP6281/1R/2/3/4/5

450 μ A, 5 MHz Rail-to-Rail Op Amp

Features

- Gain Bandwidth Product: 5 MHz (typical)
- Supply Current: $I_Q = 450 \mu\text{A}$ (typical)
- Supply Voltage: 2.2V to 6.0V
- Rail-to-Rail Input/Output
- Extended Temperature Range: -40°C to $+125^\circ\text{C}$
- Available in Single, Dual, and Quad Packages
- Single with $\overline{\text{CS}}$ (**MCP6283**)
- Dual with $\overline{\text{CS}}$ (**MCP6285**)

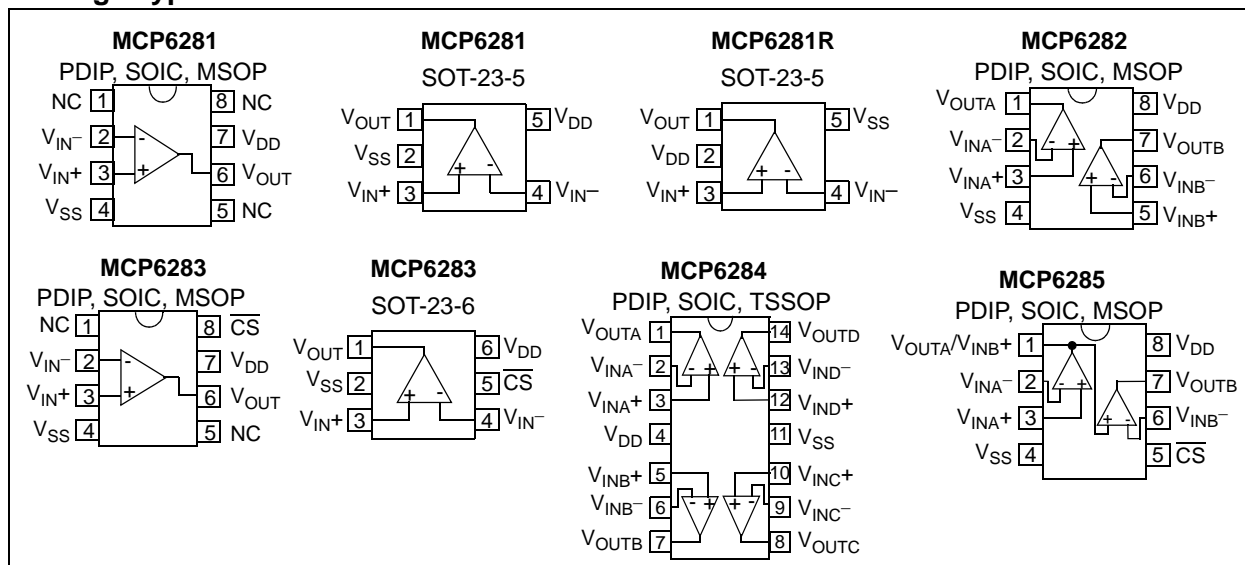
Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- SPICE Macro Models
- FilterLab[®] Software
- Mindi[™] Circuit Designer & Simulator
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Package Types



Description

The Microchip Technology Inc. MCP6281/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 5 MHz Gain Bandwidth Product (GBWP) and a 65° phase margin. This family also operates from a single supply voltage as low as 2.2V, while drawing 450 μA (typical) quiescent current. Additionally, the MCP6281/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of $V_{DD} + 300 \text{ mV}$ to $V_{SS} - 300 \text{ mV}$. This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6285 has a Chip Select ($\overline{\text{CS}}$) input for dual op amps in an 8-pin package. This device is manufactured by cascading the two op amps (the output of op amp A connected to the non-inverting input of op amp B). The $\overline{\text{CS}}$ input puts the device in Low-power mode.

The MCP6281/1R/2/3/4/5 family operates over the Extended Temperature Range of -40°C to $+125^\circ\text{C}$. It also has a power supply range of 2.2V to 6.0V.

MCP6281/1R/2/3/4/5

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|--|------------------------------------|
| $V_{DD} - V_{SS}$ | 7.0V |
| Current at Input Pins | ± 2 mA |
| Analog Inputs (V_{IN+} , V_{IN-}) †† | $V_{SS} - 1.0V$ to $V_{DD} + 1.0V$ |
| All Other Inputs and Outputs | $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$ |
| Difference Input Voltage | $ V_{DD} - V_{SS} $ |
| Output Short Circuit Current | Continuous |
| Current at Output and Supply Pins | ± 30 mA |
| Storage Temperature..... | $-65^{\circ}C$ to $+150^{\circ}C$ |
| Maximum Junction Temperature (T_J) | $+150^{\circ}C$ |
| ESD Protection On All Pins (HBM; MM) | ≥ 4 kV; 400V |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”.

DC ELECTRICAL SPECIFICATIONS

| Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.2V$ to $+5.5V$, $V_{SS} = GND$, $V_{OUT} \approx V_{DD}/2$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ k Ω to V_L and CS is tied low. (refer to Figure 1-2 and Figure 1-3). | | | | | | |
|--|----------------------------|----------------|--------------|----------------|-------------------|--|
| Parameters | Sym | Min | Typ | Max | Units | Conditions |
| Input Offset | | | | | | |
| Input Offset Voltage | V_{OS} | -3.0 | — | +3.0 | mV | $V_{CM} = V_{SS}$ (Note 1) |
| Input Offset Voltage (Extended Temperature) | V_{OS} | -5.0 | — | +5.0 | mV | $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $V_{CM} = V_{SS}$ (Note 1) |
| Input Offset Temperature Drift | $\Delta V_{OS}/\Delta T_A$ | — | ± 1.7 | — | $\mu V/^{\circ}C$ | $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $V_{CM} = V_{SS}$ (Note 1) |
| Power Supply Rejection Ratio | PSRR | 70 | 90 | — | dB | $V_{CM} = V_{SS}$ (Note 1) |
| Input Bias, Input Offset Current and Impedance | | | | | | |
| Input Bias Current | I_B | — | ± 1.0 | — | pA | Note 2 |
| At Temperature | I_B | — | 50 | 200 | pA | $T_A = +85^{\circ}C$ (Note 2) |
| At Temperature | I_B | — | 2 | 5 | nA | $T_A = +125^{\circ}C$ (Note 2) |
| Input Offset Current | I_{OS} | — | ± 1.0 | — | pA | Note 3 |
| Common Mode Input Impedance | Z_{CM} | — | $10^{13} 6$ | — | ΩpF | Note 3 |
| Differential Input Impedance | Z_{DIFF} | — | $10^{13} 3$ | — | ΩpF | Note 3 |
| Common Mode (Note 4) | | | | | | |
| Common Mode Input Range | V_{CMR} | $V_{SS} - 0.3$ | — | $V_{DD} + 0.3$ | V | |
| Common Mode Rejection Ratio | CMRR | 70 | 85 | — | dB | $V_{CM} = -0.3V$ to $2.5V$, $V_{DD} = 5V$ |
| Common Mode Rejection Ratio | CMRR | 65 | 80 | — | dB | $V_{CM} = -0.3V$ to $5.3V$, $V_{DD} = 5V$ |
| Open-Loop Gain | | | | | | |
| DC Open-Loop Gain (Large Signal) | A_{OL} | 90 | 110 | — | dB | $V_{OUT} = 0.2V$ to $V_{DD} - 0.2V$, $V_{CM} = V_{SS}$ (Note 1) |
| Output | | | | | | |
| Maximum Output Voltage Swing | V_{OL} , V_{OH} | $V_{SS} + 15$ | — | $V_{DD} - 15$ | mV | 0.5V input overdrive |
| Output Short Circuit Current | I_{SC} | — | ± 25 | — | mA | |
| Power Supply | | | | | | |
| Supply Voltage | V_{DD} | 2.2 | — | 6.0 | V | (Note 5) |
| Quiescent Current per Amplifier | I_Q | 300 | 450 | 570 | μA | $I_O = 0$ |

- Note 1:** The MCP6285's V_{CM} for op amp B (pins V_{OUTA}/V_{INB+} and V_{INB-}) is $V_{SS} + 100$ mV.
- Note 2:** The current at the MCP6285's V_{INB-} pin is specified by I_B only.
- Note 3:** This specification does not apply to the MCP6285's V_{OUTA}/V_{INB+} pin.
- Note 4:** The MCP6285's V_{INB-} pin (op amp B) has a common mode range (V_{CMR}) of $V_{SS} + 100$ mV to $V_{DD} - 100$ mV. The MCP6285's V_{OUTA}/V_{INB+} pin (op amp B) has a voltage range specified by V_{OH} and V_{OL} .
- Note 5:** All parts with date codes November 2007 and later have been screened to ensure operation at $V_{DD} = 6.0V$. However, the other minimum and maximum specifications are measured at 2.4V and/or 5.5V.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{OUT} \approx V_{DD}/2$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and $\overline{\text{CS}}$ is tied low. (refer to [Figure 1-2](#) and [Figure 1-3](#)).

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|-----------------------------|----------|-----|-----|-----|------------------------|-------------------------------------|
| AC Response | | | | | | |
| Gain Bandwidth Product | GBWP | — | 5.0 | — | MHz | |
| Phase Margin at Unity-Gain | PM | — | 65 | — | ° | $G = +1\text{ V/V}$ |
| Slew Rate | SR | — | 2.5 | — | V/ μs | |
| Noise | | | | | | |
| Input Noise Voltage | E_{ni} | — | 5.2 | — | μV_{P-P} | $f = 0.1\text{ Hz to }10\text{ Hz}$ |
| Input Noise Voltage Density | e_{ni} | — | 16 | — | nV/ $\sqrt{\text{Hz}}$ | $f = 1\text{ kHz}$ |
| Input Noise Current Density | i_{ni} | — | 3 | — | fA/ $\sqrt{\text{Hz}}$ | $f = 1\text{ kHz}$ |

MCP6283/MCP6285 CHIP SELECT ($\overline{\text{CS}}$) SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{OUT} \approx V_{DD}/2$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and $\overline{\text{CS}}$ is tied low. (refer to [Figure 1-2](#) and [Figure 1-3](#)).

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|--|------------|--------------|------|--------------|---------------|---|
| CS Low Specifications | | | | | | |
| $\overline{\text{CS}}$ Logic Threshold, Low | V_{IL} | V_{SS} | — | $0.2 V_{DD}$ | V | |
| $\overline{\text{CS}}$ Input Current, Low | I_{CSL} | — | 0.01 | — | μA | $\overline{\text{CS}} = V_{SS}$ |
| CS High Specifications | | | | | | |
| $\overline{\text{CS}}$ Logic Threshold, High | V_{IH} | $0.8 V_{DD}$ | — | V_{DD} | V | |
| $\overline{\text{CS}}$ Input Current, High | I_{CSH} | — | 0.7 | 2 | μA | $\overline{\text{CS}} = V_{DD}$ |
| GND Current per Amplifier | I_{SS} | — | -0.7 | — | μA | $\overline{\text{CS}} = V_{DD}$ |
| Amplifier Output Leakage | — | — | 0.01 | — | μA | $\overline{\text{CS}} = V_{DD}$ |
| Dynamic Specifications (Note 1) | | | | | | |
| $\overline{\text{CS}}$ Low to Valid Amplifier Output, Turn-on Time | t_{ON} | — | 4 | 10 | μs | $\overline{\text{CS}}\text{ Low} \leq 0.2 V_{DD}$, $G = +1\text{ V/V}$, $V_{IN} = V_{DD}/2$, $V_{OUT} = 0.9 V_{DD}/2$, $V_{DD} = 5.0\text{V}$ |
| $\overline{\text{CS}}$ High to Amplifier Output High-Z | t_{OFF} | — | 0.01 | — | μs | $\overline{\text{CS}}\text{ High} \geq 0.8 V_{DD}$, $G = +1\text{ V/V}$, $V_{IN} = V_{DD}/2$, $V_{OUT} = 0.1 V_{DD}/2$ |
| Hysteresis | V_{HYST} | — | 0.6 | — | V | $V_{DD} = 5\text{V}$ |

Note 1: The input condition (V_{IN}) specified applies to both op amp A and B of the MCP6285. The dynamic specification is tested at the output of op amp B (V_{OUTB}).



FIGURE 1-1: Timing Diagram for the Chip Select ($\overline{\text{CS}}$) pin on the MCP6283 and MCP6285.

MCP6281/1R/2/3/4/5

TEMPERATURE SPECIFICATIONS

| Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +2.2V$ to $+5.5V$ and $V_{SS} = GND$. | | | | | | |
|--|---------------|-----|-----|------|-------|------------|
| Parameters | Sym | Min | Typ | Max | Units | Conditions |
| Temperature Ranges | | | | | | |
| Operating Temperature Range | T_A | -40 | — | +125 | °C | Note |
| Storage Temperature Range | T_A | -65 | — | +150 | °C | |
| Thermal Package Resistances | | | | | | |
| Thermal Resistance, 5L-SOT-23 | θ_{JA} | — | 256 | — | °C/W | |
| Thermal Resistance, 6L-SOT-23 | θ_{JA} | — | 230 | — | °C/W | |
| Thermal Resistance, 8L-PDIP | θ_{JA} | — | 85 | — | °C/W | |
| Thermal Resistance, 8L-SOIC | θ_{JA} | — | 163 | — | °C/W | |
| Thermal Resistance, 8L-MSOP | θ_{JA} | — | 206 | — | °C/W | |
| Thermal Resistance, 14L-PDIP | θ_{JA} | — | 70 | — | °C/W | |
| Thermal Resistance, 14L-SOIC | θ_{JA} | — | 120 | — | °C/W | |
| Thermal Resistance, 14L-TSSOP | θ_{JA} | — | 100 | — | °C/W | |

Note: The Junction Temperature (T_J) must not exceed the Absolute Maximum specification of $+150^\circ\text{C}$.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in [Figure 1-2](#) and [Figure 1-2](#). The bypass capacitors are laid out according to the rules discussed in [Section 4.6 “Supply Bypass”](#).



FIGURE 1-2: AC and DC Test Circuit for Most Non-Inverting Gain Conditions.



FIGURE 1-3: AC and DC Test Circuit for Most Inverting Gain Conditions.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+6.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and CS is tied low.

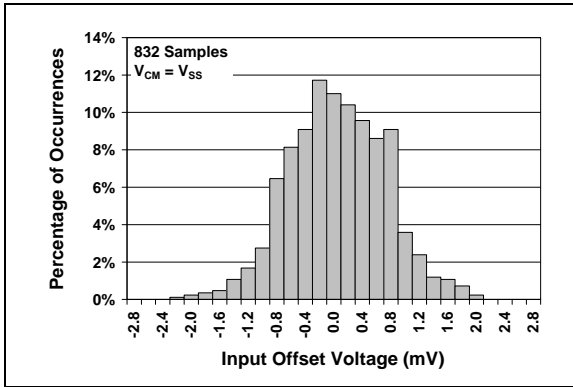


FIGURE 2-1: Input Offset Voltage.

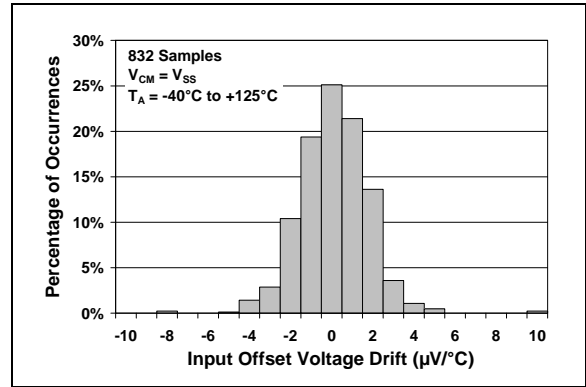


FIGURE 2-4: Input Offset Voltage Drift.

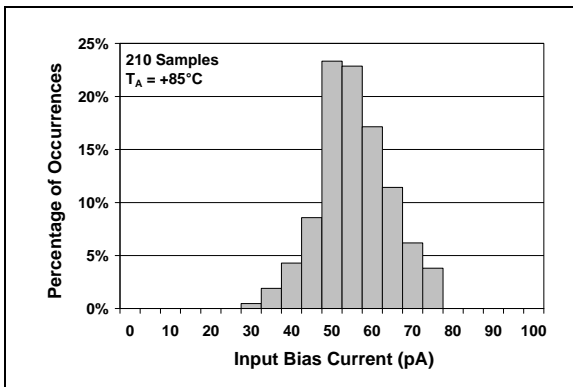


FIGURE 2-2: Input Bias Current at $T_A = +85^\circ\text{C}$.

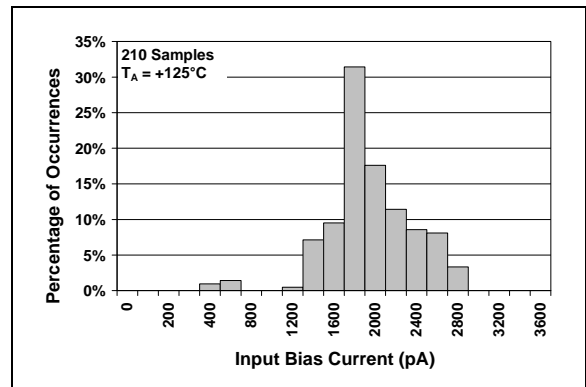


FIGURE 2-5: Input Bias Current at $T_A = +125^\circ\text{C}$.

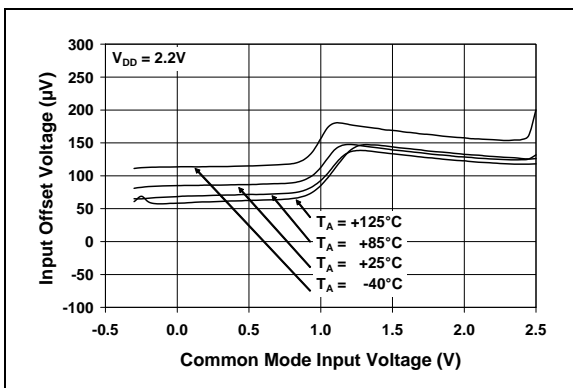


FIGURE 2-3: Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD} = 2.2\text{V}$.

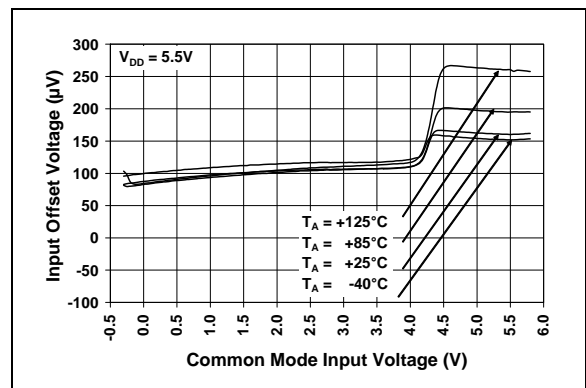


FIGURE 2-6: Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD} = 5.5\text{V}$.

MCP6281/1R/2/3/4/5

TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+6.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and CS is tied low.



FIGURE 2-7: Input Offset Voltage vs. Output Voltage.



FIGURE 2-10: Input Bias, Input Offset Currents vs. Ambient Temperature.



FIGURE 2-8: CMRR, PSRR vs. Frequency.



FIGURE 2-11: CMRR, PSRR vs. Ambient Temperature.



FIGURE 2-9: Input Bias, Offset Currents vs. Common Mode Input Voltage at $T_A = +85^\circ\text{C}$.



FIGURE 2-12: Input Bias, Offset Currents vs. Common Mode Input Voltage at $T_A = +125^\circ\text{C}$.

TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+6.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and CS is tied low.



FIGURE 2-13: Quiescent Current vs. Power Supply Voltage.



FIGURE 2-16: Output Voltage Headroom vs. Output Current Magnitude.



FIGURE 2-14: Open-Loop Gain, Phase vs. Frequency.



FIGURE 2-17: Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.

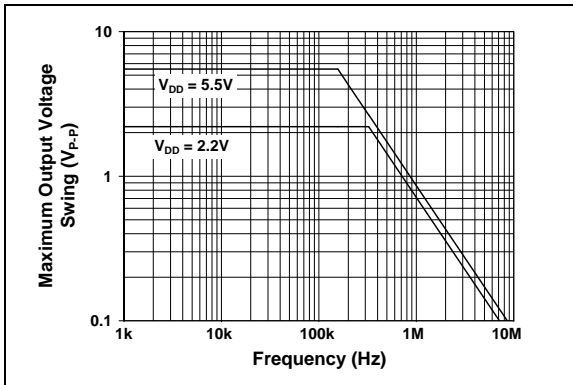


FIGURE 2-15: Maximum Output Voltage Swing vs. Frequency.

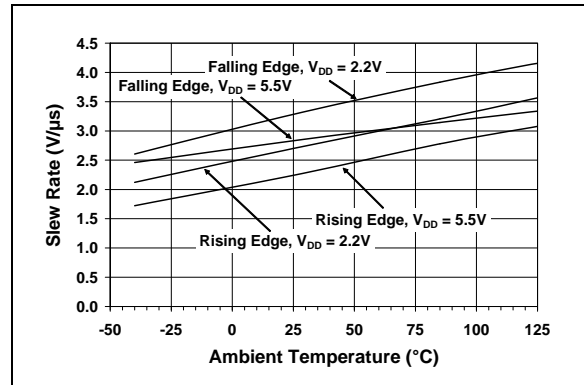


FIGURE 2-18: Slew Rate vs. Ambient Temperature.

MCP6281/1R/2/3/4/5

TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+6.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and $\overline{\text{CS}}$ is tied low.



FIGURE 2-19: Input Noise Voltage Density vs. Frequency.



FIGURE 2-22: Input Noise Voltage Density vs. Common Mode Input Voltage at 1 kHz.



FIGURE 2-20: Output Short Circuit Current vs. Power Supply Voltage.



FIGURE 2-23: Channel-to-Channel Separation vs. Frequency (MCP6282 and MCP6284 only).

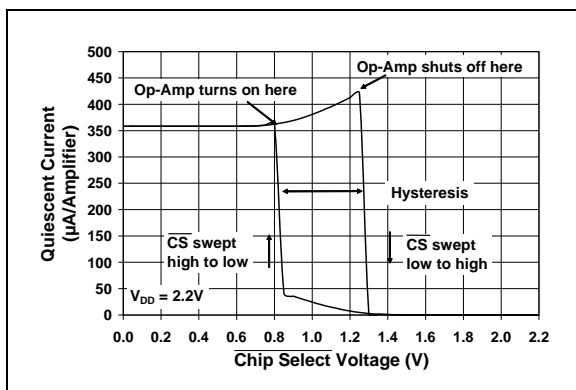


FIGURE 2-21: Quiescent Current vs. Chip Select ($\overline{\text{CS}}$) Voltage at $V_{DD} = 2.2\text{V}$ (MCP6283 and MCP6285 only).

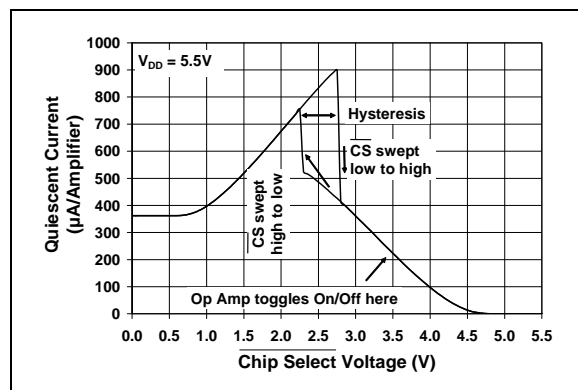


FIGURE 2-24: Quiescent Current vs. Chip Select ($\overline{\text{CS}}$) Voltage at $V_{DD} = 5.5\text{V}$ (MCP6283 and MCP6285 only).

TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+6.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and $\overline{\text{CS}}$ is tied low.



FIGURE 2-25: Large-Signal, Non-inverting Pulse Response.



FIGURE 2-28: Large-Signal, Inverting Pulse Response.



FIGURE 2-26: Small-Signal, Non-inverting Pulse Response.



FIGURE 2-29: Small-Signal, Inverting Pulse Response.



FIGURE 2-27: Chip Select ($\overline{\text{CS}}$) to Amplifier Output Response Time at $V_{DD} = 2.2\text{V}$ (MCP6283 and MCP6285 only).



FIGURE 2-30: Chip Select ($\overline{\text{CS}}$) to Amplifier Output Response Time at $V_{DD} = 5.5\text{V}$ (MCP6283 and MCP6285 only).

MCP6281/1R/2/3/4/5

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.2\text{V}$ to $+6.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to V_L , $C_L = 60\text{ pF}$ and CS is tied low.

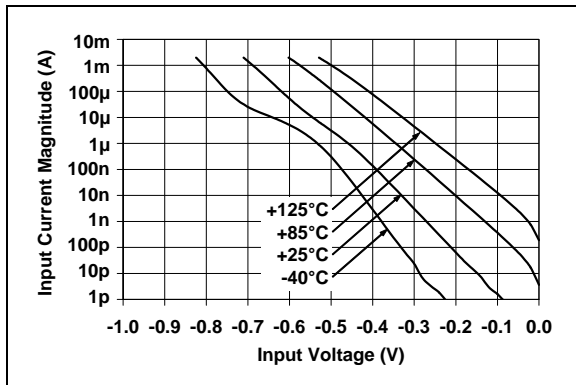


FIGURE 2-31: Measured Input Current vs. Input Voltage (below V_{SS}).

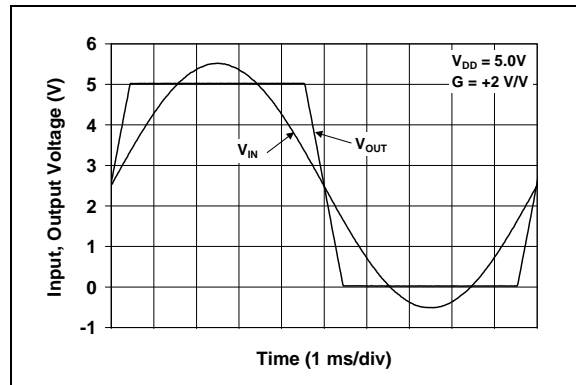


FIGURE 2-32: The MCP6281/1R/2/3/4/5 Show No Phase Reversal.

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#) (single op amps) and [Table 3-2](#) (dual and quad op amps).

TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS

| MCP6281 | | MCP6281R | MCP6283 | | Symbol | Description |
|------------------|----------|----------|------------------|----------|-----------|------------------------|
| PDIP, SOIC, MSOP | SOT-23-5 | SOT-23-5 | PDIP, SOIC, MSOP | SOT-23-6 | | |
| 6 | 1 | 1 | 6 | 1 | V_{OUT} | Analog Output |
| 2 | 4 | 4 | 2 | 4 | V_{IN-} | Inverting Input |
| 3 | 3 | 3 | 3 | 3 | V_{IN+} | Non-inverting Input |
| 7 | 5 | 2 | 7 | 6 | V_{DD} | Positive Power Supply |
| 4 | 2 | 5 | 4 | 2 | V_{SS} | Negative Power Supply |
| — | — | — | 8 | 5 | CS | Chip Select |
| 1,5,8 | — | — | 1,5 | — | NC | No Internal Connection |

TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS

| MCP6282 | MCP6284 | MCP6285 | Symbol | Description |
|------------------|-------------------|------------------|---------------------|---|
| PDIP, SOIC, MSOP | PDIP, SOIC, TSSOP | PDIP, SOIC, MSOP | | |
| 1 | 1 | — | V_{OUTA} | Analog Output (op amp A) |
| 2 | 2 | 2 | V_{INA-} | Inverting Input (op amp A) |
| 3 | 3 | 3 | V_{INA+} | Non-inverting Input (op amp A) |
| 8 | 4 | 8 | V_{DD} | Positive Power Supply |
| 5 | 5 | — | V_{INB+} | Non-inverting Input (op amp B) |
| 6 | 6 | 6 | V_{INB-} | Inverting Input (op amp B) |
| 7 | 7 | 7 | V_{OUTB} | Analog Output (op amp B) |
| — | 8 | — | V_{OUTC} | Analog Output (op amp C) |
| — | 9 | — | V_{INC-} | Inverting Input (op amp C) |
| — | 10 | — | V_{INC+} | Non-inverting Input (op amp C) |
| 4 | 11 | 4 | V_{SS} | Negative Power Supply |
| — | 12 | — | V_{IND+} | Non-inverting Input (op amp D) |
| — | 13 | — | V_{IND-} | Inverting Input (op amp D) |
| — | 14 | — | V_{OUTD} | Analog Output (op amp D) |
| — | — | 1 | V_{OUTA}/V_{INB+} | Analog Output (op amp A)/Non-inverting Input (op amp B) |
| — | — | 5 | CS | Chip Select |

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 MCP6285's V_{OUTA}/V_{INB+} Pin

For the MCP6285 only, the output of op amp A is connected directly to the non-inverting input of op amp B; this is the V_{OUTA}/V_{INB+} pin. This connection makes it possible to provide a Chip Select pin for duals in 8-pin packages.

3.4 Chip Select Digital Input (\overline{CS})

This is a CMOS, Schmitt-triggered input that places the part into a low-power mode of operation.

3.5 Power Supply Pins

The positive power supply (V_{DD}) is 2.2V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD} .

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

MCP6281/1R/2/3/4/5

4.0 APPLICATION INFORMATION

The MCP6281/1R/2/3/4/5 family of op amps is manufactured using Microchip's state-of-the-art CMOS process. This family is specifically designed for low-cost, low-power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6281/1R/2/3/4/5 ideal for battery-powered applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6281/1R/2/3/4/5 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-32 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS} . They also clamp any voltages that go too far above V_{DD} ; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

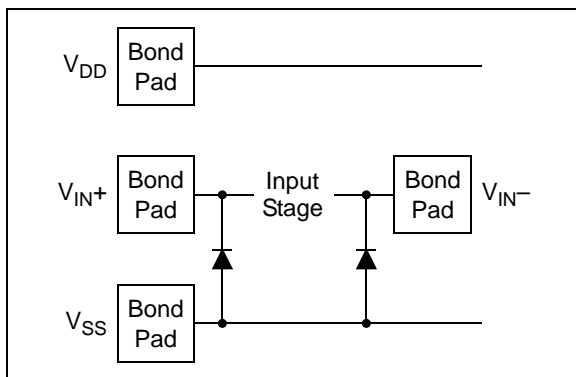


FIGURE 4-1: Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the V_{IN+} and V_{IN-} pins (see **Absolute Maximum Ratings** † at the beginning of **Section 1.0 “Electrical Characteristics”**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN+} and V_{IN-}) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN+} and V_{IN-}) from going too far above

V_{DD} , and dump any currents onto V_{DD} . When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2 .

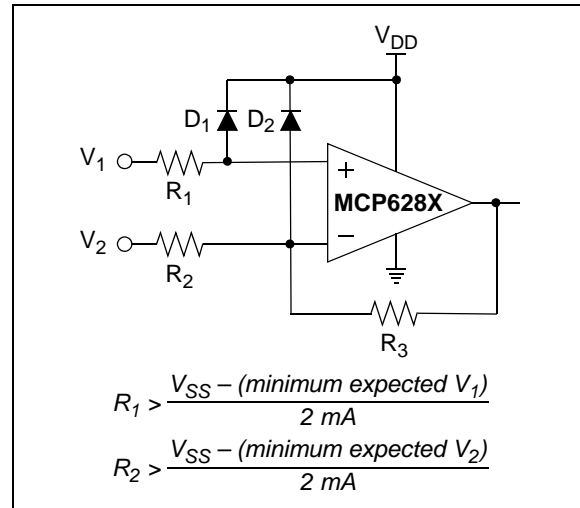


FIGURE 4-2: Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of resistors R_1 and R_2 . In this case, current through the diodes D_1 and D_2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN+} and V_{IN-}) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-31. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6281/1R/2/3/4/5 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}), while the other operates at high V_{CM} . With this topology, the device operates with V_{CM} up to 0.3V above V_{DD} and 0.3V below V_{SS} .

There is a transition in input behavior as V_{CM} is changed. It occurs when V_{CM} is near $V_{DD} - 1.2V$ (see Figure 2-3 and Figure 2-6). For the best distortion performance with non-inverting gains, avoid these regions of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6281/1R/2/3/4/5 op amp is $V_{DD} - 15 \text{ mV}$ (min.) and $V_{SS} + 15 \text{ mV}$ (max.) when $R_L = 10 \text{ k}\Omega$ is connected to $V_{DD}/2$ and $V_{DD} = 5.5\text{V}$. Refer to [Figure 2-16](#) for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer ($G = +1$) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., $> 100 \text{ pF}$ when $G = +1$), a small series resistor at the output (R_{ISO} in [Figure 4-3](#)) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will generally be lower than the bandwidth with no capacitive load.

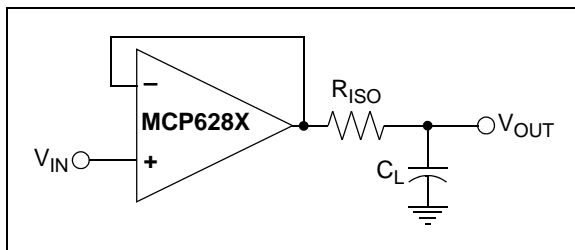


FIGURE 4-3: Output Resistor, R_{ISO} stabilizes large capacitive loads.

[Figure 4-4](#) gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the circuit's Signal Gain are equal. For inverting gains, G_N is $1 + |\text{Signal Gain}|$ (e.g., -1 V/V gives $G_N = +2 \text{ V/V}$).

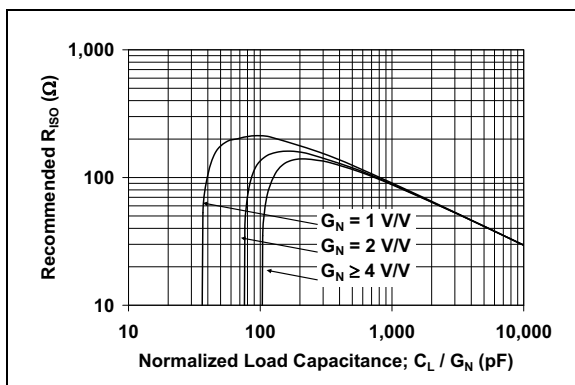


FIGURE 4-4: Recommended R_{ISO} Values for Capacitive Loads.

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO} 's value until the response is reasonable. Bench evaluation and simulations with the MCP6281/1R/2/3/4/5 SPICE macro model are helpful.

4.4 MCP628X Chip Select (\overline{CS})

The MCP6283 and MCP6285 are single and dual op amps with Chip Select (\overline{CS}), respectively. When \overline{CS} is pulled high, the supply current drops to $0.7 \mu\text{A}$ (typical) and flows through the \overline{CS} pin to V_{SS} . When this happens, the amplifier output is put into a high-impedance state. By pulling \overline{CS} low, the amplifier is enabled. The \overline{CS} pin has an internal $5 \text{ M}\Omega$ (typical) pull-down resistor connected to V_{SS} , so it will go low if the \overline{CS} pin is left floating. [Figure 1-1](#) shows the output voltage and supply current response to a \overline{CS} pulse.

4.5 Cascaded Dual Op Amps (MCP6285)

The MCP6285 is a dual op amp with Chip Select (\overline{CS}). The Chip Select input is available on what would be the non-inverting input of a standard dual op amp (pin 5). This pin is available because the output of op amp A connects to the non-inverting input of op amp B, as shown in [Figure 4-5](#). The Chip Select input, which can be connected to a microcontroller I/O line, puts the device in Low-power mode. Refer to [Section 4.4 "MCP628X Chip Select \(CS\)"](#).



FIGURE 4-5: Cascaded Gain Amplifier.

The output of op amp A is loaded by the input impedance of op amp B, which is typically $10^{13}\Omega || 6 \text{ pF}$, as specified in the DC specification table (Refer to [Section 4.3 "Capacitive Loads"](#) for further details regarding capacitive loads).

The common mode input range of these op amps is specified in the data sheet as $V_{SS} - 300 \text{ mV}$ and $V_{DD} + 300 \text{ mV}$. However, since the output of op amp A is limited to V_{OL} and V_{OH} (20 mV from the rails with a $10 \text{ k}\Omega$ load), the non-inverting input range of op amp B is limited to the common mode input range of $V_{SS} + 20 \text{ mV}$ and $V_{DD} - 20 \text{ mV}$.

MCP6281/1R/2/3/4/5

4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good, high-frequency performance. It also needs a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP6284) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



FIGURE 4-6: Unused Op Amps.

4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6281/1R/2/3/4/5 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.



FIGURE 4-7: Example Guard Ring Layout for Inverting Gain.

1. For Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
 - a. Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
 - b. Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.
2. Non-inverting Gain and Unity-Gain Buffer:
 - a. Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.
 - b. Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the common mode input voltage.

4.9 Application Circuits

4.9.1 SALLEN-KEY HIGH-PASS FILTER

The MCP6281/1R/2/3/4/5 op amps can be used in active-filter applications. Figure 4-8 shows a second-order Sallen-Key high-pass filter with a gain of 1. The output bias voltage is set by the $V_{DD}/2$ reference, which can be changed to any voltage within the output voltage range.



FIGURE 4-8: Sallen-Key High-Pass Filter.

This filter, and others, can be designed using Microchip's Design Aids; see Section 5.2 "FilterLab® Software" and Section 5.3 "Mindi™ Circuit Designer & Simulator".

4.9.2 INVERTING MILLER INTEGRATOR

Analog integrators are used in filters, control loops and measurement circuits. Figure 4-9 shows the most common implementation, the inverting Miller integrator. The non-inverting input is at $V_{DD}/2$ so that the op amp properly biases up. The switch (SW) is used to zero the output in some applications. Other applications use a feedback loop to keep the output within its linear range of operation.

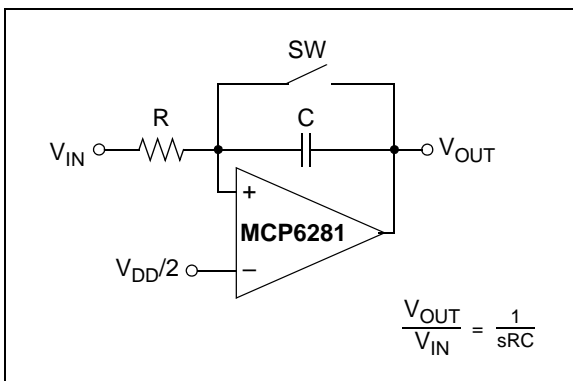


FIGURE 4-9: Miller Integrator.

4.9.3 CASCADED OP AMP APPLICATIONS

The MCP6285 provides the flexibility of Low-power mode for dual op amps in an 8-pin package. The MCP6285 eliminates the added cost and space in battery-powered applications by using two single op amps with Chip Select lines or a 10-pin device with one Chip Select line for both op amps. Since the two op amps are internally cascaded, this device cannot be used in circuits that require active or passive elements between the two op amps. However, there are several applications where this op amp configuration with Chip Select line becomes suitable. The circuits below show possible applications for this device.

4.9.3.1 Load Isolation

With the cascaded op amp configuration, op amp B can be used to isolate the load from op amp A. In applications where op amp A is driving capacitive or low resistance loads in the feedback loop (such as an integrator circuit or filter circuit), the op amp may not have sufficient source current to drive the load. In this case, op amp B can be used as a buffer.

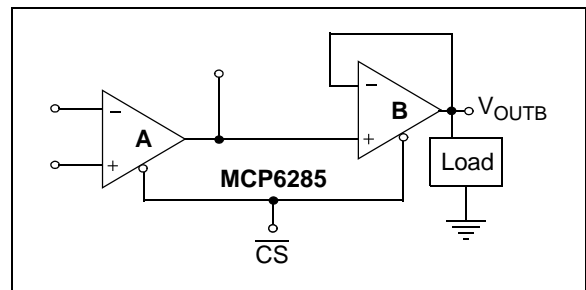


FIGURE 4-10: Isolating the Load with a Buffer.

4.9.3.2 Cascaded Gain

Figure 4-11 shows a cascaded gain circuit configuration with Chip Select. Op amps A and B are configured in a non-inverting amplifier configuration. In this configuration, it is important to note that the input offset voltage of op amp A is amplified by the gain of op amp A and B, as shown below:

$$V_{OUT} = V_{IN}G_A G_B + V_{OSA}G_A G_B + V_{OSB}G_B$$

Where:

- G_A = op amp A gain
- G_B = op amp B gain
- V_{OSA} = op amp A input offset voltage
- V_{OSB} = op amp B input offset voltage

Therefore, it is recommended to set most of the gain with op amp A and use op amp B with relatively small gain (e.g., a unity-gain buffer).

MCP6281/1R/2/3/4/5



FIGURE 4-11: Cascaded Gain Circuit Configuration.

4.9.3.3 Difference Amplifier

Figure 4-12 shows op amp A configured as a difference amplifier with Chip Select. In this configuration, it is recommended to use well-matched resistors (e.g., 0.1%) to increase the Common Mode Rejection Ratio (CMRR). Op amp B can be used to provide additional gain and isolate the load from the difference amplifier.



FIGURE 4-12: Difference Amplifier Circuit.

4.9.3.4 Buffered Non-inverting Integrator

Figure 4-13 shows a lossy non-inverting integrator that is buffered and has a Chip Select input. Op amp A is configured as a non-inverting integrator. In this configuration, matching the impedance at each input is recommended. R_F is used to provide a feedback loop at frequencies $\ll 1/(2\pi R_1 C_1)$ and makes this a lossy integrator (it has a finite gain at DC). Op amp B is used to isolate the load from the integrator.



FIGURE 4-13: Buffered Non-inverting Integrator with Chip Select.

4.9.3.5 Inverting Integrator with Active Compensation and Chip Select

Figure 4-14 uses an active compensator (op amp B) to compensate for the non-ideal op amp characteristics introduced at higher frequencies. This circuit uses op amp B as a unity-gain buffer to isolate the integration capacitor C_1 from op amp A and drives the capacitor with low-impedance source. Since both op amps are matched very well, they provide a higher quality integrator.

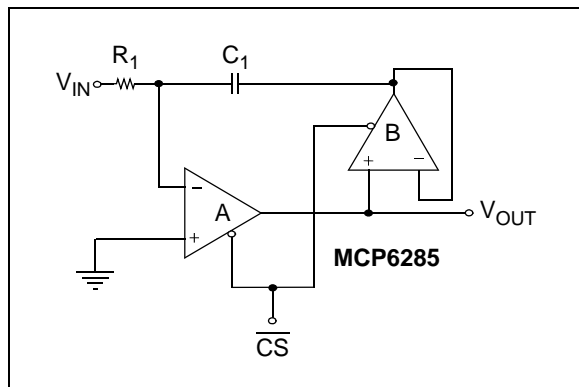


FIGURE 4-14: Integrator Circuit with Active Compensation.

4.9.3.6 Second-Order MFB Low-Pass Filter with an Extra Pole-Zero Pair

Figure 4-15 is a second-order multiple feedback low-pass filter with Chip Select. Use the FilterLab[®] software from Microchip to determine the R and C values for the op amp A's second-order filter. Op amp B can be used to add a pole-zero pair using C_3 , R_6 , and R_7 .



FIGURE 4-15: Second-Order Multiple Feedback Low-Pass Filter with an Extra Pole-Zero Pair.

4.9.3.7 Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair

Figure 4-16 is a second-order Sallen-Key low-pass filter with Chip Select. Use the FilterLab[®] software from Microchip to determine the R and C values for the op amp A's second-order filter. Op amp B can be used to add a pole-zero pair using C₃, R₅ and R₆.

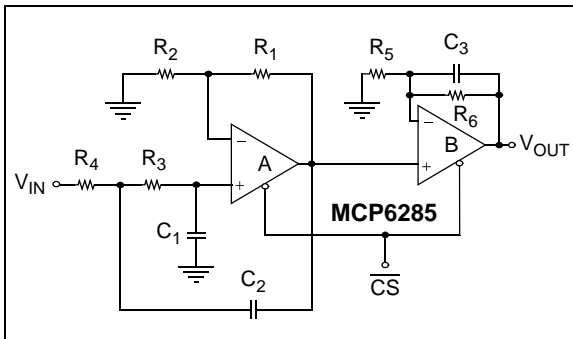


FIGURE 4-16: Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair and Chip Select.

4.9.3.8 Capacitorless Second-Order Low-Pass filter with Chip Select

The low-pass filter shown in Figure 4-17 does not require external capacitors and uses only three external resistors; the op amp's GBWP sets the corner frequency. R₁ and R₂ are used to set the circuit gain and R₃ is used to set the Q. To avoid gain peaking in the frequency response, Q needs to be low (lower values need to be selected for R₃). Note that the amplifier bandwidth varies greatly over temperature and process. However, this configuration provides a low-cost solution for applications with high bandwidth requirements.

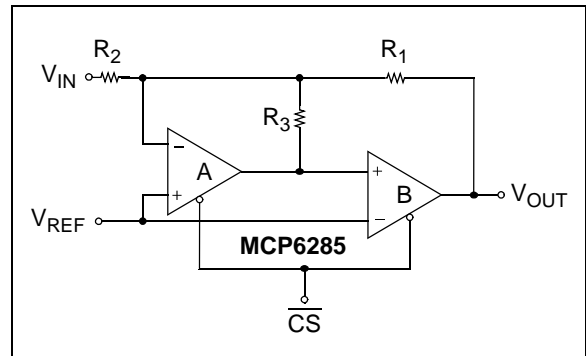


FIGURE 4-17: Capacitorless Second-Order Low-Pass Filter with Chip Select.

MCP6281/1R/2/3/4/5

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6281/1R/2/3/4/5 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6281/1R/2/3/4/5 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab[®] Software

Microchip's FilterLab[®] software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi[™] Circuit Designer & Simulator

Microchip's Mindi[™] Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- **P/N SOIC8EV:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board*
- **P/N SOIC14EV:** *14-Pin SOIC/TSSOP/DIP Evaluation Board*

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications"*, DS00722

AN723: *"Operational Amplifier AC Specifications and Applications"*, DS00723

AN884: *"Driving Capacitive Loads With Op Amps"*, DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990

These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

5-Lead SOT-23 (MCP6281 and MCP6281R)



| Device | Code |
|----------|------|
| MCP6281 | CHNN |
| MCP6281R | EUNN |

Note: Applies to 5-Lead SOT-23.

Example:



6-Lead SOT-23 (MCP6283)



Example:



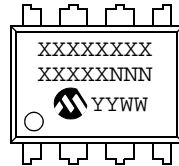
8-Lead MSOP



Example:



8-Lead PDIP (300 mil)



Example:



OR



| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP6281/1R/2/3/4/5

Package Marking Information (Continued)

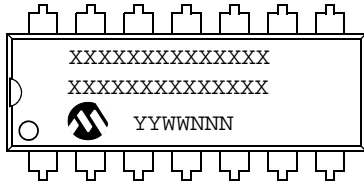
8-Lead SOIC (150 mil)



Example:



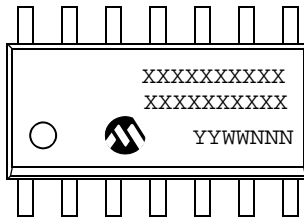
14-Lead PDIP (300 mil) (MCP6284)



Example:



14-Lead SOIC (150 mil) (MCP6284)



Example:



14-Lead TSSOP (MCP6284)



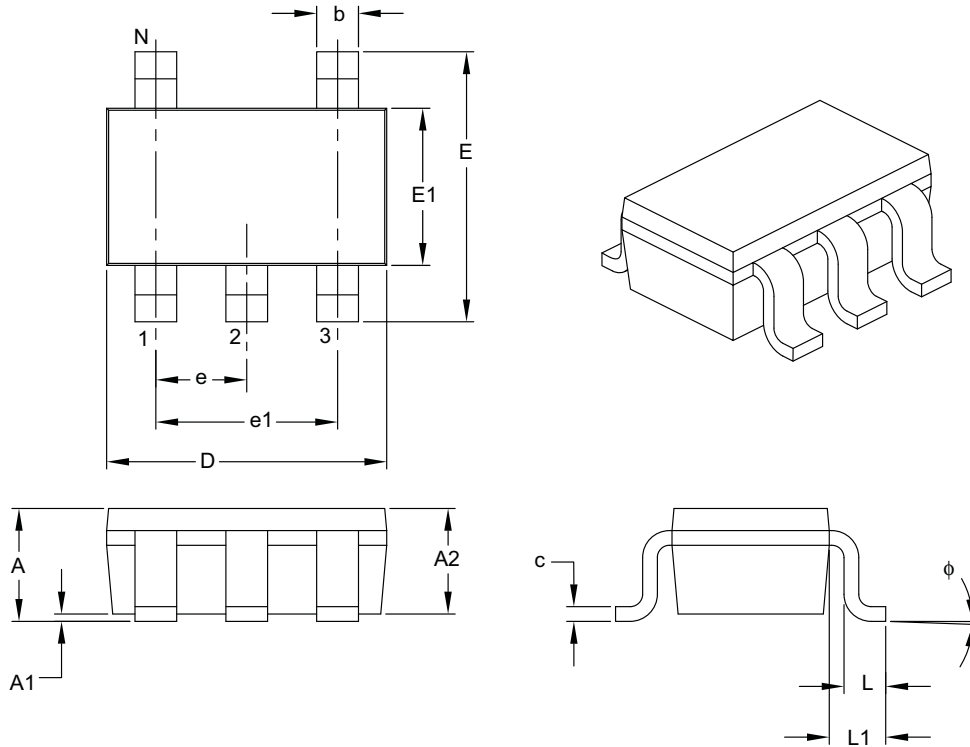
Example:



MCP6281/1R/2/3/4/5

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 5 | | |
| Lead Pitch | e | 0.95 BSC | | |
| Outside Lead Pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | – | 1.45 |
| Molded Package Thickness | A2 | 0.89 | – | 1.30 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | 2.20 | – | 3.20 |
| Molded Package Width | E1 | 1.30 | – | 1.80 |
| Overall Length | D | 2.70 | – | 3.10 |
| Foot Length | L | 0.10 | – | 0.60 |
| Footprint | L1 | 0.35 | – | 0.80 |
| Foot Angle | ϕ | 0° | – | 30° |
| Lead Thickness | c | 0.08 | – | 0.26 |
| Lead Width | b | 0.20 | – | 0.51 |

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

MCP6281/1R/2/3/4/5

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 6 | | |
| Pitch | e | 0.95 BSC | | |
| Outside Lead Pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | - | 1.30 |
| Standoff | A1 | 0.00 | - | 0.15 |
| Overall Width | E | 2.20 | - | 3.20 |
| Molded Package Width | E1 | 1.30 | - | 1.80 |
| Overall Length | D | 2.70 | - | 3.10 |
| Foot Length | L | 0.10 | - | 0.60 |
| Footprint | L1 | 0.35 | - | 0.80 |
| Foot Angle | ϕ | 0° | - | 30° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

Notes:

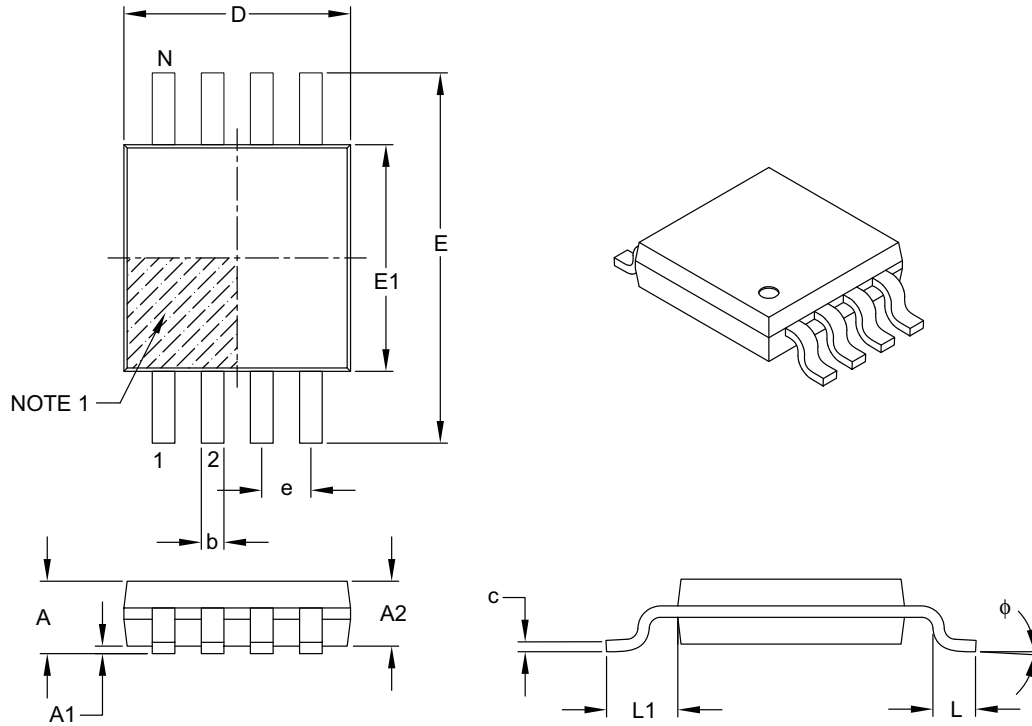
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

MCP6281/1R/2/3/4/5

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | 4.90 BSC | | |
| Molded Package Width | E1 | 3.00 BSC | | |
| Overall Length | D | 3.00 BSC | | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | 0.95 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

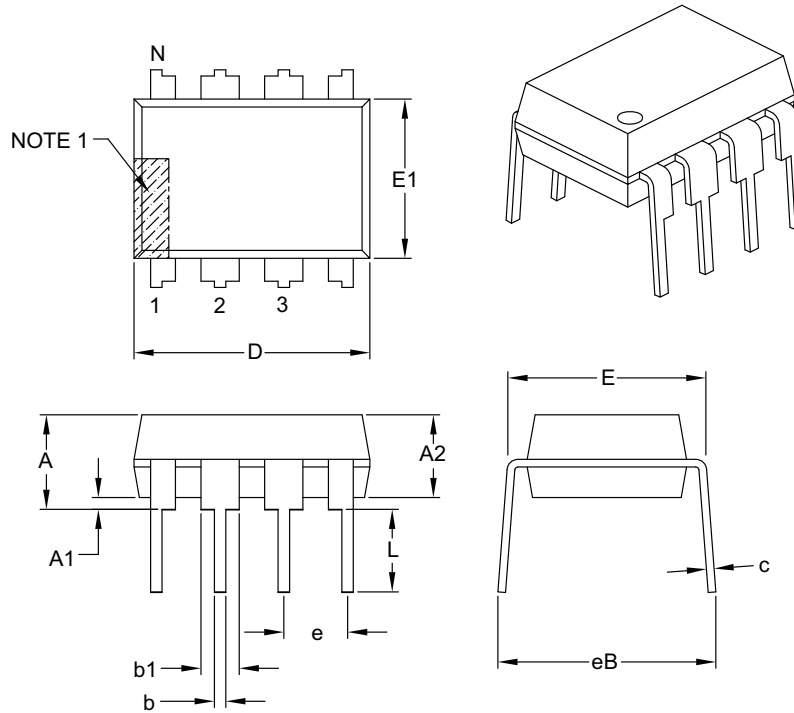
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

MCP6281/1R/2/3/4/5

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | INCHES | | |
|----------------------------|----|-------|----------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | | |
| Pitch | e | | .100 BSC | | |
| Top to Seating Plane | A | – | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 | |
| Base to Seating Plane | A1 | .015 | – | – | |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 | |
| Molded Package Width | E1 | .240 | .250 | .280 | |
| Overall Length | D | .348 | .365 | .400 | |
| Tip to Seating Plane | L | .115 | .130 | .150 | |
| Lead Thickness | c | .008 | .010 | .015 | |
| Upper Lead Width | b1 | .040 | .060 | .070 | |
| Lower Lead Width | b | .014 | .018 | .022 | |
| Overall Row Spacing § | eB | – | – | – | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

MCP6281/1R/2/3/4/5

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES | | |
|----------------------------|-------|----------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 14 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .735 | .750 | .775 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

MCP6281/1R/2/3/4/5

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

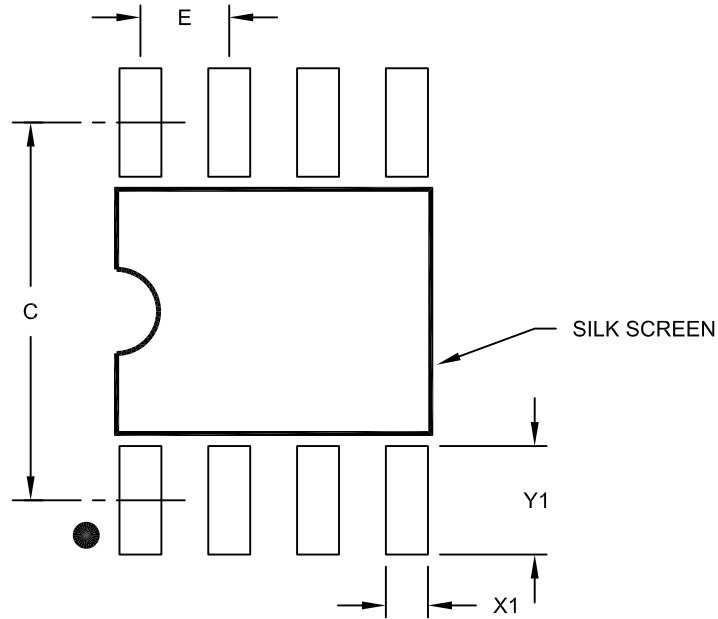
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

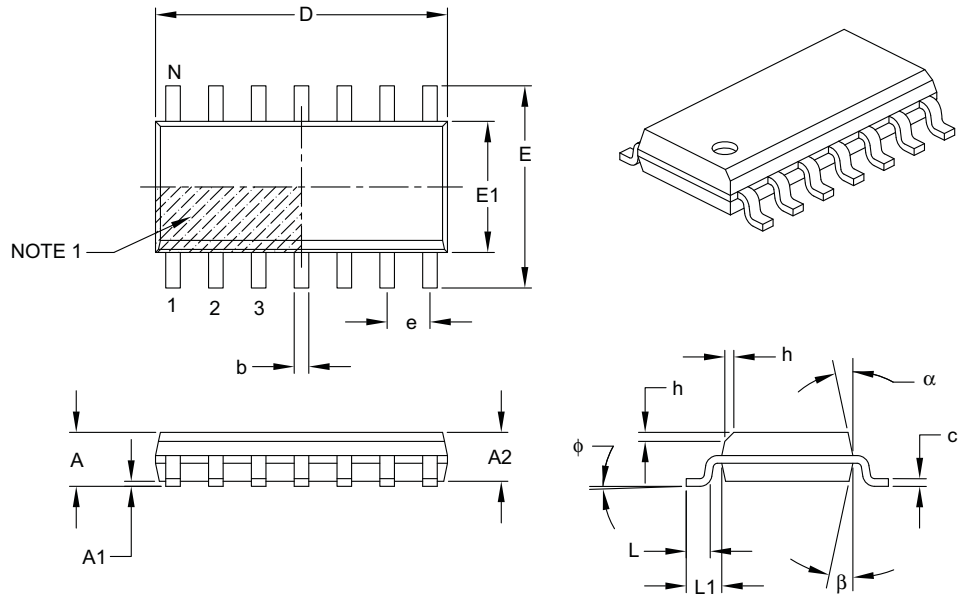
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

MCP6281/1R/2/3/4/5

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 14 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 8.65 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

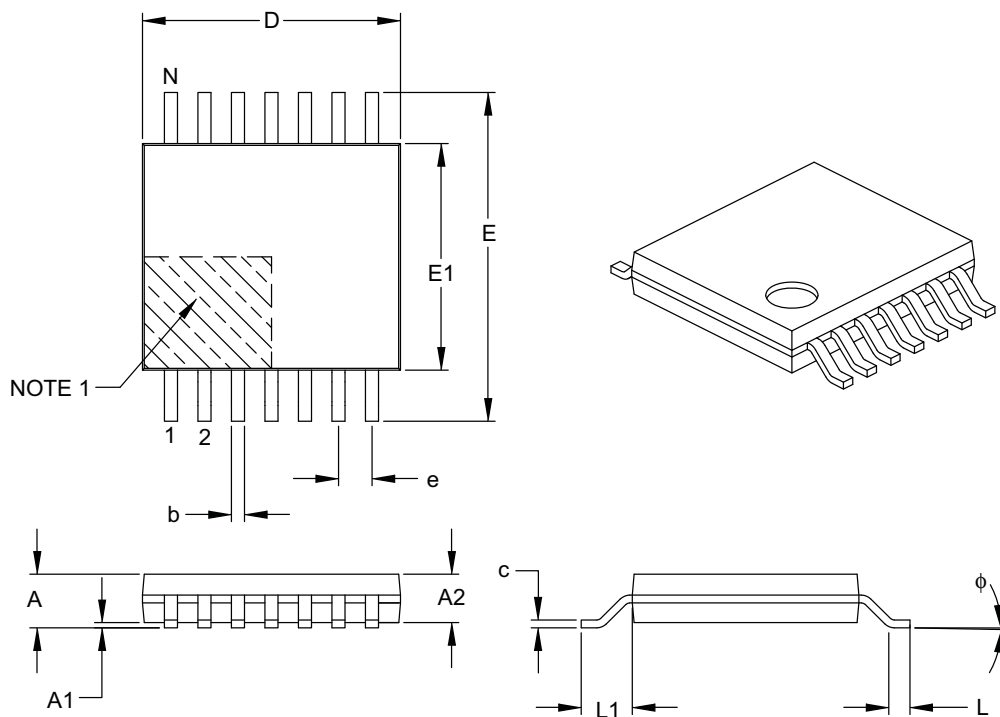
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

MCP6281/1R/2/3/4/5

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 14 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | 6.40 BSC | | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 4.90 | 5.00 | 5.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

MCP6281/1R/2/3/4/5

NOTES:

APPENDIX A: REVISION HISTORY

Revision E (February 2008)

The following is the list of modifications:

1. Updated notes to **Section 1.0 “Electrical Characteristics”**.
2. Increased absolute maximum voltage range of input pins. Increased maximum operating supply voltage (V_{DD}).
3. Added **Section 1.1 “Test Circuits”**.
4. Added Figure 2-32.
5. Updated Table 3-1 and Table 3-2 in **Section 3.0 “Pin Descriptions”**.
6. Added **Section 4.1.1 “Phase Reversal”**, **Section 4.1.2 “Input Voltage and Current Limits”**, and **Section 4.1.3 “Normal Operation”**.
7. Added **Section 4.7 “Unused Op Amps”**.
8. Updated **Section 5.0 “Design AIDS”**.
9. Updated package outline drawings in **Section 6.0 “Packaging Information”**.

Revision D (December 2004)

The following is the list of modifications:

1. Added SOT-23-5 packages for the MCP6281 and MCP6281R single op amps.
2. Added SOT-23-6 package for the MCP6283 single op amp.
3. Added **Section 3.0 “Pin Descriptions”**.
4. Corrected application circuits (**Section 4.9 “Application Circuits”**).
5. Added SOT-23-5 and SOT-23-6 packages and corrected package marking information (**Section 6.0 “Packaging Information”**).
6. Added Appendix A: Revision History.

Revision C (June 2004)

The following is the list of modifications:

1. Undocumented changes.

Revision B (October 2003)

The following is the list of modifications:

1. Undocumented changes.

Revision A (June 2003)

- Original data sheet release.

MCP6281/1R/2/3/4/5

NOTES:

MCP6281/1R/2/3/4/5

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | — | X | /XX | |
|--------------------|-----------------|-------------------|-----|--|
| Device | | Temperature Range | | Package |
| Device: | MCP6281: | | | Single Op Amp |
| | MCP6281T: | | | Single Op Amp (Tape and Reel) (SOIC, MSOP, SOT-23-5) |
| | MCP6281RT: | | | Single Op Amp (Tape and Reel) (SOT-23-5) |
| | MCP6282: | | | Dual Op Amp |
| | MCP6282T: | | | Dual Op Amp (Tape and Reel) (SOIC, MSOP) |
| | MCP6283: | | | Single Op Amp with \overline{CS} |
| | MCP6283T: | | | Single Op Amp with \overline{CS} (Tape and Reel) (SOIC, MSOP, SOT-23-6) |
| | MCP6284: | | | Quad Op Amp |
| | MCP6284T: | | | Quad Op Amp (Tape and Reel) (SOIC, TSSOP) |
| | MCP6285: | | | Dual Op Amp with \overline{CS} |
| | MCP6285T: | | | Dual Op Amp with \overline{CS} (Tape and Reel) (SOIC, MSOP) |
| Temperature Range: | E | = | | -40°C to +125°C |
| Package: | CH | = | | Plastic Small Outline Transistor (SOT-23), 6-lead (MCP6283 only) |
| | MS | = | | Plastic MSOP, 8-lead |
| | P | = | | Plastic DIP (300 mil body), 8-lead, 14-lead |
| | OT | = | | Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6281, MCP6281R only) |
| | SL | = | | Plastic SOIC (3.90 mm body), 14-lead |
| | SN | = | | Plastic SOIC, (3.90 mm body), 8-lead |
| | ST | = | | Plastic TSSOP (4.4 mm body), 14-lead |
| Examples: | | | | |
| a) | MCP6281-E/SN: | | | Extended Temperature, 8LD SOIC package. |
| b) | MCP6281-E/MS: | | | Extended Temperature, 8LD MSOP package. |
| c) | MCP6281-E/P: | | | Extended Temperature, 8LD PDIP package. |
| d) | MCP6281T-E/OT: | | | Tape and Reel, Extended Temperature, 5LD SOT-23 package. |
| e) | MCP6281RT-E/OT: | | | Tape and Reel, Extended Temperature, 5LD SOT-23 package. |
| a) | MCP6282-E/SN: | | | Extended Temperature, 8LD SOIC package. |
| b) | MCP6282-E/MS: | | | Extended Temperature, 8LD MSOP package. |
| c) | MCP6282-E/P: | | | Extended Temperature, 8LD PDIP package. |
| d) | MCP6282T-E/SN: | | | Tape and Reel, Extended Temperature, 8LD SOIC package. |
| a) | MCP6283-E/SN: | | | Extended Temperature, 8LD SOIC package. |
| b) | MCP6283-E/MS: | | | Extended Temperature, 8LD MSOP package. |
| c) | MCP6283-E/P: | | | Extended Temperature, 8LD PDIP package. |
| d) | MCP6283T-E/CH: | | | Tape and Reel, Extended Temperature, 6LD SOT-23 package. |
| a) | MCP6284-E/P: | | | Extended Temperature, 14LD PDIP package. |
| b) | MCP6284T-E/SL: | | | Tape and Reel, Extended Temperature, 14LD SOIC package. |
| c) | MCP6284-E/SL: | | | Extended Temperature, 14LD SOIC package. |
| d) | MCP6284-E/ST: | | | Extended Temperature, 14LD TSSOP package. |
| a) | MCP6285-E/SN: | | | Extended Temperature, 8LD SOIC package. |
| b) | MCP6285-E/MS: | | | Extended Temperature, 8LD MSOP package. |
| c) | MCP6285-E/P: | | | Extended Temperature, 8LD PDIP package. |
| d) | MCP6285T-E/SN: | | | Tape and Reel, Extended Temperature, 8LD SOIC package. |

MCP6281/1R/2/3/4/5

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, rPIC and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, PICkit, PICDEM, PICDEM.net, PICtail, PIC³² logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rLAB, Select Mode, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2008, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А