

## Quad Channel Ultrasound Echo Multiplexer with T/R Switch

### Features

- ▶ Quad channel analog echo signal MUX switches
- ▶  $\pm 130\text{V}$  20ns T/R switch built-in for each channel
- ▶  $17\Omega$  total on-resistance for low insertion loss
- ▶  $0.8\text{nV}/\text{rt.Hz}$  low RF input noise at  $5\text{MHz}$
- ▶ DC to  $100\text{MHz}$  small signal bandwidth
- ▶  $-65\text{dB}$  off-Isolation and  $-55\text{dB}$  crosstalk
- ▶ Single  $+5\text{V}$  power supply
- ▶ Low power consumption
- ▶  $20\text{MHz}$  serial interface  $3.3\text{V}$  CMOS logic
- ▶  $-55\text{dB}$  HD2 very low echo signal distortions

### Applications

- ▶ Medical imaging ultrasound beamforming receiver
- ▶ Software programmable echo multiplex switching
- ▶ High resolution phase array ultrasound NDT
- ▶ Ultrasonic phase array receiver focusing
- ▶ Array PZT transducer echo phase processing

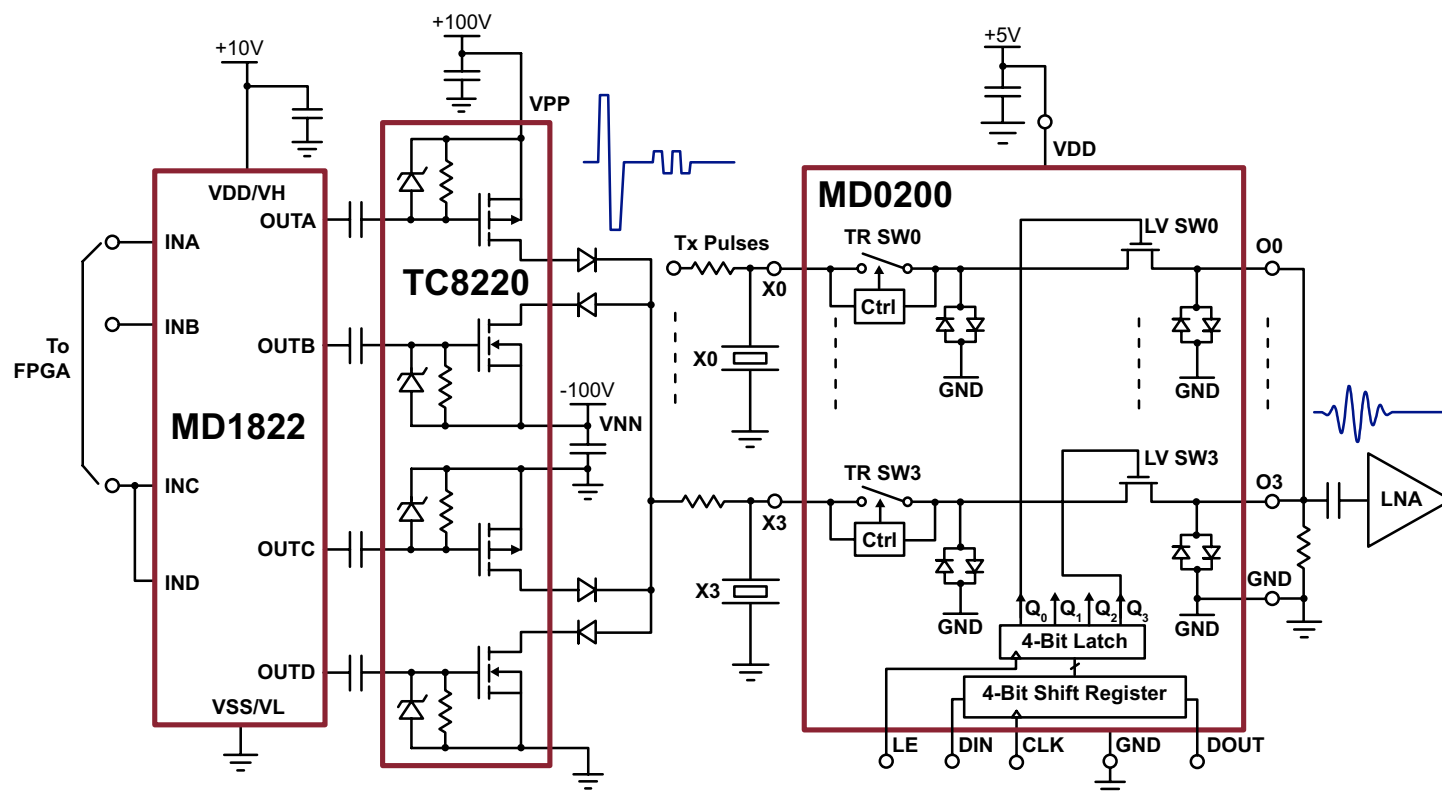
### General Description

The MD0200 is a multi-channel, low voltage, analog multiplex switch with a high voltage T/R switch and diode voltage limiter circuit. It is designed for medical ultrasound image system receive beamforming applications. It also can be used in NDT and other ultrasound applications.

The MD0200 circuit consists of a low voltage CMOS analog switch and digital logic serial interface circuits. This analog switch not only has very low insertion loss and noise and wide frequency response, it also has high isolation and low channel to channel crosstalk. The inputs of the analog switch are connected to the output of the two terminal type of ultrasound T/R switch, and two back-to-back diode voltage limiter circuits.

The shift-register and latch-register serial interface has allowed the IC maximum flexibility to connect a large number of channels together to form the echo multiplexing dynamic-focusing circuit for ultrasound image receive beamforming.

### Block Diagram



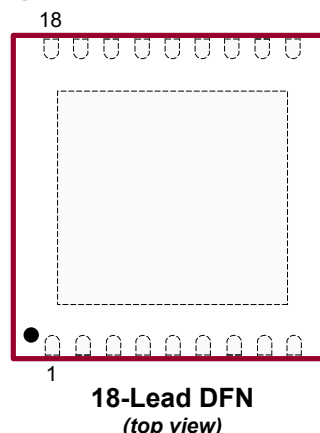
## Ordering Information

| Part Number     | Package Options   | Packing   |
|-----------------|-------------------|-----------|
| MD0200K6-G      | 18-Lead DFN (5x5) | 490/Tray  |
| MD0200K6-G M932 | 18-Lead DFN (5x5) | 2500/Reel |

-G denotes a lead (Pb)-free / RoHS compliant package



## Pin Configuration



18-Lead DFN  
(top view)

## Absolute Maximum Ratings<sup>1</sup>

| Parameter                       | Value           |
|---------------------------------|-----------------|
| GND reference voltage           | 0V              |
| X0~X3 input pins to GND voltage | 0 to $\pm 140V$ |
| V <sub>DD</sub> positive supply | -0.5V to +6.5V  |
| All logic input pins            | -0.5V to +6.5V  |
| Maximum junction temperature    | +125°C          |
| Storage temperature range       | -65°C to 150°C  |

### Note:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Typical Thermal Resistance

| Package     | $\theta_{ja}$ |
|-------------|---------------|
| 18-Lead DFN | 30°C/W        |

## Product Marking



L = Lot Number  
YY = Last Digit of Year Sealed  
WW = Code for Week Sealed  
A = Assembler ID  
C = Country of Origin  
— = "Green" Packaging

18-Lead DFN

Package may or may not include the following marks: Si or

## Operating Supply Voltages (Over operating conditions unless otherwise specified, V<sub>DD</sub> = +5V, T<sub>j</sub> = 25°C)

| Sym               | Parameter                                                       | Min  | Typ       | Max  | Unit     | Conditions                                                     |
|-------------------|-----------------------------------------------------------------|------|-----------|------|----------|----------------------------------------------------------------|
| V <sub>SIG</sub>  | Signal input range (p-p)                                        | -    | $\pm 400$ | -    | mV       | ---                                                            |
| V <sub>DD</sub>   | Positive voltage power supply                                   | 4.75 | 5.00      | 5.25 | V        | T <sub>A</sub> = 0 to 70°C                                     |
| R <sub>ON</sub>   | Total switch ON-resistance X <sub>0-3</sub> to O <sub>0-3</sub> | -    | 17.5      | -    | $\Omega$ | I <sub>X</sub> = $\pm 5.0mA$ , V <sub>X0-3</sub> = $\pm 300mV$ |
| $\Delta R_{ON}$   | Ch to Ch R <sub>ON</sub> difference                             | -    | $\pm 5$   | -    | %        | ---                                                            |
| V <sub>F</sub>    | Diode forward voltage                                           | -    | 0.8       | 1.0  | V        | 1mA                                                            |
|                   |                                                                 | -    | 1.25      | 1.50 |          | 100mA                                                          |
| I <sub>FM</sub>   | Diode forward continuous current                                | -    | 100       | -    | mA       | ---                                                            |
| I <sub>DDQ</sub>  | V <sub>DD</sub> supply current 0MHz                             | -    | 0.1       | 0.2  | mA       | f <sub>CLK</sub> = 0Hz                                         |
| I <sub>DD20</sub> | V <sub>DD</sub> supply current 20MHz                            | -    | 8.0       | 10   | mA       | f <sub>CLK</sub> = 20Hz                                        |
| HD2               | Second harmonic distortion                                      | -    | -55       | -    | dB       | 5MHz sine wave, $\pm 300mV$ p-p input                          |

## T/R Switch Characteristics (Over operating conditions unless otherwise specified, $V_{DD} = +5V$ , $T_J = 25^\circ C$ )

| Sym           | Parameter                                             | Min       | Typ       | Max       | Unit     | Conditions                                 |
|---------------|-------------------------------------------------------|-----------|-----------|-----------|----------|--------------------------------------------|
| $V_X$         | Max $X_{0-3}$ to GND input voltage                    | $\pm 130$ | -         | -         | V        | $I_X = \pm 500\mu A$                       |
| $R_{TRSW}$    | Switch ON-resistance of T/R SW $X_{0-3}$ to $O_{0-3}$ | -         | 15        | -         | $\Omega$ | $I_X = \pm 5.0mA$ , $V_{X0-3} = \pm 300mV$ |
| $V_{TRIP}$    | $VX_{0-3}$ trip point to turn off                     | -         | $\pm 1.0$ | $\pm 2.0$ | V        | ---                                        |
| $V_{OFF}$     | T/R switch turn off voltage                           | -         | $\pm 2.0$ | -         | V        | $I_{A-B} = \pm 1.0mA$                      |
| $I_{PEAK}$    | Peak T/R switch current                               | -         | $\pm 60$  | -         | mA       | ---                                        |
| $T_{OFF}$     | Turn-OFF time                                         | -         | -         | 20        | ns       | ---                                        |
| $T_{ON}$      | Turn-ON time                                          | -         | -         | 20        | ns       | ---                                        |
| $C_{SW(ON)}$  | Switch ON-capacitance                                 | -         | 15        | -         | pF       | T/R SW = ON                                |
| $C_{SW(OFF)}$ | Switch OFF-capacitance                                | -         | 9.0       | -         | pF       | $V_{(X0-3)} = \pm 25V$                     |
| BW            | Small signal bandwidth                                | -         | 100       | -         | MHz      | $R_{LOAD} = 50\Omega$                      |

## Clock and Logic I/O Characteristics (Over operating conditions unless otherwise specified, $V_{DD} = +5V$ , $T_J = 25^\circ C$ )

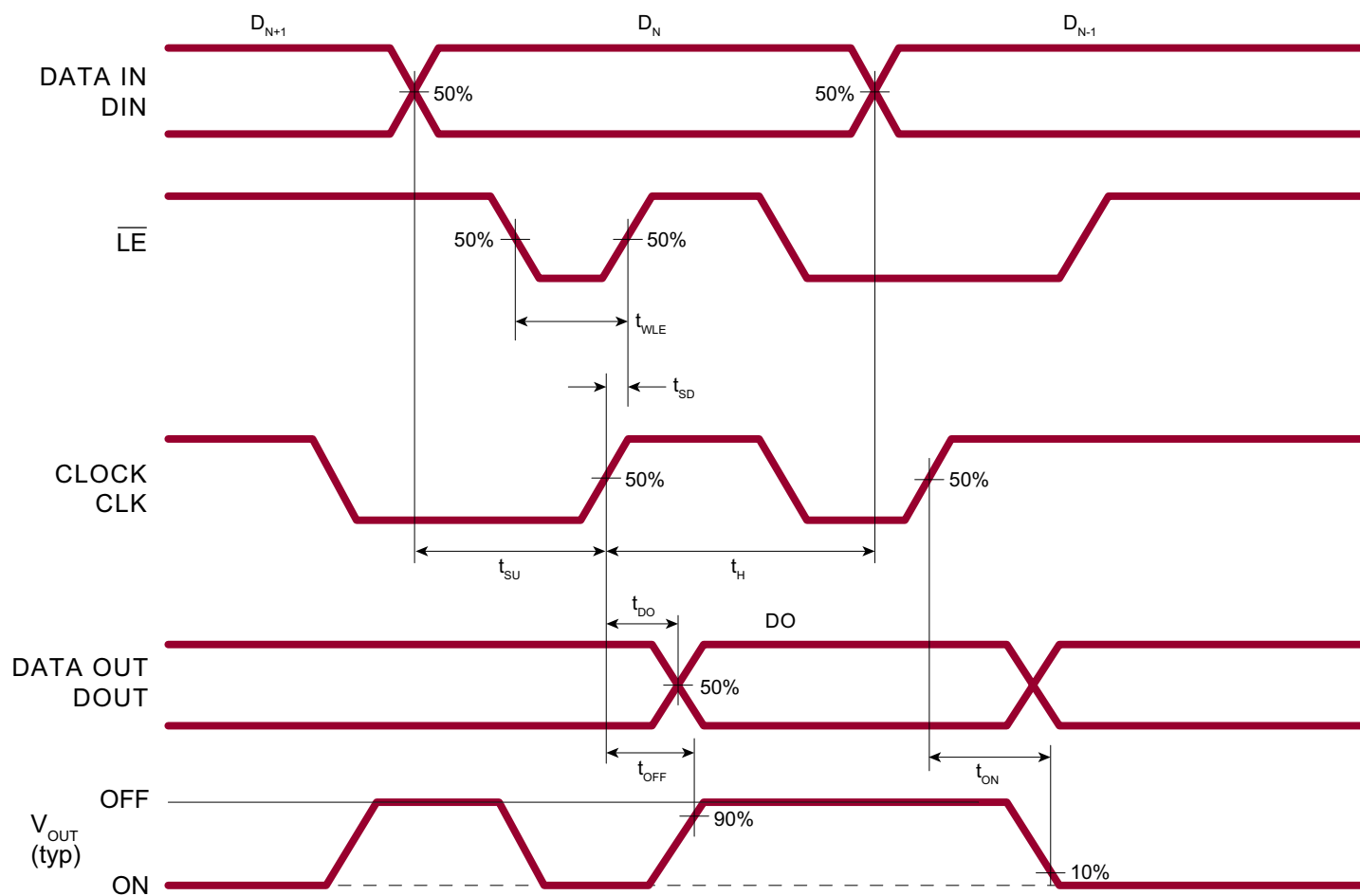
|          |                           |      |     |      |         |                       |
|----------|---------------------------|------|-----|------|---------|-----------------------|
| $V_{IH}$ | Input logic high voltage  | 2.5  | 3.3 | 5.0  | V       | Design for 3.3V Logic |
| $V_{IL}$ | Input logic low voltage   | 0    | -   | 0.6  | V       |                       |
| $I_{IH}$ | Input logic high current  | -    | -   | 1.0  | $\mu A$ | ---                   |
| $I_{IL}$ | Input logic low current   | -1.0 | -   | -    | $\mu A$ | ---                   |
| $C_{IN}$ | Input capacitance         | -    | 10  | 12   | pF      | ---                   |
| $I_{OH}$ | Output logic high current | -    | -   | -2.0 | mA      | ---                   |
| $I_{OL}$ | Output logic low current  | -    | -   | 2.0  | mA      | ---                   |
| $V_{OH}$ | Output logic high voltage | 4.5  | -   | -    | V       | $I_{OH} = -2.0mA$     |
| $V_{OL}$ | Output logic low voltage  | -    | -   | 0.35 | V       | $I_{OL} = -2.0mA$     |

## AC Electrical Characteristics (Over operating conditions unless otherwise specified, $V_{DD} = +5V$ , $T_J = 25^\circ C$ )

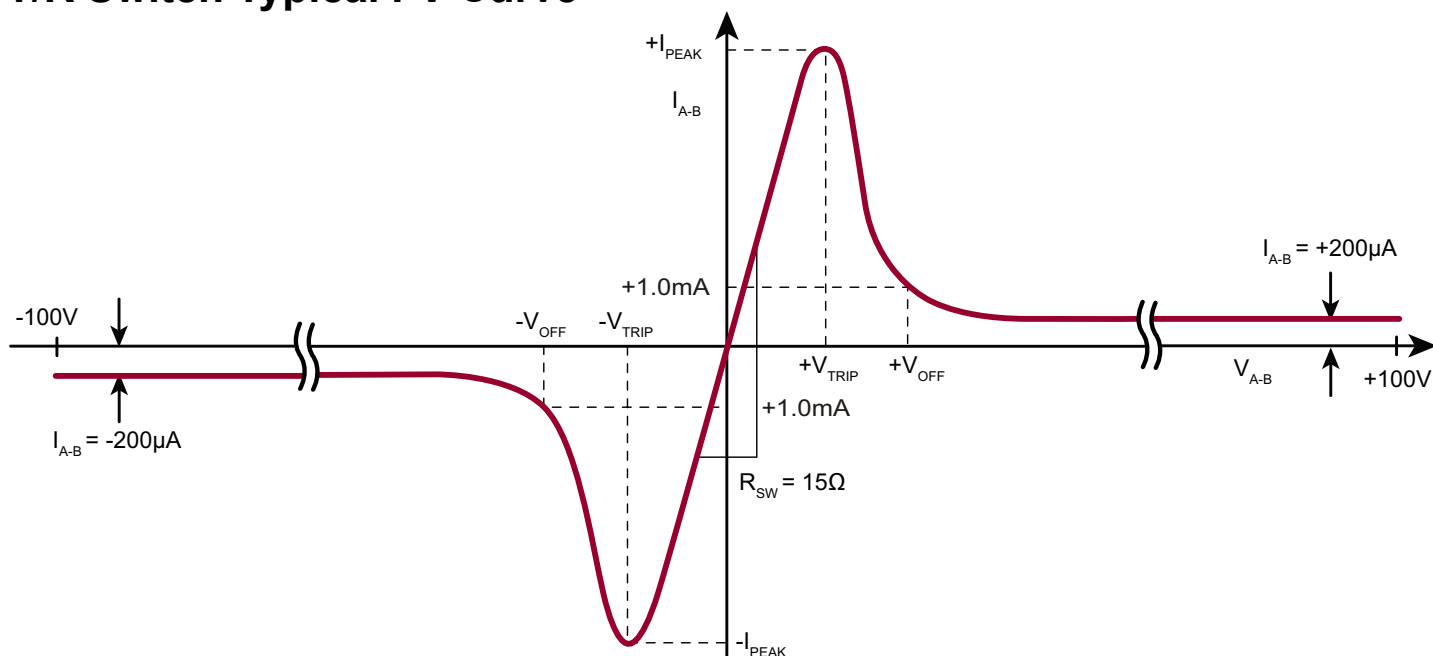
|             |                                         |    |     |     |     |                                                     |
|-------------|-----------------------------------------|----|-----|-----|-----|-----------------------------------------------------|
| $Q_C$       | LV SW charge injection                  | -  | 3.0 | 7.0 | pC  | $V_{(X0-3)} = 0V$ ,<br>$O3 \sim 1$ to GND 1nF load  |
| BW          | Small signal bandwidth                  | -  | 100 | -   | MHz | $R_{LOAD} = 50\Omega$                               |
| $K_O$       | OFF-Isolation                           | -  | -60 | -   | dB  | At 10MHz,<br>$R_{LOAD} = 50\Omega$ , $\pm 300mVp-p$ |
| $K_{CR}$    | On-channel crosstalk                    | -  | -55 | -   | dB  |                                                     |
| $C_{(ON)}$  | On-capacitance output to GND            | -  | 42  | 45  | pF  | From $O0 \sim O3$ to GND                            |
| $C_{(OFF)}$ | OFF-capacitance output to GND           | -  | 22  | 25  | pF  | ---                                                 |
| $f_{CLK}$   | Clock frequency                         | 20 | 25  | -   | MHz | ---                                                 |
| $t_{SD}$    | Setup time before $\overline{LE}$ rises | 10 | -   | -   | ns  | ---                                                 |
| $t_H$       | Data hold time                          | 10 | -   | -   | ns  | ---                                                 |
| $t_r/t_f$   | CLK rise or fall time                   | -  | -   | 5.0 | ns  | ---                                                 |

**AC Electrical Characteristics (cont.)** (Over operating conditions unless otherwise specified,  $V_{DD} = +5V$ ,  $T_j = 25^\circ C$ )

| Sym       | Parameter                     | Min | Typ | Max | Unit    | Conditions                                                                  |
|-----------|-------------------------------|-----|-----|-----|---------|-----------------------------------------------------------------------------|
| $t_{WLE}$ | Time width of $\overline{LE}$ | 10  | -   |     | ns      | ---                                                                         |
| $t_{SU}$  | Data setup time               | 10  | -   |     | ns      | ---                                                                         |
| $t_{DO}$  | CLK delay time to data out    | -   | -   |     | ns      | ---                                                                         |
| $dv/dt$   | Maximum $V_x$ slew rate       | -   | -   |     | V/ns    | ---                                                                         |
| $t_{ON}$  | ON time delay                 | -   | 3.0 | 5.0 | $\mu s$ | From CLK rise 50% to the switch full on or off time, at $\overline{LE} = 0$ |
| $t_{OFF}$ | OFF time delay                | -   | 3.0 | 5.0 | $\mu s$ |                                                                             |
| $V_{SPK}$ | Spike of LV SW turning ON     | -   | 5.0 | 10  | mV      | 50 $\Omega$ on O0~3 to GND<br>1k $\Omega$ on X0~3 to GND                    |
|           | Spike of LV SW turning OFF    | -   | 5.0 | 10  |         |                                                                             |

**Logic Timing Waveforms**


## T/R Switch Typical I-V Curve



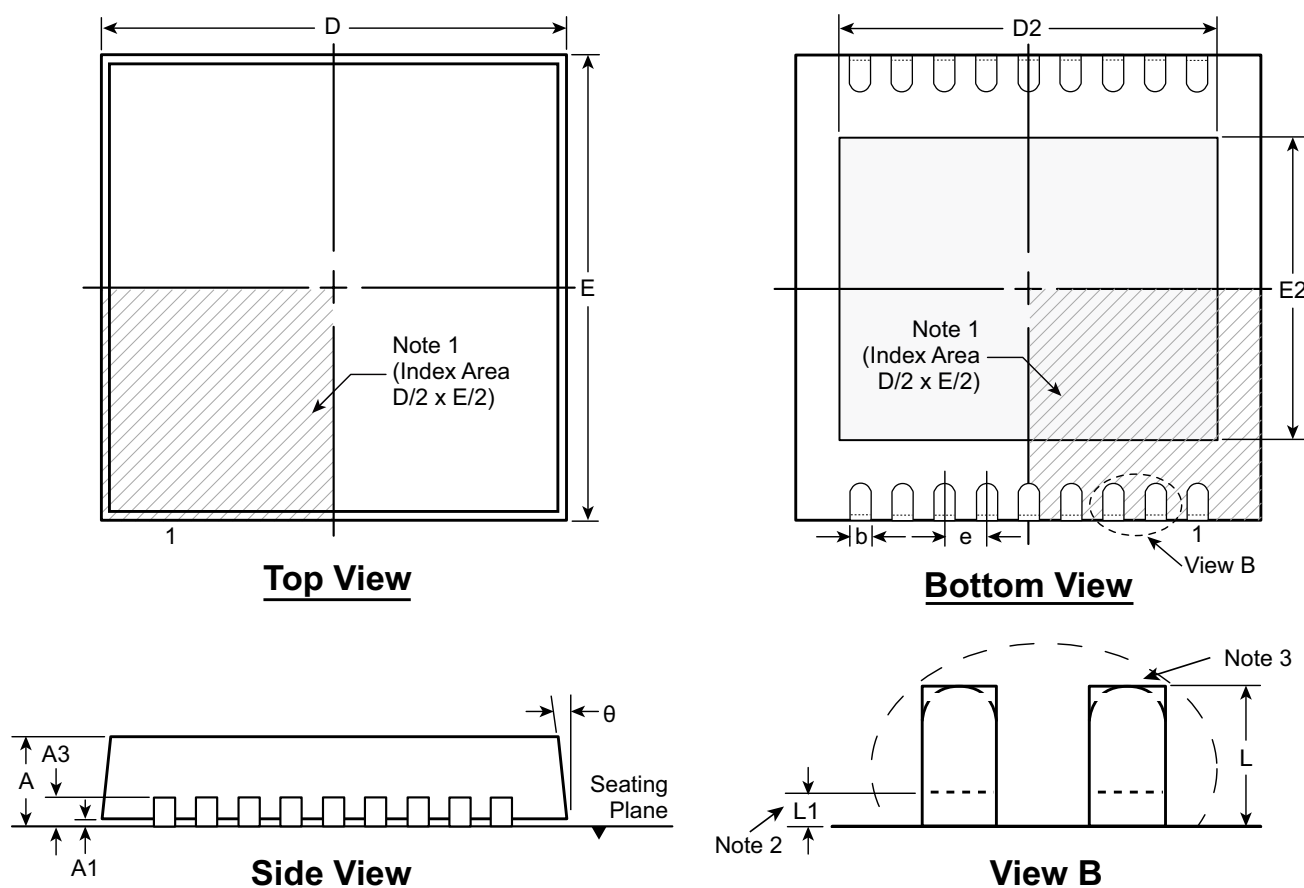
## Pin Description

| Pin | Name                   | Description                                                                                                                                                                      |
|-----|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | O0                     | Low voltage analog switch channel 0 output                                                                                                                                       |
| 2   | O1                     | Low voltage analog switch channel 1 output                                                                                                                                       |
| 3   | DIN                    | Serial Data Input                                                                                                                                                                |
| 4   | CLK                    | Shift register clock input                                                                                                                                                       |
| 5   | VDD                    | Positive voltage power supply +5V                                                                                                                                                |
| 6   | $\overline{\text{LE}}$ | Latch-Enable input - the switch status latched at the rising edge of $\overline{\text{LE}}$ . When $\overline{\text{LE}}$ is low the shift registers data flow through the latch |
| 7   | DOUT                   | Serial Data Output                                                                                                                                                               |
| 8   | O2                     | Low voltage analog switch channel 2 output                                                                                                                                       |
| 9   | O3                     | Low voltage analog switch channel 3 output                                                                                                                                       |
| 10  | NC                     | No internal connection                                                                                                                                                           |
| 11  | X3                     | T/R switch channel 3 high voltage input                                                                                                                                          |
| 12  | NC                     | No internal connection                                                                                                                                                           |
| 13  | X2                     | T/R switch channel 2 high voltage input                                                                                                                                          |
| 14  | NC                     | No internal connection                                                                                                                                                           |
| 15  | X1                     | T/R switch channel 1 high voltage input                                                                                                                                          |
| 16  | NC                     | No internal connection                                                                                                                                                           |
| 17  | X0                     | T/R switch channel 0 high voltage input                                                                                                                                          |
| 18  | NC                     | No internal connection                                                                                                                                                           |
| DAP | GND                    | The bottom thermal pad of DFN-18, Ground (0V)                                                                                                                                    |

**Note:** DAP must be connected to the ground on the PCB.

# 18-Lead DFN Package Outline (K6)

5.00x5.00mm body, 1.00mm height (max), 0.50mm pitch



## Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol            |     | A    | A1   | A3          | b    | D     | D2                | E     | E2                | e           | L                 | L1    | θ   |
|-------------------|-----|------|------|-------------|------|-------|-------------------|-------|-------------------|-------------|-------------------|-------|-----|
| Dimension<br>(mm) | MIN | 0.80 | 0.00 | 0.20<br>REF | 0.18 | 4.85* | 4.20 <sup>†</sup> | 4.85* | 3.50 <sup>†</sup> | 0.50<br>BSC | 0.30 <sup>†</sup> | 0.00* | 0°  |
|                   | NOM | 0.90 | 0.02 |             | 0.25 | 5.00  | 4.35 <sup>†</sup> | 5.00  | 3.65 <sup>†</sup> |             | 0.40 <sup>†</sup> | -     | -   |
|                   | MAX | 1.00 | 0.05 |             | 0.30 | 5.15* | 4.45 <sup>†</sup> | 5.15* | 3.75 <sup>†</sup> |             | 0.50 <sup>†</sup> | 0.15  | 14° |

JEDEC Registration MO-229, Variation VJJD-2, Issue C, Aug 2003.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #:** DSPD-18DFNK65X5P050, Version A013111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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