LatticeEC™ Standard Evaluation Board – Revision B

User's Guide

April 2007
ebug10_01.4

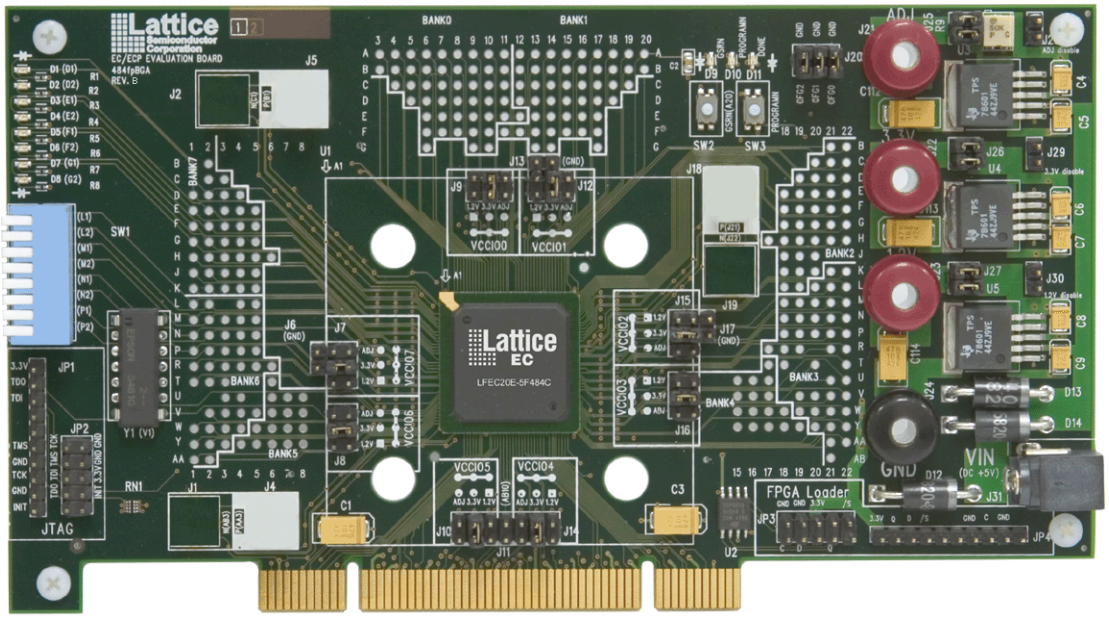
Introduction

The LatticeEC Standard Evaluation Board provides a convenient platform to evaluate, test and debug user designs, including designs requiring PCI. The information in this document pertains only to boards marked as 'Rev B'. This marking is located on the front of the board, beneath the Lattice logo.

Features

- Required voltages supplied by PCI or one external 5V DC supply
- ispVM® System programming support
- SPI3 Flash device included for low cost, non-volatile configuration storage
- PCI edge connector (120-pin) for 32-bit PCI interface
- Large Prototyping Area with access to over 290 I/O pins
- Optional SMA/SMB connectors (up to six) for high-speed clock and data interfacing

Figure 1. LatticeEC Standard Evaluation Board



Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 7 inches by 3.9 inches. The environmental specifications are as follows:

- Operating temperature: 0ºC to 55ºC
- Storage temperature: -40ºC to 75ºC
- Humidity: < 95% without condensation
- VDC input (+/- 10%) up to 4A, or 3.3V input from PCI backplane

Additional Resources

Additional resources related to this board can be downloaded from the web at www.latticesemi.com/boards. Click on the appropriate evaluation board, then see the blue "Resources" box on the right of the screen for items such as: updated documentation, software, sample designs, IP evaluation bitstreams, and more.

Table 1. Embedded Functions

Description	Source	LatticeEC Pin	Notes
33.33MHz clock	On-Board Oscillator	V1/AB10	3.3V TTL Output

The 3.3V oscillator socket accepts both full-size and half-size oscillators and can route to different clock inputs, depending on its position within the socket. The 16-pin socket will allow connection to PLL clock pin V1 when the bottom of the oscillator is aligned to socket pins 8 and 9. When the top of the oscillator is aligned to socket pins 1 and 16, the clock is provided to primary clock pin AB10.

LatticeEC Device

This board features a LatticeEC FPGA with a 1.2V DC core. It can accommodate all pin-compatible LatticeEC devices in plastic 484-ball fpBGA (1mm pitch) packages. A complete description of this device can be found in the LatticeECP/EC Family Data Sheet on the Lattice web site at www.latticesemi.com.

Programming Headers

Four programming headers are provided on the evaluation board, providing access to the LatticeEC JTAG port or the SPI Flash device. Both 1x10 and 2x5 formats are available for compatibility with all Lattice download cables. The pinouts for the headers are provided in Tables 2 and 3.

Note: An ispDOWNLOAD® cable is included with each ispLEVER®-Base or ispLEVER-Advanced design tool shipment. Cables may also be purchased separately from Lattice.

Table 2. JTAG Programming Headers

Function	JP1 (1x10)	JP2 (2x5)
V_{CC} (3.3V)	1	6
TDO	2	7
TDI	3	5
TMS	6	3
TCK	8	1
INITN	10	8
GND	7, 9	2, 4

Note: When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (V_{CC}).

Table 3. Flash Programming Headers

Function	JP4 (1x10)	JP3 (2x5)
V_{CC} (3.3V)	1	6
SFLASH_Q	2	7
SFLASH_D	3	5
SFLASH_S_N	4	10
SFLASH_C	8	1
GND	7, 9	2, 4

Note: When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (V_{CC}).

Power Setup

For stand-alone board operation (i.e. outside of a PCI backplane), the evaluation board may be supplied with a single 5V DC power supply. On-board regulators will provide the necessary supply voltages.

The on-board regulators supply 3.3V, 1.2V, and an adjustable voltage. The adjustable voltage is set by the potentiometer R9 at the upper right corner of the board and can be set to a value between 1.22V and 3.25V.

5V DC power may be applied using the power jack at J31 using an AC adapter such as the Condor Electronics S-5V0-4A0-U11-206IP, or similar. Requirements for the power jack are listed in Table 4.

Table 4. Power Jack J31 Specifications

Polarity	Positive Center
Inside Diameter	0.1" (2.5mm)
Outside Diameter	0.218" (5.5mm)
Current Capacity	Up to 4A

When the evaluation board is inserted into a PCI backplane, all on-board power will be derived from the PCI 3.3V power rail. When plugged into the PCI slot, the on-board 3.3V regulator (U4) will be disabled automatically, allowing 3.3V to be supplied directly from the PCI host system.

Power can also be supplied directly for each individual supply rail using banana jack connectors. To enable this mode of operation, the appropriate jumpers must be removed. All power sources must be regulated to the specifications in Table 5. No special power sequencing is required for the evaluation board.

Note: A single 3.3V supply can also be used to supply all three required voltages to the LatticeEC Standard Evaluation Board. This can be achieved by disabling the 3.3V on-board regulator through the installation of jumper J29. 3.3V power can then be supplied directly to banana jack J22, providing power to the remaining regulators.

Table 5. Individual Control of Supplies

Supply	Jack	Jumper	Requirement
3.3V	J22	J26	3.3V +/- 0.3V
1.2V	J23	J27	1.2V +/- 5%
VCC_ADJ	J21	J25	User-defined[1]

Note: If the user-defined adjustable voltage is used for any of the LatticeEC sysIO™ banks, it must be set to a supported voltage between 1.2V DC and 3.3V DC.

The jumpers listed in Table 6 allow the user to select the voltage (V_{CCIO}) applied to each of the eight I/O banks of the LatticeEC device. Certain restrictions apply depending on which features of the board are being used.

Table 6. sysIO Bank Settings

sysIO Bank	Jumper	Settings
0	J9	1-2 -> VCC_1.2v 3-4 -> VCC_3.3v 5-6 -> VCC_ADJ
1	J12	
2	J15	
3	J16	
4	J14	
5	J10	
6	J8	
7	J7	

Table 7. sysIO Bank Considerations

Bank	Setting
0	Any[1]
1	Any[1]
2	Any[1]
3	3.3V if SPI configuration mode selected, otherwise any
4	3.3V when PCI interface used, otherwise any
5	3.3V when PCI interface used, otherwise any
6	Any[1]
7	Any[1]

1. "Any" refers to any supported voltage between 1.2V and 3.3V.

The following tables detail the various standards supported by the LatticeEC FPGA Input/Output (sysIO) structures. More information can be found in Lattice technical note number TN1056, *LatticeECP/EC sysIO Usage Guide*, available on the Lattice web site at www.latticesemi.com.

Table 8. Mixed Voltage Support

	Input sysIO Standards					Output sysIO Standards				
V_{CCIO}	1.2V	1.5V	1.8V	2.5V	3.3V	1.2V	1.5V	1.8V	2.5V	3.3V
1.2V	Yes			Yes	Yes	Yes				
1.5V	Yes	Yes		Yes	Yes		Yes			
1.8V	Yes		Yes	Yes	Yes			Yes		
2.5V	Yes			Yes	Yes				Yes	
3.3V	Yes			Yes	Yes					Yes

For example, if V_{CCIO} is 3.3V then signals from devices powered by 1.2V, 2.5V or 3.3V can be input and the thresholds will be correct (assuming the user has selected the desired input level using ispLEVER software). Output levels are tied directly to V_{CCIO}.

Table 9. sysIO Standards Supported per Bank

Description	Top Side Banks 0-1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
Types of I/O Buffers	Single-ended	Single-ended and Differential	Single-ended	Single-ended and Differential
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I, III HSTL18_I, II, III SSTL18D Class I, SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I, III, HSTL18D Class I, III PCI33 LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I, III HSTL18D Class I, III PCI33 LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II, SSTL33D Class I, II HSTL15D Class I, III HSTL18D Class I, III PCI33 LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II, SSTL33D_I, II HSTL15D Class I, III HSTL18D Class I, III PCI33 LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]
Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Clock Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
PCI Support	PCI33 with clamp	PCI33 no clamp	PCI33 with clamp	PCI no clamp
LVDS Output Buffers		LVDS (3.5mA) Buffers		LVDS (3.5mA) Buffers

1. These differential standards are implemented by using complementary LVCMOS driver with external resistor pack.

PCI

The LatticeEC Evaluation Board is designed to interface directly to PCI 2.2 compatible systems using the PCI edge connector. All necessary signals required for 32-bit PCI operation are provided to the connector, as shown in Tables 10 and 11.

Table 10. PCI Connections – Solder Side

J32	Description	LatticeEC Pin	sysIO Bank
6	PCI_INTA_N	AB5	5
7	PCI_INTC_N	AB6	5
15	PCI_RST_N	AB7	5
17	PCI_GNT_N	Y8	5
20	PCI_AD30	AB9	5
22	PCI_AD28	Y9	5
23	PCI_AD26	V9	5
25	PCI_AD24	AA10	5

Table 10. PCI Connections – Solder Side (Continued)

J32	Description	LatticeEC Pin	sysIO Bank
26	PCI_IDSEL	W10	5
28	PCI_AD22	U10	5
29	PCI_AD20	AA11	5
31	PCI_AD18	W11	5
32	PCI_AD16	AB12	4
34	PCI_FRAME_N	Y12	4
36	PCI_TRDY_N	V12	5
38	PCI_STOP_N	AA13	4
43	PCI_PAR	U13	4
44	PCI_AD15	AA14	4
46	PCI_AD13	W14	4
47	PCI_AD11	U14	4
49	PCI_AD9	AA15	4
52	PCI_CBE0_N	AA16	4
54	PCI_AD6	V15	4
55	PCI_AD4	AA17	4
57	PCI_AD2	AA18	4
58	PCI_AD0	AB19	4

Table 11. PCI Connections - Component Side

J3	Description	LatticeEC Pin	sysIO Bank
7	PCI_INTB_N	AA6	5
8	PCI_INTD_N	AA7	5
9	PCI_PRSNT1_N	Y7	5
11	PCI_PRSNT2_N	W8	5
16	PCI_CLK	U20	3
18	PCI_REQ_N	AB8	5
20	PCI_AD31	AA8	5
21	PCI_AD29	AA9	5
23	PCI_AD27	W9	5
24	PCI_AD25	U9	5
26	PCI_CBE3_N	Y10	5
27	PCI_AD23	V10	5
29	PCI_AD21	AB11	5
30	PCI_AD19	Y11	5
32	PCI_AD17	V11	5
33	PCI_CBE2_N	AA12	4
35	PCI_IRDY_N	W12	4
37	PCI_DEVSEL_N	AB13	4
40	PCI_PERR_N	W13	4
42	PCI_SERR_N	V13	4
44	PCI_CBE1_N	AB14	4
45	PCI_AD14	Y14	4

Table 11. PCI Connections - Component Side (Continued)

J3	Description	LatticeEC Pin	sysIO Bank
47	PCI_AD12	V14	4
48	PCI_AD10	AB15	4
52	PCI_AD8	Y15	4
53	PCI_AD7	W15	4
55	PCI_AD5	AB16	4
56	PCI_AD3	AB17	4
58	PCI_AD1	AB18	4

Prototype Area

For general purpose I/Os, numerous test points are provided for direct access. The test points are labeled according to the associated I/O pin location, and are listed in Table .

Table 12. LatticeEC Pins Accessible at Test Points

A3 (0)	B20 (1)	D13 (1)	F6 (0)	H5 (7)	M3 (6)	R21 (3)	W6 (5)
A4 (0)	B21 (2)	D14 (1)	F7 (0)	H6 (7)	M4 (6)	R22 (3)	W7 (5)
A6 (0)	B22 (2)	D15 (1)	F8 (0)	H17 (2)	M5 (6)	T1 (6)	W16 (4)
A7 (0)	C1 (7)	D16 (1)	F9 (0)	H18 (2)	M18 (3)	T2 (6)	W17 (4)
A8 (0)	C2 (7)	D17 (1)	F10 (0)	H19 (2)	M19 (3)	T3 (6)	W18 (4)
A9 (0)	C3 (7)	D18 (1)	F11 (1)	H20 (2)	M20 (3)	T6 (5)	W19 (3)
A10 (0)	C4 (0)	D19 (2)	F12 (1)	H21 (2)	M21 (3)	T17 (4)	W20 (3)
A11 (0)	C5 (0)	D20 (2)	F13 (1)	H22 (2)	M22 (3)	T18 (3)	W21 (3)
A12 (1)	C6 (0)	D21 (2)	F14 (1)	J1[1] (7)	N1[2] (6)	T20[3] (3)	W22 (3)
A13 (1)	C7 (0)	D22 (2)	F15 (1)	J2[1] (7)	N2[2] (6)	T22 (3)	Y1 (6)
A14 (1)	C8 (0)	E1 (7)	F16 (1)	J3 (7)	N3 (6)	U3 (6)	Y2 (6)
A15 (1)	C9 (0)	E2 (7)	F17 (1)	J4 (7)	N4 (6)	U4 (6)	Y3 (6)
A16 (1)	C10 (0)	E3 (7)	F18 (2)	J5 (7)	N5 (6)	U6 (5)	Y4 (5)
A17 (1)	C11 (0)	E4 (7)	F19 (2)	J18 (2)	N18 (3)	U7 (5)	Y5 (5)
A18 (1)	C12 (1)	E5 (7)	F20 (2)	J19 (2)	N19 (3)	U8 (5)	Y6 (5)
A19[4] (1)	C13 (1)	E6 (0)	F21 (2)	J20 (2)	N20 (3)	U15 (4)	Y16 (4)
A20 (1)	C14 (1)	E7 (0)	F22 (2)	K1[1] (7)	N21 (3)	U16 (4)	Y17 (4)
AA1 (6)	C15 (1)	E8 (0)	G1[1] (7)	K2[1] (7)	N22 (3)	U17 (4)	Y18 (4)
AA2 (6)	C16 (1)	E9 (0)	G2[1] (7)	K3 (7)	P1[2] (6)	U21[3] (3)	Y19 (4)
B1 (7)	C17 (1)	E10 (0)	G3 (7)	K4 (7)	P2[2] (6)	U22 (3)	Y20 (3)
B2 (7)	C18 (1)	E11 (0)	G4 (7)	K5 (7)	P3 (6)	V2 (6)	Y21[5] (3)
B3 (0)	C19 (1)	E12 (0)	G5 (7)	K18 (2)	P4 (6)	V3 (6)	Y22 (3)
B4 (0)	C20 (2)	E13 (1)	G6 (0)	K19 (2)	P5 (6)	V4 (6)	AA3 (5)
B5 (0)	C21 (2)	E14 (1)	G9 (0)	K20 (2)	P18 (3)	V6 (5)	AA4 (5)
B7 (0)	C22 (2)	E15 (1)	G10 (0)	K21 (3)	P19 (3)	V7 (5)	AA5 (5)
B8 (0)	D1 (7)	E16 (1)	G13 (1)	K22 (3)	P20 (3)	V8 (5)	AA19 (4)
B9 (0)	D2 (7)	E17 (1)	G14 (1)	L1[2] (6)	P21 (3)	V16 (4)	AA20 (4)
B10 (0)	D3 (7)	E18 (2)	G17 (1)	L2[2] (6)	P22 (3)	V17 (4)	AA21 (3)
B11 (0)	D4 (7)	E19 (2)	G18 (2)	L4 (6)	R1 (6)	V19 (3)	AA22 (3)
B12 (1)	D5 (0)	E20 (2)	G19 (2)	L5 (6)	R2 (6)	V20 (3)	AB3 (5)
B13 (1)	D6 (0)	E21 (2)	G20 (2)	L18 (2)	R3 (6)	V21[3] (3)	AB4 (5)

Table 12. LatticeEC Pins Accessible at Test Points (Continued)

B14 (1)	D7 (0)	E22 (2)	G21 (2)	L19 (2)	R4 (6)	V22[3] (3)	AB20 (4)
B15 (1)	D8 (0)	F1 (7)	G22 (2)	L20 (3)	R5 (6)	W1 (6)	AB21 (3)
B16 (1)	D9 (0)	F2 (7)	H1[1] (7)	L21 (3)	R6 (6)	W2 (6)	
B17 (1)	D10 (0)	F3 (7)	H2[1] (7)	L22 (3)	R17 (3)	W3 (6)	
B18 (1)	D11 (0)	F4 (7)	H3 (7)	M1[2] (6)	R18 (3)	W4 (6)	
B19 (1)	D12 (1)	F5 (7)	H4 (7)	M2[2] (6)	R19 (3)	W5 (5)	

Note: sysIO Bank indicated in parenthesis.
1. Also connected to LEDs. See Table 15 for more information.
2. Also connected to SW1. See Table 13 for more information.
3. Also connected to SPI configuration signals. See Figures 11 and 12.
4. Also connected to momentary switch SW2.
5. Also connected to J34.

Switches

Switch 1 (SW1) on the left side of the board is an eight-switch block that is part of the prototyping area. The pull-up resistors associated with SW1 are wired to 3.3V but any I/O voltage up to 3.3V may be used. A switch in the down position produces a low (0), while the up position produces a high (1).

Table 13. SW1 Connections

Switch	I/O Ball	sysIO Bank
SW1(1)	L1	6
SW1(2)	L2	6
SW1(3)	M1	6
SW1(4)	M2	6
SW1(5)	N1	6
SW1(6)	N2	6
SW1(7)	P1	6
SW1(8)	P2	6

SW2 is a momentary switch that the user can define for any purpose, such as a global reset. SW2 is wired to I/O ball A19 (bank 1) and applies a low logic level when depressed.

SW3 is a momentary switch that, when pressed, forces the FPGA to start its programming cycle.

Jumpers

A jumper installed on J34 provides a connection between the configuration clock (CCLK) and a general-purpose I/O. This connection is provided for programming the SPI Flash device via the ispJTAG™ interface. For more information, please refer to Lattice technical note number TN1078, *SPI Serial Flash Programming Using ispJTAG on LatticeECP/EC FPGAs.*

The headers at J28, J29, and J30 (not installed) allow the user to disable the voltage regulators. J28 is used to disable the adjustable voltage, J29 for 3.3V, and J30 for 1.2V. Installing the jumper disables the regulator.

The jumpers at J25, J26, and J27 disconnect the regulators from the rest of the board. These jumpers are removed if the user is supplying the voltage with an external supply. For normal operation, install all of these jumpers. The jumpers must be installed horizontally. See Table 5 for more information.

The jumpers at J20 determine which type of device the FPGA expects to receive programming information from and whether the FPGA will be master or slave during the transfer. Table 14 lists the possible configuration modes. Installing the jumper produces a low (0), removing the jumper produces a high (1).

Table 14. LatticeEC Configuration Mode Settings

CFG2	CFG1	CFG0	Configuration Mode
0	0	0	SPI3 Flash
0	0	1	SPIX Flash
1	0	0	Master Serial
1	0	1	Slave Serial
1	1	0	Master Parallel
1	1	1	Slave Parallel
X	X	X	ispJTAG (always available)

LEDs

Eight user-definable LEDs are provided on the upper left side of the board above SW1. These LEDs are each wired to a separate general purpose I/O as defined in the Table 15. The current limiting resistors associated with these LEDs are wired to 3.3V but it is safe to use any FPGA I/O voltage. The LED will light when its associated I/O pin is driven low.

Table 15. LED Connections

LED	I/O Ball	sysIO Bank
D1	G1	7
D2	G2	7
D3	H1	7
D4	H2	7
D5	J1	7
D6	J2	7
D7	K1	7
D8	K2	7

Miscellaneous

Pads are provided in six locations to allow the user to install SMA or SMB style connectors. This allows a high-speed interface for clocks or general purpose I/O. Table 16 indicates the I/O pin connections to each SMA connector pad. The dimensions on the pads are such that any standard SMA or SMB connector with dimensions similar to the Molex 73391-0060 are compatible.

Table 16. SMA Connections

Location	I/O Ball	sysIO Bank	Description
J1	AA2	6	GP I/O (T)
J4	AA1	6	GP I/O (C)
J5	B6	0	GP I/O (T)
J2	A5	0	GP I/O (C)
J18	J21	2	PCLKT, GP I/O
J19	J22	2	PCLKC, GP I/O

Note: T and C can be used as a differential pair.

Download Procedure

Requirements:

- PC with ispVM System v.14.2 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

- ispDOWNLOAD Cable (pDS4102-DL2, HW7265-DL3, HW-USB-1A, etc.)

JTAG Download

The LatticeEC device can be configured easily via its JTAG port. The device is SRAM-based, so it must remain powered on to retain its configuration when programmed in this fashion.

1. Connect the ispDOWNLOAD cable to the appropriate header. JP1 is used for the 1x10 cable, while JP2 is used for the 2x5 version.

   Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP/EC FPGA device and render the board inoperable.*

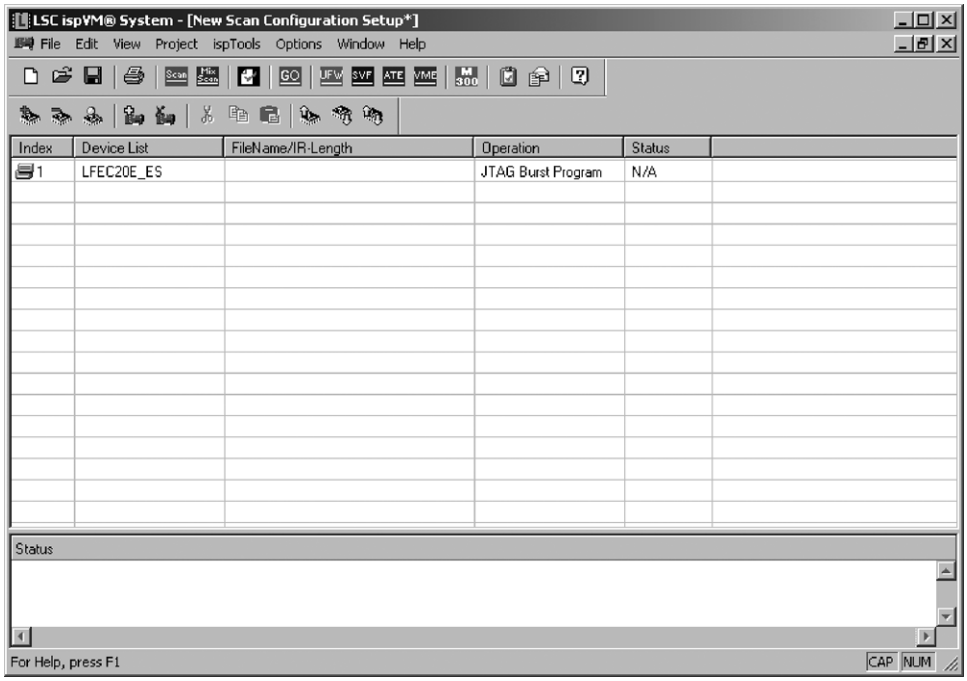
2. Connect the LatticeEC Evaluation Board to an external 5V supply.

3. When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (V_{CC}).

4. Start the ispVM System software.

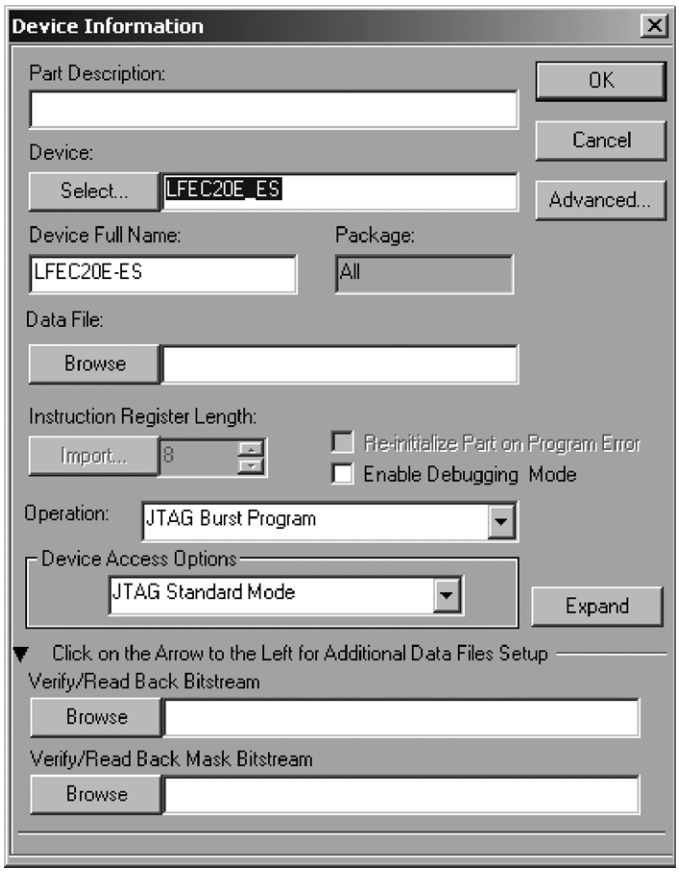
5. Press the 'SCAN' button located in the toolbar. The LatticeEC device should be automatically detected. The resulting screen should be similar to Figure 2.

Figure 2. ispVM System Interface



6. Double-click the device to open the device information dialog, as shown in Figure 3. In the device information dialog, click the Browse button located under 'Data File'. Locate the desired bitstream file (.bit). Click OK to both dialog boxes.

Figure 3. Device Information Dialog



7. Click the green 'GO' button. This will begin the download process into the device.

8. Upon successful download, the device will be operational.

SPI Flash Download

For non-volatile storage of configuration memory, the LatticeEC device features an interface compatible with low-cost SPI3 Flash memory devices. ispVM System has the capability to program the SPI3 Flash device directly. During the LatticeEC power-up cycle, the data stored in the SPI3 Flash device is automatically read into configuration memory.

1. Install all three jumpers at J20 (000). This enables SPI3 mode by setting the CFG pins of the LatticeEC device.

   Note: If the SPI3 Flash and the LatticeEC devices are blank, remove all three jumpers from J20. This configures the device in Slave Parallel mode, preventing the CCLK output from toggling. After the Flash device is programmed, the jumpers should be reinstalled.

2. Connect the ispDOWNLOAD cable to the appropriate header. JP4 is used for the 1x10 cable, while JP3 is used for the 2x5 version.

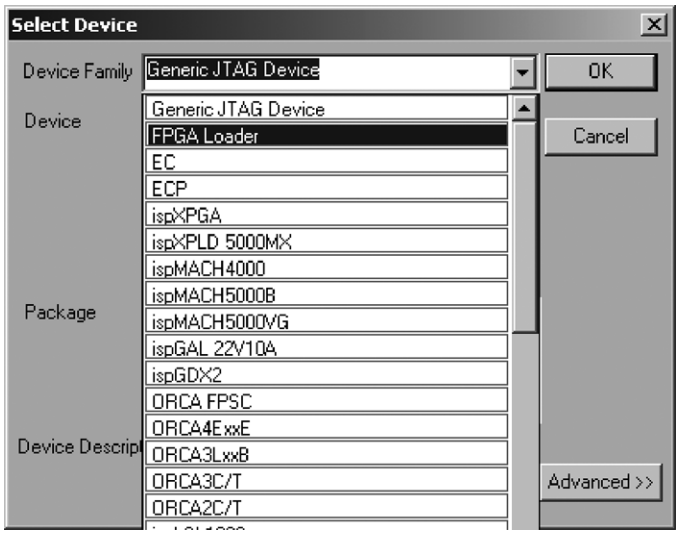
   Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any*

other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP/EC FPGA device and render the board inoperable.

When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (V_{CC}).

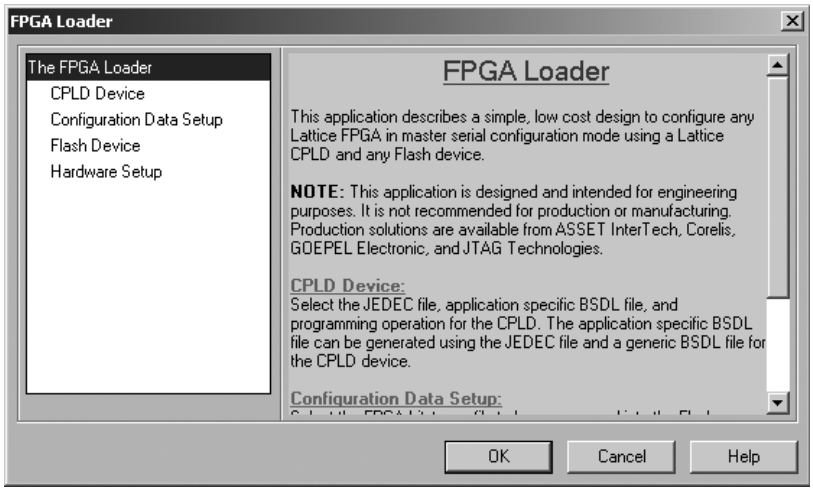
3. Connect the evaluation board to an external 5V supply.
4. Start the ispVM System software.
5. Create a new chain file (File->New).
6. Insert a new device into the chain (Edit->Add Device).
7. In the resulting Device Information dialog, press the 'Select' button (see Figure 4).

Figure 4. Device Selection Dialog



8. Use the pull-down menu in the 'Device Family' field to choose the device 'FPGA Loader'. Press OK. The resulting dialog should resemble Figure 5.

Figure 5. FPGA Loader Setup

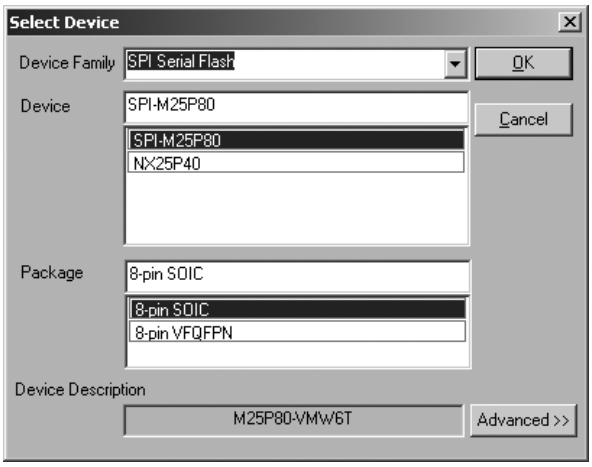


9. Choose the 'Flash Device' page and press the 'Select' button.

10. Select the 'SPI Serial Flash' family and choose the device SPI-M25P80, as shown in Figure 6. Press OK.

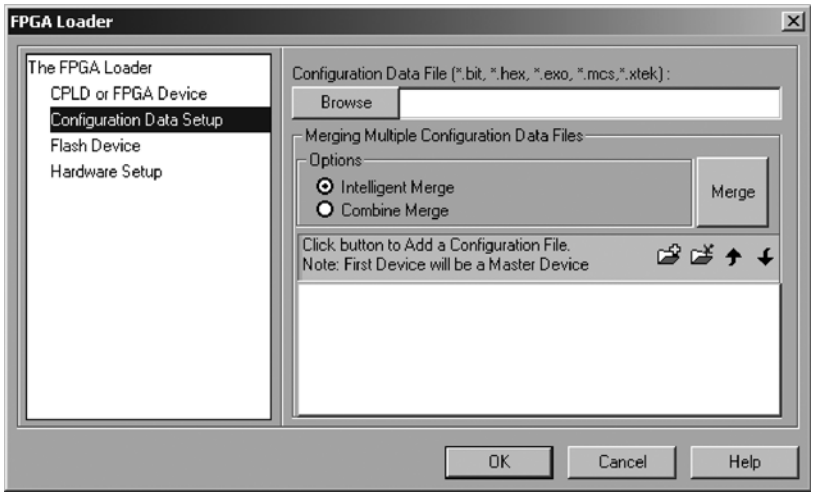
    Note: It may be necessary to select an alternate SPI3 Flash device, as the part number is subject to change.

Figure 6. SPI Device Selection



11. Choose the 'Configuration Data Setup' page, as shown in Figure 7.

Figure 7. Configuration Data Setup Page



12. Click the 'Browse' button near the top of the window. Browse to the desired bitstream (.bit) file, created by ispLEVER.

13. Press OK to exit the FPGA Loader setup.

14. Click the green 'GO' button. This will begin the download process into the Flash device.

15. Once the operation is complete, press SW3, which forces the LatticeEC device to reconfigure. The data should then automatically transfer from the Flash to the FPGA.

    Note: If the mode was set to Slave Parallel (all jumpers removed) from Step 1, reinstall all three jumpers before depressing SW3 to enable SPI3 configuration mode.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeEC6 Evaluation Board - Standard	LFEC6E-L-EV	
LatticeEC20 Evaluation Board - Standard	LFEC20E-L-EV	
LatticeECP20 Evaluation Board - Standard	LFECP20E-L-EV	
ispLEVER (HDL) (Base) with Lattice EC6 Development Kit	LS-EC6-BASE-PC-N	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
March 2007	01.3	Added Ordering Information section.
April 2007	01.4	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.

Appendix A. Schematics

Figure 8. Evaluation Board Block Diagram

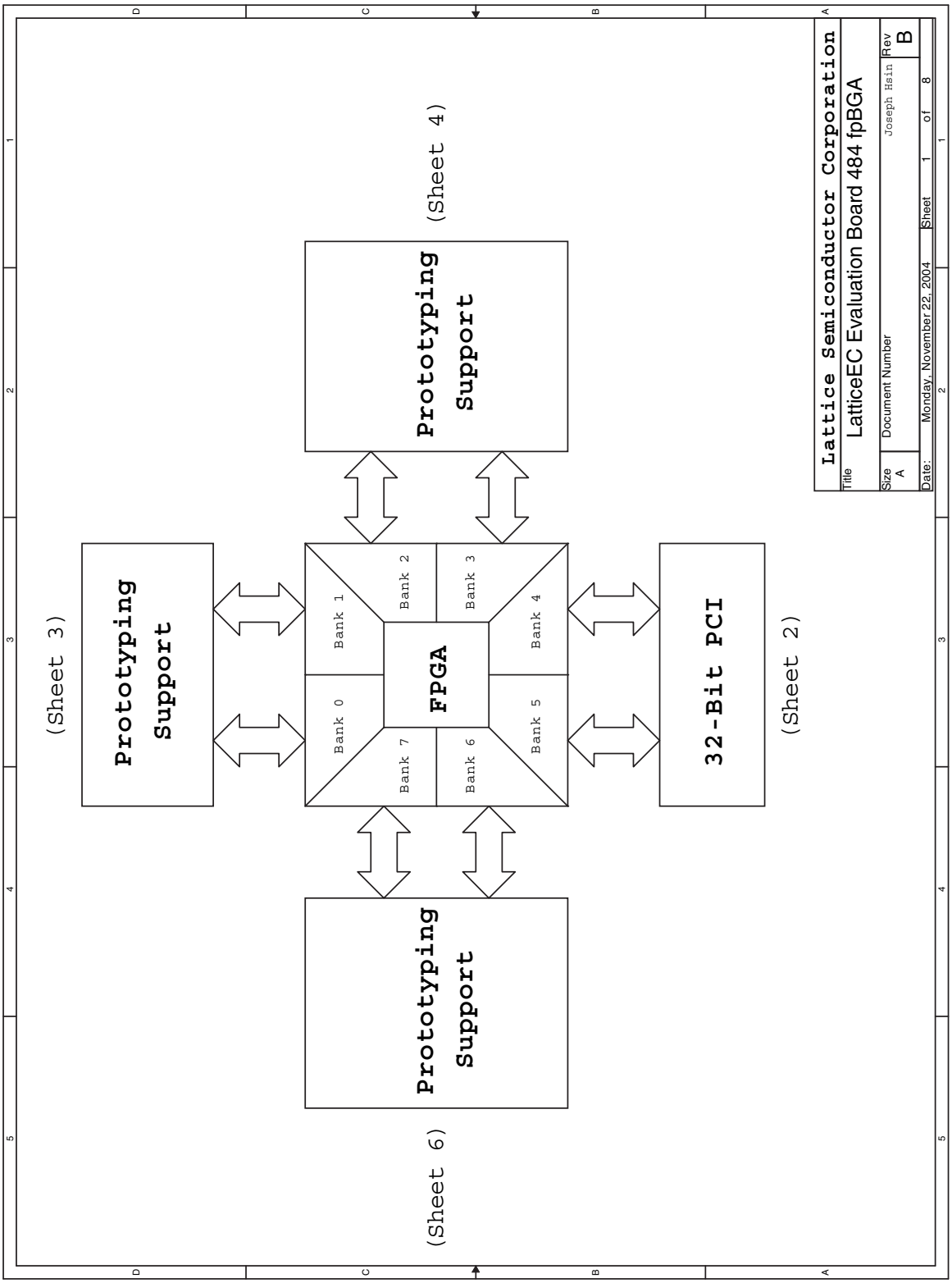


Figure 9. 32-Bit PCI Interface

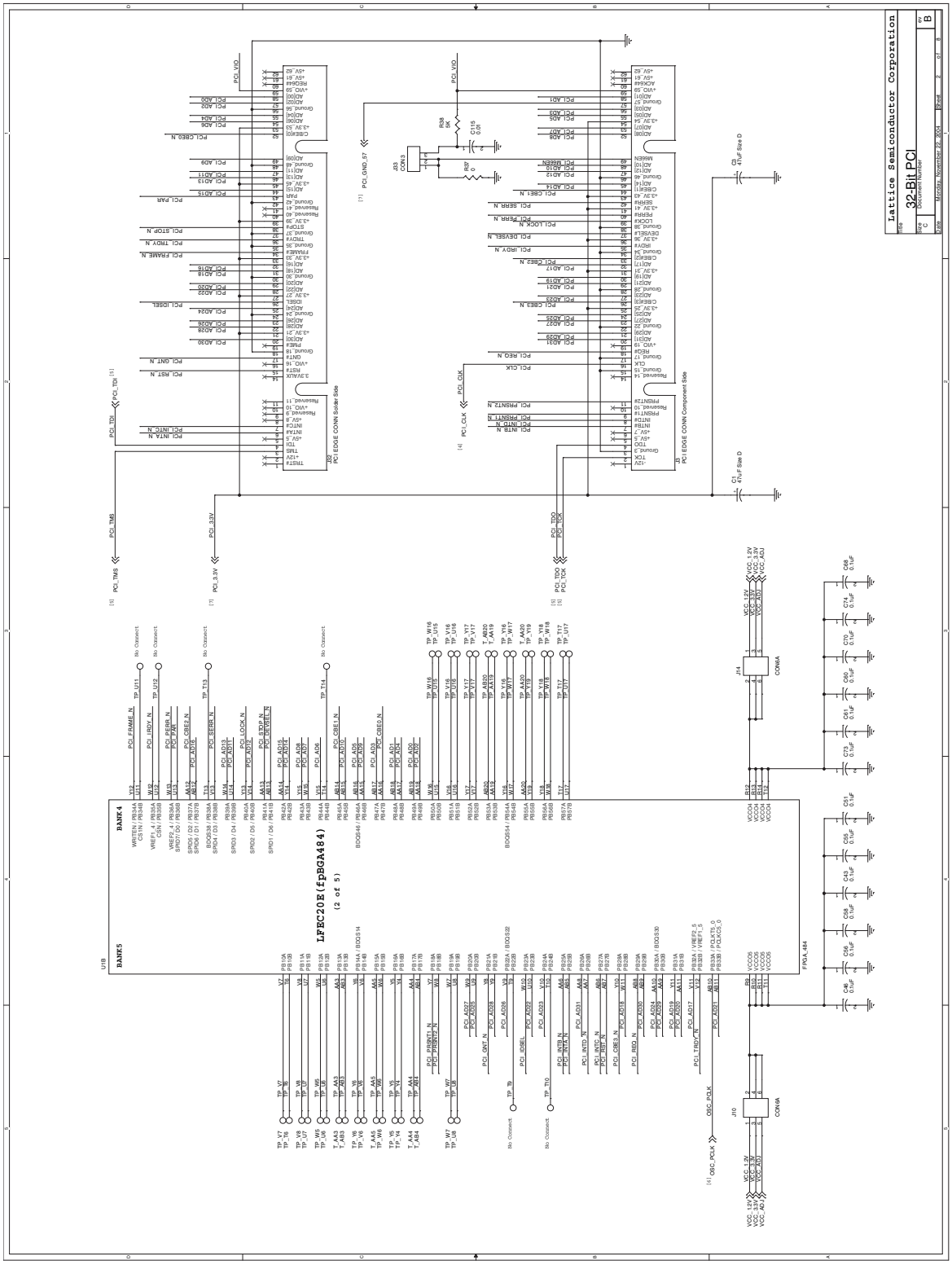


Figure 10. Prototyping Support

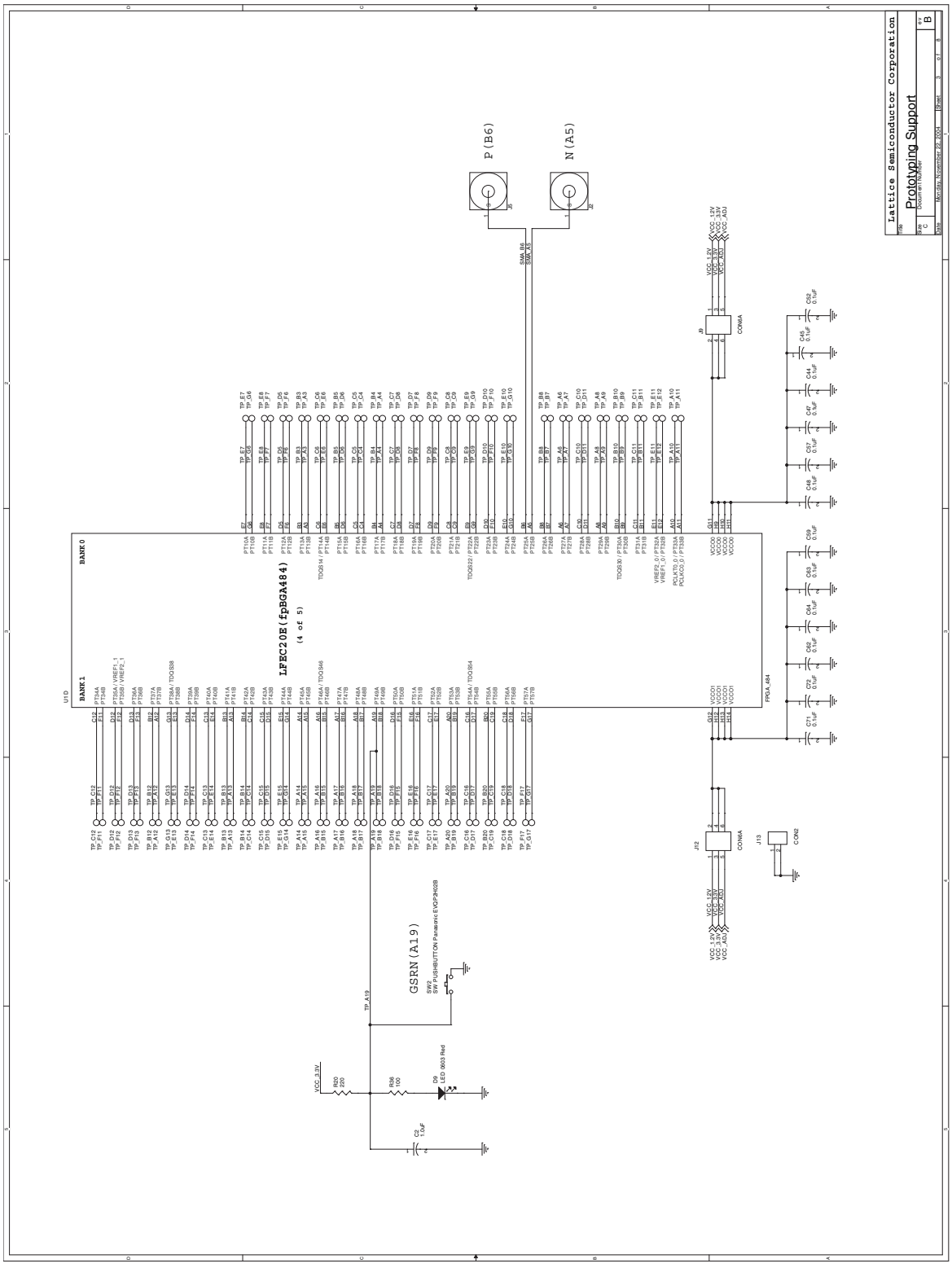


Figure 11. Prototyping Support

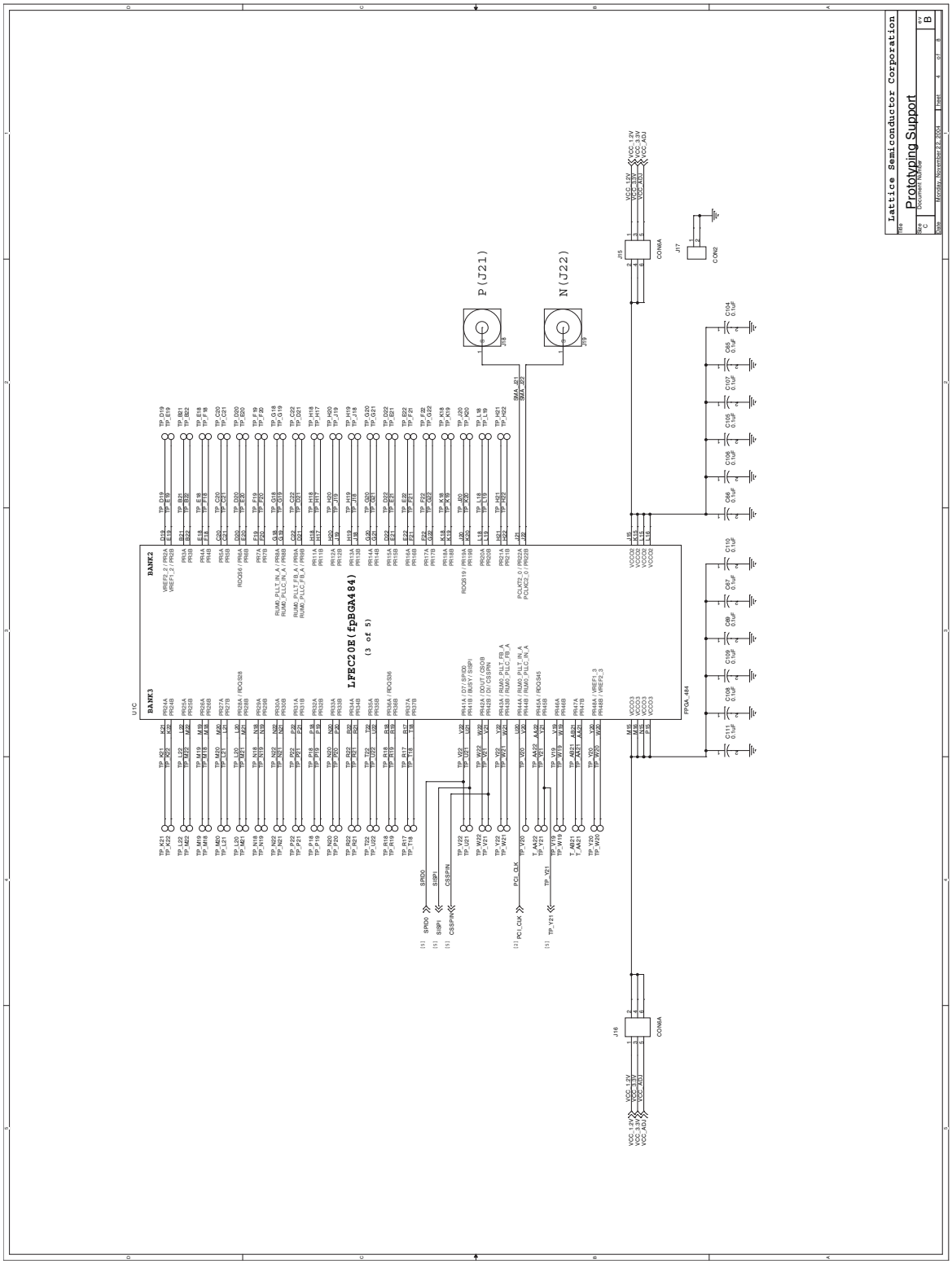


Figure 12. JTAG and FPGA Programming

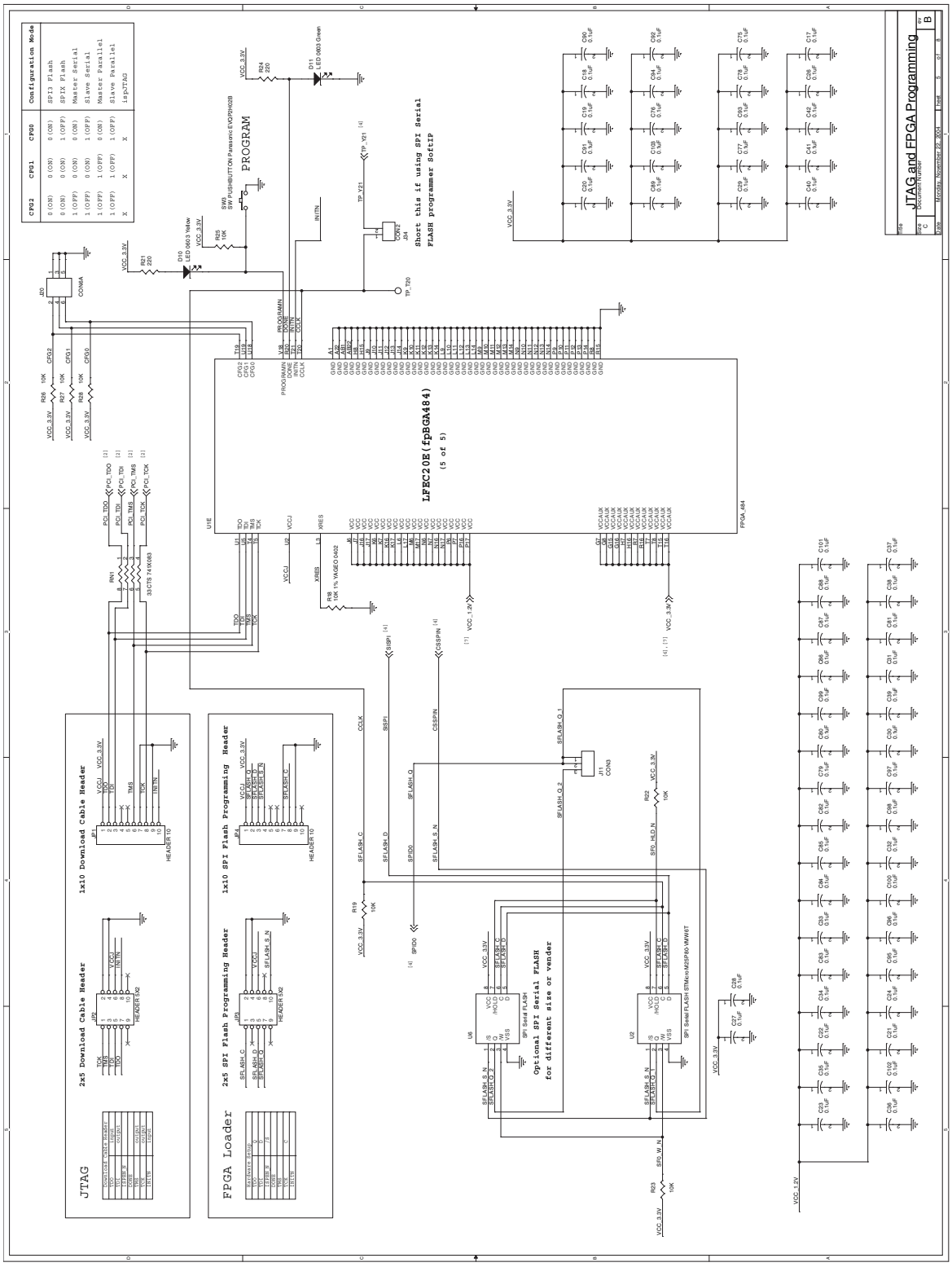


Figure 13. Prototyping Support

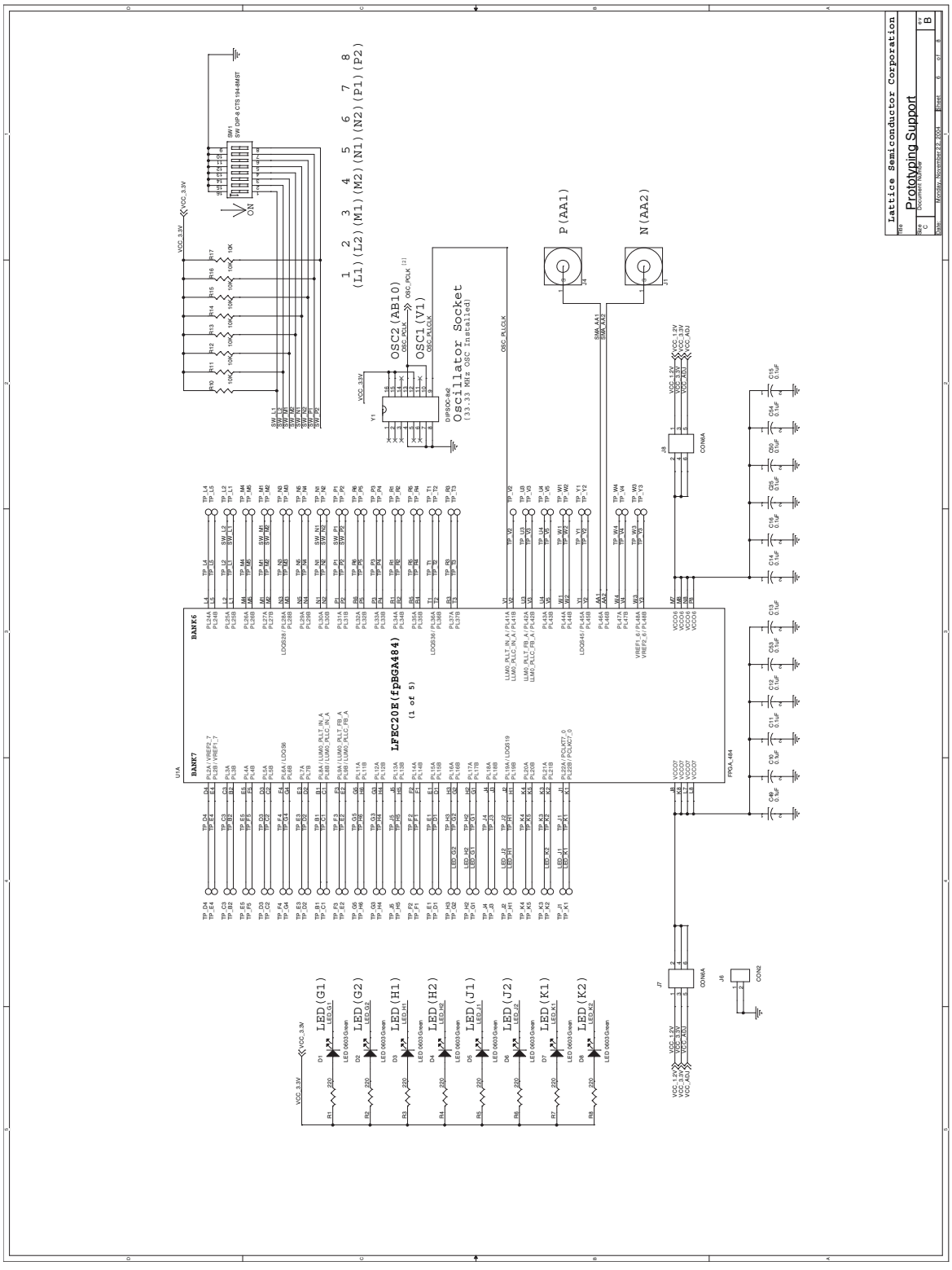


Figure 14. Power

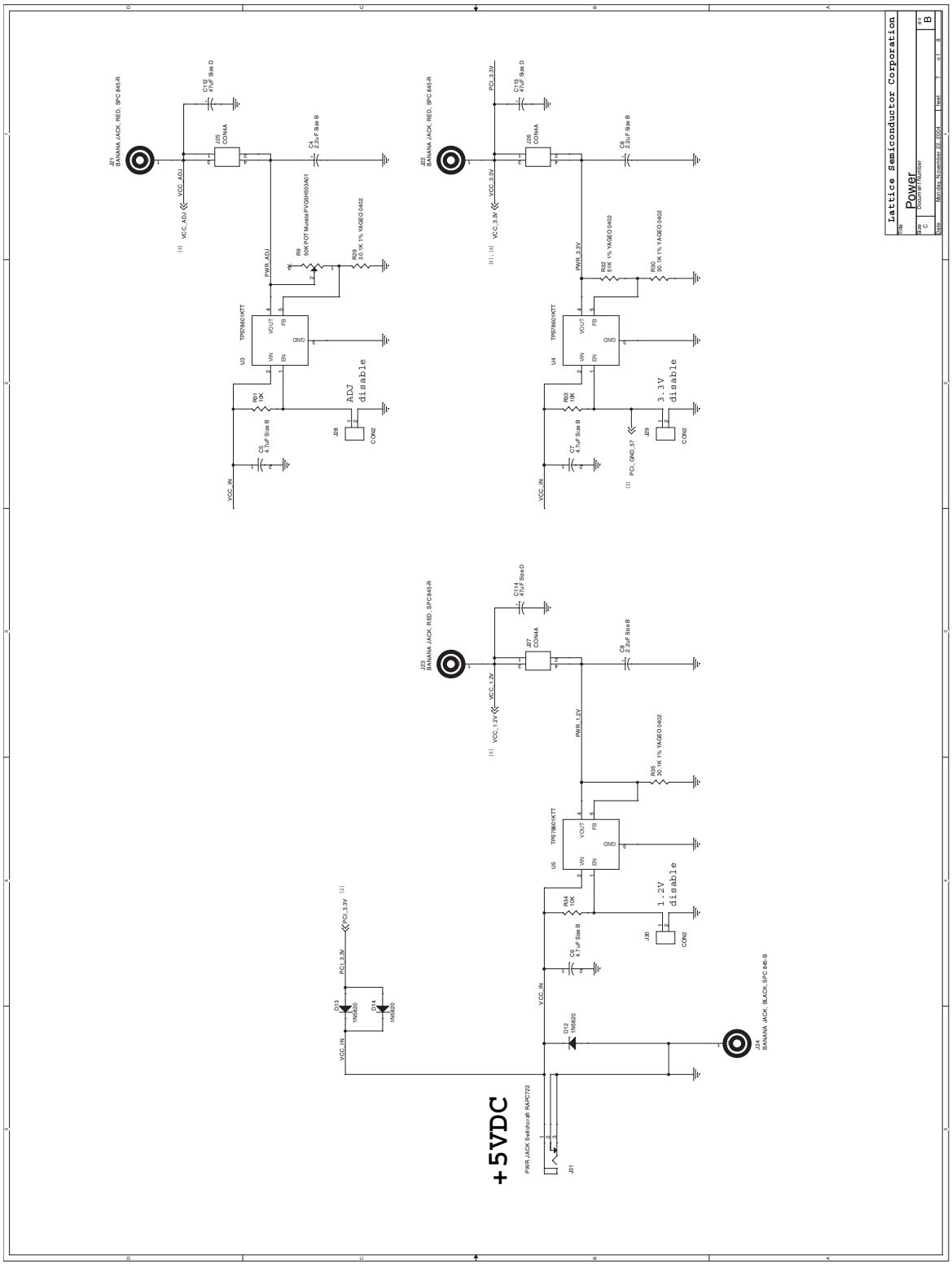
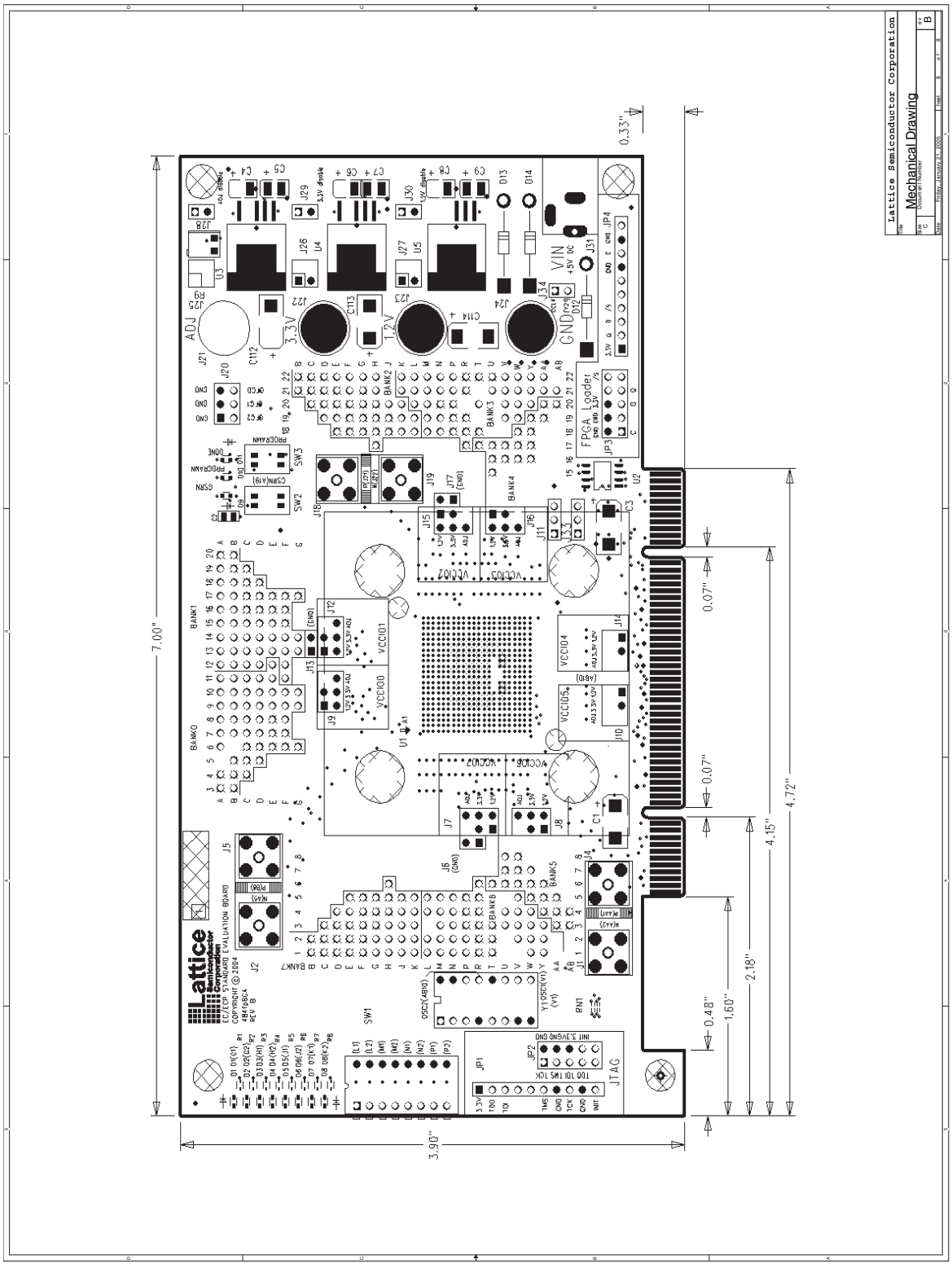


Figure 15. Mechanical Drawing



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