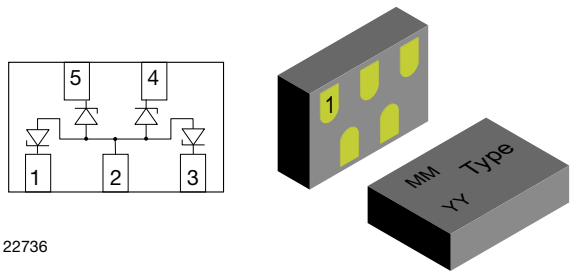
4-Line BUS-Port ESD Protection Array - Flow Through Design



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FEATURES

- Compact chip level page CLP1007-5L
- Length = 1 mm; width = 0.7 mm; height = 0.27 mm
- 4-lines, unidirectional ESD protection array
- Low leakage current I_R < 0.1 µA
- Low capacitance at V_R = 0 V = 0.9 pF (typ.)
- Ideal for high speed data line like
  - HDMI, DisplayPort, eSATA
  - USB, 1394/firewire
  - Thunderbolt
- ESD immunity acc. IEC 61000-4-2
  ± 15 kV contact discharge
  ± 15 kV air discharge
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

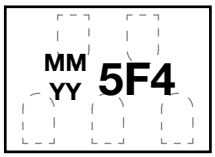
Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

MARKING



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Pin 1

5F4 = type code
MM = date code month
YY = date code year

DESIGN SUPPORT TOOLS click logo to get started

3D Models Available

ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS54FD-SD1	VBUS54FD-SD1-G4-08	10 000	10 000

PACKAGE DATA					
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS54FD-SD1	CLP1007-5L	5F4	0.1 mg	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	I_{PPM}	3	A
Peak pulse power	Acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	P_{PP}	45	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 15	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 15	
Operating temperature	Junction temperature	T_J	-40 to +125	°C
Storage temperature		T_{STG}	-55 to +150	°C

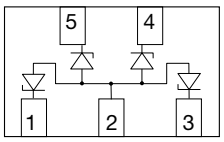
ELECTRICAL CHARACTERISTICS (pin 1, 3, 4 or 5 to pin 2) (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITIONS/REMARKS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	4	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5.5	V
Reverse voltage	at I_R = 0.1 µA	V_R	5.5	-	-	V
Reverse current	at V_{RWM} = 5.5 V	I_R	-	< 1 nA	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	6.9	7.5	8.7	V
Reverse clamping voltage	at I_{PP} = 1 A	V_C	-	9.5	11	V
	at I_{PP} = I_{PPM} = 3 A	V_C	-	12.9	15	V
Forward clamping voltage	at I_{PP} = 1 A	V_F	-	1.8	2.2	V
	at I_{PP} = 3 A	V_F	-	3	4	V
Capacitance	at V_R = 0 V; f = 1 MHz	C_D	-	0.9	1	pF
	at V_R = 3.3 V; f = 1 MHz		-	0.9	1	pF
Clamping voltage	Transmission Line Pulse (TLP); t_p = 100 ns, I_{TLP} = 8 A	V_{C-TLP}	-	18	-	V
Clamping voltage	Transmission Line Pulse (TLP); t_p = 100 ns, I_{TLP} = 16 A	V_{C-TLP}	-	24	-	V
Dynamic resistance	Transmission Line Pulse (TLP); t_p = 100 ns	V_{C-TLP}	-	0.93	-	Ω

APPLICATION NOTE

The **VBUS54FD-SD1** is a four-line ESD protection device with the characteristic of a Z-diode with a high ESD immunity and a very low capacitance which makes it usable for high frequency applications like USB 2.0, USB 3.0 or HDMI.
With the **VBUS54FD-SD1** four high speed data lines can be protected against transient voltage signals like ESD (electro static discharge). Connected to the data line (pin 1, 3 and pin 4, 5) and to ground (pin 2) negative transients will be clamped close below the ground level while positive transients will be clamped close above the 5.5 V working range. The clamping behavior of the **VBUS54FD-SD1** is bidirectional but asymmetrical (**BiAs**) and so it offers the best protection for applications running up to 5.5 V.

Pin configuration:

- Pin 2 is the central ground pin and has to be connected to ground
- Pin 1, 3 and 4, 5 are the inputs for the data lines D_{1+} and D_{1-} and D_{2+} and D_{2-}



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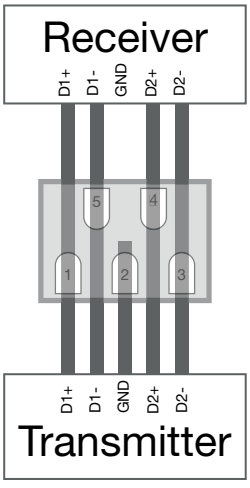

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FLOW THROUGH DESIGN

Modern digital transmission lines can be clocked up to 480 Mbit/s (USB 2.0) or 1.65 Gbit/s (HDMI).
At such high data rates the transmission lines like cables or the line traces on the PCBs have to be very homogeneous regarding their surge impedance. This requires well defined trace dimensions as trace width and distance which have to be calculated depending on the requested surge impedance (e.g. 50 Ω) and the PCB material and layer dimensions. Any device connected to the data lines - like ESD protection devices - have to be connected with minimal changes in these trace dimensions and distances.
With the package in the so called “Flow Through Design” this is possible. The lines are running straight along the PCB while the **VBUS54FD-SD1** is placed on top without any vias or loops.

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

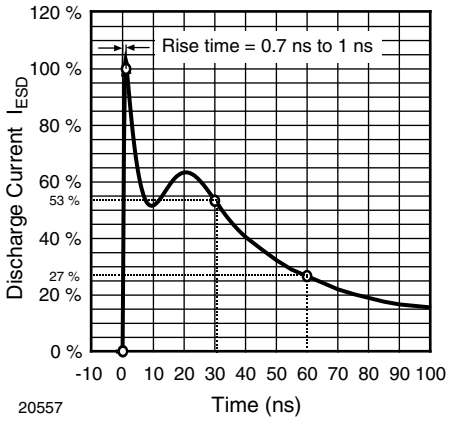


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

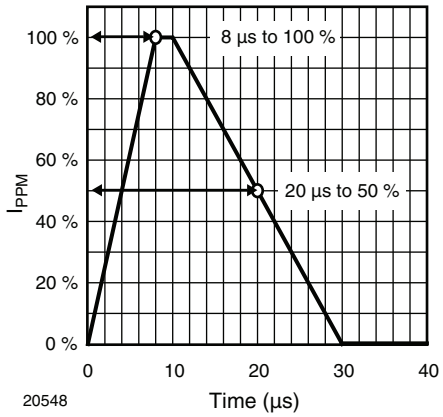


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

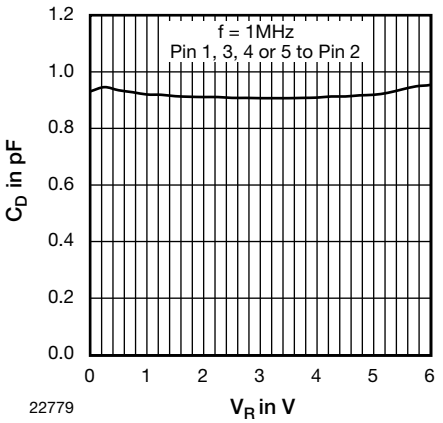


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

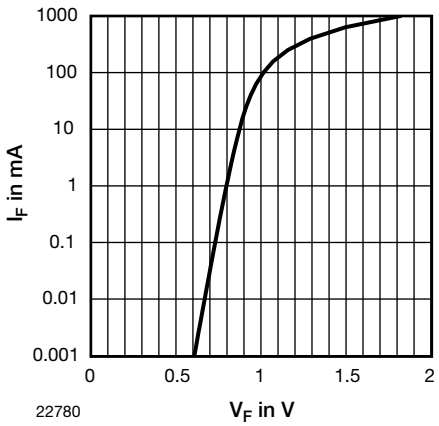


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

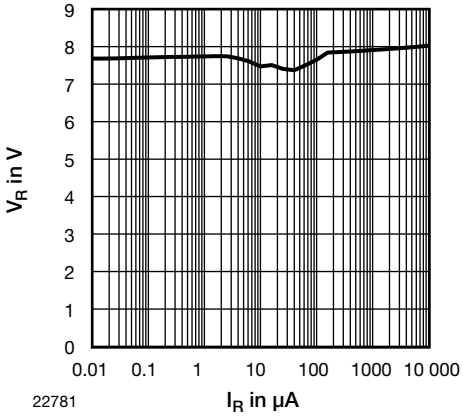


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

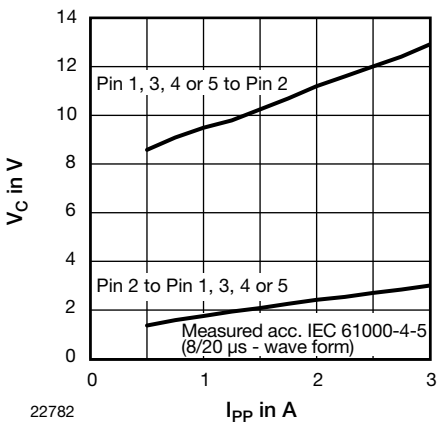


Fig. 6 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

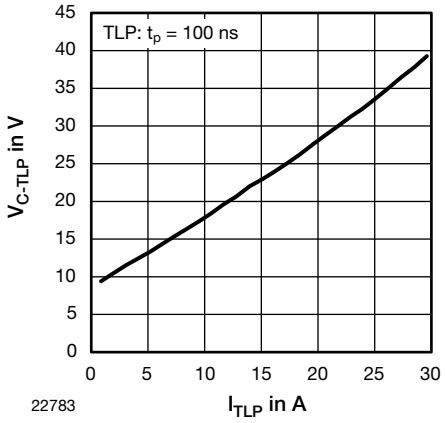
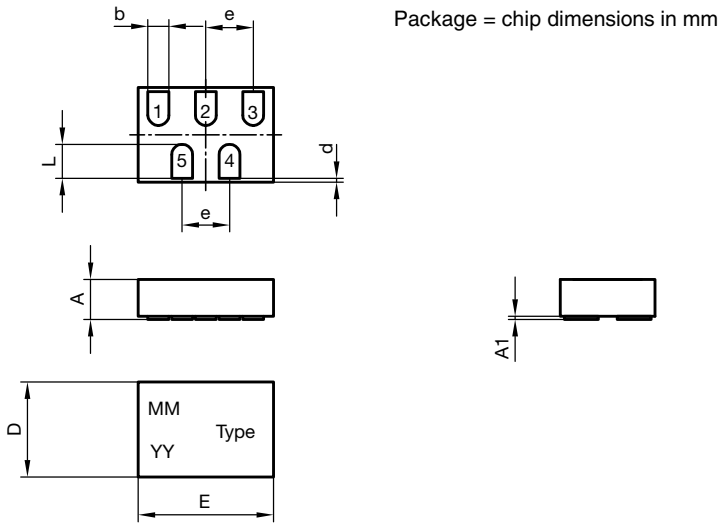


Fig. 7 - Typical Clamping Performance at 100 ns Transmission Line Pulse (TLP)

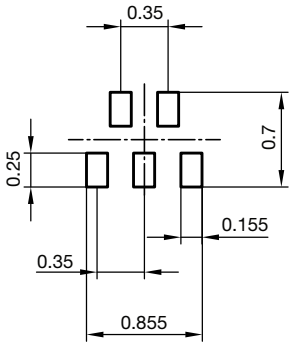
PACKAGE DIMENSIONS in millimeters: **CLP1007-5L**



Package = chip dimensions in mm

	Millimeters	
	min.	max.
A	0.25	0.29
A1	-	0.02
b	0.13	0.15
D	0.68	0.73
E	0.98	1.03
e	0.35	
L	0.23	0.27
Radius	0.075	
e	0.03	

foot print recommendation:



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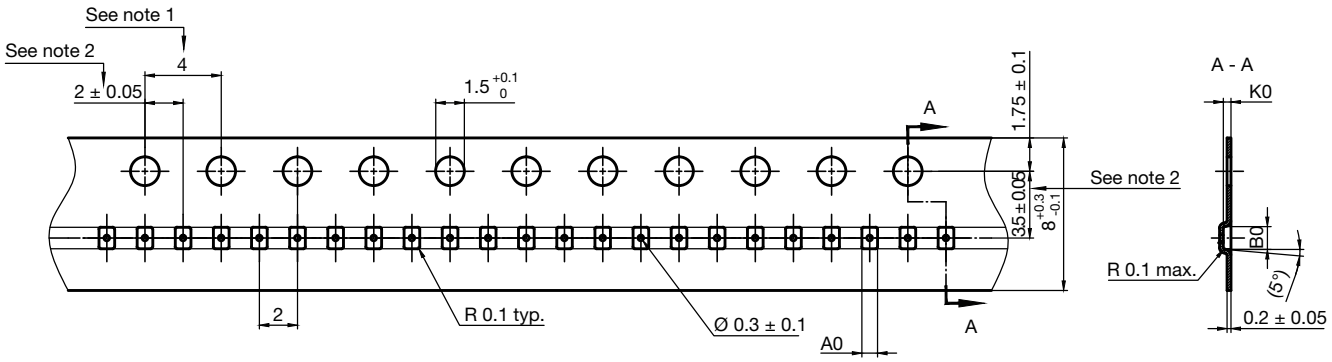
Footprint and soldering recommendation:
please see Application Note: www.vishay.com/doc?85917

CARRIER TAPE in millimeters: **CLP1007-5L**



A0 = 0.82 ± 0.05
B0 = 1.12 ± 0.05
K0 = 0.40 ± 0.05

Notes:
1. 10 Sprocket hole pitch cumulative tolerance ± 0.2
2. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole
3. A0 and B0 are calculated on a plane at a distance “R” above the bottom of the pocket

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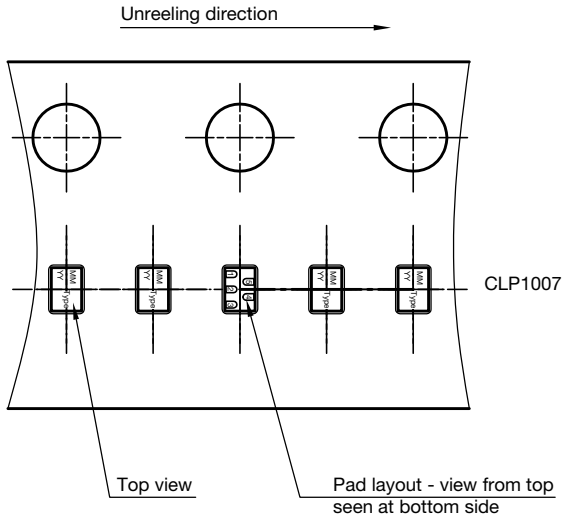
ORIENTATION IN CARRIER TAPE: CLP1007-5L



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