

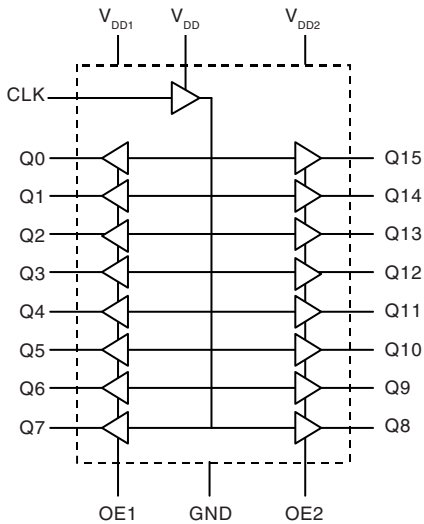
### General Description

The 8343-01 is a low skew, 1-to-16 LVCMOS/LVTTTL Fanout Buffer. The 8343-01 single ended clock input accepts LVCMOS or LVTTTL input levels. The ICS8343-01 operates at 3.3V, 2.5V and mixed 3.3V input and 2.5V supply modes over the commercial temperature range. Guaranteed output and part-to-part skew characteristics make the 8343-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

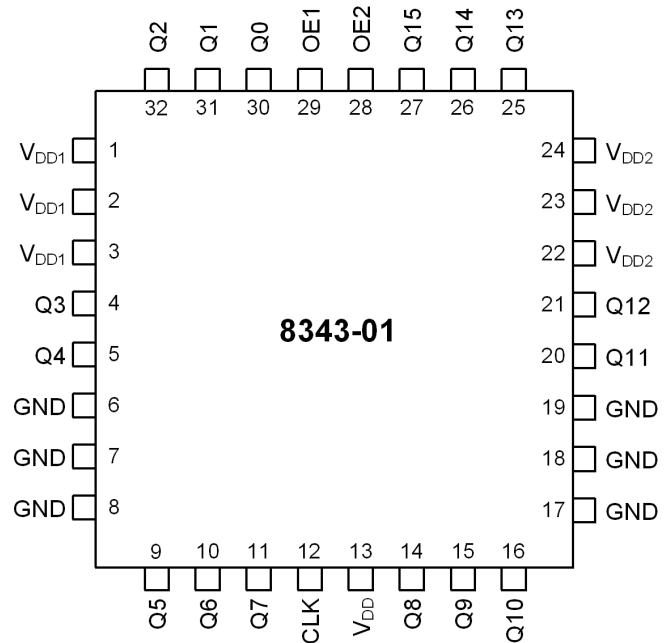
### Features

- 16 LVCMOS/LVTTTL outputs
- One LVCMOS/LVTTTL clock input
- CLK can accept the following input levels: LVCMOS, LVTTTL
- Maximum output frequency: 200MHz
- Dual output enable inputs facilitates 1-to-16 or 1-to-8 input to output modes
- All inputs are 5V tolerant
- Output skew: 250ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Full 3.3V and 2.5V or mixed 3.3V core/2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free packaging
- Industrial temperature information available upon request

### Block Diagram



### Pin Assignment



**32-Lead LQFP**  
**7mm x 7mm x 1.4mm body package**  
**Y Package**  
 (Top View)

## Pin Descriptions and Characteristics

Table 1. Pin Descriptions<sup>1</sup>

| Number | Name             | Type   |          | Description  |
|--------|------------------|--------|----------|--|
| 1      | V <sub>DD1</sub> | Power  |          | Q0 through Q7 output supply pin.   |
| 2      | V <sub>DD1</sub> | Power  |          | Q0 through Q7 output supply pin.   |
| 3      | V <sub>DD1</sub> | Power  |          | Q0 through Q7 output supply pin.   |
| 4      | Q3               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 5      | Q4               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 6      | GND              | Power  |          | Power supply ground.   |
| 7      | GND              | Power  |          | Power supply ground.   |
| 8      | GND              | Power  |          | Power supply ground.   |
| 9      | Q5               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 10     | Q6               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 11     | Q7               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 12     | CLK              | Input  | Pulldown | LVC MOS/LVTTL clock input / 5V tolerant.   |
| 13     | V <sub>DD</sub>  | Power  |          | Core supply pin.   |
| 14     | Q8               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 15     | Q9               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 16     | Q10              | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 17     | GND              | Power  |          | Power supply ground.   |
| 18     | GND              | Power  |          | Power supply ground.   |
| 19     | GND              | Power  |          | Power supply ground.   |
| 20     | Q11              | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 21     | Q12              | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 22     | V <sub>DD2</sub> | Power  |          | Q8 through Q15 output supply pin.  |
| 23     | V <sub>DD2</sub> | Power  |          | Q8 through Q15 output supply pin.  |
| 24     | V <sub>DD2</sub> | Power  |          | Q8 through Q15 output supply pin.  |
| 25     | Q13              | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 26     | Q14              | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 27     | Q15              | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 28     | OE2              | Input  | Pullup   | Output enable. When low forces outputs Q8 through Q15 to HiZ state. 5V tolerant. LVC MOS/LVTTL interface levels. |
| 29     | OE1              | Input  | Pullup   | Output enable. When low forces outputs Q0 through Q7 to HiZ state. 5V tolerant. LVC MOS/LVTTL interface levels.  |
| 30     | Q0               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 31     | Q1               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |
| 32     | Q2               | Output |          | LVC MOS/LVTTL clock output. 7Ω typical output impedance.   |

NOTE 1: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol         | Parameter                                  | Test Conditions                     | Minimum | Typical | Maximum | Units      |
|----------------|--|-------------------------------------|---------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance                          |                                     |         | 4       |         | pF         |
| $C_{PD}$       | Power Dissipation Capacitance (per output) | $V_{DD}, V_{DD1}, V_{DD2} = 3.465V$ |         | 11      |         | pF         |
|                |  | $V_{DD1}, V_{DD2} = 2.63V$          |         | 9       |         | pF         |
| $R_{PULLUP}$   | Input Pullup Resistor                      |                                     |         | 51      |         | k $\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor                    |                                     |         | 51      |         | k $\Omega$ |
| $R_{OUT}$      | Output Impedance                           | $V_{DD}, V_{DD1}, V_{DD2} = 3.3V$   | 5       | 7       | 12      | $\Omega$   |

**Table 3. Function Table<sup>1</sup>**

| Inputs |     | Outputs |        |
|--------|-----|---------|--------|
| OE1    | OE2 | Q0:Q7   | Q8:Q15 |
| 0      | 0   | HiZ     | HiZ    |
| 1      | 0   | Active  | HiZ    |
| 0      | 1   | HiZ     | Active |
| 1      | 1   | Active  | Active |

NOTE 1: OE1 and OE2 are 5V tolerant.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *Section , "DC Electrical Characteristics" or AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                     | Rating                    |
|--|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDx} + 0.5V$ |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |
| Maximum Junction Temperature, $T_{JMAX}$ | 125°C                     |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DD1} = V_{DD2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol    | Parameter                          | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|------------------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage                |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDx}$ | Output Supply Voltage <sup>1</sup> |                 | 3.135   | 3.3     | 3.465   | V     |
|           |                                    |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current               |                 |         |         | 35      | mA    |
| $I_{DDx}$ | Output Supply Current <sup>2</sup> |                 |         |         | 14      | mA    |

NOTE 1:  $V_{DDx}$  denotes  $V_{DD1}$  and  $V_{DD2}$ .

NOTE 2:  $I_{DDx}$  denotes the sum of  $I_{DD1}$  and  $I_{DD2}$ .

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol    | Parameter                          | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|------------------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage                |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDx}$ | Output Supply Voltage <sup>1</sup> |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current               |                 |         |         | 34      | mA    |
| $I_{DDx}$ | Output Supply Current <sup>2</sup> |                 |         |         | 13      | mA    |

NOTE 1:  $V_{DDx}$  denotes  $V_{DD1}$  and  $V_{DD2}$ .

NOTE 2:  $I_{DDx}$  denotes the sum of  $I_{DD1}$  and  $I_{DD2}$ .

**Table 4C. LVCMOS / LVTTTL DC Characteristics,  $V_{DD} = V_{DD1} = V_{DD2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol    | Parameter                        | Test Conditions                          | Minimum  | Typical | Maximum        | Units   |
|-----------|----------------------------------|--|--|---------|----------------|---------|
| $V_{IH}$  | Input High Voltage               | OE1, OE2                                 | 2  |         | $V_{DD} + 0.3$ | V       |
|           |                                  | CLK                                      | 2  |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$  | Input Low Voltage                | OE1, OE2                                 | -0.3   |         | 0.8            | V       |
|           |                                  | CLK                                      | -0.3   |         | 1.3            | V       |
| $I_{IH}$  | Input High Current               | OE1, OE2                                 | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$           |         | 5              | $\mu A$ |
|           |                                  | CLK                                      | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$           |         | 150            | $\mu A$ |
| $I_{IL}$  | Input Low Current                | OE1, OE2                                 | $V_{DD} = 3.465V$ or $2.625V$ ,<br>$V_{IN} = 0V$ | -150    |                | $\mu A$ |
|           |                                  | CLK                                      | $V_{DD} = 3.465V$ or $2.625V$ ,<br>$V_{IN} = 0V$ | -5      |                | $\mu A$ |
| $V_{OH}$  | Output High Voltage <sup>1</sup> | $V_{DD1} = V_{DD2} = 3.465V$             | 2.6  |         |                | V       |
|           |                                  | $V_{DD1} = V_{DD2} = 2.625V$             | 1.8  |         |                | V       |
| $V_{OL}$  | Output Low Voltage               | $V_{DD1} = V_{DD2} = 3.465V$ or $2.625V$ |  |         | 0.5            | V       |
| $I_{OZL}$ | Output Tristate Current Low      |  |  |         | 5              | $\mu A$ |
| $I_{OZH}$ | Output Tristate Current High     |  |  |         | 5              | $\mu A$ |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDx}/2$ . See Parameter Measurement Information, "Output Load Test Circuit Diagrams".

## AC Electrical Characteristics

**Table 5A. AC Electrical Characteristics,  $V_{DD} = V_{DD1} = V_{DD2} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ <sup>1</sup>**

| Symbol       | Parameter                         | Test Conditions                       | Minimum               | Typical        | Maximum               | Units |
|--------------|-----------------------------------|---------------------------------------|-----------------------|----------------|-----------------------|-------|
| $f_{MAX}$    | Output Frequency                  |                                       |                       |                | 200                   | MHz   |
| $t_{pLH}$    | Propagation Delay <sup>2</sup>    | $f \leq 200MHz$                       | 2.0                   |                | 4.0                   | ns    |
| $t_{sk(o)}$  | Output Skew <sup>3, 4</sup>       | Measured on rising edge @ $V_{DDx}/2$ |                       |                | 250                   | ps    |
| $t_{sk(pp)}$ | Part-to-Part Skew <sup>4, 5</sup> | Measured on rising edge @ $V_{DDx}/2$ |                       |                | 700                   | ps    |
| $t_R / t_F$  | Output Rise/ Fall Time            | 20% to 80%                            | 0.4                   |                | 1.5                   | ns    |
| odc          | Output Duty Cycle                 | $f \leq 133MHz$                       | 45                    |                | 55                    | %     |
| $t_{PW}$     | Output Pulse Width                | $f > 133MHz$                          | $t_{PERIOD}/2 - 0.25$ | $t_{PERIOD}/2$ | $t_{PERIOD}/2 + 0.25$ | ns    |

NOTE 1: All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 2: Measured from  $V_{DD}/2$  of the input to  $V_{DDx}/2$  of the output.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDx}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDx}/2$ .

**Table 5B. AC Electrical Characteristics,  $V_{DD} 3.3V \pm 5\%$ ,  $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ <sup>1</sup>**

| Symbol       | Parameter                         | Test Conditions                       | Minimum | Typical | Maximum | Units |
|--------------|-----------------------------------|---------------------------------------|---------|---------|---------|-------|
| $f_{MAX}$    | Output Frequency                  |                                       |         |         | 200     | MHz   |
| $t_{pLH}$    | Propagation Delay <sup>2</sup>    | $f \leq 200MHz$                       | 2.0     |         | 4.5     | ns    |
| $t_{sk(o)}$  | Output Skew <sup>3, 4</sup>       | Measured on rising edge @ $V_{DDx}/2$ |         |         | 250     | ps    |
| $t_{sk(pp)}$ | Part-to-Part Skew <sup>4, 5</sup> | Measured on rising edge @ $V_{DDx}/2$ |         |         | 700     | ps    |
| $t_R / t_F$  | Output Rise/ Fall Time            | 20% to 80%                            | 0.4     |         | 1.0     | ns    |
| odc          | Output Duty Cycle                 | $f \leq 133MHz$                       | 40      |         | 60      | %     |

NOTE 1: All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 2: Measured from  $V_{DD}/2$  of the input to  $V_{DDx}/2$  of the output.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDx}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDx}/2$ .

**Table 5C. AC Electrical Characteristics,  $V_{DD} = V_{DD2} = 3.3V \pm 5\%$ ,  $V_{DD1} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ <sup>1</sup>**

| Symbol      | Parameter                | Test Conditions                       | Minimum | Typical | Maximum | Units |
|-------------|--------------------------|---------------------------------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency         |                                       |         |         | 200     | MHz   |
| $t_{sk(o)}$ | Output Skew <sup>2</sup> | Measured on rising edge @ $V_{DDx}/2$ |         |         | 250     | ps    |

NOTE 1: All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 2: Defined as skew across outputs at the same supply voltages within a bank, and with equal load conditions.

**Table 5D. AC Electrical Characteristics,  $V_{DD} 3.3V \pm 5\%$ ,  $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ <sup>1</sup>**

| Symbol       | Parameter                         | Test Conditions                       | Minimum | Typical | Maximum | Units |
|--------------|-----------------------------------|---------------------------------------|---------|---------|---------|-------|
| $f_{MAX}$    | Output Frequency                  |                                       |         |         | 133     | MHz   |
| $t_{pLH}$    | Propagation Delay <sup>2</sup>    | $f \leq 200MHz$                       | 2.0     |         | 4.0     | ns    |
| $t_{sk(o)}$  | Output Skew <sup>3, 4</sup>       | Measured on rising edge @ $V_{DDx}/2$ |         |         | 250     | ps    |
| $t_{sk(pp)}$ | Part-to-Part Skew <sup>4, 5</sup> | Measured on rising edge @ $V_{DDx}/2$ |         |         | 1       | ns    |
| $t_R / t_F$  | Output Rise/ Fall Time            | 20% to 80%                            | 0.4     |         | 1.0     | ns    |
| odc          | Output Duty Cycle                 | $f \leq 133MHz$                       | 40      |         | 60      | %     |

NOTE 1: All parameters measured at  $f_{MAX}$  unless noted otherwise.

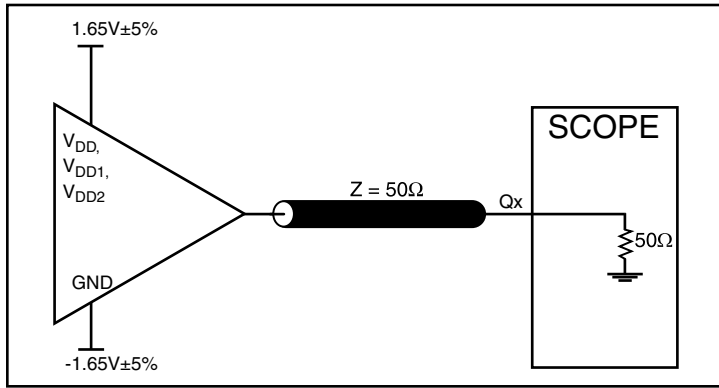
NOTE 2: Measured from  $V_{DD}/2$  of the input to  $V_{DDx}/2$  of the output.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDx}/2$ .

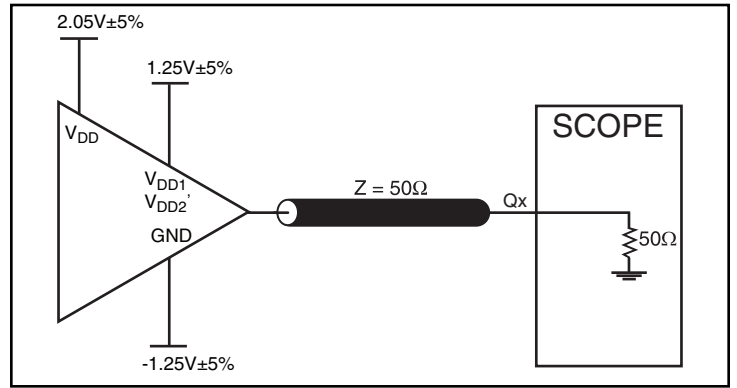
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDx}/2$ .

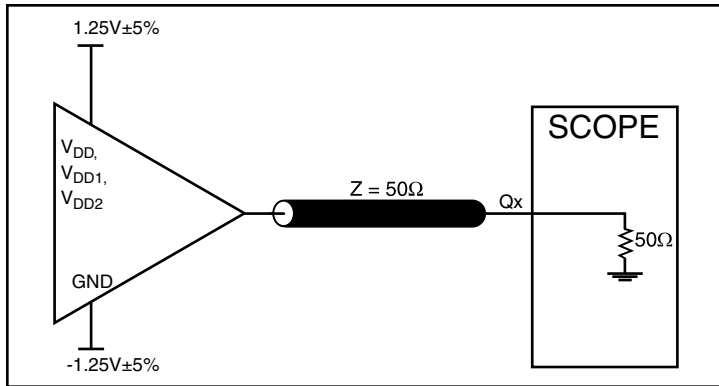
## Parameter Measurement Information



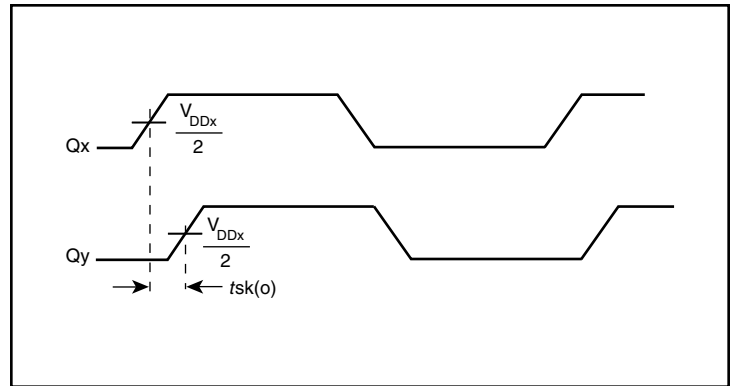
**3.3V Core/3.3V Output Load Test Circuit**



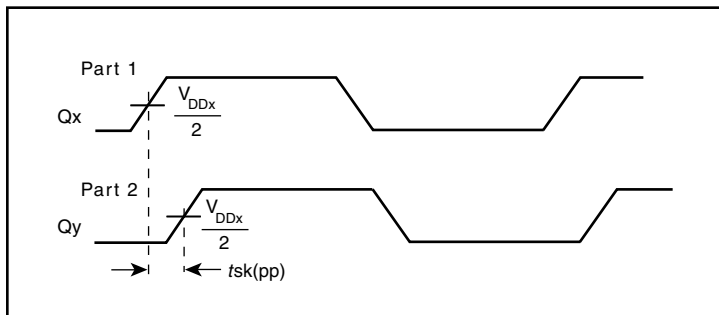
**3.3V Core/2.5V Output Load Test Circuit**



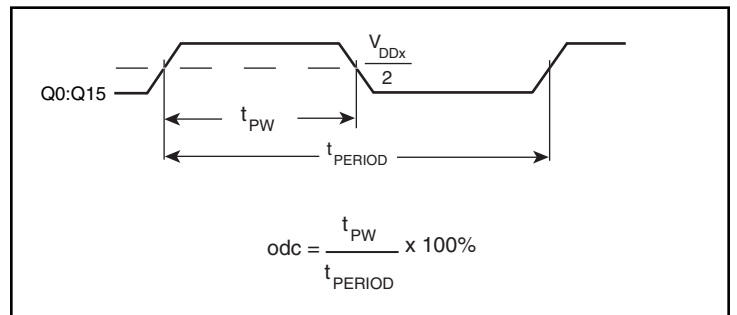
**2.5V Core/2.5V Output Load Test Circuit**



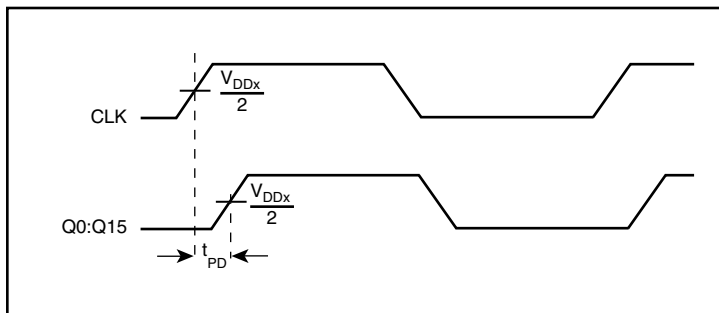
**Output Skew**



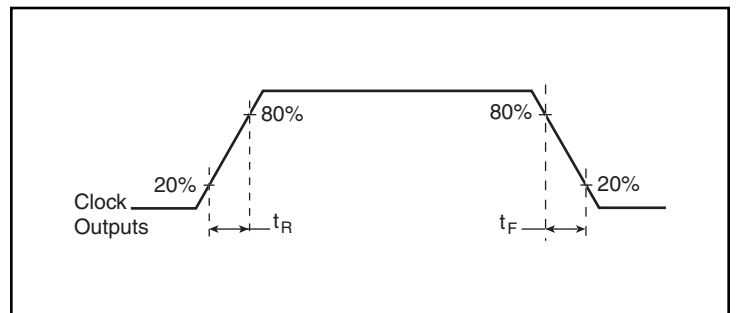
**Part-to-Part Skew**



**Output Duty Cycle/Pulse Width/Period**



**Propagation Delay**



**Output Rise/Fall Time**



## Reliability Information

**Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 32-Lead LQFP<sup>1</sup>**

| $\theta_{JA}$ by Velocity                    |          |          |          |
|--|----------|----------|----------|
| Linear Feet per Minute                       | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE 1: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Transistor Count

The transistor count for 8343-01 is 985.

## Package Outline and Package Dimensions

### Package Outline - Y Suffix for 32-Lead LQFP

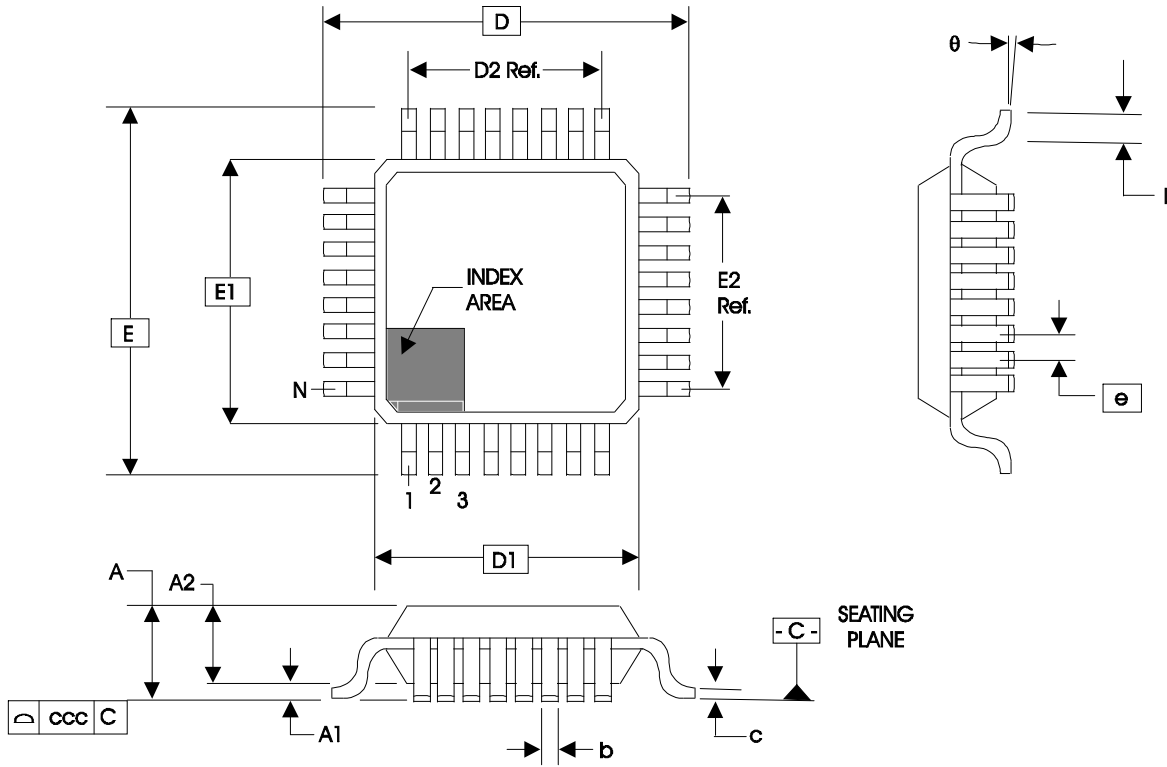


Table 7. Package Dimensions

| JEDEC Variation<br>All Dimensions in Millimeters |            |         |         |
|--|------------|---------|---------|
| Symbol   | Minimum    | Nominal | Maximum |
| N  |            | 32      |         |
| A  | –          | –       | 1.60    |
| A1   | 0.05       | –       | 0.15    |
| A2   | 1.35       | 1.40    | 1.45    |
| b  | 0.30       | 0.37    | 0.45    |
| c  | 0.09       | –       | 0.20    |
| D  | 9.00 Basic |         |         |
| D1   | 7.00 Basic |         |         |
| D2   | 5.60 Ref.  |         |         |
| E  | 9.00 Basic |         |         |
| E1   | 7.00 Basic |         |         |
| E2   | 5.60 Ref.  |         |         |
| e  | 0.80 Basic |         |         |
| L  | 0.45       | 0.60    | 0.75    |
| $\theta$   | 0°         | –       | 7°      |
| ccc  | –          | –       | 0.10    |

## Ordering Information

**Table 8. Ordering Information**

| Part/Order Number | Marking      | Package                  | Shipping Packaging | Temperature |
|-------------------|--------------|--------------------------|--------------------|-------------|
| 8343AY-01LF       | ICS8343AY01L | "Lead-Free" 32-Lead LQFP | Tray               | 0°C to 70°C |
| 8343AY-01LFT      | ICS8343AY01L | "Lead-Free" 32-Lead LQFP | Tape & Reel        | 0°C to 70°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change   | Date    |
|-----|-------|------|---|---------|
| A   | T2    | 2    | Pin Characteristics Table - changed $C_{IN}$ 4pF max to 4pF typical.<br>Added to $R_{OUT}$ , 5 $\Omega$ min. and 12 $\Omega$ max. | 9/18/03 |
|     | T8    | 11   | Ordering Information correct package column from 48 Lead to 32 Lead.  |         |
| B   | T5C   | 5    | Added Mixed AC Characteristics Table.<br>Updated format.  | 8/13/04 |
| B   | T8    | 9    | Added Lead-Free marking to Ordering Information Table.  | 9/16/04 |
| B   |       | 1    | Updated format and contact information.<br>General Description: Deleted HiPerClockS reference.                                    | 8/25/14 |
|     | T1    | 2    | Re-organized table sequentially.  |         |
|     | T8    | 10   | Removed leaded option.  |         |



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Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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