



ATmega809/1609/3209/4809 – 48-pin

48-pin Data Sheet – megaAVR® 0-series

Introduction

The ATmega809/1609/3209/4809 microcontrollers of the megaAVR® 0-series are using the AVR® processor with hardware multiplier, running at up to 20 MHz, with a wide range of Flash sizes up to 48 KB, up to 6 KB of SRAM, and 256 bytes of EEPROM in 28-, 32-, 40-, or 48-pin package. The series uses the latest technologies from Microchip with a flexible and low-power architecture including Event System and SleepWalking, accurate analog features and advanced peripherals.

The devices described here offer Flash sizes from 8 KB to 48 KB in a 48-pin package.

Features

- AVR® CPU
 - Single-cycle I/O access
 - Two-level interrupt controller
 - Two-cycle hardware multiplier
- Memories
 - Up to 48 KB In-system self-programmable Flash memory
 - 256B EEPROM
 - Up to 6 KB SRAM
 - Write/Erase endurance:
 - Flash 10,000 cycles
 - EEPROM 100,000 cycles
 - Data retention: 40 Years at 55°C
- System
 - Power-on Reset (POR) circuit
 - Brown-out Detector (BOD)
 - Clock options:
 - 16/20 MHz low-power internal oscillator
 - 32.768 kHz Ultra Low-Power (ULP) internal oscillator
 - 32.768 kHz external crystal oscillator
 - External clock input
 - Single pin Unified Program Debug Interface (UPDI)
 - Three sleep modes:
 - Idle with all peripherals running for immediate wake-up
 - Standby
 - Configurable operation of selected peripherals

- SleepWalking peripherals
 - Power-Down with limited wake-up functionality
- Peripherals
 - One 16-bit Timer/Counter type A (TCA) with a dedicated period register and three compare channels
 - Four 16-bit Timer/Counter type B with input capture (TCB)
 - One 16-bit Real-Time Counter (RTC) running from an external crystal or an internal RC oscillator
 - Four USART with fractional baud rate generator, auto-baud, and start-of-frame detection
 - Master/slave Serial Peripheral Interface (SPI)
 - Dual mode Master/Slave TWI with dual address match
 - Standard mode (Sm, 100 kHz)
 - Fast mode (Fm, 400 kHz)
 - Fast mode plus (Fm+, 1 MHz)
 - Event System for CPU independent and predictable inter-peripheral signaling
 - Configurable Custom Logic (CCL) with up to four programmable Look-up Tables (LUT)
 - One Analog Comparator (AC) with a scalable reference input
 - One 10-bit 150 ksps Analog to Digital Converter (ADC)
 - Five selectable internal voltage references: 0.55V, 1.1V, 1.5V, 2.5V, and 4.3V
 - CRC code memory scan hardware
 - Optional automatic scan before code execution is allowed
 - Watchdog Timer (WDT) with Window mode, with separate on-chip oscillator
 - External interrupt on all general purpose pins
- I/O and Packages:
 - 41 programmable I/O lines
 - 48-pin UQFN 6x6 and TQFP 7x7
- Temperature Range: -40°C to 125°C
- Speed Grades -40°C to 105°C:
 - 0-5 MHz @ 1.8V – 5.5V
 - 0-10 MHz @ 2.7V – 5.5V
 - 0-20 MHz @ 4.5V – 5.5V
- Speed Grades -40°C to 125°C:
 - 0-8 MHz @ 2.7V - 5.5V
 - 0-16 MHz @ 4.5V - 5.5V

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1. Block Diagram



2. Pinout






2.1 48-pin UQFN/TQFP



Power

-  Input supply
-  Ground
-  GPIO on VDD power domain
-  GPIO on AVDD power domain

Functionality

-  Programming, debug
-  Clock, crystal
-  TWI
-  Digital functions only
-  Analog functions

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I/O Multiplexing and Considerations

3. I/O Multiplexing and Considerations

3.1 Multiplexed Signals

| UQFN48/ TQFP48 | Pin name ^(1,2) | Special | ADC0 | AC0 | USARTn | SPI0 | TWI0 | TCA0 | TCBn | EVSYS | CCL-LUTn |
|-------------------|---------------------------|---------|-------|-----|-----------------------|---------------------|------------------------|----------------------|---------------------|-----------------------|----------------------|
| 44 | PA0 | EXTCLK | | | 0,TxD | | | 0-WO0 | | | 0-IN0 |
| 45 | PA1 | | | | 0,RxD | | | 0-WO1 | | | 0-IN1 |
| 46 | PA2 | TWI | | | 0,XCK | | SDA(MS) | 0-WO2 | 0-WO | EVOUTA | 0-IN2 |
| 47 | PA3 | TWI | | | 0,XDIR | | SCL(MS) | 0-WO3 | 1-WO | | 0-OUT |
| 48 | PA4 | | | | 0,TxD ⁽³⁾ | MOSI | | 0-WO4 | | | |
| 1 | PA5 | | | | 0,RxD ⁽³⁾ | MISO | | 0-WO5 | | | |
| 2 | PA6 | | | | 0,XCK ⁽³⁾ | SCK | | | | | 0-OUT ⁽³⁾ |
| 3 | PA7 | CLKOUT | | OUT | 0,XDIR ⁽³⁾ | SS | | | | EVOUTA ⁽³⁾ | |
| 4 | PB0 | | | | 3,TxD | | | 0-WO0 ⁽³⁾ | | | |
| 5 | PB1 | | | | 3,RxD | | | 0-WO1 ⁽³⁾ | | | |
| 6 | PB2 | | | | 3,XCK | | | 0-WO2 ⁽³⁾ | | EVOUTB | |
| 7 | PB3 | | | | 3,XDIR | | | 0-WO3 ⁽³⁾ | | | |
| 8 | PB4 | | | | 3,TxD ⁽³⁾ | | | 0-WO4 ⁽³⁾ | 2-WO ⁽³⁾ | | |
| 9 | PB5 | | | | 3,RxD ⁽³⁾ | | | 0-WO5 ⁽³⁾ | 3-WO | | |
| 10 | PC0 | | | | 1,TxD | MOSI ⁽³⁾ | | 0-WO0 ⁽³⁾ | 2-WO | | 1-IN0 |
| 11 | PC1 | | | | 1,RxD | MISO ⁽³⁾ | | 0-WO1 ⁽³⁾ | 3-WO ⁽³⁾ | | 1-IN1 |
| 12 | PC2 | TWI | | | 1,XCK | SCK ⁽³⁾ | SDA(MS) ⁽³⁾ | 0-WO2 ⁽³⁾ | | EVOUTC | 1-IN2 |
| 13 | PC3 | TWI | | | 1,XDIR | SS ⁽³⁾ | SCL(MS) ⁽³⁾ | 0-WO3 ⁽³⁾ | | | 1-OUT |
| 14 | VDD | | | | | | | | | | |
| 15 | GND | | | | | | | | | | |
| 16 | PC4 | | | | 1,TxD ⁽³⁾ | | | 0-WO4 ⁽³⁾ | | | |
| 17 | PC5 | | | | 1,RxD ⁽³⁾ | | | 0-WO5 ⁽³⁾ | | | |
| 18 | PC6 | | | | 1,XCK ⁽³⁾ | | | | | | 1-OUT ⁽³⁾ |
| 19 | PC7 | | | | 1,XDIR ⁽³⁾ | | | | | EVOUTC ⁽³⁾ | |
| 20 | PD0 | | AIN0 | | | | | 0-WO0 ⁽³⁾ | | | 2-IN0 |
| 21 | PD1 | | AIN1 | P3 | | | | 0-WO1 ⁽³⁾ | | | 2-IN1 |
| 22 | PD2 | | AIN2 | P0 | | | | 0-WO2 ⁽³⁾ | | EVOUTD | 2-IN2 |
| 23 | PD3 | | AIN3 | N0 | | | | 0-WO3 ⁽³⁾ | | | 2-OUT |
| 24 | PD4 | | AIN4 | P1 | | | | 0-WO4 ⁽³⁾ | | | |
| 25 | PD5 | | AIN5 | N1 | | | | 0-WO5 ⁽³⁾ | | | |
| 26 | PD6 | | AIN6 | P2 | | | | | | | 2-OUT ⁽³⁾ |
| 27 | PD7 | VREFA | AIN7 | N2 | | | | | | EVOUTD ⁽³⁾ | |
| 28 | AVDD | | | | | | | | | | |
| 29 | GND | | | | | | | | | | |
| 30 | PE0 | | AIN8 | | | MOSI ⁽³⁾ | | 0-WO0 ⁽³⁾ | | | |
| 31 | PE1 | | AIN9 | | | MISO ⁽³⁾ | | 0-WO1 ⁽³⁾ | | | |
| 32 | PE2 | | AIN10 | | | SCK ⁽³⁾ | | 0-WO2 ⁽³⁾ | | EVOUTE | |
| 33 | PE3 | | AIN11 | | | SS ⁽³⁾ | | 0-WO3 ⁽³⁾ | | | |
| 34 | PF0 | TOSC1 | | | 2,TxD | | | 0-WO0 ⁽³⁾ | | | 3-IN0 |
| 35 | PF1 | TOSC2 | | | 2,RxD | | | 0-WO1 ⁽³⁾ | | | 3-IN1 |
| 36 | PF2 | TWI | AIN12 | | 2,XCK | | SDA(S) ⁽³⁾ | 0-WO2 ⁽³⁾ | | EVOUTF | 3-IN2 |
| 37 | PF3 | TWI | AIN13 | | 2,XDIR | | SCL(S) ⁽³⁾ | 0-WO3 ⁽³⁾ | | | 3-OUT |

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.....continued

| UQFN48/ TQFP48 | Pin name ^(1,2) | Special | ADC0 | AC0 | USARTn | SPI0 | TWI0 | TCA0 | TCBn | EVSYS | CCL-LUTn |
|-------------------|---------------------------|---------|-------|-----|----------------------|------|------|----------------------|---------------------|-------|----------------------|
| 38 | PF4 | | AIN14 | | 2,TxD ⁽³⁾ | | | 0-WO4 ⁽³⁾ | 0-WO ⁽³⁾ | | |
| 39 | PF5 | | AIN15 | | 2,RxD ⁽³⁾ | | | 0-WO5 ⁽³⁾ | 1-WO ⁽³⁾ | | |
| 40 | PF6 | RESET | | | 2,XCK ⁽³⁾ | | | | | | 3-OUT ⁽³⁾ |
| 41 | UPDI | | | | | | | | | | |
| 42 | VDD | | | | | | | | | | |
| 43 | GND | | | | | | | | | | |

Note:

1. Pin names are of type Pxn, with x being the PORT instance (A,B,C, ...) and n the pin number. Notation for signals is PORTx_PINn. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection.
3. Alternate pin positions. For selecting the alternate positions, refer to the PORTMUX documentation.

4. Electrical Characteristics

4.1 Disclaimer

All typical values are measured at $T = 25^{\circ}\text{C}$ and $V_{\text{DD}} = 3\text{V}$ unless otherwise specified. All minimum and maximum values are valid across operating temperature and voltage unless otherwise specified.

Typical values given should be considered for design guidance only, and actual part variation around these values is expected.

4.2 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute Maximum Ratings

| Symbol | Description | Conditions | Min. | Max. | Unit |
|-----------------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------|---------------------|--------------------|
| V_{DD} | Power Supply Voltage | | -0.5 | 6 | V |
| I_{VDD} | Current into a V_{DD} pin | $T_{\text{A}}=[-40, 85]^{\circ}\text{C}$ | - | 200 | mA |
| | | $T_{\text{A}}=[85, 125]^{\circ}\text{C}$ | - | 100 | mA |
| I_{GND} | Current out of a GND pin | $T_{\text{A}}=[-40, 85]^{\circ}\text{C}$ | - | 200 | mA |
| | | $T_{\text{A}}=[85, 125]^{\circ}\text{C}$ | - | 100 | mA |
| V_{PIN} | Pin voltage with respect to GND | | -0.5 | $V_{\text{DD}}+0.5$ | V |
| I_{PIN} | I/O pin sink/source current | | -40 | 40 | mA |
| $I_{\text{c1}}^{(1)}$ | I/O pin injection current except for the RESET pin | $V_{\text{pin}} < \text{GND}-0.6\text{V}$ or $5.5\text{V} < V_{\text{pin}} \leq 6.1\text{V}$ $4.9\text{V} < V_{\text{DD}} \leq 5.5\text{V}$ | -1 | 1 | mA |
| $I_{\text{c2}}^{(1)}$ | I/O pin injection current except for the RESET pin | $V_{\text{pin}} < \text{GND}-0.6\text{V}$ or $V_{\text{pin}} \leq 5.5\text{V}$ $V_{\text{DD}} \leq 4.9\text{V}$ | -15 | 15 | mA |
| T_{storage} | Storage temperature | | -65 | 150 | $^{\circ}\text{C}$ |

Note:

- If V_{PIN} is lower than $\text{GND}-0.6\text{V}$, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (\text{GND}-0.6\text{V} - V_{\text{pin}})/I_{\text{CN}}$.
 - If V_{PIN} is greater than $V_{\text{DD}}+0.6\text{V}$, then a current limiting resistor is required. The positive DC injection current limiting resistor is calculated as $R = (V_{\text{pin}}-(V_{\text{DD}}+0.6))/I_{\text{CN}}$.

4.3 General Operating Ratings

The device must operate within the ratings listed in this section in order for all other electrical characteristics and typical characteristics of the device to be valid.

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Table 4-2. General Operating Conditions

| Symbol | Description | Condition | Min. | Max. | Unit |
|----------|-----------------------------|-----------|--------------------|------|------|
| V_{DD} | Operating Supply Voltage | | 1.8 ⁽¹⁾ | 5.5 | V |
| T_A | Operating temperature range | | -40 | 125 | °C |

Note:

1. Operation is guaranteed down to 1.8V or VBOD with BODLEVEL0, whichever is lower.

Table 4-3. Operating Voltage and Frequency

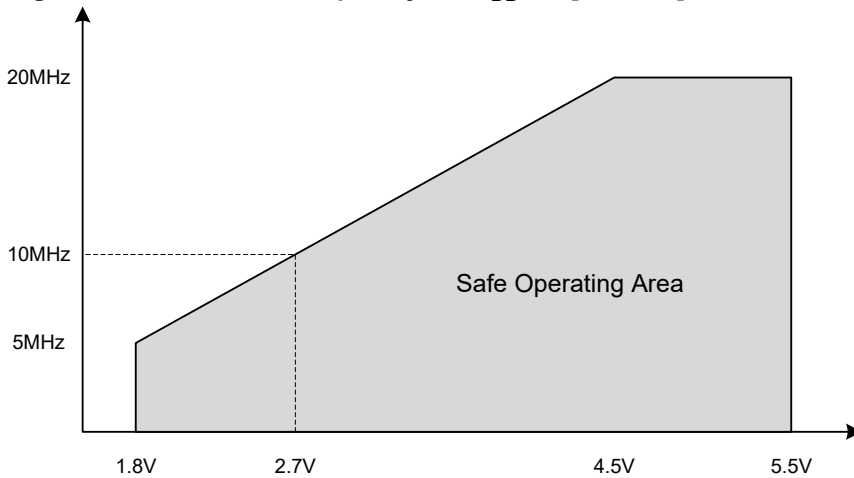
| Symbol | Description | Condition | Min. | Max. | Unit |
|----------------|------------------------------------------|-----------------------------------------------------|------|------|------|
| f_{CLK_CPU} | Nominal operating system clock frequency | $V_{DD}=[1.8, 5.5]V$ $T_A=[-40, 105]°C^{(1)(4)}$ | 0 | 5 | MHz |
| | | $V_{DD}=[2.7, 5.5]V$ $T_A=[-40, 105]°C^{(2)(4)}$ | 0 | 10 | |
| | | $V_{DD}=[4.5, 5.5]V$ $T_A=[-40, 105]°C^{(3)(4)}$ | 0 | 20 | |
| | | $V_{DD}=[2.7, 5.5]V$ $T_A=[-40, 125]°C^{(2)}$ | 0 | 8 | |
| | | $V_{DD}=[4.5, 5.5]V$ $T_A=[-40, 125]°C^{(2)}$ | 0 | 16 | |

Note:

1. Operation is guaranteed down to BOD triggering level, V_{BOD} with BODLEVEL0.
2. Operation is guaranteed down to BOD triggering level, V_{BOD} with BODLEVEL2.
3. Operation is guaranteed down to BOD triggering level, V_{BOD} with BODLEVEL7.
4. These specifications do not apply to automotive range parts (-VAO).

The maximum CPU clock frequency depends on V_{DD} . As shown in the figure below, the Maximum Frequency vs. V_{DD} is linear between $1.8V < V_{DD} < 2.7V$ and $2.7V < V_{DD} < 4.5V$.

Figure 4-1. Maximum Frequency vs. V_{DD} for $[-40, 105]^{\circ}\text{C}$



4.4 Power Considerations

The average die junction temperature, T_J (in $^{\circ}\text{C}$) is given from the formula

$$T_J = T_A + P_D \cdot R_{\theta JA}$$

where P_D is the total power dissipation.

The total thermal resistance of a package ($R_{\theta JA}$) can be separated into two components, $R_{\theta JC}$ and $R_{\theta CA}$, representing the barrier to heat flow from the semiconductor junction to the package (case) surface ($R_{\theta JC}$) and from the case to the outside ambient air ($R_{\theta CA}$). These terms are related by the equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

$R_{\theta JC}$ is device related and cannot be influenced by the user. However, $R_{\theta CA}$ is user dependent and can be minimized by thermal management techniques such as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce $R_{\theta CA}$ so that $R_{\theta JA}$ approximately equals $R_{\theta JC}$.

The power dissipation curve is negatively sloped as ambient temperature increase. The maximum power dissipation is therefore at minimum ambient temperature while the highest junction temperature occurs at the maximum ambient temperature.

Table 4-4. Power Dissipation and Junction Temperature vs Temperature

| Package | T_A Range | $R_{\theta JA}$ ($^{\circ}\text{C}/\text{W}$) | P_D (W) Typical | $T_J - T_A$ ($^{\circ}\text{C}$) Typical |
|---------|------------------------------------------------|-------------------------------------------------|-------------------|--------------------------------------------|
| UQFN48 | -40°C to 125°C | | 1.0 | |
| TQFP48 | -40°C to 125°C | | 1.0 | |

4.5 Power Consumption

The values are measured power consumption under the following conditions, except where noted:

- $V_{DD}=3\text{V}$
- $T_A=25^{\circ}\text{C}$
- OSC20M used as system clock source, except where otherwise specified

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- System power consumption measured with peripherals disabled and I/O ports driven low with inputs disabled

Table 4-5. Power Consumption in Active and Idle Mode

| Mode | Description | Condition | Typ. | Max. | Unit | |
|----------------------------------------------|--------------------------|----------------------------------------------|------------------------|---------------------------------------|---------------------|-----|
| Active | Active power consumption | f _{CLK_CPU} =20 MHz (OSC20M) | V _{DD} =5V | 8.5 | - | mA |
| | | f _{CLK_CPU} =10 MHz (OSC20M div2) | V _{DD} =5V | 4.3 | - | mA |
| | | | V _{DD} =3V | 2.3 | - | mA |
| | | f _{CLK_CPU} =5 MHz (OSC20M div4) | V _{DD} =5V | 2.2 | - | mA |
| | | | V _{DD} =3V | 1.2 | - | mA |
| | | | V _{DD} =2V | 0.75 | - | mA |
| | | f _{CLK_CPU} =32.768 kHz (OSCULP32K) | V _{DD} =5V | 16.4 | - | μA |
| | | | V _{DD} =3V | 9.0 | - | μA |
| | | | V _{DD} =2V | 6.0 | - | μA |
| | | Idle | Idle power consumption | f _{CLK_CPU} =20 MHz (OSC20M) | V _{DD} =5V | 2.8 |
| f _{CLK_CPU} =10 MHz (OSC20M div2) | V _{DD} =5V | | | 1.4 | - | mA |
| | V _{DD} =3V | | | 0.8 | - | mA |
| f _{CLK_CPU} =5 MHz (OSC20M div4) | V _{DD} =5V | | | 0.7 | - | mA |
| | V _{DD} =3V | | | 0.4 | - | mA |
| | V _{DD} =2V | | | 0.25 | - | mA |
| f _{CLK_CPU} =32.768 kHz (OSCULP32K) | V _{DD} =5V | | | 5.6 | - | μA |
| | V _{DD} =3V | | | 2.8 | - | μA |
| | V _{DD} =2V | | | 1.8 | - | μA |

Table 4-6. Power Consumption in Power-Down, Standby and Reset Mode

| Mode | Description | Condition | Typ. 25°C | Max. 85°C ⁽¹⁾ | Max. 125°C | Unit | |
|---------|---------------------------|------------------------------------------------------------|---------------------|-----------------------------|---------------|------|----|
| Standby | Standby power consumption | RTC running at 1.024 kHz from external XOSC32K (CL=7.5 pF) | V _{DD} =3V | 0.7 | - | - | μA |
| | | RTC running at 1.024 kHz from internal OSCULP32K | V _{DD} =3V | 0.7 | 6.0 | 16.0 | μA |

.....continued

| Mode | Description | Condition | Typ. 25°C | Max. 85°C ⁽¹⁾ | Max. 125°C | Unit |
|------------------------|----------------------------------------------------------------------------------------|-------------------------|----------------------------|-----------------------------|---------------|------|
| Power Down/ Standby | Power down/ Standby power consumption are the same when all peripherals are stopped | All peripherals stopped | V _{DD} =3V 0.1 | 5.0 | 15.0 | μA |
| Reset | Reset power consumption | RESET line pulled low | V _{DD} =3V 100 | - | - | μA |

Note:

1. These parameters are for design guidance only and are not tested.

4.6 Peripherals Power Consumption

The table below can be used to calculate the additional current consumption for the different I/O peripherals in the various operating modes.

Some peripherals will request the clock to be enabled when operating in STANDBY. See the peripheral chapter for further information.

Operating conditions:

- V_{DD}=3V
- T=25°C
- OSC20M at 1 MHz used as system clock source, except where otherwise specified
- In Idle Sleep mode, except where otherwise specified

Table 4-7. Peripherals Power Consumption

| Peripheral | Conditions | Typ. ⁽¹⁾ | Unit |
|---------------------------|-------------------------------|---------------------|------|
| BOD | Continuous | 19 | μA |
| | Sampling @ 1 kHz | 1.2 | |
| TCA | 16-bit count @ 1 MHz | 13.0 | μA |
| TCB | 16-bit count @ 1 MHz | 7.4 | μA |
| RTC | 16-bit count @ OSCULP32K | 1.2 | μA |
| WDT (including OSCULP32K) | | 0.7 | μA |
| OSC20M | | 130 | μA |
| AC | Fast Mode ⁽²⁾ | 92 | μA |
| | Low-Power Mode ⁽²⁾ | 45 | |
| ADC ⁽³⁾ | 50 ksps | 330 | μA |
| | 100 ksps | 340 | |

|continued | | | |
|-------------------|--------------------|---------------------|------|
| Peripheral | Conditions | Typ. ⁽¹⁾ | Unit |
| XOSC32K | $C_L=7.5$ pF | 0.5 | μA |
| OSCUPLP32K | | 0.4 | μA |
| USART | Enable @ 9600 Baud | 13.0 | μA |
| SPI (Master) | Enable @ 100 kHz | 2.1 | μA |
| TWI (Master) | Enable @ 100 kHz | 24.0 | μA |
| TWI (Slave) | Enable @ 100 kHz | 17.0 | μA |
| Flash programming | Erase Operation | 1.5 | mA |
| | Write Operation | 3.0 | |

Note:

1. Current consumption of the module only. To calculate the total internal power consumption of the microcontroller, add this value to the base power consumption given in “Power Consumption” section in electrical characteristics.
2. CPU in Standby mode.
3. Average power consumption with ADC active in Free-Running mode.

4.7 BOD and POR Characteristics

Table 4-8. Power Supply Characteristics

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---------------------|----------------|-----------|------|------|--------------------|------|
| SRON ⁽¹⁾ | Power-on Slope | | - | - | 100 ⁽²⁾ | V/ms |

Note:

1. For design guidance only and not tested in production.
2. A slope faster than the maximum rating can trigger a reset of the device if changing the voltage level after an initial power-up.

Table 4-9. Power-on Reset (POR) Characteristics

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------------------------|--------------------------------------------------|--------------------|------|--------------------|------|
| V _{POR} | POR threshold voltage on V _{DD} falling | V _{DD} falls/rises at 0.5V/ms or slower | 0.8 ⁽¹⁾ | - | 1.6 ⁽¹⁾ | V |
| | POR threshold voltage on V _{DD} rising | | 1.4 ⁽¹⁾ | - | 1.8 | |

Note:

1. For design guidance only and not tested in production.

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Table 4-10. Brown-out Detector (BOD) Characteristics

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|----------------------|------------------------------------------|--------------------------------------------|------|------|------|------|
| V _{BOD} | BOD detection level (falling/ rising) | BODLEVEL0 | 1.7 | 1.8 | 2.0 | V |
| | | BODLEVEL2 | 2.4 | 2.6 | 2.9 | |
| | | BODLEVEL7 | 3.9 | 4.3 | 4.5 | |
| V _{HYS} | Hysteresis | BODLEVEL0 | - | 25 | - | mV |
| | | BODLEVEL2 | - | 40 | - | |
| | | BODLEVEL7 | - | 80 | - | |
| t _{BOD} | Detection time | Continuous | - | 7 | - | μs |
| | | Sampled, 1 kHz | - | 1 | - | ms |
| | | Sampled, 125 Hz | - | 8 | - | |
| t _{startup} | Start-up time | Time from enable to ready | - | 40 | - | μs |
| V _{INT} | Interrupt level 0 | Percentage above the selected BOD level | - | 4 | - | % |
| | Interrupt level 1 | | - | 13 | - | |
| | Interrupt level 2 | | - | 25 | - | |

4.8 External Reset Characteristics

Table 4-11. External Reset Characteristics

| Mode | Description | Condition | Min. | Typ. | Max. | Unit |
|----------------------|---------------------------------------------------------------------|------------------------|---------------------|------|----------------------|------|
| V _{VIH_RST} | Input Voltage for $\overline{\text{RESET}}$ | | 0.7×V _{DD} | - | V _{DD} +0.2 | V |
| V _{VIL_RST} | Input Low Voltage for $\overline{\text{RESET}}$ | | -0.2 | - | 0.3×V _{DD} | |
| t _{MIN_RST} | Minimum pulse width on $\overline{\text{RESET}}$ pin ⁽¹⁾ | | - | - | 2.5 | μs |
| R _{p_RST} | $\overline{\text{RESET}}$ pull-up resistor | V _{Reset} =0V | 20 | 35 | 50 | kΩ |

Note:

- These parameters are for design guidance only and are not production tested.

4.9 Oscillators and Clocks

Operating conditions:

- V_{DD}=3V, except where specified otherwise

Table 4-12. 20 MHz Internal Oscillator (OSC20M) Characteristics

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---------------------|-------------------------------|-----------|----------------------------|------|------|------|
| f _{OSC20M} | Factory calibration frequency | FREQSEL=0 | T _A =25°C, 3.0V | | 16 | MHz |
| | | FREQSEL=1 | | | 20 | |

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Electrical Characteristics

.....continued

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit | |
|----------------------|----------------------------------------------------------------------------------------------------|-------------------------------------------------------|---------------------------------------------------------|------|------|------|---|
| f _{CAL} | Frequency calibration range | OSC16M ⁽²⁾ | 14.5 | | 17.5 | MHz | |
| | | OSC20M ⁽²⁾ | 18.5 | | 21.5 | MHz | |
| E _{TOTAL} | Total error with 16 MHz and 20 MHz frequency selection | From target frequency | T _A =25°C, 3.0V | -1.5 | | 1.5 | % |
| | | | T _A =[0, 70]°C, V _{DD} =[1.8, 3.6]V | -2.0 | | 2.0 | % |
| | | | Full operation range | -4.0 | | 4.0 | |
| E _{DRIFT} | Accuracy with 16 MHz and 20 MHz frequency selection relative to the factory-stored frequency value | Factory calibrated V _{DD} =3V ⁽¹⁾ | T _A =[0, 70]°C, V _{DD} =[1.8, 5.5]V | -1.8 | | 1.8 | % |
| Δf _{OSC20M} | Calibration step size | | - | 0.75 | - | % | |
| D _{OSC20M} | Duty cycle | | - | 50 | - | % | |
| t _{startup} | Start-up time | Within 2% accuracy | - | 12 | - | μs | |

Note:

1. See also the description of OSC20M on calibration.
2. Oscillator Frequencies above speed specification must be divided so the CPU clock is always within specification.

Table 4-13. 32.768 kHz Internal Oscillator (OSCULP32K) Characteristics

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|------------------------|-----------------------------------|---------------------------------------------------------|------|--------|------|------|
| f _{OSCULP32K} | Factory calibration frequency | | | 32.768 | | kHz |
| | Factory calibration accuracy | T _A =25°C, 3.0V | -3 | | 3 | % |
| E _{TOTAL} | Total error from target frequency | T _A =[0, 70]°C, V _{DD} =[1.8, 3.6]V | -10 | | +10 | % |
| | | Full operation range | -20 | | +20 | |
| D _{OSCULP32K} | Duty cycle | | | 50 | | % |
| t _{startup} | Start-up time | | - | 250 | - | μs |

Table 4-14. 32.768 kHz External Crystal Oscillator (XOSC32K) Characteristics

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|--------------------------|-----------------------------------------|------------------------|------|--------|------|------|
| f _{out} | Frequency | | - | 32.768 | - | kHz |
| t _{startup} | Start-up time | C _L =7.5 pF | - | 300 | - | ms |
| C _L | Crystal load capacitance ⁽¹⁾ | | 7.5 | - | 12.5 | pF |
| C _{TOSC1/TOSC2} | Parasitic pin capacitance | | - | 5.5 | - | pF |

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Electrical Characteristics

.....continued

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|--------------------|------------------------------------------------|---------------|------|------|------|------------|
| ESR ⁽¹⁾ | Equivalent Series Resistance - Safety Factor=3 | $C_L=7.5$ pF | - | - | 80 | k Ω |
| | | $C_L=12.5$ pF | - | - | 40 | |

Note:

1. This parameter is for design guidance only and not production tested.

Figure 4-2. External Clock Waveform Characteristics



Table 4-15. External Clock Characteristics

| Symbol | Description | Condition | $V_{DD}=[1.8, 5.5]$ V | | $V_{DD}=[2.7, 5.5]$ V | | $V_{DD}=[4.5, 5.5]$ V | | Unit |
|-------------------------|---------------------------------------------------|-----------|-----------------------|------|-----------------------|------|-----------------------|------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| f_{CLCL} | Frequency | | 0 | 5.0 | 0.0 | 10.0 | 0.0 | 20.0 | MHz |
| t_{CLCL} | Clock Period | | 200 | - | 100 | - | 50 | - | ns |
| $t_{CHCX}^{(1)}$ | High Time | | 80 | - | 40 | - | 20 | - | ns |
| $t_{CLCX}^{(1)}$ | Low Time | | 80 | - | 40 | - | 20 | - | ns |
| $t_{CLCH}^{(1)}$ | Rise Time (for maximum frequency) | | - | 40 | - | 20 | - | 10 | ns |
| $t_{CHCL}^{(1)}$ | Fall Time (for maximum frequency) | | - | 40 | - | 20 | - | 10 | ns |
| $\Delta t_{CLCL}^{(1)}$ | Change in period from one clock cycle to the next | | - | 20 | - | 20 | - | 20 | % |

Note:

1. This parameter is for design guidance only and not production tested.

4.10 I/O Pin Characteristics

Table 4-16. I/O Pin Characteristics ($T_A=[-40, 85]^\circ\text{C}$, $V_{DD}=[1.8, 5.5]$ V unless otherwise noted)

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|----------|--------------------|-----------|---------------------|------|------------------------|------|
| V_{IL} | Input Low Voltage | | -0.2 | - | $0.3 \times V_{DD}$ | V |
| V_{IH} | Input High Voltage | | $0.7 \times V_{DD}$ | - | $V_{DD} + 0.2\text{V}$ | V |

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Electrical Characteristics

.....continued

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------------------------------|-----------------------------------------------------------------------------|---------------------------------------------------------|------|--------|------|------|
| I _{IH} / I _{IL} | I/O pin Input Leakage Current | V _{DD} =5.5V, pin high | - | < 0.05 | - | μA |
| | | V _{DD} =5.5V, pin low | - | < 0.05 | - | |
| V _{OL} | I/O pin drive strength | V _{DD} =1.8V, I _{OL} =1.5 mA | - | - | 0.36 | V |
| | | V _{DD} =3.0V, I _{OL} =7.5 mA | - | - | 0.6 | |
| | | V _{DD} =5.0V, I _{OL} =15 mA | - | - | 1 | |
| V _{OH} | I/O pin drive strength | V _{DD} =1.8V, I _{OH} =1.5 mA | 1.44 | - | - | V |
| | | V _{DD} =3.0V, I _{OH} =7.5 mA | 2.4 | - | - | |
| | | V _{DD} =5.0V, I _{OH} =15 mA | 4 | - | - | |
| I _{total} | Maximum combined I/O sink/ source current per pin group ^(1,2) | T _A =125°C | - | - | 100 | mA |
| | Maximum combined I/O sink/ source current per pin group ^(1,2) | T _A =25°C | - | - | 200 | |
| t _{RISE} | Rise time | V _{DD} =3.0V, load=20 pF | - | 2.5 | - | ns |
| | | V _{DD} =5.0V, load=20 pF | - | 1.5 | - | |
| | | V _{DD} =3.0V, load=20 pF, slew rate enabled | - | 19 | - | |
| | | V _{DD} =5.0V, load=20 pF, slew rate enabled | - | 9 | - | |
| t _{FALL} | Fall time | V _{DD} =3.0V, load=20 pF | - | 2.0 | - | ns |
| | | V _{DD} =5.0V, load=20 pF | - | 1.3 | - | |
| | | V _{DD} =3.0V, load=20 pF, slew rate enabled | - | 21 | - | |
| | | V _{DD} =5.0V, load=20 pF, slew rate enabled | - | 11 | - | |
| C _{pin} | I/O pin capacitance except for TOSC, VREFA, and TWI pins | | - | 3.5 | - | pF |
| C _{pin} | I/O pin capacitance on TOSC pins | | - | 4 | - | pF |
| C _{pin} | I/O pin capacitance on TWI pins | | - | 10 | - | pF |
| C _{pin} | I/O pin capacitance on VREFA pin | | - | 14 | - | pF |
| R _p | Pull-up resistor | | 20 | 35 | 50 | kΩ |

Note:

1. Pin group A (PA[7:0]), PF[6:2]), pin group B (PB[7:0], PC[7:0]), pin group C (PD:7:0, PE[3:0], PF[1:0]). For 28-pin and 32-pin devices pin group A and B should be seen as a single group. The combined continuous sink/source current for each individual group should not exceed the limits.
2. These parameters are for design guidance only and are not production tested.

4.11 USART

Figure 4-3. USART in SPI Mode - Timing Requirements in Master Mode



Table 4-17. USART in SPI Master Mode - Timing Characteristics

| Symbol ⁽¹⁾ | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|---------------------|-----------|------|----------------------|------|------|
| f_{SCK} | SCK clock frequency | Master | - | - | 10 | MHz |
| t_{SCK} | SCK period | Master | 100 | - | - | ns |
| t_{SCKW} | SCK high/low width | Master | - | $0.5 \times t_{SCK}$ | - | ns |
| t_{SCKR} | SCK rise time | Master | - | 2.7 | - | ns |
| t_{SCKF} | SCK fall time | Master | - | 2.7 | - | ns |
| t_{MIS} | MISO setup to SCK | Master | - | 10 | - | ns |
| t_{MIH} | MISO hold after SCK | Master | - | 10 | - | ns |
| t_{MOS} | MOSI setup to SCK | Master | - | $0.5 \times t_{SCK}$ | - | ns |
| t_{MOH} | MOSI hold after SCK | Master | - | 1.0 | - | ns |

Note:

1. These parameters are for design guidance only and are not production tested.

4.12 SPI

Figure 4-4. SPI - Timing Requirements in Master Mode

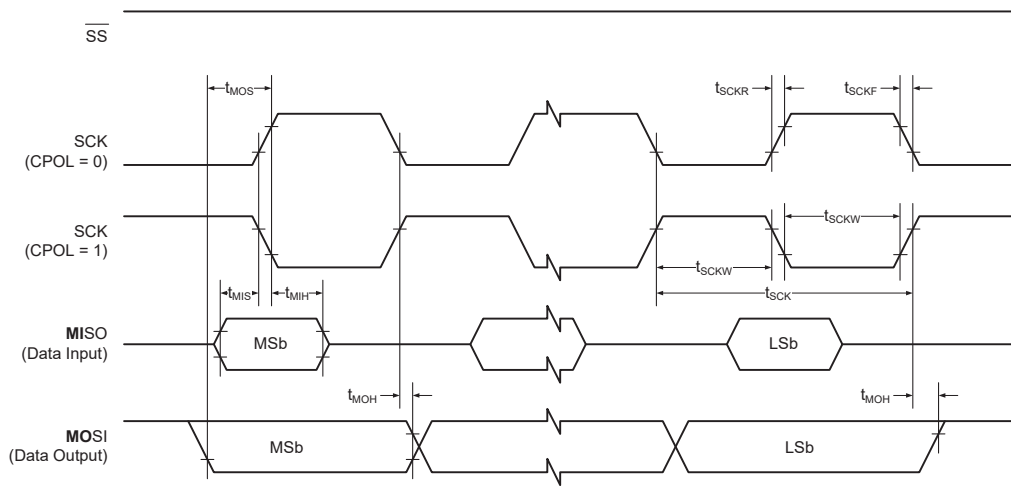


Figure 4-5. SPI - Timing Requirements in Slave Mode

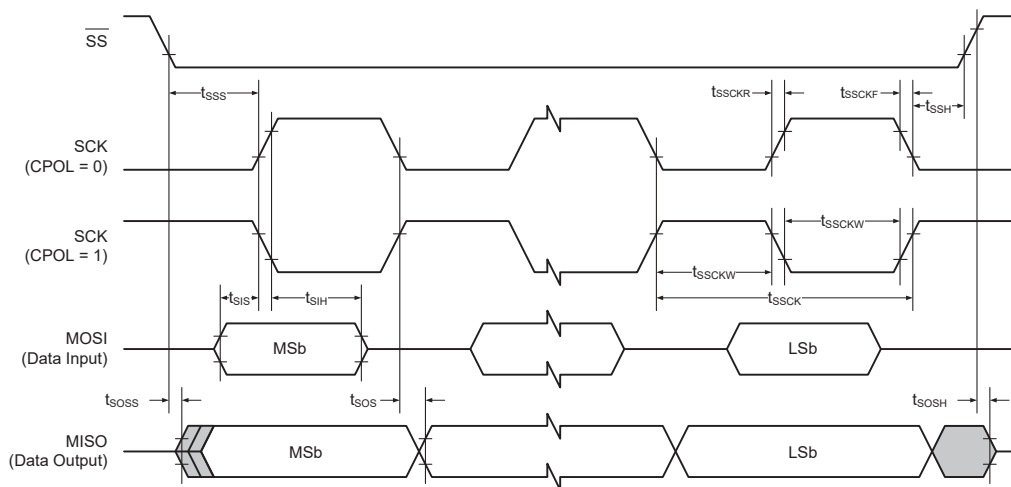


Table 4-18. SPI - Timing Characteristics

| Symbol ⁽¹⁾ | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|---------------------|-----------|------|-----------------|------|------|
| f_{SCK} | SCK clock frequency | Master | - | - | 10 | MHz |
| t_{SCK} | SCK period | Master | 100 | - | - | ns |
| t_{SCKW} | SCK high/low width | Master | - | $0.5 \cdot SCK$ | - | ns |
| t_{SCKR} | SCK rise time | Master | - | 2.7 | - | ns |
| t_{SCKF} | SCK fall time | Master | - | 2.7 | - | ns |
| t_{MIS} | MISO setup to SCK | Master | - | 10 | - | ns |
| t_{MIH} | MISO hold after SCK | Master | - | 10 | - | ns |
| t_{MOS} | MOSI setup to SCK | Master | - | $0.5 \cdot SCK$ | - | ns |
| t_{MOH} | MOSI hold after SCK | Master | - | 1.0 | - | ns |

.....continued

| Symbol ⁽¹⁾ | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|---------------------------|-----------|----------------------|------|------|------|
| f_{SSCK} | Slave SCK clock frequency | Slave | - | - | 5 | MHz |
| t_{SSCK} | Slave SCK period | Slave | $4 \cdot t_{Clkper}$ | - | - | ns |
| t_{SSCKW} | SCK high/low width | Slave | $2 \cdot t_{Clkper}$ | - | - | ns |
| t_{SSCKR} | SCK rise time | Slave | - | - | 1600 | ns |
| t_{SSCKF} | SCK fall time | Slave | - | - | 1600 | ns |
| t_{SIS} | MOSI setup to SCK | Slave | 3.0 | - | - | ns |
| t_{SIH} | MOSI hold after SCK | Slave | t_{Clkper} | - | - | ns |
| t_{SSS} | SS setup to SCK | Slave | 21 | - | - | ns |
| t_{SSH} | SS hold after SCK | Slave | 20 | - | - | ns |
| t_{SOS} | MISO setup to SCK | Slave | - | 8.0 | - | ns |
| t_{SOH} | MISO hold after SCK | Slave | - | 13 | - | ns |
| t_{SOSS} | MISO setup after SS low | Slave | - | 11 | - | ns |
| t_{SOSH} | MISO hold after SS low | Slave | - | 8.0 | - | ns |

Note:

1. These parameters are for design guidance only and are not production tested.

4.13 TWI

Figure 4-6. TWI - Timing Requirements



Table 4-19. TWI - Timing Characteristics

| Symbol ⁽¹⁾ | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------|---------------------|------|---------------------|------|
| f_{SCL} | SCL clock frequency | Max. frequency requires system clock at 10 MHz, which, in turn, requires $V_{DD}=[2.7, 5.5]V$ and $T=[-40, 105]^{\circ}C$ | 0 | - | 1000 | kHz |
| V_{IH} | Input high voltage | | $0.7 \times V_{DD}$ | - | - | V |
| V_{IL} | Input low voltage | | - | - | $0.3 \times V_{DD}$ | V |

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|continued | | | | | | | |
|-----------------------|----------------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------|-----------------------|------------------------------------|------|----|
| Symbol ⁽¹⁾ | Description | Condition | Min. | Typ. | Max. | Unit | |
| V _{HYS} | Hysteresis of Schmitt trigger inputs | | 0.1×V _{DD} | | 0.4×V _{DD} | V | |
| V _{OL} | Output low voltage | I _{load} =20 mA, Fast mode+ | - | - | 0.2×V _{DD} | V | |
| | | I _{load} =3 mA, Normal mode, V _{DD} >2V | - | - | 0.4V | | |
| | | I _{load} =3 mA, Normal mode, V _{DD} ≤2V | - | - | 0.2×V _{DD} | | |
| I _{OL} | Low-level output current | f _{SCL} ≤400 kHz, V _{OL} =0.4V | 3 | - | - | mA | |
| | | f _{SCL} ≤1 MHz, V _{OL} =0.4V | 20 | - | - | | |
| C _B | Capacitive load for each bus line | f _{SCL} ≤100 kHz | - | - | 400 | pF | |
| | | f _{SCL} ≤400 kHz | - | - | 400 | | |
| | | f _{SCL} ≤1 MHz | - | - | 550 | | |
| t _R | Rise time for both SDA and SCL | f _{SCL} ≤100 kHz | - | - | 1000 | ns | |
| | | f _{SCL} ≤400 kHz | 20 | - | 300 | | |
| | | f _{SCL} ≤1 MHz | - | - | 120 | | |
| t _{OF} | Output fall time from V _{IHmin} to V _{ILmax} | 10 pF < capacitance of bus line < 400 pF | f _{SCL} ≤400 kHz | 20+0.1×C _B | - | 300 | ns |
| | | | f _{SCL} ≤1 MHz | 20+0.1×C _B | - | 120 | |
| t _{SP} | Spikes suppressed by the input filter | | 0 | - | 50 | ns | |
| I _L | Input current for each I/O pin | 0.1×V _{DD} <V _I <0.9×V _{DD} | - | - | 1 | μA | |
| C _I | Capacitance for each I/O pin | | - | - | 10 | pF | |
| R _P | Value of pull-up resistor | f _{SCL} ≤100 kHz | (V _{DD} -V _{OL(max)}) / I _{OL} | - | 1000 ns / (0.8473×C _B) | Ω | |
| | | f _{SCL} ≤400 kHz | - | - | 300 ns / (0.8473×C _B) | | |
| | | f _{SCL} ≤1 MHz | - | - | 120 ns / (0.8473×C _B) | | |
| t _{HD;STA} | Hold time (repeated) Start condition | f _{SCL} ≤100 kHz | 4.0 | - | - | μs | |
| | | f _{SCL} ≤400 kHz | 0.6 | - | - | | |
| | | f _{SCL} ≤1 MHz | 0.26 | - | - | | |

|continued | | | | | | |
|-----------------------|--------------------------------------------------|----------------------------|------|------|------|------|
| Symbol ⁽¹⁾ | Description | Condition | Min. | Typ. | Max. | Unit |
| t _{LOW} | Low period of SCL Clock | f _{SCL} ≤ 100 kHz | 4.7 | - | - | μs |
| | | f _{SCL} ≤ 400 kHz | 1.3 | - | - | |
| | | f _{SCL} ≤ 1 MHz | 0.5 | - | - | |
| t _{HIGH} | High period of SCL Clock | f _{SCL} ≤ 100 kHz | 4.0 | - | - | μs |
| | | f _{SCL} ≤ 400 kHz | 0.6 | - | - | |
| | | f _{SCL} ≤ 1 MHz | 0.26 | - | - | |
| t _{SU;STA} | Setup time for a repeated Start condition | f _{SCL} ≤ 100 kHz | 4.7 | - | - | μs |
| | | f _{SCL} ≤ 400 kHz | 0.6 | - | - | |
| | | f _{SCL} ≤ 1 MHz | 0.26 | - | - | |
| t _{HD;DAT} | Data hold time | f _{SCL} ≤ 100 kHz | 0 | - | 3.45 | μs |
| | | f _{SCL} ≤ 400 kHz | 0 | - | 0.9 | |
| | | f _{SCL} ≤ 1 MHz | 0 | - | 0.45 | |
| t _{SU;DAT} | Data setup time | f _{SCL} ≤ 100 kHz | 250 | - | - | ns |
| | | f _{SCL} ≤ 400 kHz | 100 | - | - | |
| | | f _{SCL} ≤ 1 MHz | 50 | - | - | |
| t _{SU;STO} | Setup time for Stop condition | f _{SCL} ≤ 100 kHz | 4 | - | - | μs |
| | | f _{SCL} ≤ 400 kHz | 0.6 | - | - | |
| | | f _{SCL} ≤ 1 MHz | 0.26 | - | - | |
| t _{BUF} | Bus free time between a Stop and Start condition | f _{SCL} ≤ 100 kHz | 4.7 | - | - | μs |
| | | f _{SCL} ≤ 400 kHz | 1.3 | - | - | |
| | | f _{SCL} ≤ 1 MHz | 0.5 | - | - | |

Note:

1. These parameters are for design guidance only and are not production tested.

4.14 VREF

Table 4-20. Internal Voltage Reference Characteristics

| Symbol ⁽¹⁾ | Description | Min. | Typ. | Max. | Unit |
|-----------------------|---------------|------|------|------|------|
| t _{start} | Start-up time | - | 25 | - | μs |

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Electrical Characteristics

.....continued

| Symbol ⁽¹⁾ | Description | Min. | Typ. | Max. | Unit |
|-----------------------|-------------------------------------|------|------|------|------|
| V _{DD} | Power supply voltage range for 0V55 | 1.8 | - | 5.5 | V |
| | Power supply voltage range for 1V1 | 1.8 | - | 5.5 | |
| | Power supply voltage range for 1V5 | 1.8 | - | 5.5 | |
| | Power supply voltage range for 2V5 | 3.0 | - | 5.5 | |
| | Power supply voltage range for 4V3 | 4.8 | - | 5.5 | |

Note:

1. These parameters are for design guidance only and are not production tested.

Table 4-21. ADC Internal Voltage Reference Characteristics⁽¹⁾

| Symbol ⁽²⁾ | Description | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|----------------------------|--------------------------------------------------|------|------|------|------|
| 1V1 | Internal reference voltage | V _{DD} =[1.8V, 5.5V] T=[0 - 105]°C | -2.0 | | 2.0 | % |
| 0V55 1V5 2V5 4V3 | Internal reference voltage | V _{DD} =[1.8V, 5.5V] T=[0 - 105]°C | -3.0 | | 3.0 | |
| 0V55 1V1 1V5 2V5 4V3 | Internal reference voltage | V _{DD} =[1.8V, 5.5V] T=[-40 - 125]°C | -5.0 | | 5.0 | |

Note:

1. These values are based on characterization and not covered by production test limits.
2. The symbols xxxx refer to the respective values of the ADC0REFSEL bit field in the VREF.CTRLA register.

Table 4-22. AC Internal Voltage Reference Characteristics⁽¹⁾

| Symbol ⁽²⁾ | Description | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|----------------------------|--------------------------------------------------|------|------|------|------|
| 0V55 1V1 1V5 2V5 | Internal reference voltage | V _{DD} =[1.8V, 5.5V] T=[0 - 105]°C | -3.0 | | 3.0 | % |
| 0V55 1V1 1V5 2V5 4V3 | Internal reference voltage | V _{DD} =[1.8V, 5.5V] T=[-40 - 125]°C | -5.0 | | 5.0 | |

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Note:

1. These values are based on characterization and not covered by production test limits.
2. The symbols xxxx refer to the respective values of the AC0REFSEL bit field in the VREF.CTRLA register.

4.15 ADC

4.15.1 Internal Reference Characteristics

Operating conditions:

- $V_{DD} = 1.8$ to $5.5V$
- Temperature = $-40^{\circ}C$ to $125^{\circ}C$
- DUTYCYC = 25%
- $CLK_{ADC} = 13 * f_{ADC}$
- SAMPCAP is 10 pF for 0.55V reference, while it is set to 5 pF for $V_{REF} \geq 1.1V$
- Applies for all allowed combinations of V_{REF} selections and Sample Rates unless otherwise noted

Table 4-23. Power Supply, Reference, and Input Range

| Symbol | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------|---------------------|-----------------------------|------|------|--------------|------|
| V_{DD} | Supply voltage | $CLK_{ADC} \leq 1.5$ MHz | 1.8 | - | 5.5 | V |
| | | $CLK_{ADC} > 1.5$ MHz | 2.7 | - | 5.5 | |
| V_{REF} | Reference voltage | REFSEL = Internal reference | 0.55 | - | $V_{DD}-0.5$ | V |
| | | REFSEL = External reference | 1.1 | - | V_{DD} | |
| | | REFSEL = V_{DD} | 1.8 | - | 5.5 | |
| C_{IN} | Input capacitance | SAMPCAP=5 pF | - | 5 | - | pF |
| | | SAMPCAP=10 pF | - | 10 | - | |
| V_{IN} | Input voltage range | | 0 | - | V_{REF} | V |
| I_{BAND} | Input bandwidth | $1.1V \leq V_{REF}$ | - | - | 57.5 | kHz |

Table 4-24. Clock and Timing Characteristics⁽¹⁾

| Symbol | Description | Conditions | Min. | Typ. | Max. | Unit |
|-------------|---------------------------|----------------------------------------|------|------|------|--------------------|
| f_{ADC} | Sample rate | $1.1V \leq V_{REF}$ | 15 | - | 115 | ksps |
| | | $1.1V \leq V_{REF}$ (8-bit resolution) | 15 | - | 150 | |
| | | $V_{REF}=0.55V$ (10 bits) | 7.5 | - | 20 | |
| CLK_{ADC} | Clock frequency | $V_{REF}=0.55V$ (10 bits) | 100 | - | 260 | kHz |
| | | $1.1V \leq V_{REF}$ (10 bits) | 200 | - | 1500 | |
| | | $1.1V \leq V_{REF}$ (8-bit resolution) | 200 | - | 2000 | |
| T_s | Sampling time | | 2 | 2 | 33 | CLK_{ADC} cycles |
| T_{CONV} | Conversion time (latency) | Sampling time = $2 CLK_{ADC}$ | 8.7 | - | 50 | μs |

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Electrical Characteristics

.....continued

| Symbol | Description | Conditions | Min. | Typ. | Max. | Unit |
|--------------------|---------------|---------------------------|------|------|------|------|
| T _{START} | Start-up time | Internal V _{REF} | - | 22 | - | μs |

Note:

1. These parameters are for design guidance only and are not production tested.

Table 4-25. Accuracy Characteristics Internal Reference⁽²⁾

| Symbol | Description | Conditions | Min. | Typ. | Max. | Unit | |
|--------------------|----------------------------|-----------------------------------------------------|----------------------------|------|------|------|-----|
| Res | Resolution | | - | 10 | - | bit | |
| INL | Integral Non-linearity | REFSEL = INTERNAL V _{REF} =0.55V | f _{ADC} =7.7 ksps | - | 1.0 | - | LSB |
| | | REFSEL = INTERNAL or VDD | f _{ADC} =15 ksps | - | 1.0 | - | |
| | | REFSEL = INTERNAL or VDD 1.1V ≤ V _{REF} | f _{ADC} =77 ksps | - | 1.0 | - | |
| | | | f _{ADC} =115 ksps | - | 1.2 | - | |
| DNL ⁽¹⁾ | Differential Non-linearity | REFSEL = INTERNAL V _{REF} = 0.55V | f _{ADC} =7.7 ksps | - | 0.6 | - | LSB |
| | | REFSEL = INTERNAL V _{REF} = 1.1V | f _{ADC} =15 ksps | - | 0.4 | - | |
| | | REFSEL = INTERNAL or VDD 1.5V ≤ V _{REF} | f _{ADC} =15 ksps | - | 0.4 | - | |
| | | REFSEL = INTERNAL or VDD 1.1V ≤ V _{REF} | f _{ADC} =77 ksps | - | 0.4 | - | |
| | | REFSEL = INTERNAL 1.1V ≤ V _{REF} | f _{ADC} =115 ksps | - | 0.5 | - | |
| | | REFSEL = VDD 1.8V ≤ V _{REF} | f _{ADC} =115 ksps | - | 0.9 | - | |

|continued | | | | | | | |
|----------------|-------------------|--------------------------|-------------------------------|------|------|------|-----|
| Symbol | Description | Conditions | Min. | Typ. | Max. | Unit | |
| EABS | Absolute accuracy | REFSEL = INTERNAL | T=[0-105]°C | - | <10 | - | LSB |
| | | V _{REF} = 1.1V | V _{DD} = [1.8V-3.6V] | | | | |
| | | | V _{DD} = [1.8V-3.6V] | - | <15 | - | |
| | | REFSEL = V _{DD} | | - | 2.5 | - | |
| | REFSEL = INTERNAL | | - | <35 | - | | |
| EGAIN | Gain error | REFSEL = INTERNAL | T=[0-105]°C | - | ±15 | - | LSB |
| | | V _{REF} = 1.1V | V _{DD} = [1.8V-3.6V] | | | | |
| | | | V _{DD} = [1.8V-3.6V] | - | ±20 | - | |
| | | REFSEL = V _{DD} | | - | 2 | - | |
| | REFSEL = INTERNAL | | - | ±35 | - | | |
| EOFF | Offset error | REFSEL = INTERNAL | | - | -1 | - | LSB |
| | | V _{REF} = 0.55V | | | | | |
| | | REFSEL = INTERNAL | | - | -0.5 | - | LSB |
| | | 1.1V ≤ V _{REF} | | | | | |

Note:

1. A DNL error of less than or equal to 1 LSB ensures a monotonic transfer function with no missing codes.
2. These parameters are for design guidance only and are not production tested.
3. Reference setting and f_{ADC} must fulfill the specification in “Clock and Timing Characteristics” and “Power supply, Reference, and Input Range” tables.

4.15.2 External Reference Characteristics

Operating conditions:

- V_{DD} = 1.8 to 5.5V
- Temperature = -40°C to 125°C
- DUTYCYC = 25%
- CLK_{ADC} = 13 * f_{ADC}
- SAMPCAP is 5 pF

The accuracy characteristics numbers are based on the characterization of the following input reference levels and V_{DD} ranges:

- V_{ref} = 1.8V, V_{DD} = 1.8 to 5.5V
- V_{ref} = 2.6V, V_{DD} = 2.7 to 5.5V
- V_{ref} = 4.096V, V_{DD} = 4.5 to 5.5V

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Electrical Characteristics

- $V_{ref} = 4.3V$, $V_{DD} = 4.5$ to $5.5V$

Table 4-26. ADC Accuracy Characteristics External Reference⁽²⁾

| Symbol | Description | Conditions | Min. | Typ. | Max. | Unit |
|--------------------|----------------------------|--------------------|------|------|------|------|
| Res | Resolution | | - | 10 | - | bit |
| INL | Integral Non-linearity | $f_{ADC}=15$ ksps | - | 0.9 | - | LSB |
| | | $f_{ADC}=77$ ksps | - | 0.9 | - | |
| | | $f_{ADC}=115$ ksps | - | 1.2 | - | |
| DNL ⁽¹⁾ | Differential Non-linearity | $f_{ADC}=15$ ksps | - | 0.2 | - | LSB |
| | | $f_{ADC}=77$ ksps | - | 0.4 | - | |
| | | $f_{ADC}=115$ ksps | - | 0.8 | - | |
| EABS | Absolute accuracy | $f_{ADC}=15$ ksps | - | 2 | - | LSB |
| | | $f_{ADC}=77$ ksps | - | 2 | - | |
| | | $f_{ADC}=115$ ksps | - | 2 | - | |
| EGAIN | Gain error | $f_{ADC}=15$ ksps | - | 2 | - | LSB |
| | | $f_{ADC}=77$ ksps | - | 2 | - | |
| | | $f_{ADC}=115$ ksps | - | 2 | - | |
| E0FF | Offset error | | - | -0.5 | - | LSB |

Note:

1. A DNL error of less than or equal to 1 LSB ensures a monotonic transfer function with no missing codes.
2. These parameters are for design guidance only and are not production tested.

4.16 AC

Table 4-27. Analog Comparator Characteristics, Low-Power Mode Disabled

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|-------------|-----------------------|-----------------------------------|------|----------|----------|---------|
| V_{IN} | Input voltage | | -0.2 | - | V_{DD} | V |
| C_{IN} | Input pin capacitance | PD1 to PD6 | - | 3.5 | - | pF |
| | | PD7 | - | 14 | - | |
| V_{OFF} | Input offset voltage | $0.7V < V_{IN} < (V_{DD} - 0.7V)$ | -20 | ± 5 | +20 | mV |
| | | $V_{IN} = [-0.2V, V_{DD}]$ | -40 | ± 20 | +40 | |
| I_L | Input leakage current | | - | 5 | - | nA |
| T_{START} | Start-up time | | - | 1.3 | - | μs |

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Electrical Characteristics

.....continued

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|------------------|-------------------|----------------------------------------|------|------|------|------|
| V _{HYS} | Hysteresis | HYSMODE=0x0 | - | 0 | - | mV |
| | | HYSMODE=0x1 | - | 10 | - | |
| | | HYSMODE=0x2 | - | 25 | - | |
| | | HYSMODE=0x3 | - | 50 | - | |
| t _{PD} | Propagation delay | 25 mV Overdrive, V _{DD} ≥2.7V | - | 50 | - | ns |

Table 4-28. Analog Comparator Characteristics, Low-Power Mode Enabled

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|--------------------|-----------------------|--------------------------------------------------|------|------|-----------------|------|
| V _{IN} | Input voltage | | -0.2 | - | V _{DD} | V |
| C _{IN} | Input pin capacitance | PD1 to PD6 | - | 3.5 | - | pF |
| | | PD7 | - | 14 | - | |
| V _{OFF} | Input offset voltage | 0.7V < V _{IN} < (V _{DD} -0.7V) | -30 | ±10 | +30 | mV |
| | | V _{IN} =[0V, V _{DD}] | -50 | ±30 | +50 | |
| I _L | Input leakage current | | - | 5 | - | nA |
| T _{START} | Start-up time | | - | 1.3 | - | µs |
| V _{HYS} | Hysteresis | HYSMODE=0x0 | - | 0 | - | mV |
| | | HYSMODE=0x1 | - | 10 | - | |
| | | HYSMODE=0x2 | - | 25 | - | |
| | | HYSMODE=0x3 | - | 50 | - | |
| t _{PD} | Propagation delay | 25 mV overdrive, V _{DD} ≥2.7V | - | 150 | - | ns |

4.17 UPDI Timing

UPDI Enable Sequence ⁽¹⁾

| Symbol | Description | Min. | Max. | Unit |
|-------------------|--------------------------------------|------|-------|------|
| T _{RES} | Duration of Handshake/Break on RESET | 10 | 200 | µs |
| T _{UPDI} | Duration of UPDI.txd=0 | 10 | 200 | µs |
| T _{Deb0} | Duration of Debugger.txd=0 | 0.2 | 1 | µs |
| T _{DebZ} | Duration of Debugger.txd=z | 200 | 14000 | µs |

Note:

1. These parameters are for design guidance only and are not production tested.

4.18 Programming Time

See the table below for typical programming times for Flash and EEPROM.

Table 4-29. Programming Times

| Symbol | Typical Programming Time |
|-------------------|--------------------------|
| Page Buffer Clear | 7 CLK_CPU cycles |
| Page Write | 2 ms |
| Page Erase | 2 ms |
| Page Erase-Write | 4 ms |
| Chip Erase | 4 ms |
| EEPROM Erase | 4 ms |

5. Typical Characteristics

5.1 Power Consumption

5.1.1 Supply Currents in Active Mode

Figure 5-1. Active Supply Current vs. Frequency (1-20 MHz) at T=25°C

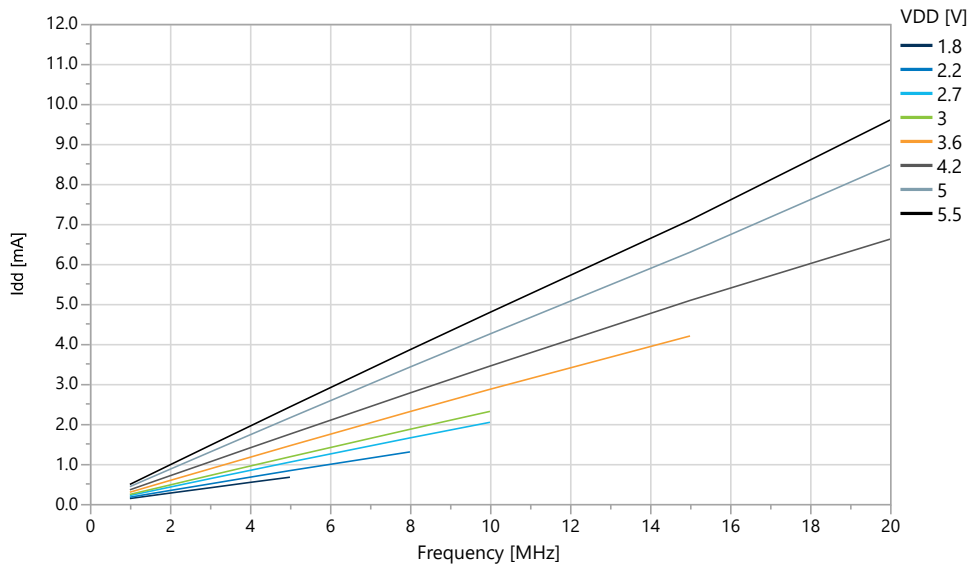


Figure 5-2. Active Supply Current vs. Frequency [0.1, 1.0] MHz at T=25°C



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Typical Characteristics

Figure 5-3. Active Supply Current vs. Temperature (f=20 MHz OSC20M)



Figure 5-4. Active Supply Current vs. V_{DD} (f=[1.25, 20] MHz OSC20M) at T=25°C

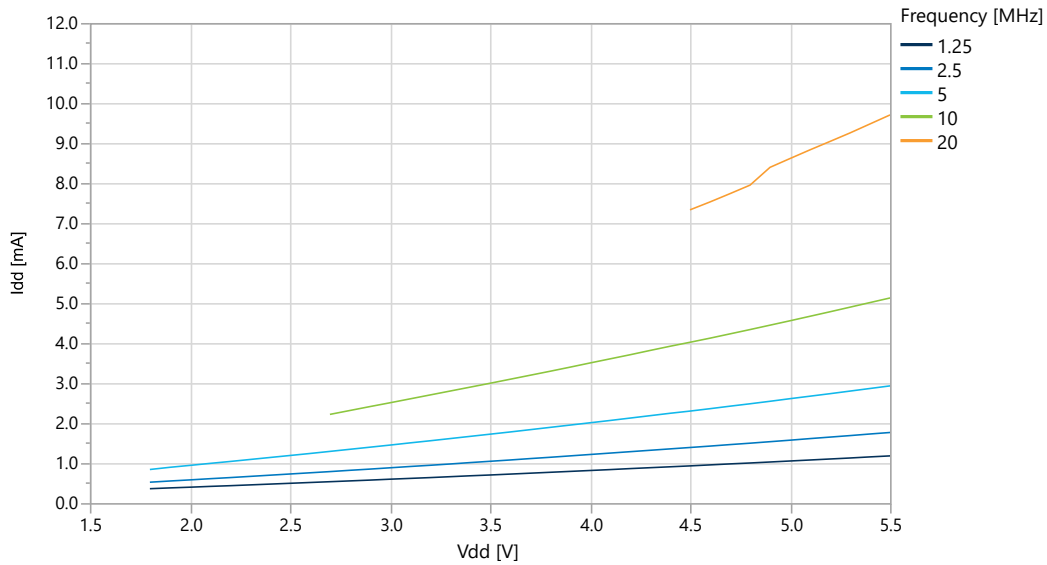


Figure 5-5. Active Supply Current vs. V_{DD} (f=32.768 kHz OSCULP32K)



5.1.2 Supply Currents in Idle Mode

Figure 5-6. Idle Supply Current vs. Frequency (1-20 MHz) at T=25 $^{\circ}C$



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Typical Characteristics

Figure 5-7. Idle Supply Current vs. Low Frequency (0.1-1.0 MHz) at T=25°C



Figure 5-8. Idle Supply Current vs. Temperature (f=20 MHz OSC20M)

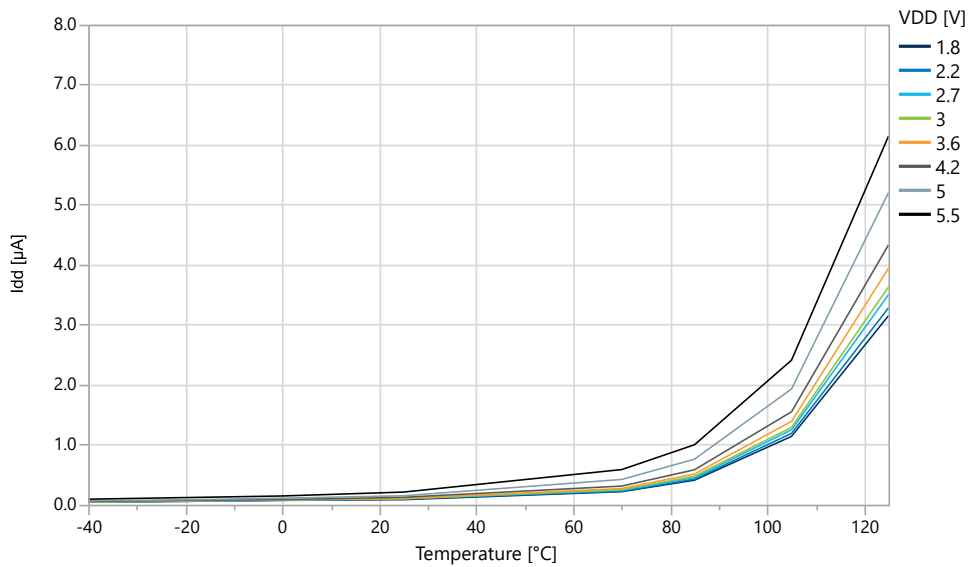


Figure 5-9. Idle Supply Current vs. V_{DD} (f=32.768 kHz OSCULP32K)



5.1.3 Supply Currents in Power-Down Mode

Figure 5-10. Power-Down Mode Supply Current vs. Temperature (all functions disabled)



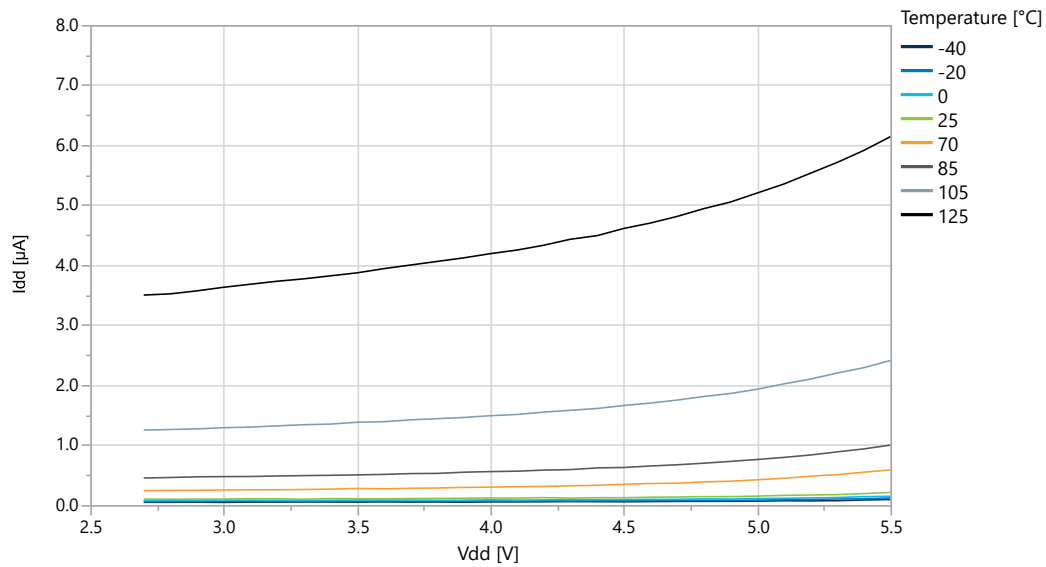
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Typical Characteristics

Figure 5-11. Power-Down Mode Supply Current vs. V_{DD} (all functions disabled)



Figure 5-12. Power-Down Mode Supply Current vs. V_{DD} (all functions disabled)



5.1.4 Supply Currents in Standby Mode

Figure 5-13. Standby Mode Supply Current vs. V_{DD} (RTC running with internal OSCULP32K)

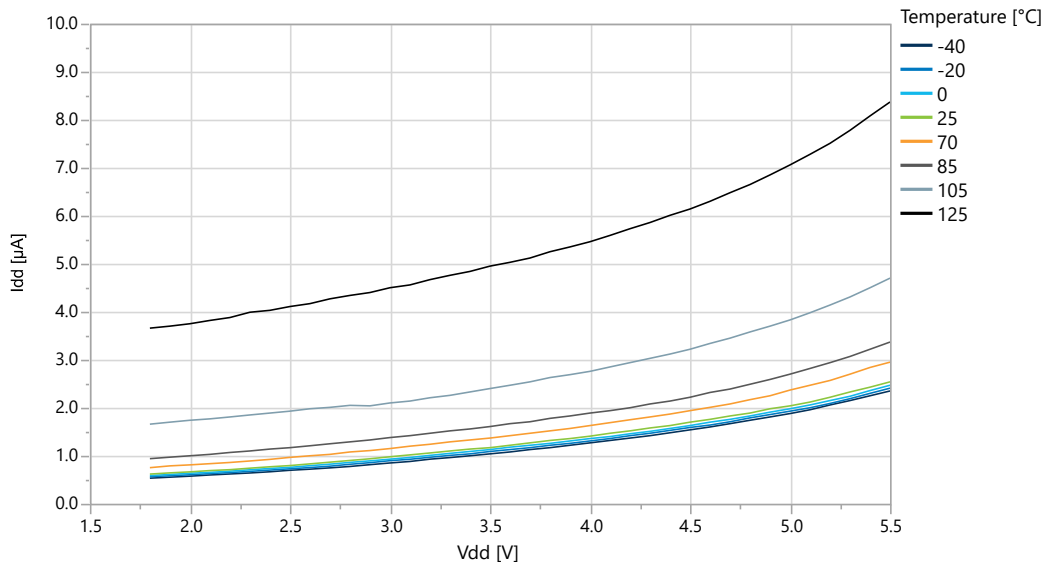


Figure 5-14. Standby Mode Supply Current vs. V_{DD} (Sampled BOD running at 125 Hz)

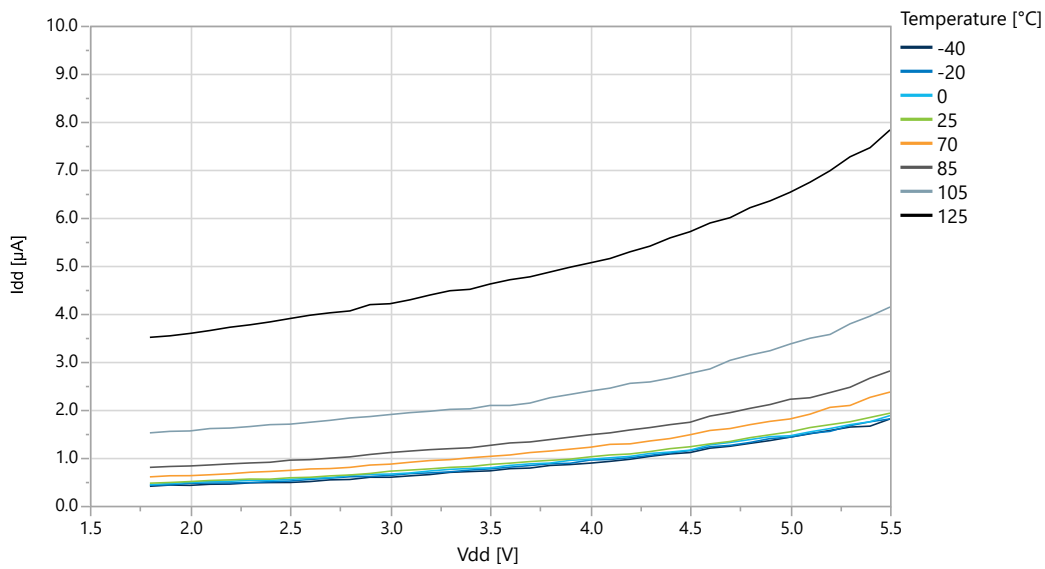


Figure 5-15. Standby Mode Supply Current vs. V_{DD} (Sampled BOD running at 1 kHz)



5.1.5 Power-on Supply Currents

Figure 5-16. Power-on Supply Current vs. V_{DD} (BOD enabled at 4.3V level)



5.2 GPIO

GPIO Input Characteristics

Figure 5-17. I/O Pin Input Hysteresis vs. V_{DD}



Figure 5-18. I/O Pin Input Threshold Voltage vs. V_{DD} ($T=25^{\circ}\text{C}$)



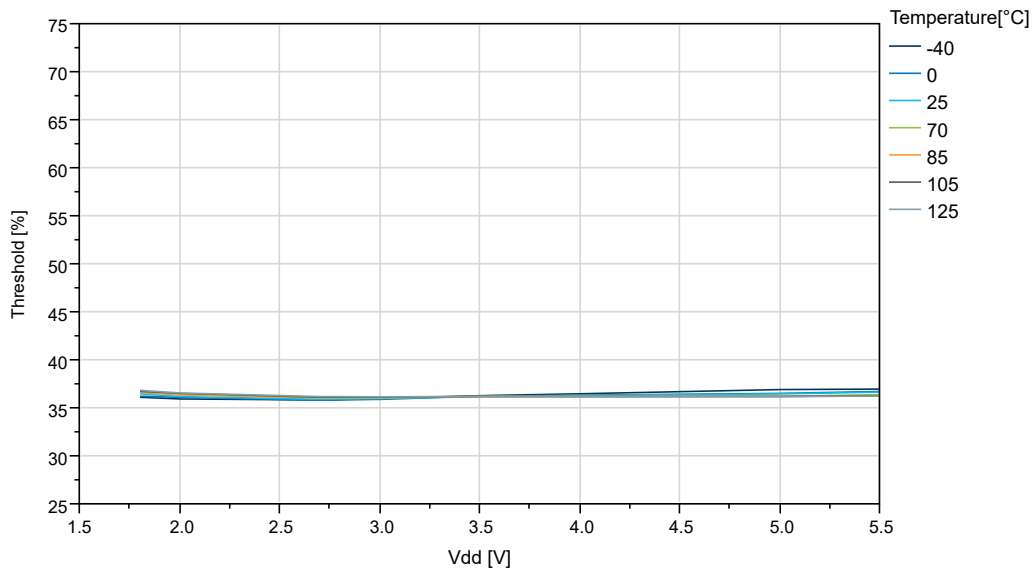
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Typical Characteristics

Figure 5-19. I/O Pin Input Threshold Voltage vs. V_{DD} (V_{IH})



Figure 5-20. I/O Pin Input Threshold Voltage vs. V_{DD} (V_{IL})



GPIO Output Characteristics

Figure 5-21. I/O Pin Output Voltage vs. Sink Current ($V_{DD}=1.8V$)

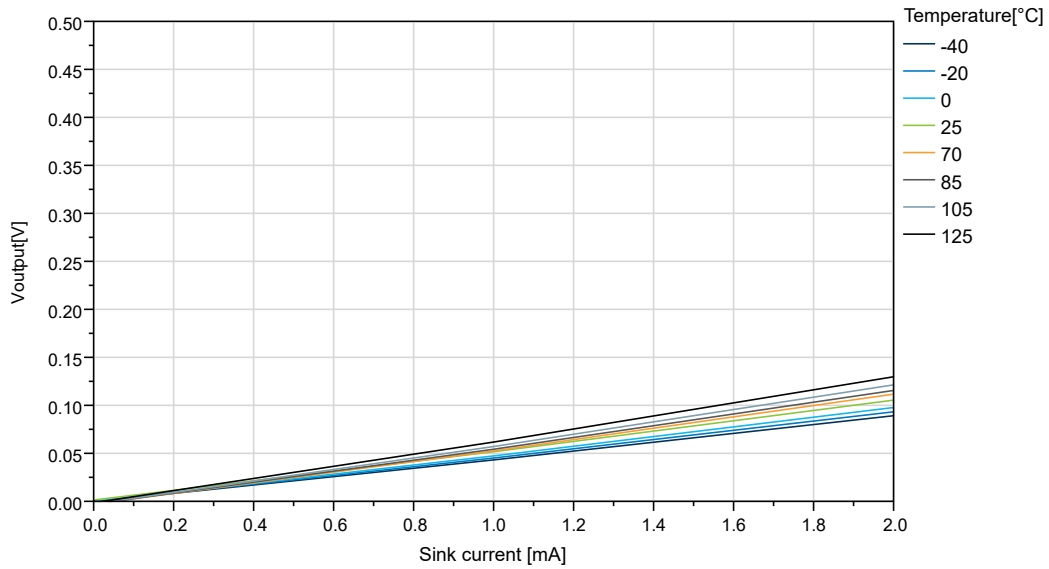
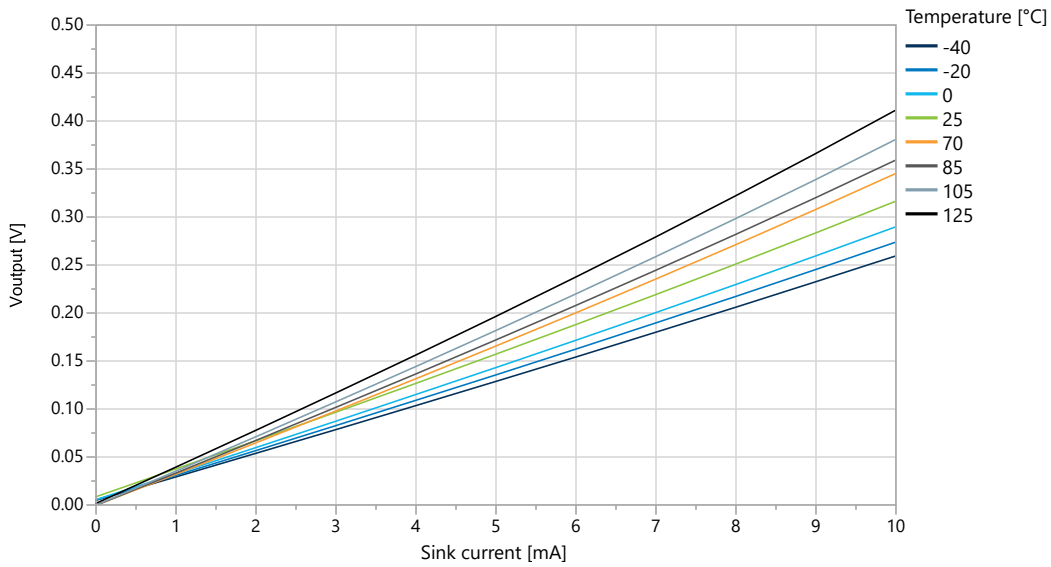


Figure 5-22. I/O Pin Output Voltage vs. Sink Current ($V_{DD}=3.0V$)



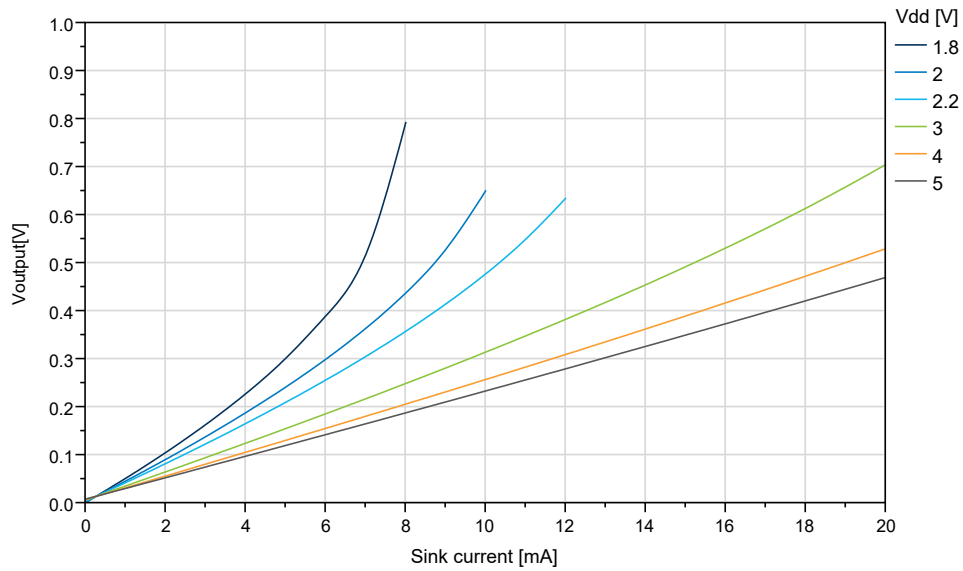
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Typical Characteristics

Figure 5-23. I/O Pin Output Voltage vs. Sink Current ($V_{DD}=5.0V$)



Figure 5-24. I/O Pin Output Voltage vs. Sink Current ($T=25^{\circ}C$)



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Typical Characteristics

Figure 5-25. I/O Pin Output Voltage vs. Source Current ($V_{DD}=1.8V$)



Figure 5-26. I/O Pin Output Voltage vs. Source Current ($V_{DD}=3.0V$)



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Typical Characteristics

Figure 5-27. I/O Pin Output Voltage vs. Source Current ($V_{DD}=5.0V$)



Figure 5-28. I/O Pin Output Voltage vs. Source Current ($T=25^{\circ}C$)



GPIO Pull-Up Characteristics

Figure 5-29. I/O Pin Pull-Up Resistor Current vs. Input Voltage ($V_{DD}=1.8V$)



Figure 5-30. I/O Pin Pull-Up Resistor Current vs. Input Voltage ($V_{DD}=3.0V$)



Figure 5-31. I/O Pin Pull-Up Resistor Current vs. Input Voltage ($V_{DD}=5.0V$)



5.3 VREF Characteristics

Figure 5-32. Internal 0.55V Reference vs. Temperature



Figure 5-33. Internal 1.1V Reference vs. Temperature



Figure 5-34. Internal 2.5V Reference vs. Temperature



Figure 5-35. Internal 4.3V Reference vs. Temperature



5.4 BOD Characteristics

BOD Current vs. V_{DD}

Figure 5-36. BOD Current vs. V_{DD} (Continuous Mode Enabled)



Figure 5-37. BOD Current vs. V_{DD} (Sampled BOD at 125 Hz)

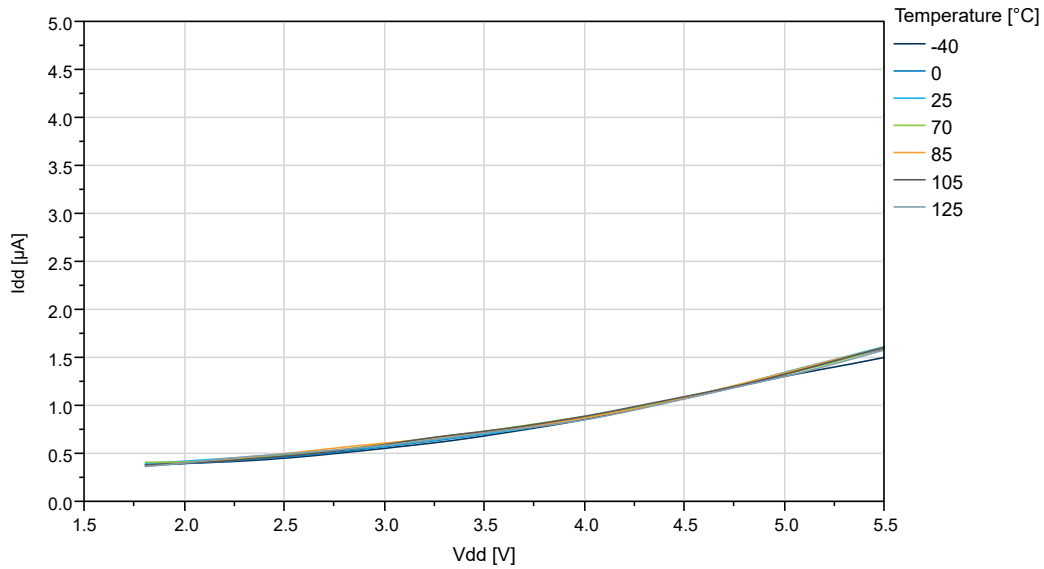


Figure 5-38. BOD Current vs. V_{DD} (Sampled BOD at 1 kHz)



BOD Threshold vs. Temperature

Figure 5-39. BOD Threshold vs. Temperature (Level 1.8V)



Figure 5-40. BOD Threshold vs. Temperature (Level 2.6V)



Figure 5-41. BOD Threshold vs. Temperature (Level 4.3V)



5.5 ADC Characteristics

Figure 5-42. Absolute Accuracy vs. V_{DD} ($f_{ADC}=115$ ksps) at $T=25^{\circ}\text{C}$, REFSEL = Internal Reference



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Typical Characteristics

Figure 5-43. Absolute Accuracy vs. V_{ref} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksp/s), REFSEL = Internal Reference



Figure 5-44. DNL Error vs. V_{DD} ($f_{ADC}=115$ ksp/s) at $T=25^{\circ}C$, REFSEL = Internal Reference



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Typical Characteristics

Figure 5-45. DNL vs. V_{ref} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksp/s), REFSEL = Internal Reference

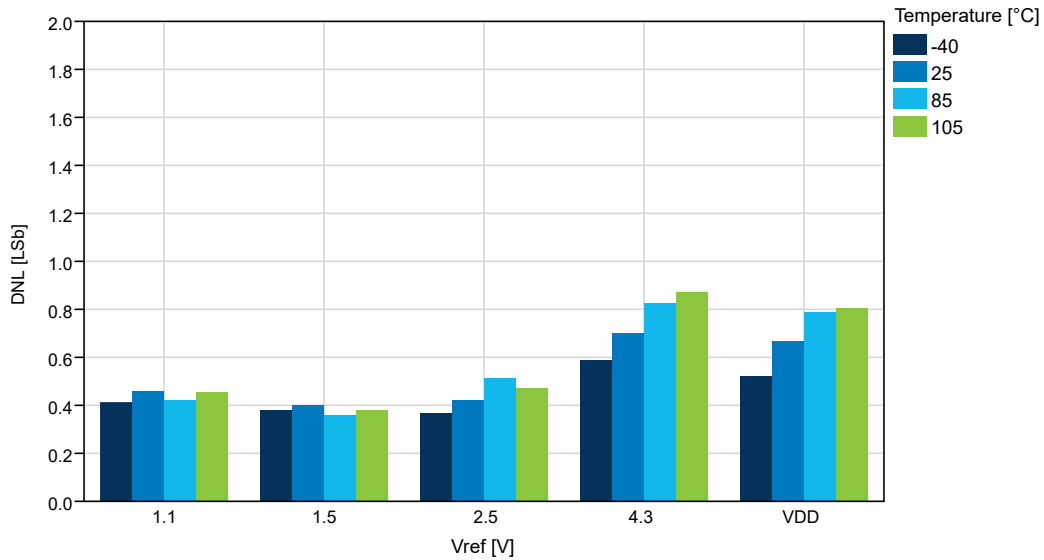


Figure 5-46. Gain Error vs. V_{DD} ($f_{ADC}=115$ ksp/s) at $T=25^{\circ}C$, REFSEL = Internal Reference



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Typical Characteristics

Figure 5-47. Gain Error vs. V_{ref} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksp/s), REFSEL = Internal Reference



Figure 5-48. INL vs. V_{DD} ($f_{ADC}=115$ ksp/s) at $T=25^{\circ}C$, REFSEL = Internal Reference



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Typical Characteristics

Figure 5-49. INL vs. V_{ref} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksp/s), REFSEL = Internal Reference



Figure 5-50. Offset Error vs. V_{DD} ($f_{ADC}=115$ ksp/s) at $T=25^{\circ}C$, REFSEL = Internal Reference



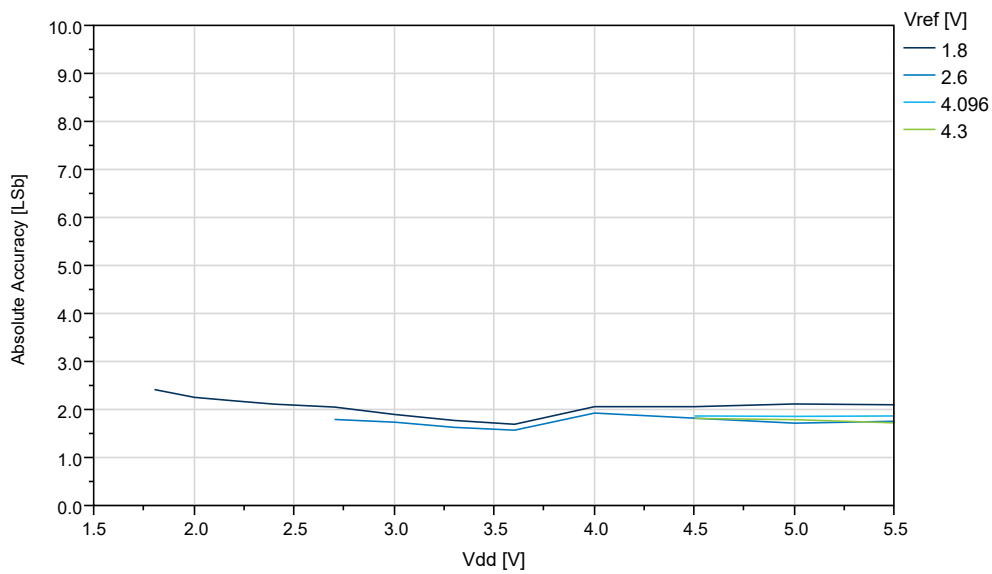
ATmega809/1609/3209/4809 – 48-pin

Typical Characteristics

Figure 5-51. Offset Error vs. V_{ref} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksps), REFSEL = Internal Reference



Figure 5-52. Absolute Accuracy vs. V_{DD} ($f_{ADC}=115$ ksps, $T=25^{\circ}C$), REFSEL = External Reference



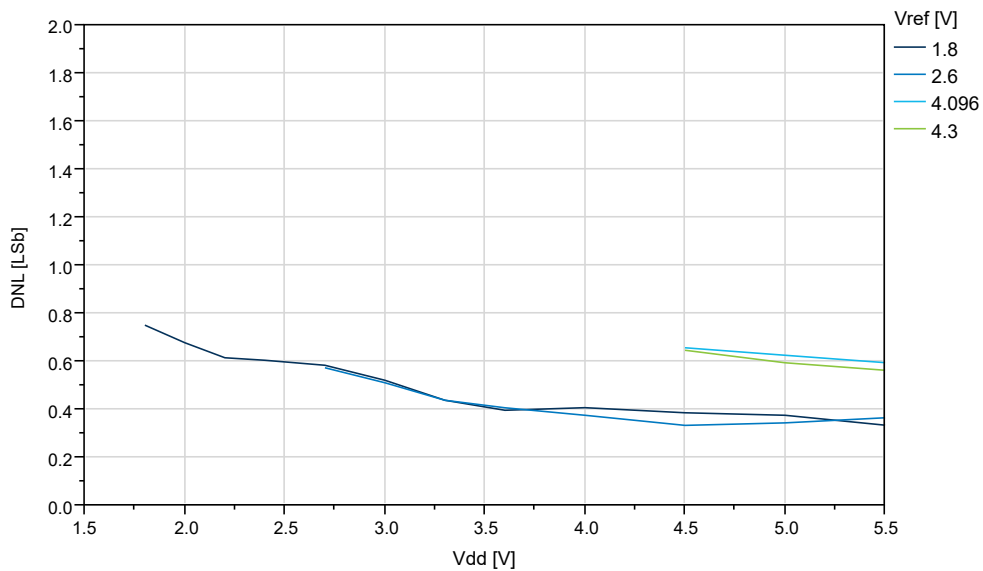
ATmega809/1609/3209/4809 – 48-pin

Typical Characteristics

Figure 5-53. Absolute Accuracy vs. V_{REF} ($V_{DD}=5.0V$, $f_{ADC}=115$ kps, REFSEL = External Reference)



Figure 5-54. DNL vs. V_{DD} ($f_{ADC}=115$ kps, $T=25^{\circ}C$, REFSEL = External Reference)



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Typical Characteristics

Figure 5-55. DNL vs. V_{REF} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksp/s, REFSEL = External Reference)



Figure 5-56. Gain vs. V_{DD} ($f_{ADC}=115$ ksp/s, $T=25^{\circ}C$, REFSEL = External Reference)



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Typical Characteristics

Figure 5-57. Gain vs. V_{REF} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksp/s, REFSEL = External Reference)



Figure 5-58. INL vs. V_{DD} ($f_{ADC}=115$ ksp/s, $T=25^{\circ}C$, REFSEL = External Reference)

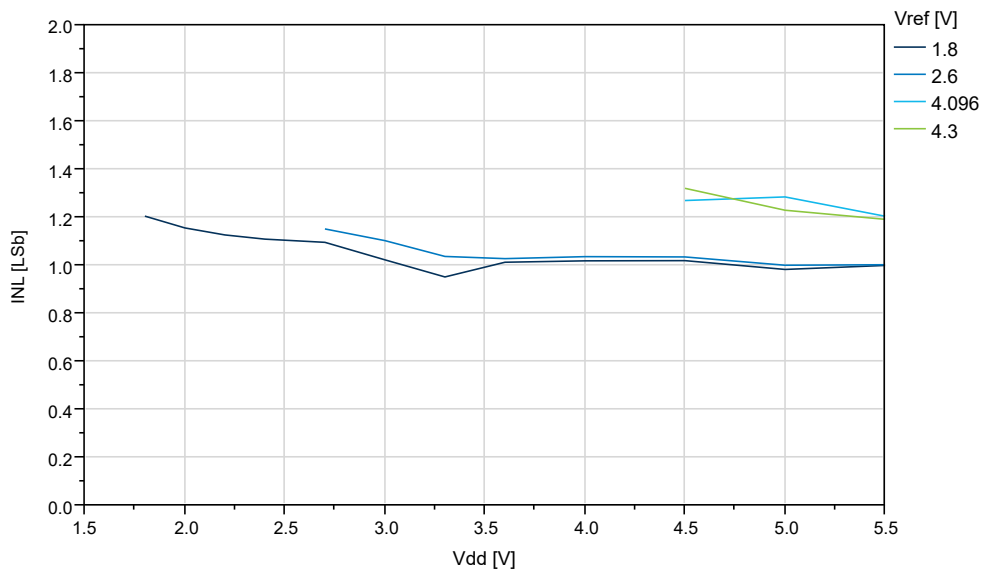


Figure 5-59. INL vs. V_{REF} ($V_{DD}=5.0V$, $f_{ADC}=115$ kps, REFSEL = External Reference)



Figure 5-60. Offset vs. V_{DD} ($f_{ADC}=115$ kps, $T=25^{\circ}C$, REFSEL = External Reference)

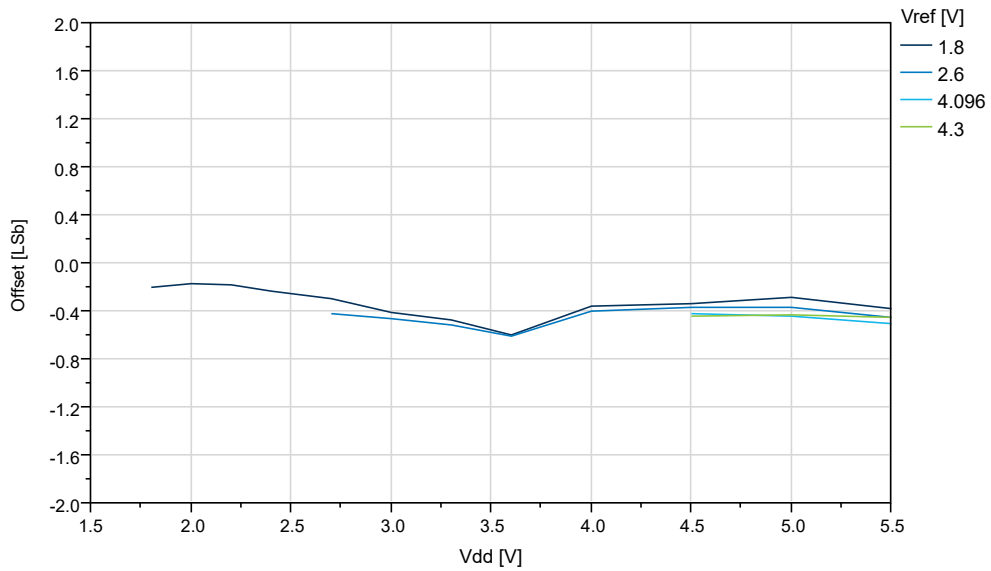
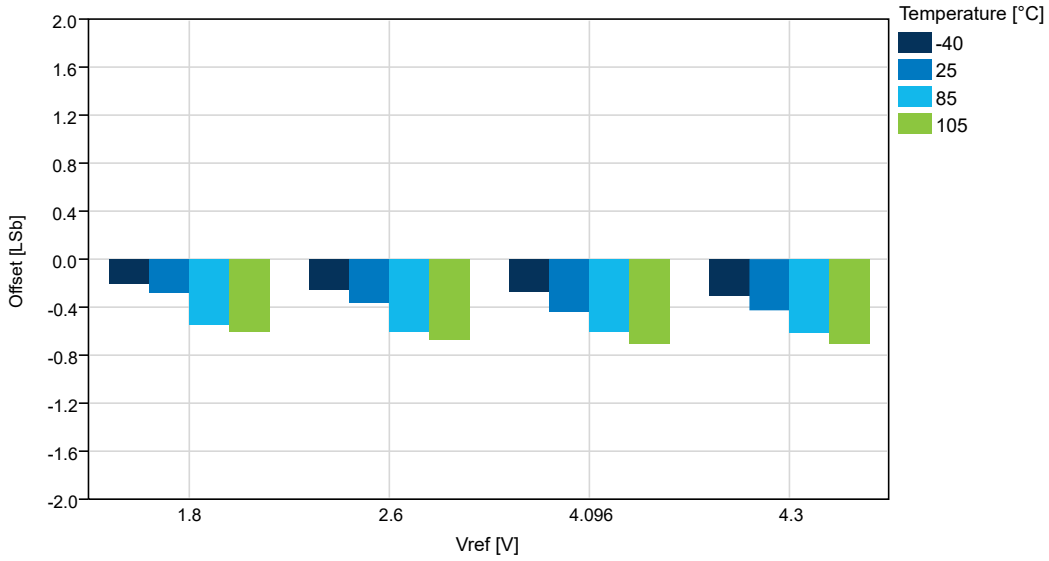


Figure 5-61. Offset vs. V_{REF} ($V_{DD}=5.0V$, $f_{ADC}=115$ ksp/s, REFSEL = External Reference)



5.6 AC Characteristics

Figure 5-62. Hysteresis vs. V_{CM} - 10 mV ($V_{DD}=5V$)

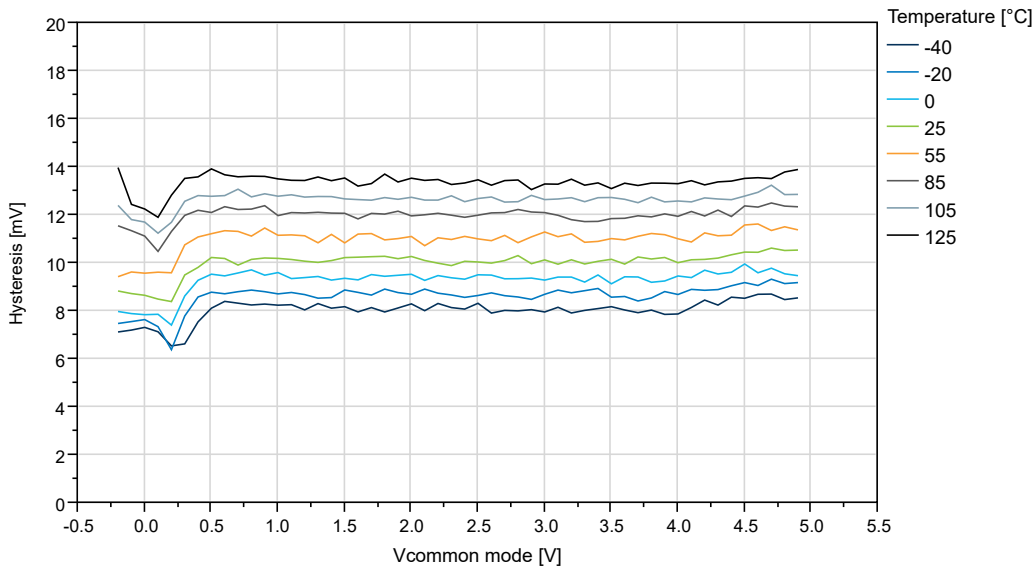


Figure 5-63. Hysteresis vs. V_{CM} - 10 mV to 50 mV ($V_{DD}=5V$, $T=25^{\circ}C$)

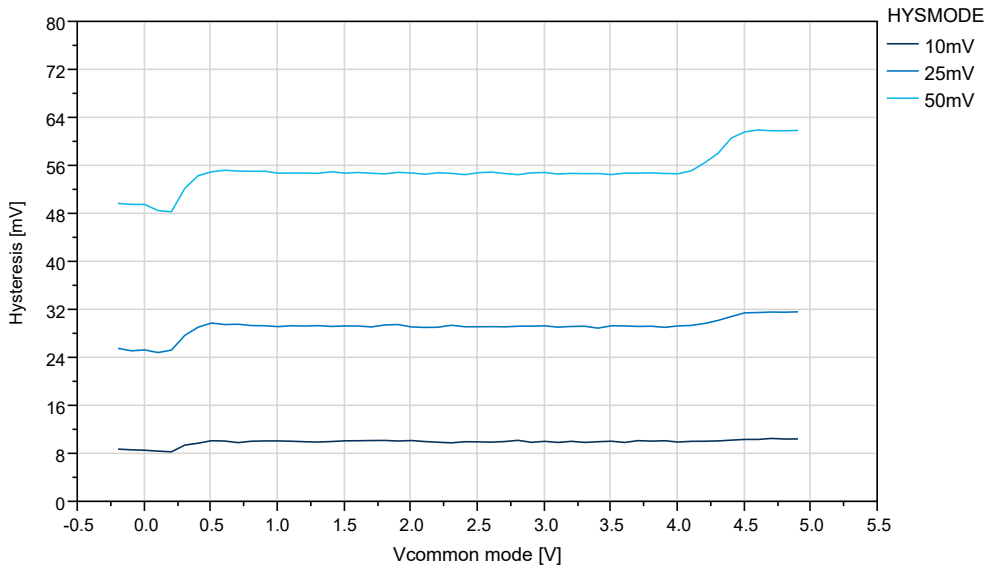


Figure 5-64. Offset vs. V_{CM} - 10 mV ($V_{DD}=5V$)

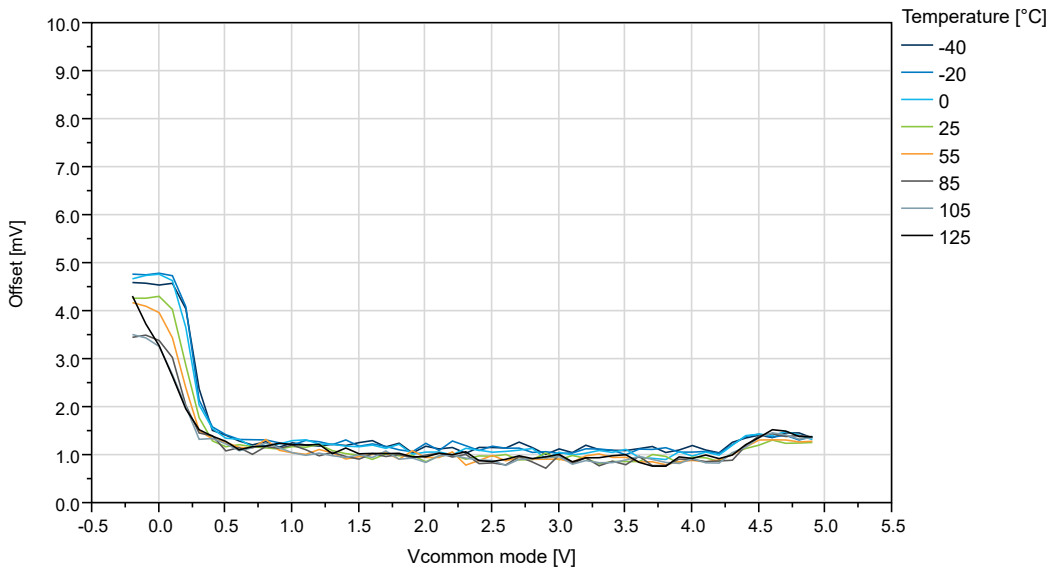


Figure 5-65. Offset vs. V_{CM} - 10 mV to 50 mV ($V_{DD}=5V$, $T=25^{\circ}C$)



5.7 OSC20M Characteristics

Figure 5-66. OSC20M Internal Oscillator: Calibration Stepsize vs. Calibration Value ($V_{DD}=3V$)



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Typical Characteristics

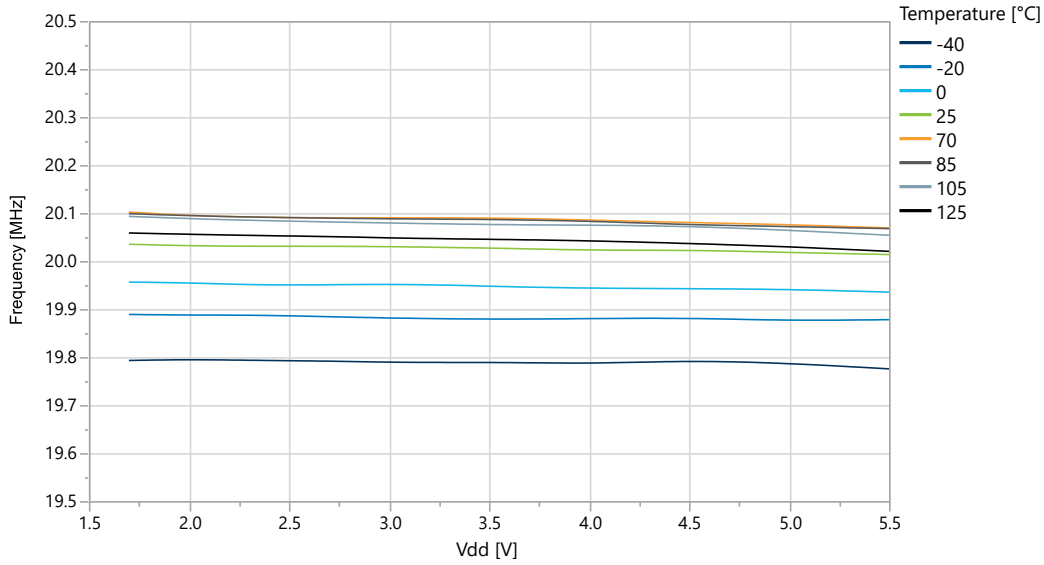
Figure 5-67. OSC20M Internal Oscillator: Frequency vs. Calibration Value ($V_{DD}=3V$)



Figure 5-68. OSC20M Internal Oscillator: Frequency vs. Temperature



Figure 5-69. OSC20M Internal Oscillator: Frequency vs. V_{DD}

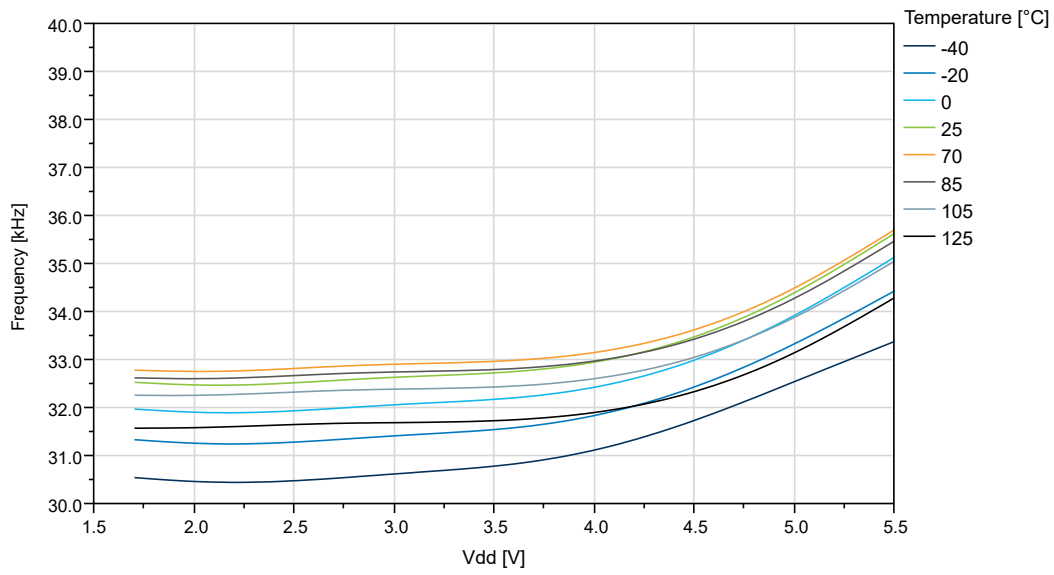


5.8 OSCULP32K Characteristics

Figure 5-70. OSCULP32K Internal Oscillator Frequency vs. Temperature



Figure 5-71. OSCULP32K Internal Oscillator Frequency vs. V_{DD}

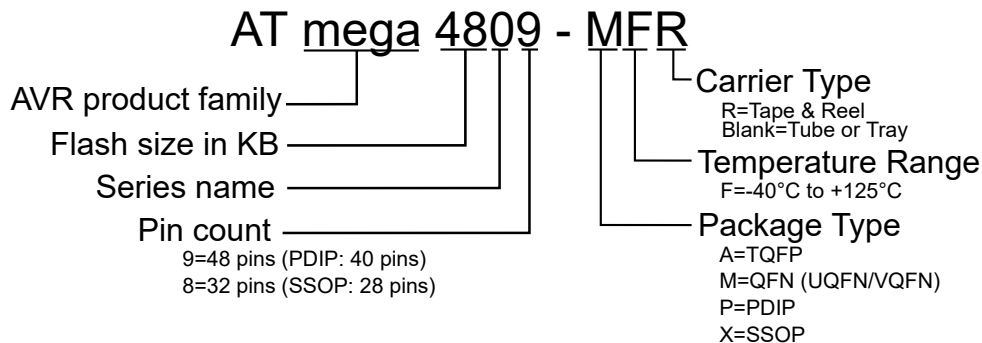


6. Ordering Information

- Available ordering options can be found by:
 - Clicking on one of the following product page links:
 - [ATmega809 Product Page](#)
 - [ATmega1609 Product Page](#)
 - [ATmega3209 Product Page](#)
 - [ATmega4809 Product Page](#)
 - Searching by product name at microchipdirect.com
 - Contacting your local sales representative

Figure 6-1. Product Identification System

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.



Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

7. Online Package Drawings

For the most recent package drawings:

1. Go to <http://www.microchip.com/packaging>.
2. Go to the package type specific page, for example VQFN.
3. Search for either Drawing Number or Style to find the most recent package drawings.

Table 7-1. Drawing Numbers

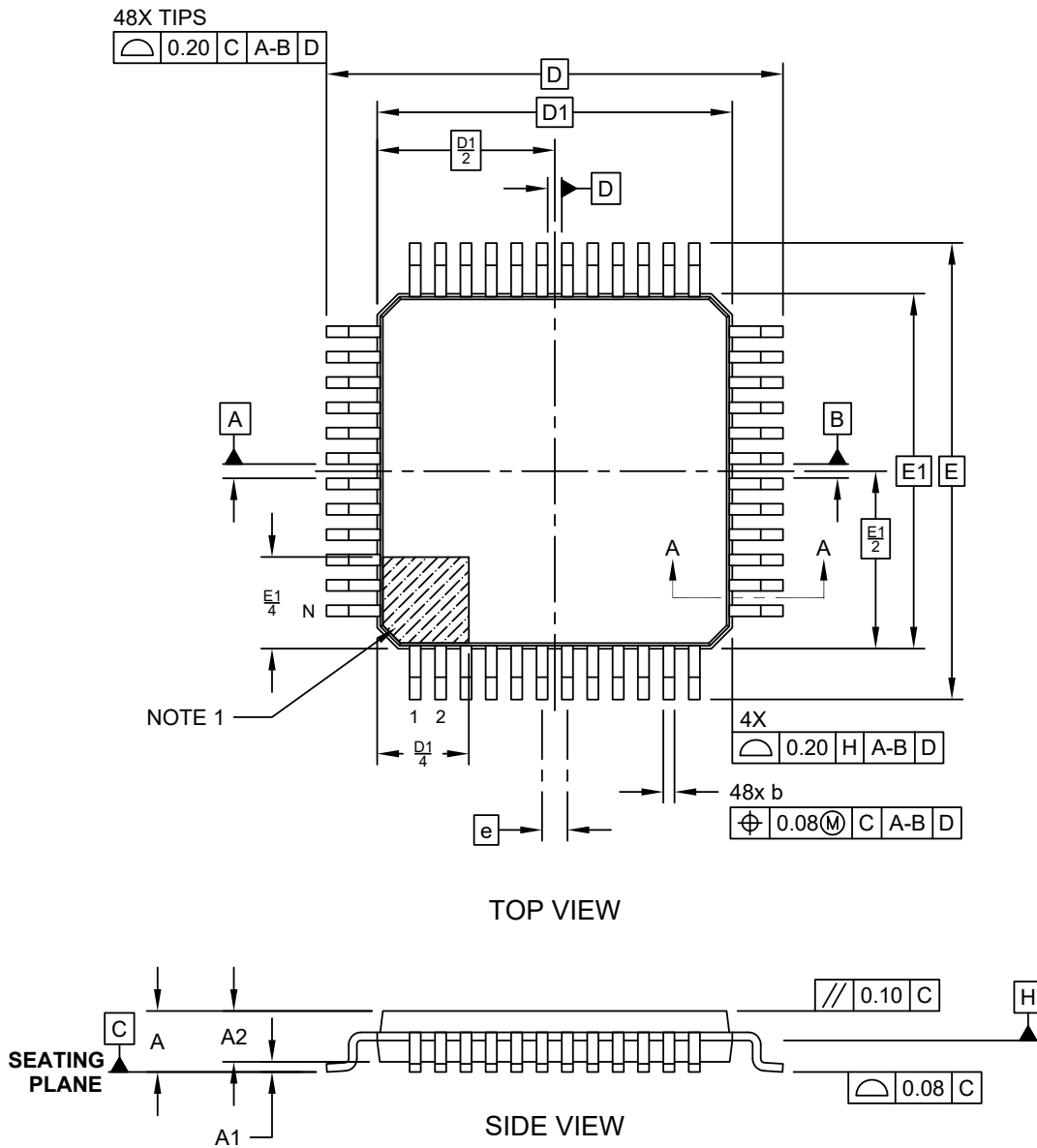
| Package Type | Drawing Number | Style |
|--------------|----------------|-------|
| UQFN48 | C04-153 | MV |
| TQFP48 | C04-300 | PT |

8. Package Drawings

8.1 48-Pin TQFP

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



ATmega809/1609/3209/4809 – 48-pin Package Drawings

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|----------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Leads | N | 48 | | |
| Lead Pitch | e | 0.50 BSC | | |
| Overall Height | A | - | - | 1.20 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | 9.00 BSC | | |
| Overall Length | D | 9.00 BSC | | |
| Molded Package Width | E1 | 7.00 BSC | | |
| Molded Package Length | D1 | 7.00 BSC | | |
| Lead Thickness | c | 0.09 | - | 0.16 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

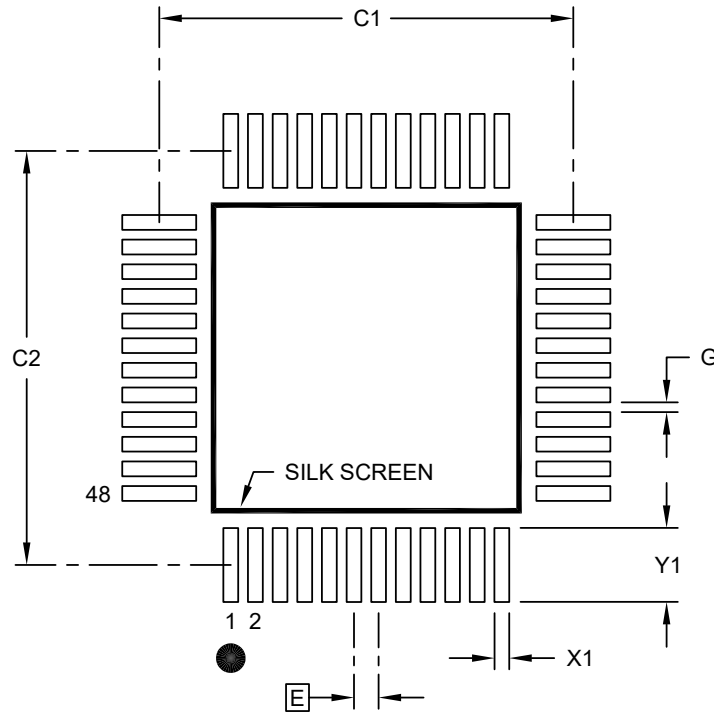
5. Datums **A-B** and **D** to be determined at center line between leads where leads exit plastic body at datum plane **H**

Microchip Technology Drawing C04-300-PT Rev A Sheet 2 of 2

ATmega809/1609/3209/4809 – 48-pin Package Drawings

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Contact Pad Spacing | C1 | | 8.40 | |
| Contact Pad Spacing | C2 | | 8.40 | |
| Contact Pad Width (X48) | X1 | | | 0.30 |
| Contact Pad Length (X48) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-PT Rev A

Table 8-1. Device and Package Maximum Weight

| | |
|-----|----|
| 140 | mg |
|-----|----|

ATmega809/1609/3209/4809 – 48-pin Package Drawings

Table 8-2. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

Table 8-3. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| J-STD-609 Material Code | e3 |

Table 8-4. Package Code

| |
|-----|
| Y8X |
|-----|

8.2 48-Pin UQFN

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-153A Sheet 1 of 2

ATmega809/1609/3209/4809 – 48-pin Package Drawings

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 48 | | |
| Pitch | e | 0.40 BSC | | |
| Overall Height | A | 0.45 | 0.50 | 0.55 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.127 REF | | |
| Overall Width | E | 6.00 BSC | | |
| Exposed Pad Width | E2 | 4.45 | 4.60 | 4.75 |
| Overall Length | D | 6.00 BSC | | |
| Exposed Pad Length | D2 | 4.45 | 4.60 | 4.75 |
| Contact Width | b | 0.15 | 0.20 | 0.25 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

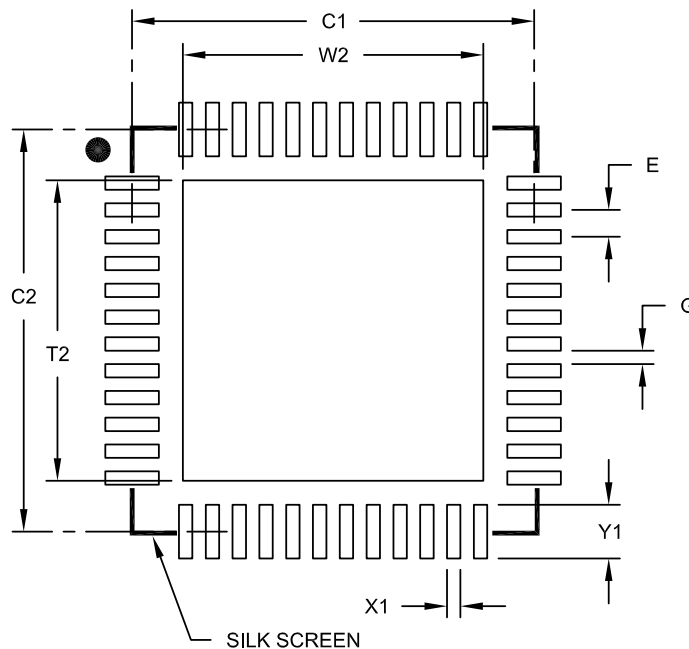
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2

ATmega809/1609/3209/4809 – 48-pin Package Drawings

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.40 BSC | | |
| Optional Center Pad Width | W2 | | | 4.45 |
| Optional Center Pad Length | T2 | | | 4.45 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (X28) | X1 | | | 0.20 |
| Contact Pad Length (X28) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.20 | | |

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

Table 8-5. Device and Package Maximum Weight

| | |
|-----|----|
| TBD | mg |
|-----|----|

ATmega809/1609/3209/4809 – 48-pin Package Drawings

Table 8-6. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL1 |
|----------------------------|------|

Table 8-7. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| J-STD-609 Material Code | e3 |

Table 8-8. Package Code

| |
|-----|
| R7X |
|-----|

9. Conventions

9.1 Memory Size and Type

Table 9-1. Memory Size and Bit Rate

| Symbol | Description |
|----------|----------------------------------------|
| KB | kilobyte ($2^{10} = 1024$) |
| MB | megabyte ($2^{20} = 1024*1024$) |
| GB | gigabyte ($2^{30} = 1024*1024*1024$) |
| b | bit (binary '0' or '1') |
| B | byte (8 bits) |
| 1 kbit/s | 1,000 bit/s rate (not 1,024 bit/s) |
| 1 Mbit/s | 1,000,000 bit/s rate |
| 1 Gbit/s | 1,000,000,000 bit/s rate |
| word | 16-bit |

9.2 Frequency and Time

Table 9-2. Frequency and Time

| Symbol | Description |
|--------|--------------------------------------|
| kHz | 1 kHz = 10^3 Hz = 1,000 Hz |
| KHz | 1 KHz = 1,024 Hz, 32 KHz = 32,768 Hz |
| MHz | 1 MHz = 10^6 Hz = 1,000,000 Hz |
| GHz | 1 GHz = 10^9 Hz = 1,000,000,000 Hz |
| ms | 1 ms = 10^{-3} s = 0.001s |
| μs | 1 μs = 10^{-6} s = 0.000001s |
| ns | 1 ns = 10^{-9} s = 0.000000001s |

10. Data Sheet Revision History

Note: The data sheet revision is independent of the die revision and the device variant (last letter of the ordering number).

10.1 Rev.B - 03/2019

| Chapter | Changes |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Entire Document | <ul style="list-style-type: none">• Added ATmega809/ATmega1609• Updated <i>Electrical Characteristics</i> section and <i>Typical Characteristics</i> section• Added package drawing for UQFN• Updated package drawing for TQFP |

10.2 Rev. A - 02/2018

Initial release.

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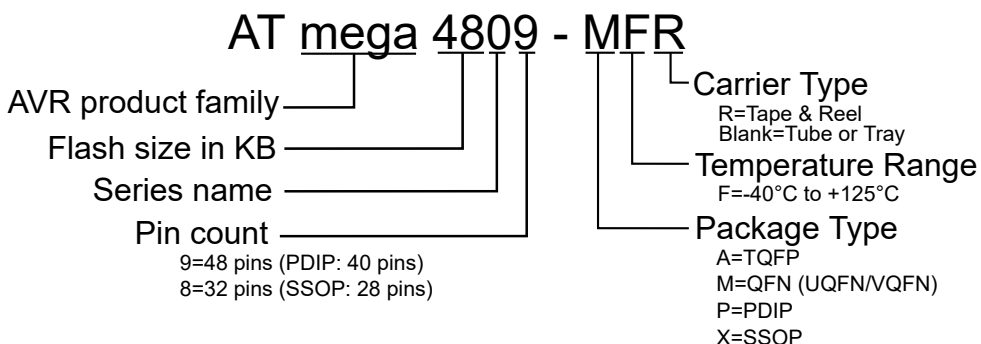
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