

LV88561, LV88562, LV88563, LV88564

Motor Driver, Single-Phase, PWM, Full-Wave, 24 V/48 V BLDC Motor



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Overview

The LV88561JA/R, LV88562JA/R, LV88563JA/R and LV88564JA/R are the pre-driver for a single-phase 24 V/48 V BLDC motor, which have the closed loop controller for motor rotation speed. These are available to control a motor with low vibration and the low noise. In addition, lead-angle adjustment is possible by external pins. Lead-angle value and lead-angle slant can be adjusted independently. Thus, the device can be driven by high efficiency and low noise with various motors. Motor speed setting curve is adjustable with using external resistor only. As a method of the rotary speed control of the motor, direct-PWM pulse input is adopted.

Features

- Single-phase Full Wave Drive Pre-driver Include Closed Loop Speed Control which is Fitting for High Voltage (24 V/48 V) Application
- Speed Control Function by PWM Duty Input (25 Hz to 100 kHz)
- Soft Start-up Function and PWM Soft Switching Phase Transition
- Soft PWM Duty Cycle Transitions
- Built-in Current Limit Circuit and Thermal Protection Circuit
- Built-in Locked Rotor Protection and Auto Recovery Circuit
- Dynamic Lead Angle Adjustment with Respect to Rotational Speed
- Lead-angle Control Parameters can be Configured
- Lineup of Different Closed Loop Gain Selection
- Lineup of Rotation Signal Output Selection
- These are Pb-Free and Halogen-Free Devices

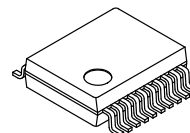
Typical Applications

- PC & Computing Equipment
- Refrigerator
- Games

LV88561, 562, 563, 564 COMPARISON TABLE

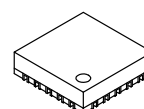
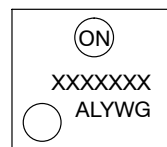
	Loop Gain	Rotation Signal
LV88561JA/R	Normal	FG
LV88562JA/R	Normal	RD
LV88563JA/R	Low	FG
LV88564JA/R	Low	RD

MARKING DIAGRAMS



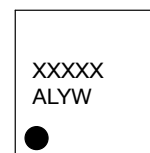
SSOP20J
CASE 565AP

(LV88561JA, LV88562JA, LV88563JA, LV88564JA)



VCT20
CASE 601AB

(LV88561R, LV88562R, LV88563R, LV88564R)



XX = Specific Device Code
A = Assembly Site (OSPI Tarlac Site Code: MP)
L = Wafer Lot Number
YW = Assembly Start Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
LV88561JA-AH LV88562JA-AH LV88563JA-AH LV88564JA-AH	SSOP20J (Pb-Free / Halogen Free)	2000 / Tape & Reel
LV88561RTXG LV88562RTXG LV88563RTXG LV88564RTXG	VCT20 (Pb-Free / Halogen Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BLOCK DIAGRAM

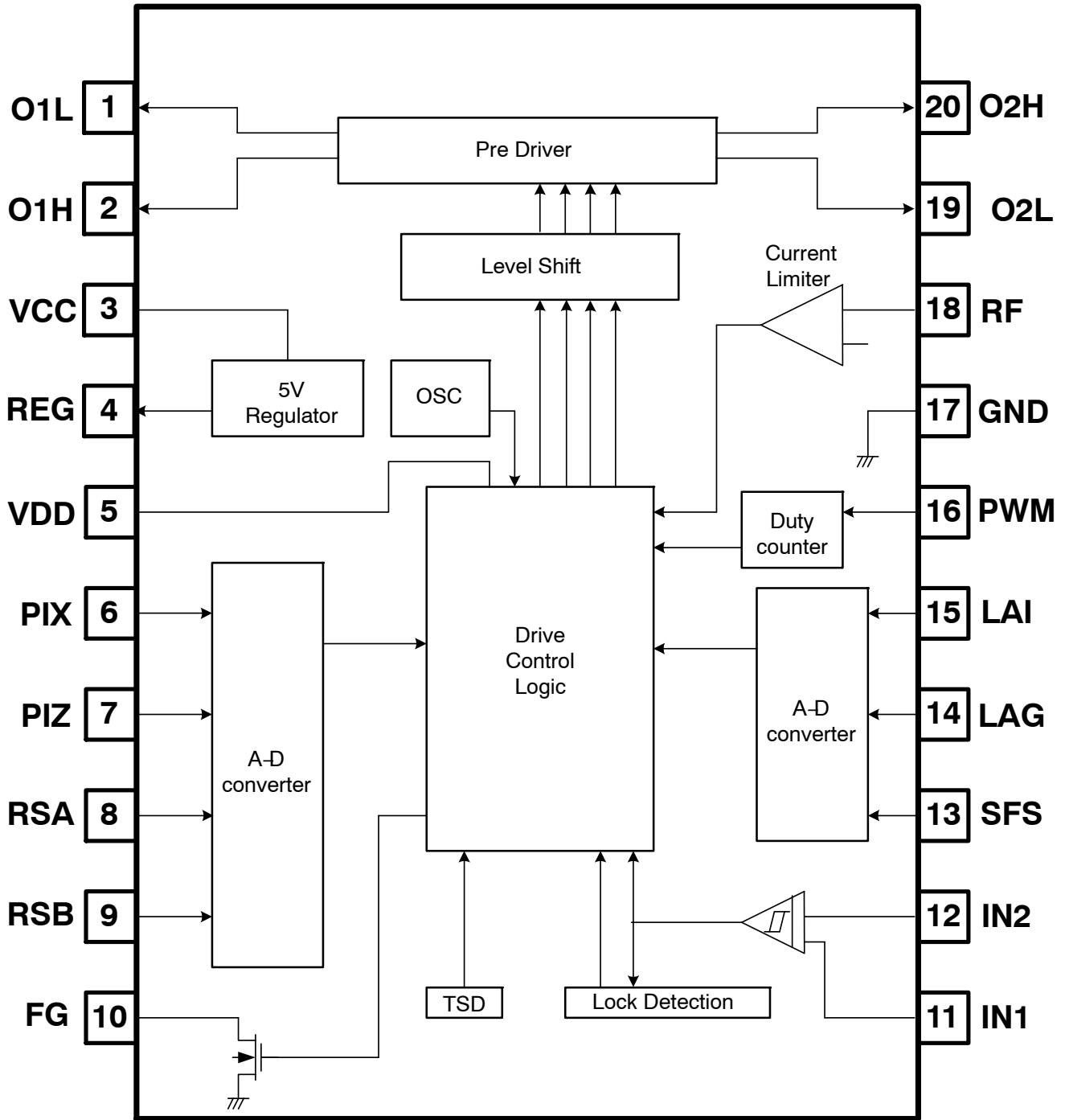


Figure 1. LV88561JA, LV88562JA, LV88563JA, LV88564JA Block Diagram

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APPLICATION CIRCUIT DIAGRAM

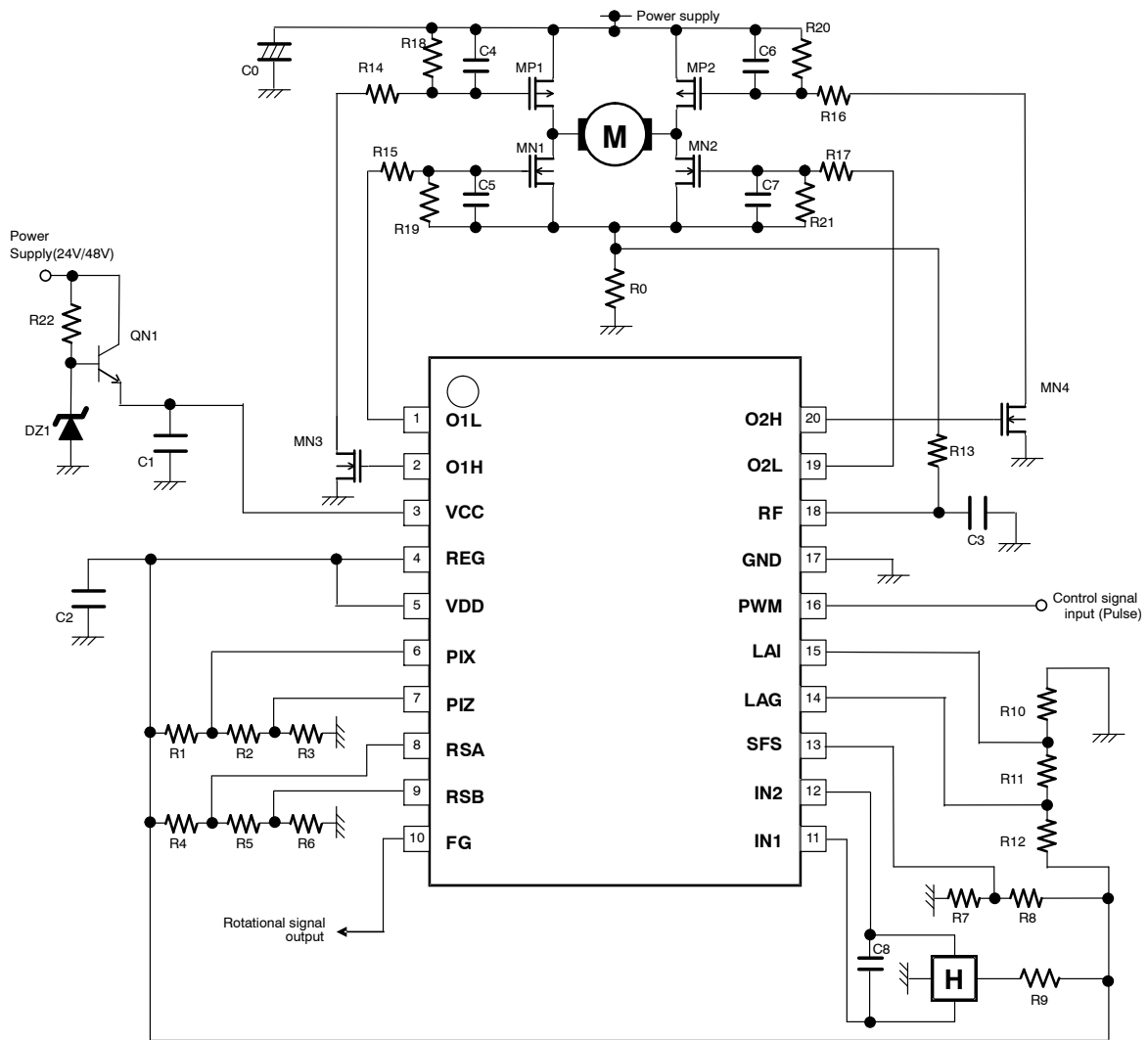


Figure 2. Single-phase BLDC Motor Drive with LV88561JA, LV88562JA, LV88563JA, LV88564JA

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Table 1. EXAMPLE COMPONENT VALUE

Device	Value	Device	Value
MP1+MN1	FW389	R14	100 Ω
MP2+MN2	FW389	R15	100 Ω
MN3,4	MCH3486	R16	100 Ω
QN1	NMBTA05LT1G	R17	100 Ω
DZ1	MM3Z12VT1G(12V Zener)	R18	*
		R19	*
R0	0.051 Ω // 0.051 Ω	R20	*
R1	0 to 50 kΩ	R21	*
R2	0 to 50 kΩ	R22	5.1 kΩ
R3	0 to 50 kΩ		
R4	0 to 50 kΩ		
R5	0 to 50 kΩ	C0	4.7 μF –10 uF
R6	0 to 50 kΩ	C1	0.1 μF – 1 μF
R7	0 to 50 kΩ	C2	0.1 μF – 1 μF
R8	0 to 50 kΩ	C3	**
R9	2.2 kΩ	C4	0 to 1500 pF
R10	0 to 50 kΩ	C5	0 to 1500 pF
R11	0 to 50 kΩ	C6	0 to 1500 pF
R12	0 to 50 kΩ	C7	0 to 1500 pF
R13	0 Ω	C8	0 to 0.1 μF

*Depend on the user circuit, MP1, MP2, MN1 and MN2.

**Depends on the user environment.

Table 2. TRUTH TABLE

Operating State	IN1	IN2	Inner-PWM State*	O1H	O1L	O2H	O2L	FG
Rotation – drive mode	L	H	On	L	H	H	L	OFF
	H	L		H	L	L	H	L
Rotation – regeneration mode	L	H	Off	L	L	H	L	OFF
	H	L		H	L	L	L	L
Lock protector	L	H	-	L	L	L	L	OFF
	H	L		L	L	L	L	L

*Inner PWM state means the OUTPUT active period decided by inner control logic. Don't match with PWM-pin input signal.

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PIN ASSIGNMENT

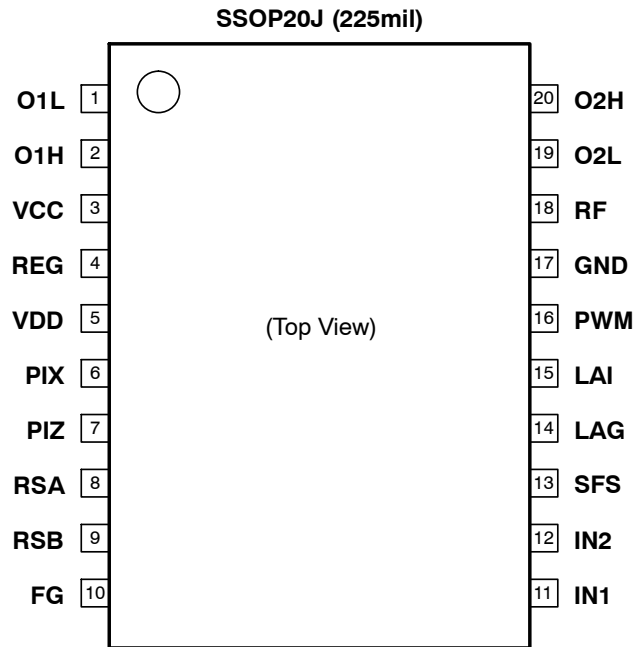


Figure 3. LV88561JA, LV88562JA, LV88563JA, LV88564JA Pin Assignment

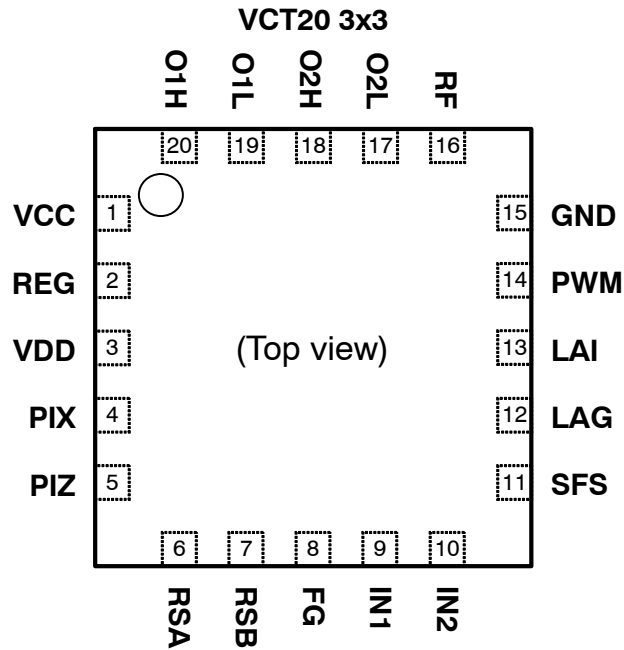


Figure 4. LV88561R, LV88562R, LV88563R, LV88564R Pin Assignment

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Table 3. PIN FUNCTION DESCRIPTION (Pin No. – SSOP20J version)

Pin No.	Pin name	Function
1 19	O1L O2L	Output pins of the low-side gate-drive signal. (See "Truth Table" on page 4 for the polarity)
2 20	O1H O2H	Output pins of the high-side gate-drive signal. (See "Truth Table" on page 4 for the polarity)
3	VCC	Power supply pin. The input voltage to this pin must be stabilized without the influence of the noise, ripple, and etc. Therefore, it is necessary to connect the capacitor near VCC pin and GND pin as much as possible.
4	REG	Output pin of the regulated voltage (5.0 V). It is necessary to connect the capacitor near this pin and GND pin for stabilizing this regulated voltage.
5	VDD	Logic circuit power supply pin. This pin should be shorted to REG pin.
6 7	PIX PIZ	PWM input duty adjust pins at the point of maximum or minimum rotation speed.
8 9	RSA RSB	Maximum or minimum rotation speed adjust pins.
10	FG	Output pin of the rotational signal. For LV88561 and LV88563, it functions as FG (Frequency Generator) and for LV88562 and LV88564, it functions as RD (Rotation Detection). This pin should be opened (disconnected) when not in use.
11 12	IN1 IN2	Hall signal input pins.
13	SFS	Soft start adjust pin.
14	LAG	Lead angle gradient adjust pin.
15	LAI	Initial lead angle adjust pin in minimum rotation speed.
16	PWM	PWM input pin of the speed control signal as the rectangular wave.
17	GND	GND pin.
18	RF	Output current detect pin. When the voltage level at this pin exceeds the internal set detection level, outputs turn to the regenerating mode.

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Table 4. MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VCC _{max}	VCC pin	20	V
Maximum output voltage	VOUT _{max}	O1H/O1L/ O2H/O2L pin	20	V
Maximum output current	IOUT _{max}	O1H/O1L/ O2H/O2L pin	50	mA
Maximum output peak current (Note 1)	IOUT _{peak}	O1H/O1L/ O2H/O2L pin	150	mA
REG pin maximum output current	I _{REG} _{max}	REG pin	20	mA
RSA/RSB/PIX/PIZ/LAI/LAG/SFS/IN1/IN2/RF pin maximum input voltage	V _{IN} max	RSA/RSB/PIX/ PIZ/LAI/LAG/IN1/ IN2/SFS/RF pin	5.5	V
PWM pin maximum input voltage	V _{PWM} _{max}	PWM pin	5.5	V
FG pin withstanding voltage	V _{FG} _{max}	FG pin	20	V
FG pin maximum output current	I _{FG} _{max}	FG pin	10	mA
Allowable power dissipation (Note 2)	P _d _{max}	LV8856xJA	0.8	W
Allowable power dissipation (Note 3)	P _d _{max}	LV8856xR	1.0	W
Operating temperature	T _{opr}		-40 to +105	°C
Storage temperature	T _{stg}		-55 to +150	°C
Maximum junction temperature	T _j _{max}		150	°C
Moisture Sensitivity Level (MSL) (Note 4)	MSL	LV8856xJA	3	-
Moisture Sensitivity Level (MSL) (Note 4)	MSL	LV8856xR	1	-
Lead Temperature Soldering Pb-Free Versions (30s or less) (Note 5)	T _{SLD}		255	°C
ESD Human body Model : HBM (Note 6)	ESD _{HBM}		±2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. IOUT_{peak} is the peak value of the motor supply current with duty_cycle < 5%.
2. Specified circuit board : 114.3 mm x 76.1 mm x 1.6 mm, glass epoxy single layer board. It has 1 oz internal power and ground planes and 1/2 oz copper traces. Please refer to Thermal Test Conditions on page 23.
3. Specified circuit board : 50.0 mm x 40.0 mm x 0.8 mm, glass epoxy 4-layer board. It has 1 oz internal power and ground planes and 1/2 oz copper traces on top and bottom of the board. Please refer to Thermal Test Conditions on page 23.
4. Moisture Sensitivity Level (MSL): IPC/JEDEC standard: J-STD-020A
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D http://www.onsemi.com/pub_link/Collateral/SOLDERRM-D.PDF
6. ESD Human Body Model is based on JEDEC standard: JESD22-A114

Table 5. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note 7) LV8856xJA	R _{θJA}	156	°C/W
Thermal Resistance, Junction-to-Ambient (Note 8) LV8856xR	R _{θJA}	125	°C/W

7. Specified circuit board : 114.3 mm x 76.1 mm x 1.6 mm, glass epoxy single layer board. It has 1 oz internal power and ground planes and 1/2 oz copper traces on top and bottom of the board. Please refer to Thermal Test Conditions on page 23.
8. Specified circuit board : 50.0 mm x 40.0 mm x 0.8 mm, glass epoxy 4-layer board. It has 1 oz internal power and ground planes and 1/2 oz copper traces on top and bottom of the board. Please refer to Thermal Test Conditions on page 23.

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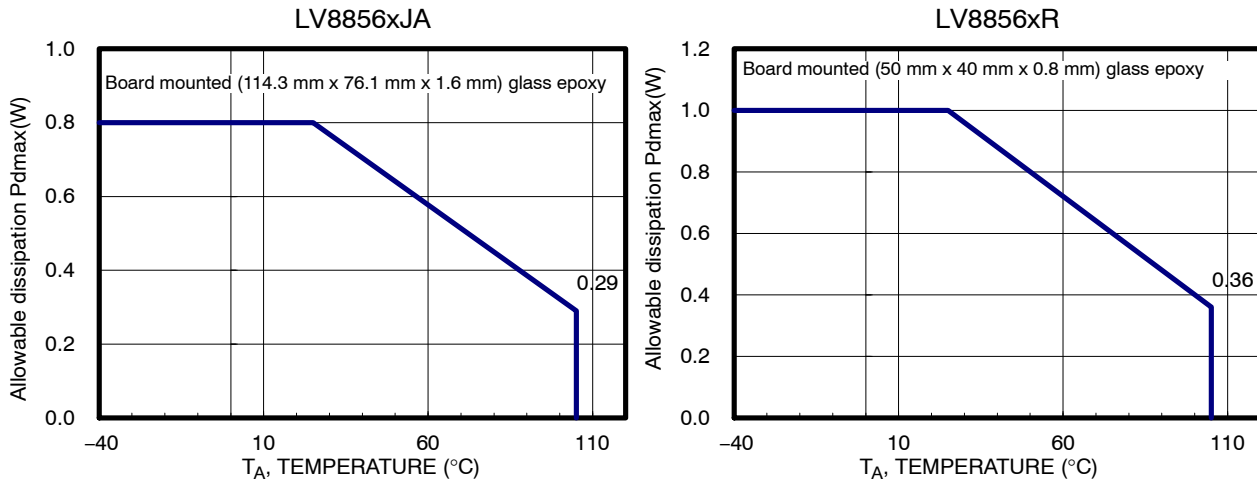


Figure 5. Power Dissipation vs Ambient Temperature Characteristic

Table 6. RECOMMENDED OPERATING RANGES (Note 9)

Parameter	Symbol	Conditions	Ratings	Unit
VCC supply voltage	VCC _{typ}	VCC pin	12	V
VCC operating supply voltage range1	VCC _{op1}	VCC pin	6.0 to 16	V
VCC operating supply voltage range2 (Note 10)	VCC _{op2}	VCC pin	3.9 to 6.0	V
PWM input frequency range	F _{pwm}	PWM pin	25 to 100k	Hz
PWM minimum input low/high pulse width	T _{wpwm}	PWM pin	100	ns
IN1 input voltage range	V _{in1}	IN1 pin	0 to VREG	V
IN2 input voltage range	V _{in2}	IN2 pin	0.3 to 0.55*VREG	V
Control input voltage range	V _{cnth}	RSA/RSB/PIX/ PIZ/LAI/LAG/SFS pin	0 to VREG	V

9. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

10. When the VCC voltage below 6.0 V, motor rotation function keep to normally until to 3.9 V. But there are possibility that the ELECTRICAL CHARACTERISTICS is varied.

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Table 7. ELECTRICAL CHARACTERISTICS at TA = 25°C, VCCOP = 12 V unless otherwise noted. (Note 11)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Circuit current	ICC			9	16	mA
O1H/O1L/O2H/O2L High-side on-resistance	ROHon	IO = 10 mA		30	80	Ω
O1H/O1L/O2H/O2L Low-side on-resistance	ROLon	IO = 10 mA		30	80	Ω
O1H/O1L/O2H/O2L PWM output frequency	fpwmo		45.6	48	50.4	kHz
PWM pin low level input voltage	Vpwml		0		0.7	V
PWM pin high level input voltage	Vpwmh		2.8		5.5	V
PWM input resolution	Δpwm			8		Bit
FG pin low level output voltage	Vfgl	IFG = 5 mA		0.2	0.3	V
FG pin leak current	Ifglk	VCC = 16 V VFG = 16 V			1	μA
REG pin output voltage	VREG		4.7	5.0	5.3	V
Lock-detection time1 (Note 12)	Tld1	Under rotation	0.27	0.3	0.33	S
Lock-detection time2 (Note 13)	Tld2	Start-up	0.63	0.7	0.77	S
Lock-Stop release time1 from 1 st to 4 th off time	Tlroff1		3.1	3.5	3.9	S
Lock-Restart on time	Tlron		0.63	0.7	0.77	S
Lock-Restart time ratio1	Rlr1	Tlroff1/Tlron		5		-
Lock-Stop release time2(Note 14) as from 5 th off time	Tlroff2		12.5	14	15.5	S
Lock-Restart time ratio2(Note 14) as from 5 th off time	Rlr2	Tlroff2/Tlron		20		-
Thermal protection detection temperature	Tthp	(Design target)	150	180		°C
Thermal protection detection hysteresis	ΔTthp	(Design target)		40		°C
Current limit detection voltage	VTHCLM	RF-GND	0.09	0.10	0.11	V
REG pin output voltage load regulation	ΔVregld	I _{REG} = -10 mA		20	50	mV
Hall input bias current	I _{hin}	IN1, IN2 = 0 V		0	1	μA
Hall input sensitivity	ΔV _{hin}		40			mV
Control input bias current	I _{ctlin}	PIX, PIZ, RSA, RSB, SFS, LAG, LAI = 0 V		0	1	μA
PWM input bias current	I _{pwmin}	VDD = 5.5 V, PWM = 0 V	14	28	42	μA
UVLO detection voltage	V _{uvdet}	VCC voltage	3.1	3.4	3.6	V
UVLO release voltage	V _{uvrls}	VCC voltage	3.3	3.6	3.9	V
UVLO hysteresis voltage	ΔV _{uv}		0.1	0.2	0.4	V

11. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

12. When the motor rotate state and the motor rotation speed reach to below 50 rpm (phase change period over 0.3s), lock protection function will activate.

13. At the motor start-up timing, the motor can't rotate until 0.7s, lock protection function work.

14. When the locked rotor state is continued for a long time, lock stop period will change from 5th off time.

TYPICAL CHARACTERISTICS

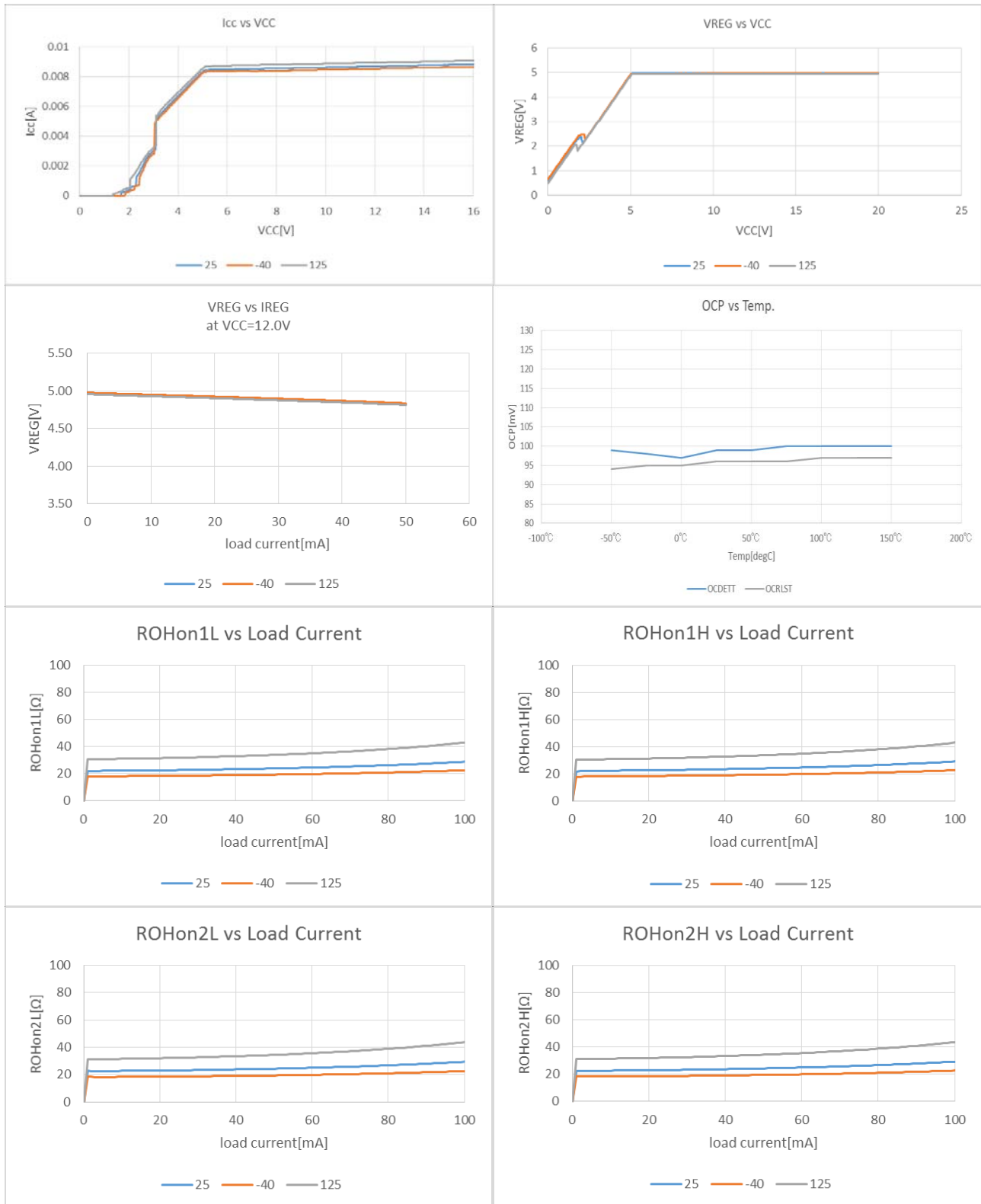


Figure 6. Typical Characteristics

EQUIVALENT CIRCUIT

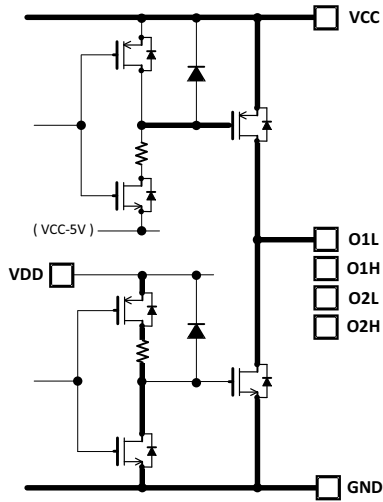


Figure 7. O1L, O1H, O2L and O2H Equivalent Circuit

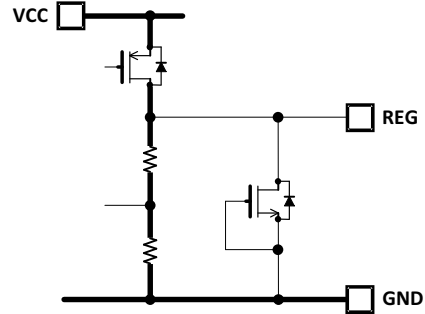


Figure 8. REG Equivalent Circuit

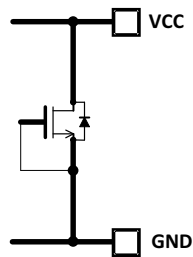


Figure 9. VCC Equivalent Circuit

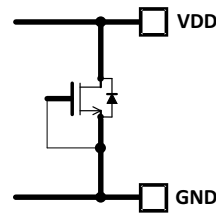


Figure 10. VDD Equivalent Circuit

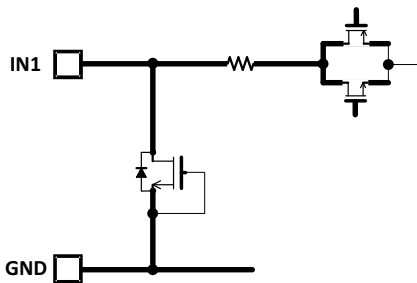


Figure 11. IN1, IN2 Equivalent Circuit

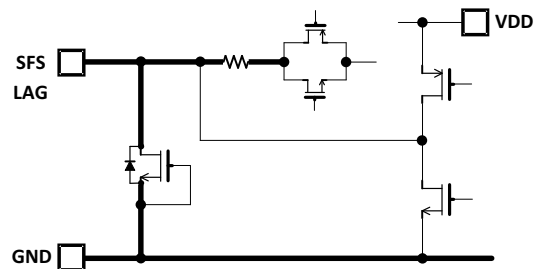


Figure 12. SFS, LAG Equivalent Circuit

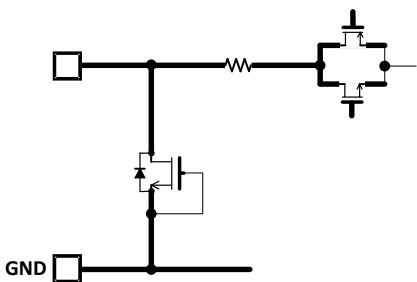


Figure 13. LAI Equivalent Circuit

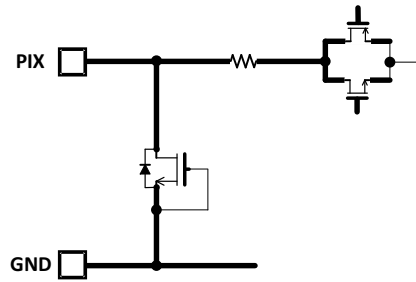


Figure 14. PIX, PIZ Equivalent Circuit

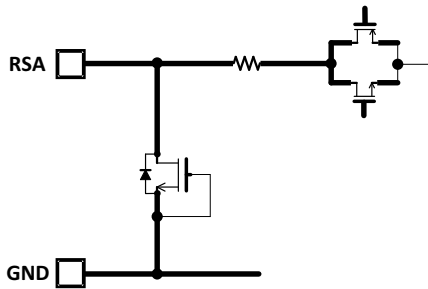


Figure 15. RSA, RSB Equivalent Circuit

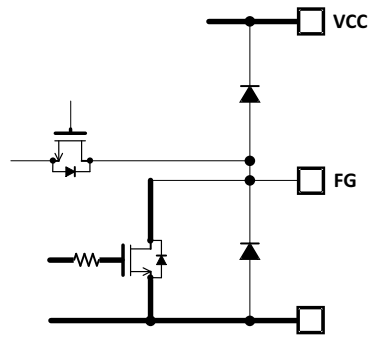


Figure 16. FG Equivalent Circuit

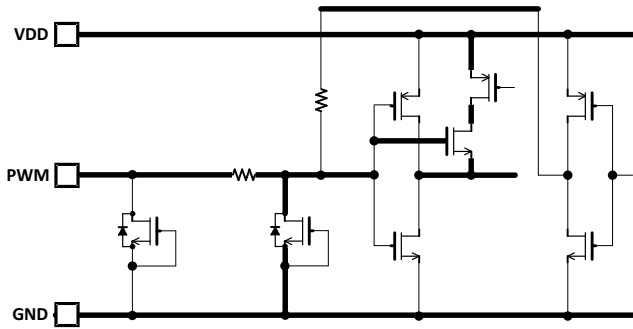


Figure 17. PWM Equivalent Circuit

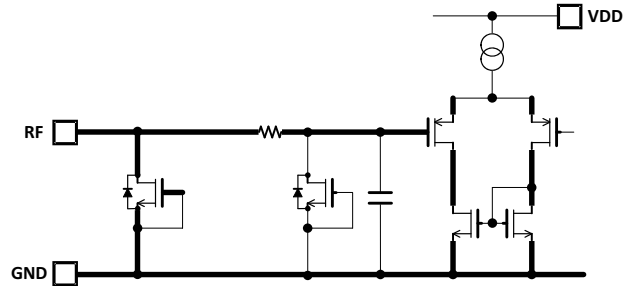


Figure 18. RF Equivalent Circuit

STATE DIAGRAM

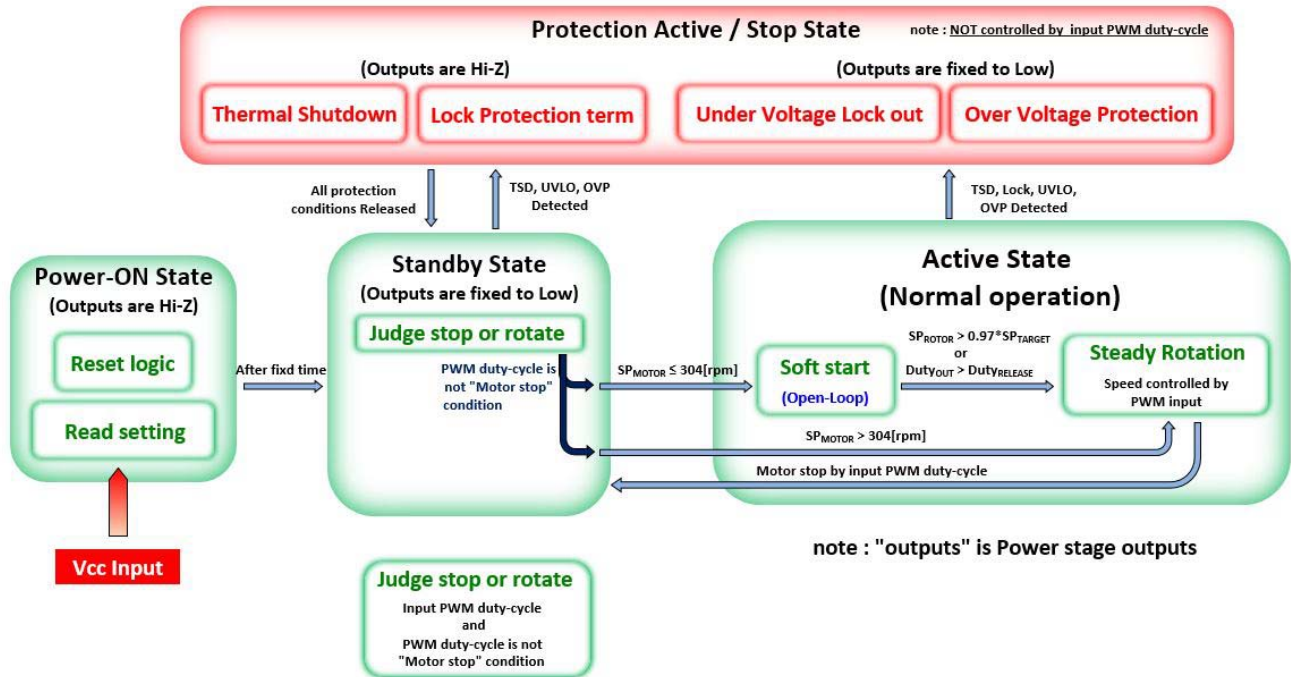


Figure 19. State Diagram

FUNCTIONAL DESCRIPTION**Loop Gain**

Motor speed loop gain of LV88563 and LV88564 is lower than that of LV88561 and LV88562. If the motor coil current generate large overshoot during motor speed transition, LV88563 and LV88564 can reduce the overshooting current but the motor rotation response speed will decrease. LV88561 and LV88562 are recommended if faster response speed is required.

Current Sense Resistor Pin (RF)

RF is current sense input terminal.

Voltage across the sense resistor represents the motor current and is compared against the internal $V_{TH_{OVC}}$ (0.10 Vtyp.) for setting the over-current limiter (CLM).

VCC and GND Pin (VCC ,GND)

Since Power FET side ground line has to tolerate surge of current, separate it from the GND pin as far away as possible and connect it point-to-point to the ground side of the capacitor (C0) between VCC and GND.

Internal 5.0 V Voltage Regulator Pin (REG, VDD)

REG is internal 5.0 V voltage regulator.

VDD is power supply for internal logic, oscillator, and protection circuits. Please connect REG and VDD.

When PIX, PIZ, RSA, RSB, LAI, LAG and SFS are used, it is recommended that application circuits are made using this output. The maximum load current of REG is 20 mA. Don't exceed this value. Place capacity from 0.1 μ F to 1.0 μ F in the close this pin.

Rotational Signal Pin (FG)

This is an open drain output pin which outputs the rotational signal. In case of LV88561 and LV88563, FG signal will come out from this pin and its frequency will represent electrical speed of a motor.

In case of LV88562 and LV88564, RD signal will come out from this pin. See page 21 "Lock detection and Lock protection" for more information about the RD signal.

Recommended pull up resistor value is 1 k Ω to 100 k Ω . Leave the pin open when not in use.

Output Pins for External FET Control (O1H , O1L , O2H, O2L)

These pins are output for external MOSFET. O1H and O2H connect to upper side P-ch FET's gate-line. O1L and O2L connect to lower side N-ch FET's gate line.

Hall-Sensor Input Pins (IN1, IN2)

Differential output signals of the hall sensor are to be interfaced at IN1 and IN2. It is recommended that 0.01 μ F capacitor is connected between both pins to filter system noise.

When a Hall IC is used, the output of the Hall IC must be connected to the pin IN1. And, the pin IN2 must be kept in the middle level of the Hall IC power supply voltage.

Command Input (PWM)

This pin reads the duty cycle of the PWM pulse and controls rotational speed. The PWM input signal level is supported from 2.5 V to 5 V. The combination with the rotational speed control by DC voltage, is impossible.

When the pin is not used, it must be connected to ground. The minimum pulse width is 100 ns.

Lead-Angle Setting Pin (LAI, LAG)

LV8856xJA/R provides the dynamic lead angle adjustment. To match the motor characteristics, set two point lead-angle, low speed side (set by LAI pin) and high speed side(set by LAG pin).

At middle range of input duty, the lead-angle is applied to calculated value for relative relationship.

The DC voltage levels applied to these pins are converted to the lead angle parameter. The voltages are fetched right after the power-on-reset. Because the internal conversion circuit works inside REG power rail, it is recommended that the LAI and LAG voltages are made from V_{REG} .

Rotation Speed Setting Pin (RSA, RSB)

LV8856xJA/R provides the feedback speed control, so this device can set the rotation speed value (RPM) directly.

To make the motor speed setting curve, set two point rotation speed value, high speed side and low speed side.

The DC voltage levels applied to these pins are converted to the rotation speed parameter. The voltages are fetched right after the power-on-reset. Because the internal conversion circuit works inside REG power rail, it is recommended that the RSA and RSB voltages are made from V_{REG} .

Rotation Speed Curve Duty Setting Pin (PIX, PIZ)

To make the motor speed setting curve, set two point input duty parameter, high speed side and low speed side.

The DC voltage levels applied to these pins are converted to the input duty parameter. The voltages are fetched right after the power-on-reset. Because the internal conversion circuit works inside REG power rail, it is recommended that the PIX and PIZ voltages are made from V_{REG} .

Soft-Start and Dead Time Setting Pin (SFS)

LV8856xJA/R provides synchronous rectification drive for high efficiency drive. External FET size is variable caused by the motor application. So this driver IC is able to choose 2 types of dead time.

Soft start function pattern is able to choose from 16 types.

The DC voltage levels applied to these pins are converted to the soft-start setting and dead time parameter. The voltage is fetched right after the power-on-reset. Because the internal conversion circuit works inside REG power rail, it is recommended that the SFS voltage is made from V_{REG} .

DETAILED DESCRIPTION

As for all numerical value used in this description, the design value or the typical value is used.

Rotation Speed Curve Setting Description

The LV8856xJA/R can set 2 points speed parameter arbitrarily.

Low speed point (LSP)

High speed point (HSP)

At middle range of input duty, the rotation speed is applied to calculated value for relative relationship.

When the input duty is lower than LSP setting duty, the LV8856xJA/R can select “motor stop” or “keep LSP rotation speed”.

When the input duty is higher than HSP setting duty, the LV8856xJA/R can select “free run” or “keep HSP rotation speed”.

Rotation speed of LSP and HSP is set by RSA and RSB pin. The case of $RSA > RSB$, “motor stop” mode applied. The case of $RSA < RSB$, “keep LSP rotation speed” mode applied.

Input duty of LSP and HSP is set by PIX and PIZ pin. The case of $PIX > PIZ$, “free run” mode applied. The case of $PIX < PIZ$, “keep HSP rotation speed” mode applied.

So LV8856xJA/R can't set decrease speed curve at input duty increase.

Figures 21 – 24 show setting curve example.

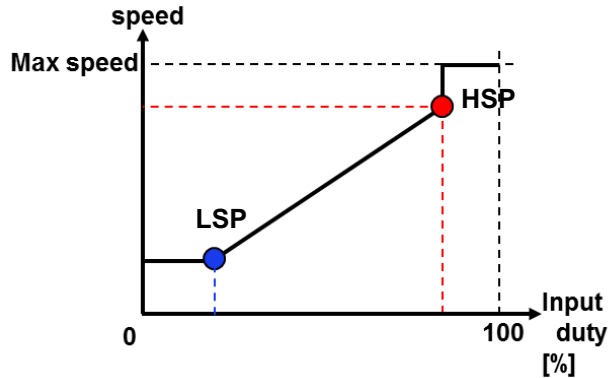


Figure 20. Image of Speed Setting Curve

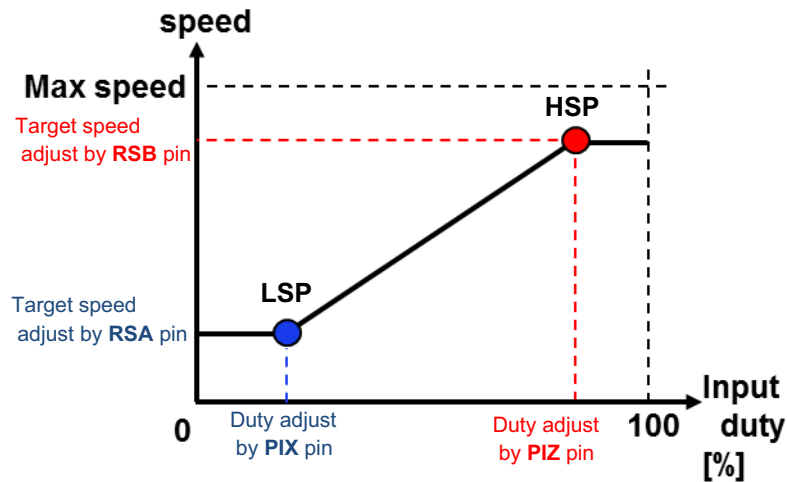


Figure 21. Speed Setting Curve Type Example 1
Minimum Speed Set and Maximum Speed Set

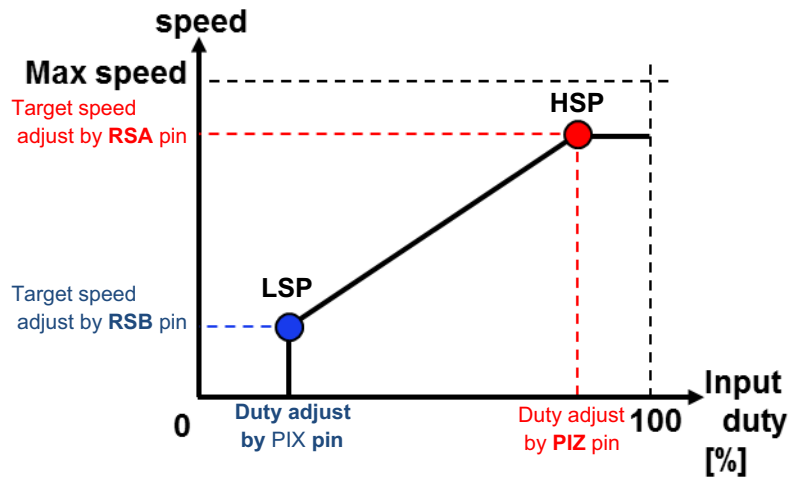


Figure 22. Speed Setting Curve Type Example 2
Motor Stop Mode and Maximum Speed Set

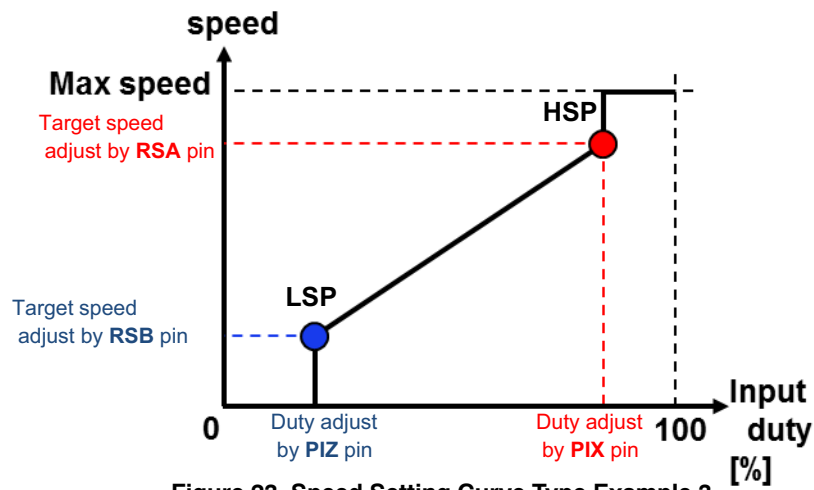


Figure 23. Speed Setting Curve Type Example 3
Motor Stop Mode and Free Run Mode

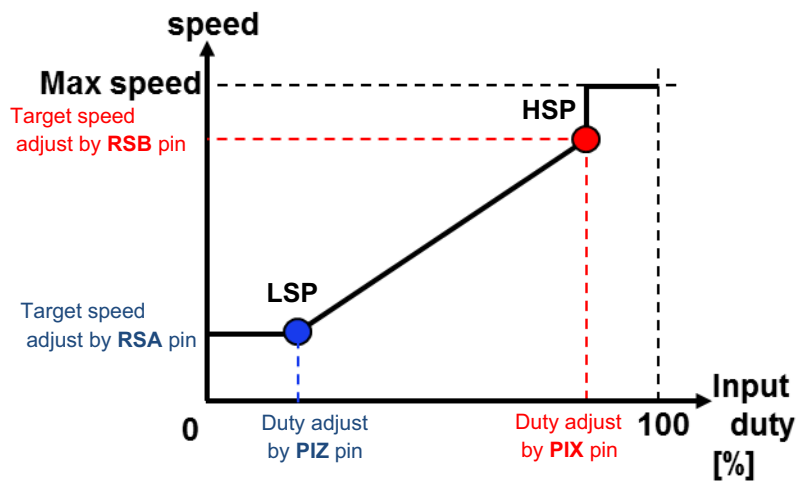


Figure 24. Speed Setting Curve Type Example 4
Minimum Speed Set and Free Run Mode

LV88561, LV88562, LV88563, LV88564

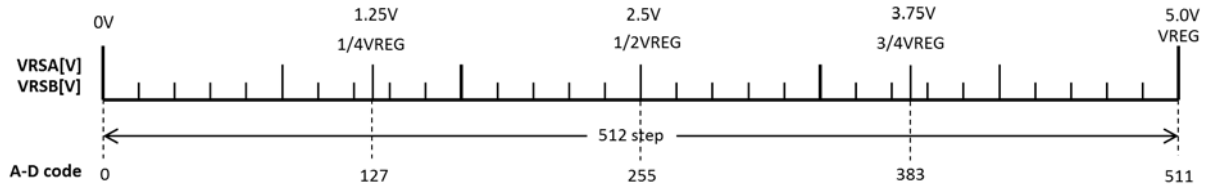


Figure 25. A-D Code Figure for RSA/RSB Pin

Voltage of RSA/RSB is calculated by below formula.

$$VRSA, VRSB[V] = \frac{VREG}{512} \times \text{Target RPM's A_D code} \quad (\text{eq. 1})$$

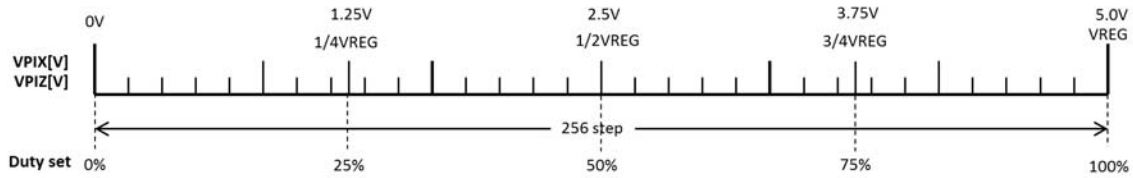


Figure 26. Input Duty Parameter Setting for PIX/PIZ Pin

Voltage of PIX/PIZ is calculated by below formula.

$$VPIX, VPIZ[V] = VREG \times \frac{\text{Target Duty}[\%]}{100} \quad (\text{eq. 2})$$

Lead-angle Setting Description

LV8856xJA/R provides the dynamic lead angle adjustment. To match the motor characteristics, set two points lead-angle amounts. Settable range is -22.225° to $+22.225^\circ$ (0.175° step). LSP's value is set by LAI pin and

HSP's value is set by LAG pin. At middle range of input duty, the lead-angle is applied to calculated value for relative relationship.

LV8856xJA/R can set delay angle setting. Minus value means delay angle.

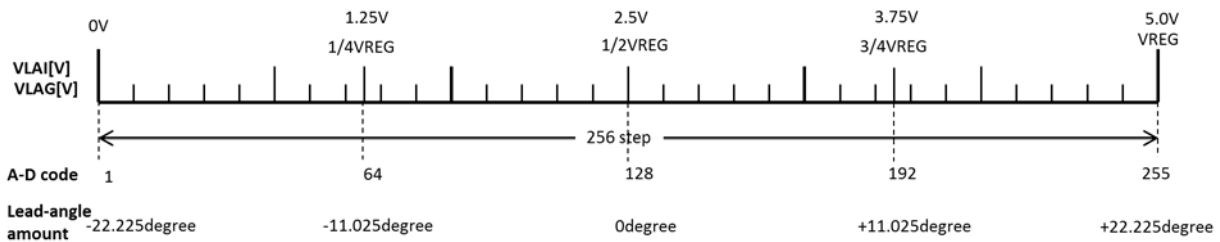


Figure 27. Lead-angle Parameter Setting for LAI/LAG Pin

Voltage of LAI/LAI is calculated by below formula.

$$VLAI, VLAG[V] = \frac{VREG}{2} + VREG \times \frac{\text{Target Lead Angle Value } [^\circ]}{44.45} \quad (\text{eq. 3})$$

Lead angle amounts of LSP and HSP doesn't care each relationship of large/small.

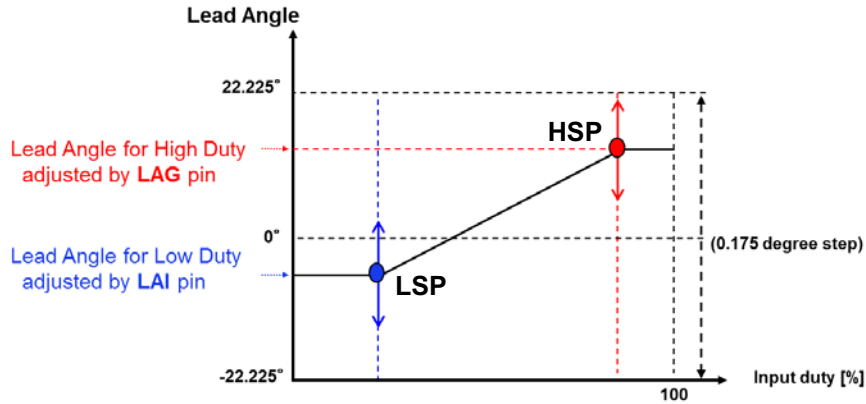


Figure 28. Image of Lead Angle Setting Curve

Lead angle	Low speed	High speed
Image		
Wave form		

Figure 29. Lead Angle Image Waveform

Soft-Start Setting Description

LV8856xJA/R has soft start function.

To avoid the motor rush current, the output PWM duty rise-up from zero slowly at the starting of motor rotation.

The soft start action release conditions are below;

Rotation speed reach to target speed decided by PWM input.

Output duty reach to "Release duty".

When reached to the release condition, change to closed-loop speed control mode.

If the motor can't rotation during 0.7s (typ), lock protection function will activate.

The recommendation of soft-start time is 1.72 s. Hence, it can be set by A-D code "0" and "31" for easy implementation by pin pull-down or pull-up.

A-D code	Soft-start time(s)	Release duty(%)	Dead time(us)
0	1.72	86	0.5
1	0.03	86	0.5
2	0.86	86	0.5
3	2.58	86	0.5
4	3.44	86	0.5
5	5.16	86	0.5
6	8.6	86	0.5
7	17.2	86	0.5
8	10	20	0.5
9	5	20	0.5
10	3	20	0.5
11	2	20	0.5
12	1.5	20	0.5
13	1	20	0.5
14	0.5	20	0.5
15	0.02	20	0.5
16	0.02	20	1
17	0.5	20	1
18	1	20	1
19	1.5	20	1
20	2	20	1
21	3	20	1
22	5	20	1
23	10	20	1
24	17.2	86	1
25	8.6	86	1
26	5.16	86	1
27	3.44	86	1
28	2.58	86	1
29	0.86	86	1
30	0.03	86	1
31	1.72	86	1

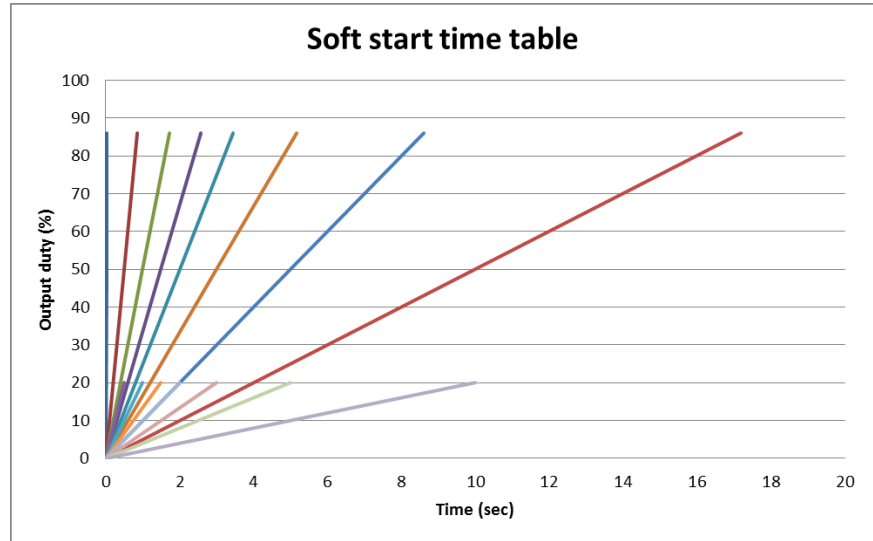


Figure 30. Soft-start and Dead Time Setting Table for SFS Pin

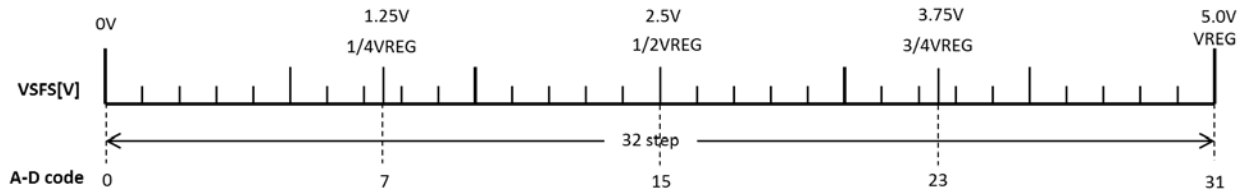


Figure 31. A-D Code Figure for SFS Pin

Voltage of SFS is calculated by below formula.

$$VSFS[V] = \frac{VREG}{32} \times \text{Target Setting's A_D Code} \quad (\text{eq. 4})$$

Output Waveform

LV8856xJA/R output PWM frequency is fixed by the inner oscillator parameter, 48 kHz (typ) which doesn't depend on input PWM frequency.

Driving method of LV8856xJA/R uses PWM soft switching drive.

Soft switching width is changed by input PWM duty.

When the input duty is HSP setting duty, soft switching width is narrow ($S/L = 20.5\%$)

On the other hand when the input duty is LSP setting duty, soft switching width becomes wide ($S/L = 46.9\%$)

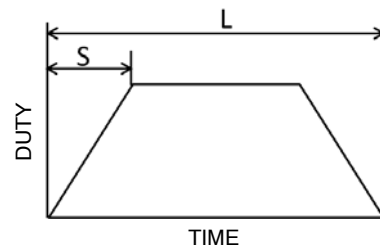


Figure 32. Image of Soft Switching Width

In this part, the rise/fall time of soft switching waveform is equal. Therefore, the "S" in the figure can be also applied to fall time as well.

At the middle range input duty, the soft switching width is applied to calculated value for relative relationship.

Protections

LV8856xJA/R has some protection function.

- Thermal shutdown protection (TSD)
- Under voltage lock out (UVLO)
- Current limiter (CLM)
- Lock protection

When TSD or Lock protection is working, external FETs are all turned off.

On the other hand, when UVLO or CLM is working, output is turned off and goes into re-circulation state.

Thermal Shutdown Protection (TSD)

When this IC’s junction temperature rises to 180°C (typ), O1H/O2H output turns to high, and O1L/O2L output turn to low. External FETs are all turns off and coil current is shut off.

Next, when IC’s junction temperature falls to 140°C (typ), thermal shutdown function is released and motor starts to rotate.

Under Voltage Lock Out (UVLO)

UVLO work voltage: VCC 3.4 V (typ)

UVLO release voltage: VCC 3.6 V (typ)

Current Limiter (CLM)

When the coil current increases and the voltage of the RF pin rises to 0.1 V (typ), the CLM operates and shut the coil current.

CLM current is adjustable by resistor value between RF–GND.

The sense resistor value is calculated as follows.

$$\text{Sense Resistor}[\Omega] = \frac{V_{TH_{CLM}}[V]}{I_{CLM}[A]} \tag{eq. 5}$$

For example, to set the CLM current threshold at 2A, the sense resistor value is

$$\text{Sense Resistor} = \frac{0.10(\text{typ})}{2.0}$$

$$\text{Res} = 0.05 [\Omega] \tag{eq. 6}$$

Lock Detection and Lock Protection

When the motor lock is happened, heat is generated because IC continues to supply electricity to the motor. And IC detects this radiated heat and turns off the electricity to the motor.

If IC does not receive the FG edge for 0.3sec (under 50rpm), the IC judges "motor lock" has occurred and the lock protection function will activate. In this mode, the RD signal goes to "High", though it is "Low" at motor starts.

When the motor restarts and IC detects 4 phase changes, the RD signal goes to "Low".

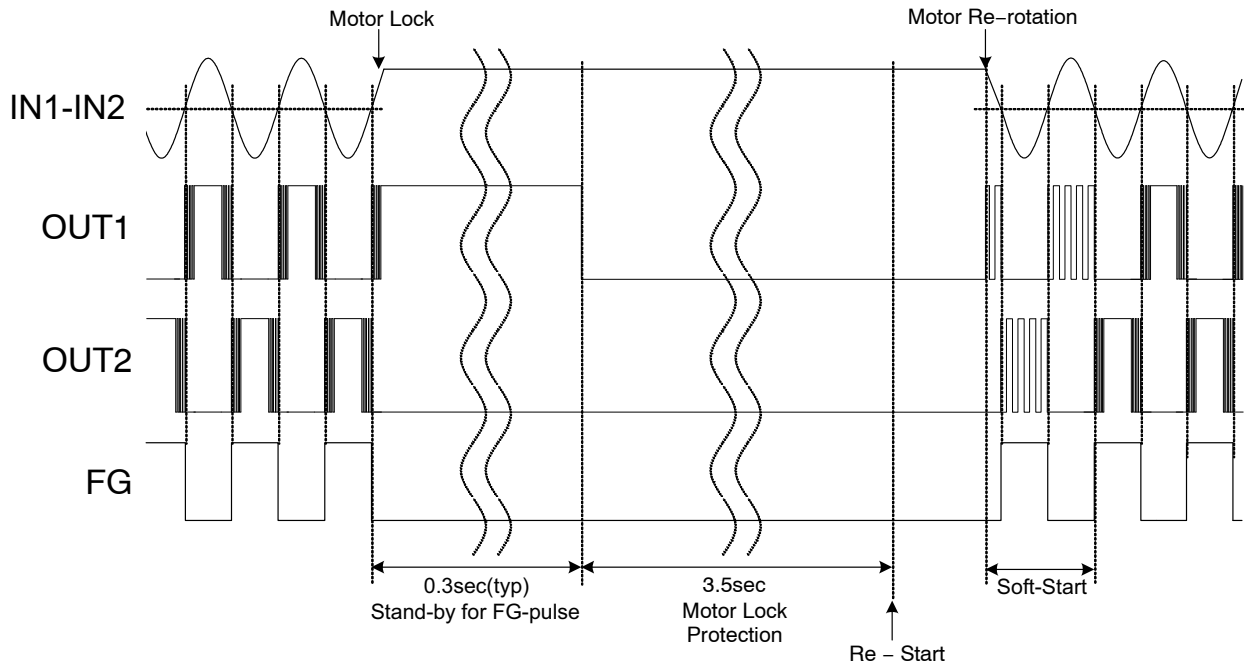


Figure 33. Image of Lock Detection and Lock Protection

It takes 3.5s for Lock protection time(1st to 4th protection time). This equals to the total of lock detection time and lock protection time. The lock detection time – the ratio is approx. 1:5 (from 1st to 4th protection time).

After 5th protection time, the lock protection time becomes 14s and protection–start time ratio is approx. 1:20 (after 5th protection time)

When the motor rotation is stopped by PWM input signal, the lock detection is reset and the motor starts to rotate smoothly once the IC receives the rotation start instruction.

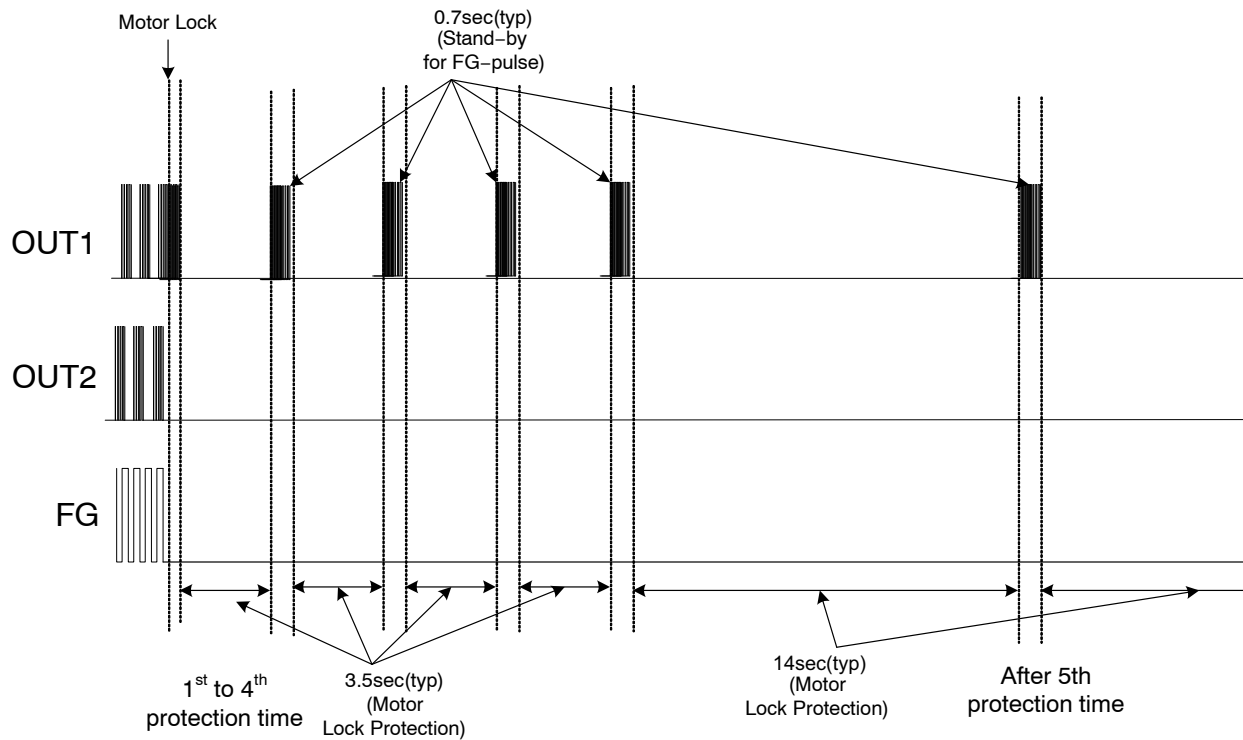


Figure 34. Image of Lock Protection Time

PCB GUIDELINES**VCC and Ground Routing**

Make sure to short-circuit power line externally by a low impedance route on one side of PCB. As high current flows into external FET to GND, connect it to GND through a low impedance route.

The capacitance connected between the VCC pin and the opposite ground is to stabilize the battery. Make sure to connect an electrolytic capacitor with capacitance value of about 1 μF (0.1 μF or greater) to eliminate low frequency noise. Also, to eliminate high frequency noise, connect a capacitor of superior frequency characteristics, with capacitance value of about 0.1 μF and make sure that the capacitor is connected as close to the pin as possible. Allow enough room in the design so the impact of PWM drive and flyback do not affect other components. Especially, when the coil inductance is large and/or the coil resistance is small, current ripple will rise so it is necessary to use a high-capacity capacitor with superior frequency characteristics. Please note that if the battery voltage rises due to the impact of the coil flyback as a result of the use of diode for preventing the break down caused by reverse connection, it is necessary to either increase the capacitance value or place Zener diode between the battery and the ground so that the voltage does not exceed its absolute maximum voltage.

When the electrolytic capacitor cannot be used, add the resistor with the value of about 1 Ω and a ceramic capacitor with the capacitor value of about 10 μF in series for the alternative use. When the battery line is extended,

(20–30 cm to 2–3 m), the battery voltage may overshoot when the power is supplied due to the impact of the routing of the inductance. Make sure that the voltage does not exceed the absolute maximum standard voltage when the power supply turns on.

These capacitance values are just for reference, so the confirmation with the actual application is essential to determine the values appropriately.

RF Routing

Power current (output current) flows through the RF line. Make sure to short-circuit the line from RF through GND as well as GND. The RF resistance must choose enough power rating.

External FET Output Pins

Since the pins have to tolerate surge of current, make sure that the wires are thick and short enough when designing the PCB board.

Thermal Test Conditions

LV8856xJA (x = 1,2,3 or 4)

Size: 114.3 mm x 76.1 mm x 1.6 mm

Material: Glass epoxy single layer board

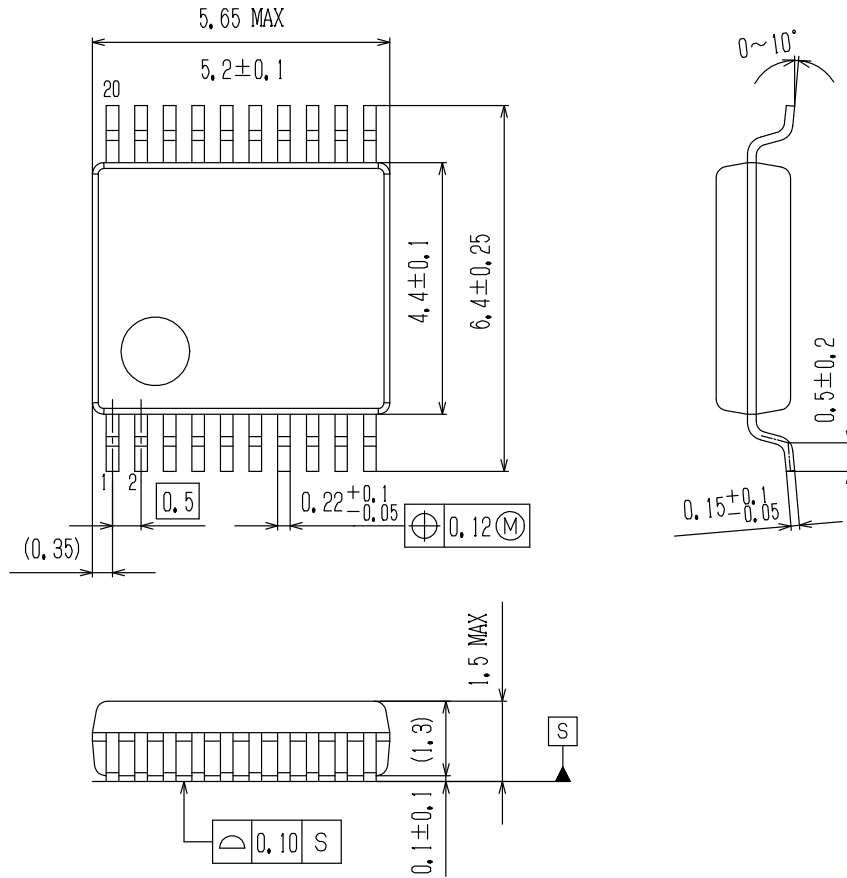
LV8856xR (x = 1,2,3 or 4)

Size: 50.0 mm x 40.0 mm x 0.8 mm

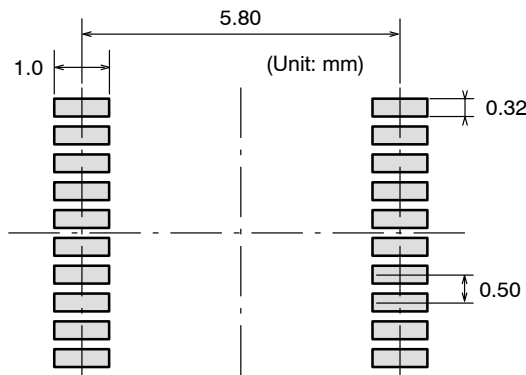
Material: Glass epoxy 4-layer board

PACKAGE DIMENSIONS

SSOP20J (225mil)
CASE 565AP
ISSUE A



SOLDERING FOOTPRINT*



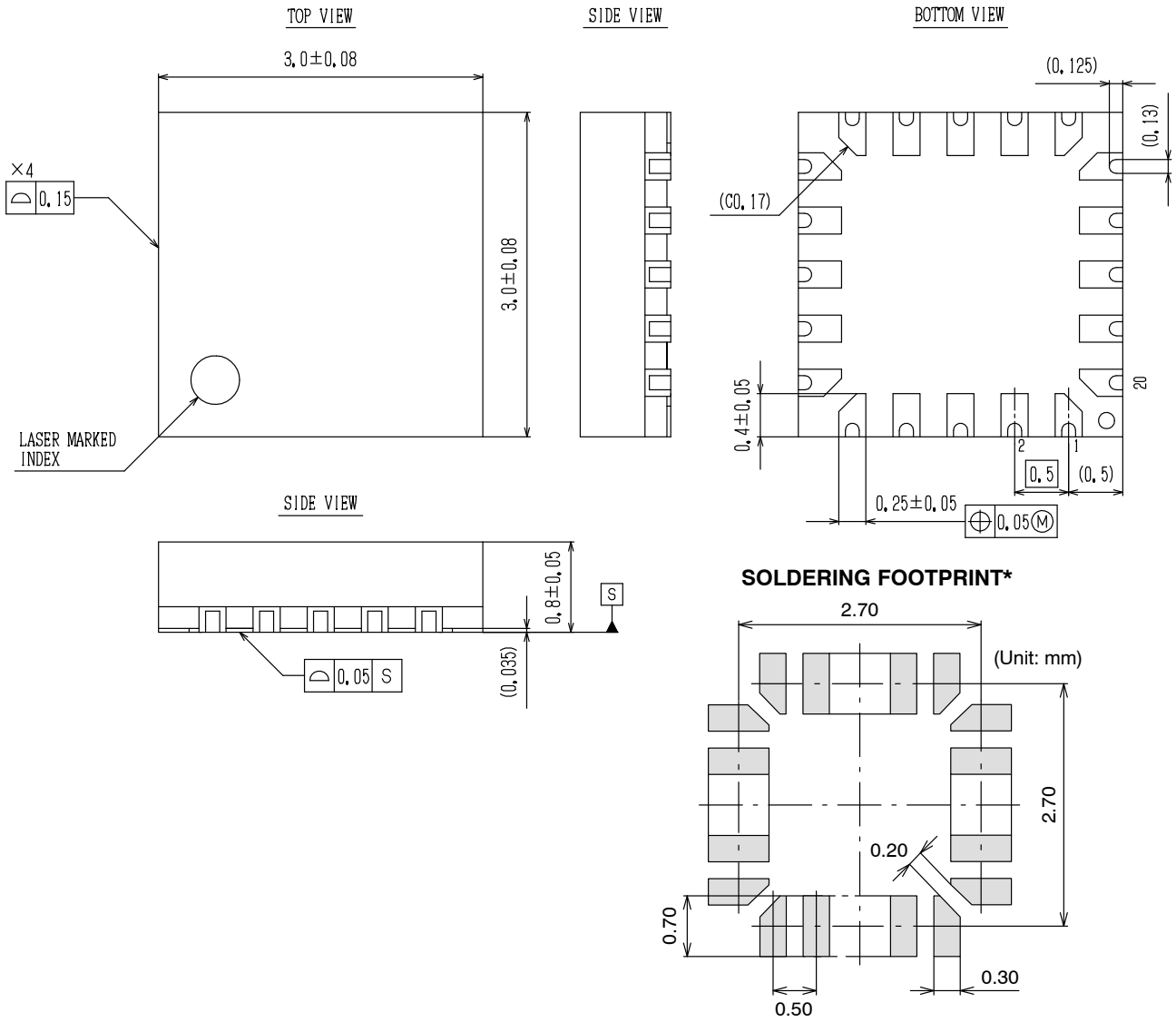
NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LV88561, LV88562, LV88563, LV88564


PACKAGE DIMENSIONS

VCT20 3x3, 0.5P
CASE 601AB
ISSUE A



NOTE: The measurements are not to guarantee but for reference only.

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