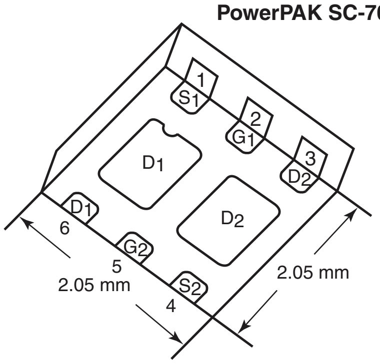
N- and P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

	V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)	Q_g (Typ.)
N-Channel	12	0.029 at V_{GS} = 4.5 V	4.5[a]	5.6 nC
		0.034 at V_{GS} = 2.5 V	4.5[a]	
		0.044 at V_{GS} = 1.8 V	4.5[a]	
		0.065 at V_{GS} = 1.5 V	4.5[a]	
P-Channel	- 12	0.041 at V_{GS} = - 4.5 V	- 4.5[a]	10.5 nC
		0.060 at V_{GS} = - 2.5 V	- 4.5[a]	
		0.110 at V_{GS} = - 1.8 V	- 3.5	
		0.174 at V_{GS} = - 1.5 V	- 1	

PowerPAK SC-70-6 Dual



Ordering Information:
SiA527DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

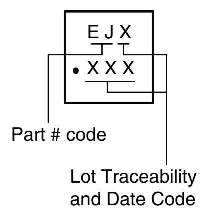
- TrenchFET® Power MOSFETs
- Thermally Enhanced PowerPAK® SC-70 Package
  - Small Footprint Area
  - Low On-Resistance
- 100 % R_g Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

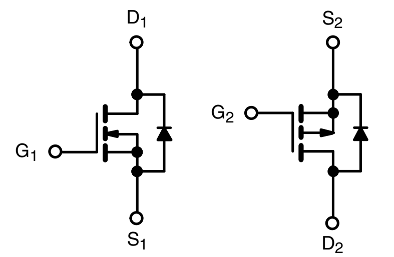
Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Portable Devices Such as Smart Phones, Tablet PCs and Mobile Computing
  - Load Switches
  - Power Management
  - DC/DC Converters

Marking Code





N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	12	- 12	V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	4.5[a]	- 4.5[a]	A
	T_C = 70 °C		4.5[a]	- 4.5[a]	
	T_A = 25 °C		4.5[a,b,c]	- 4.5[a,b,c]	
	T_A = 70 °C		4.5[a,b,c]	- 4.4[b,c]	
Pulsed Drain Current (t = 100 µs)		I_{DM}	20	- 15	
Source Drain Current Diode Current	T_C = 25 °C	I_S	4.5[a]	- 4.5[a]	
	T_A = 25 °C		1.6[b,c]	- 1.6[b,c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	7.8	7.8	W
	T_C = 70 °C		5	5	
	T_A = 25 °C		1.9[b,c]	1.9[b,c]	
	T_A = 70 °C		1.2[b,c]	1.2[b,c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[d,e]			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	N-Channel Typ.	N-Channel Max.	P-Channel Typ.	P-Channel Max.	Unit
Maximum Junction-to-Ambient[b,f]	t ≤ 5 s	R_{thJA}	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16	12.5	16	

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 110 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	12			V
		V_{GS} = 0 V, I_D = - 250 µA	P-Ch	- 12			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch		12		mV/°C
		I_D = - 250 µA	P-Ch		- 3.6		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch		- 2.5		
		I_D = - 250 µA	P-Ch		2.4		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	0.4		1	V
		$V_{DS} = V_{GS}$, I_D = - 250 µA	P-Ch	- 0.4		- 1	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 12 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = - 12 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 12 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch			10	
		V_{DS} = - 12 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch			- 10	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, V_{GS} = 4.5 V	N-Ch	15			A
		$V_{DS} \leq - 5$ V, V_{GS} = - 4.5 V	P-Ch	- 10			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 5 A	N-Ch		0.024	0.029	Ω
		V_{GS} = - 4.5 V, I_D = - 4.3 A	P-Ch		0.033	0.041	
		V_{GS} = 2.5 V, I_D = 4.6 A	N-Ch		0.028	0.034	
		V_{GS} = - 2.5 V, I_D = - 3.6 A	P-Ch		0.049	0.060	
		V_{GS} = 1.8 V, I_D = 4.1 A	N-Ch		0.032	0.044	
		V_{GS} = - 1.8 V, I_D = - 1.5 A	P-Ch		0.070	0.110	
		V_{GS} = 1.5 V, I_D = 2 A	N-Ch		0.042	0.065	
		V_{GS} = - 1.5 V, I_D = - 1 A	P-Ch		0.095	0.174	
Forward Transconductance[b]	g_{fs}	V_{DS} = 6 V, I_D = 5 A	N-Ch		21		S
		V_{DS} = - 6 V, I_D = - 4.6 A	P-Ch		12		
Dynamic[a]							
Input Capacitance	C_{iss}	N-Channel V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 6 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		500		pF
			P-Ch		1500		
Output Capacitance	C_{oss}		N-Ch		160		
			P-Ch		260		
Reverse Transfer Capacitance	C_{rss}		N-Ch		100		
			P-Ch		250		
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 8 V, I_D = 6.5 A	N-Ch		9.7	15	nC
		V_{DS} = - 6 V, V_{GS} = - 8 V, I_D = - 5.6 A	P-Ch		17	26	
		N-Channel V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 6.5 A P-Channel V_{DS} = - 6 V, V_{GS} = - 4.5 V, I_D = - 5.6 A	N-Ch		5.6	8.5	
			P-Ch		10.5	16	
Gate-Source Charge	Q_{gs}		N-Ch		0.72		
			P-Ch		2.3		
Gate-Drain Charge	Q_{gd}		N-Ch		0.74		
			P-Ch		2.5		
Gate Resistance	R_g	f = 1 MHz	N-Ch	0.7	3.5	7	Ω
			P-Ch	1.1	5.5	11	

Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

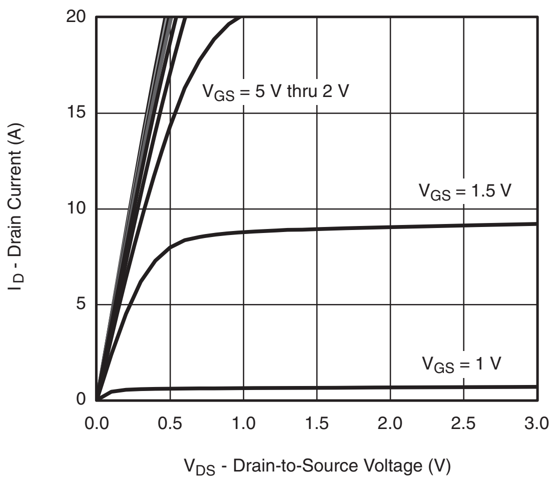
For technical questions, contact:: pmostechsupport@vishay.com

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 6 V, R_L = 1.2 Ω $I_D \cong$ 5.2 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-Channel V_{DD} = - 6 V, R_L = 1.3 Ω $I_D \cong$ - 4.5 A, V_{GEN} = - 4.5 V, R_g = 1 Ω	N-Ch		10	15	ns
			P-Ch		22	35	
Rise Time	t_r		N-Ch		10	15	
			P-Ch		22	35	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		22	30	
			P-Ch		32	50	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		15	25	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 6 V, R_L = 1.2 Ω $I_D \cong$ 5.2 A, V_{GEN} = 8 V, R_g = 1 Ω P-Channel V_{DD} = - 6 V, R_L = 1.3 Ω $I_D \cong$ - 4.5 A, V_{GEN} = - 8 V, R_g = 1 Ω	N-Ch		5	10	
			P-Ch		10	15	
Rise Time	t_r		N-Ch		10	15	
			P-Ch		10	15	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		18	30	
			P-Ch		30	40	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		12	20	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	N-Ch			4.5	A
			P-Ch			- 4.5	
Pulse Diode Forward Current (t = 100 µs)	I_{SM}		N-Ch			20	
			P-Ch			- 15	
Body Diode Voltage	V_{SD}	I_S = 5.2 A, V_{GS} = 0 V	N-Ch		0.85	1.2	V
		I_S = - 4.5 A, V_{GS} = 0 V	P-Ch		- 0.87	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel I_F = 5.2 A, dI//dt = 100 A/µs, T_J = 25 °C P-Channel I_F = - 4.5 A, dI/dt = - 100 A/µs, T_J = 25 °C	N-Ch		20	40	ns
			P-Ch		30	60	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		5	10	nC
			P-Ch		15	30	
Reverse Recovery Fall Time	t_a		N-Ch		8		ns
			P-Ch		15		
Reverse Recovery Rise Time	t_b		N-Ch		12		
			P-Ch		15		

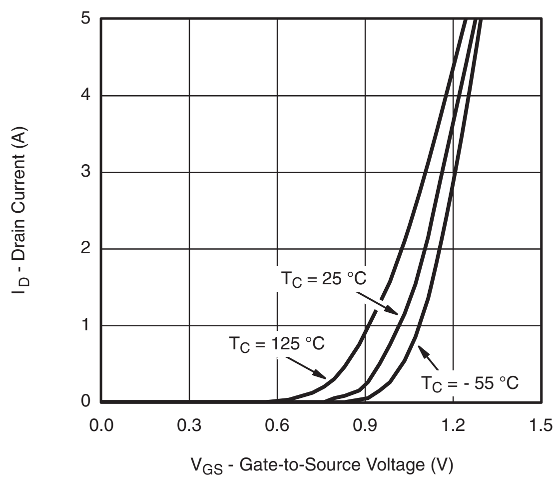
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

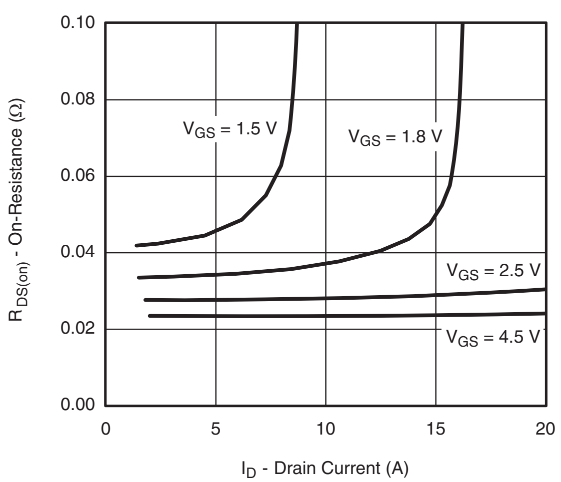
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



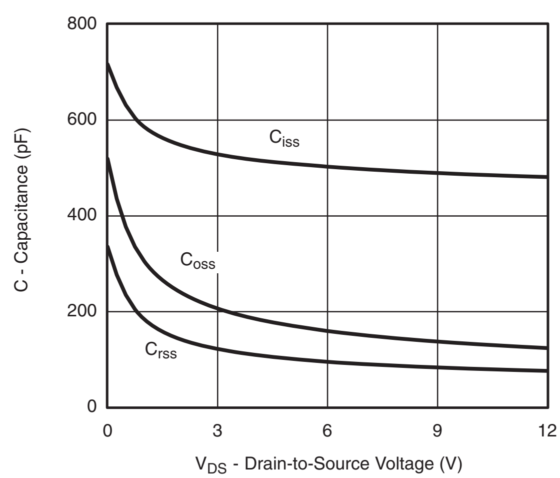
Output Characteristics



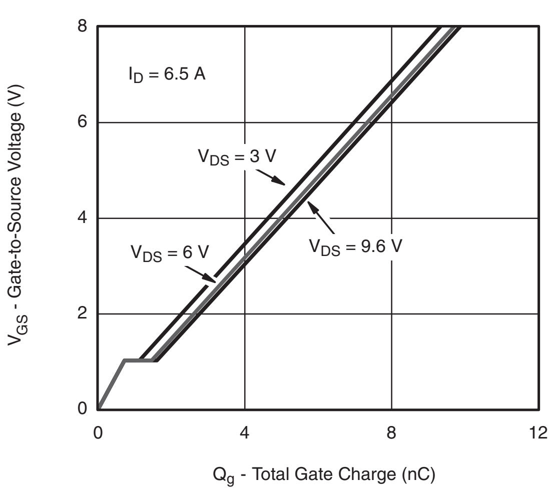
Transfer Characteristics



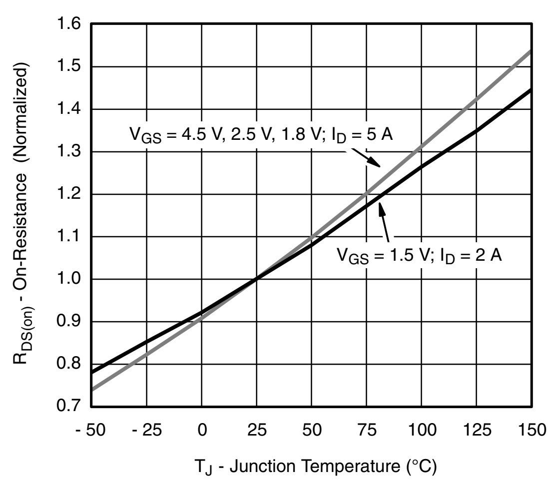
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

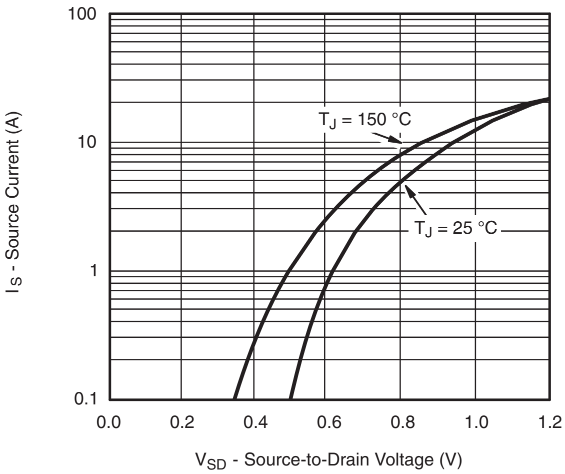


Gate Charge

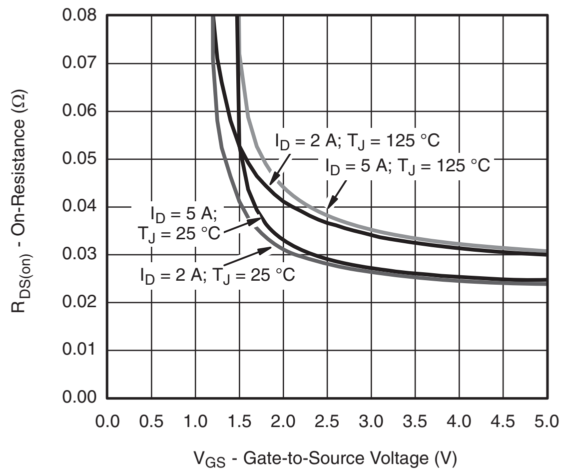


On-Resistance vs. Junction Temperature

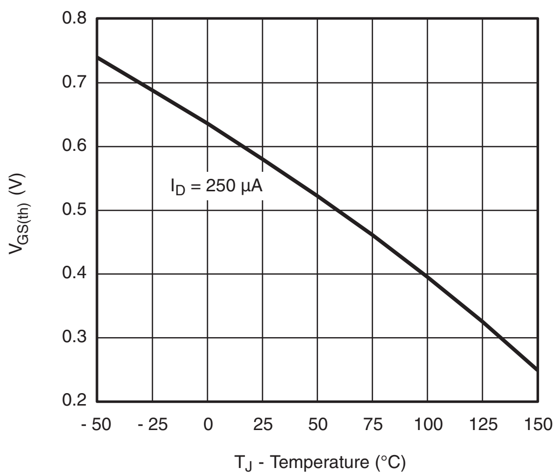
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



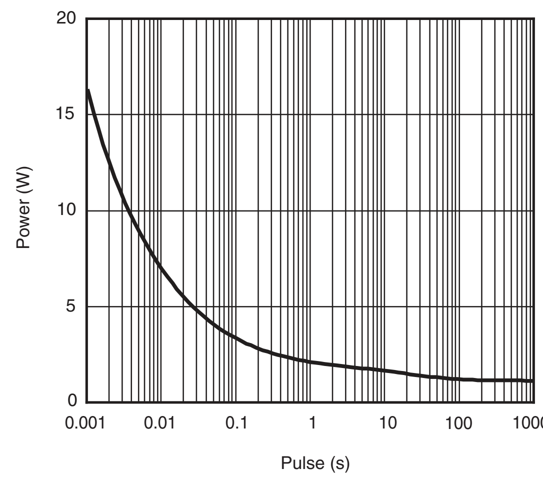
Source-Drain Diode Forward Voltage



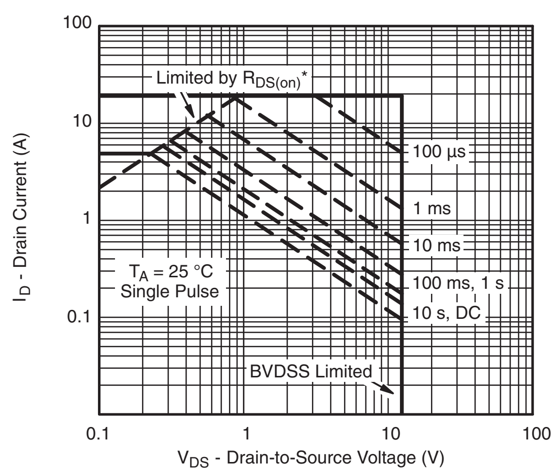
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



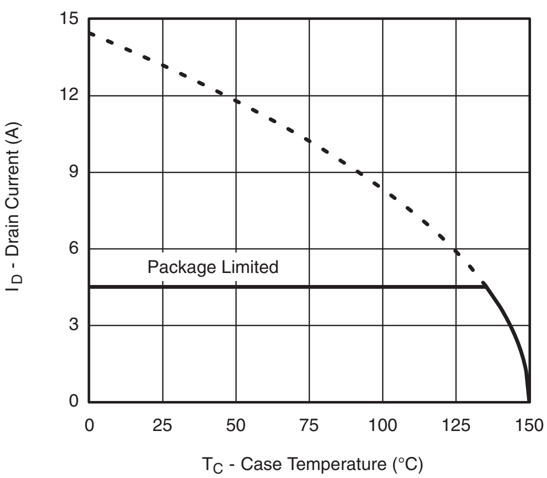
Single Pulse Power (Junction-to-Ambient)



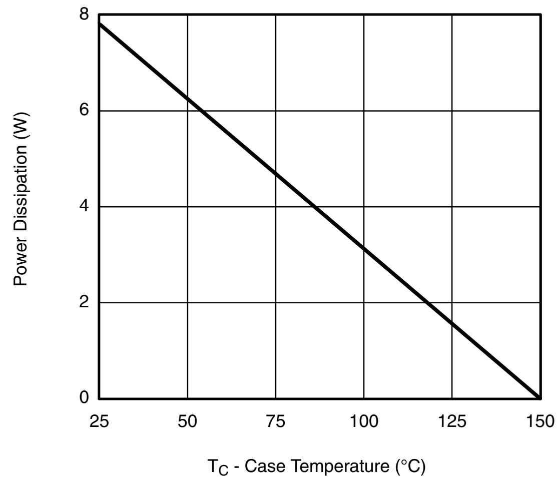
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



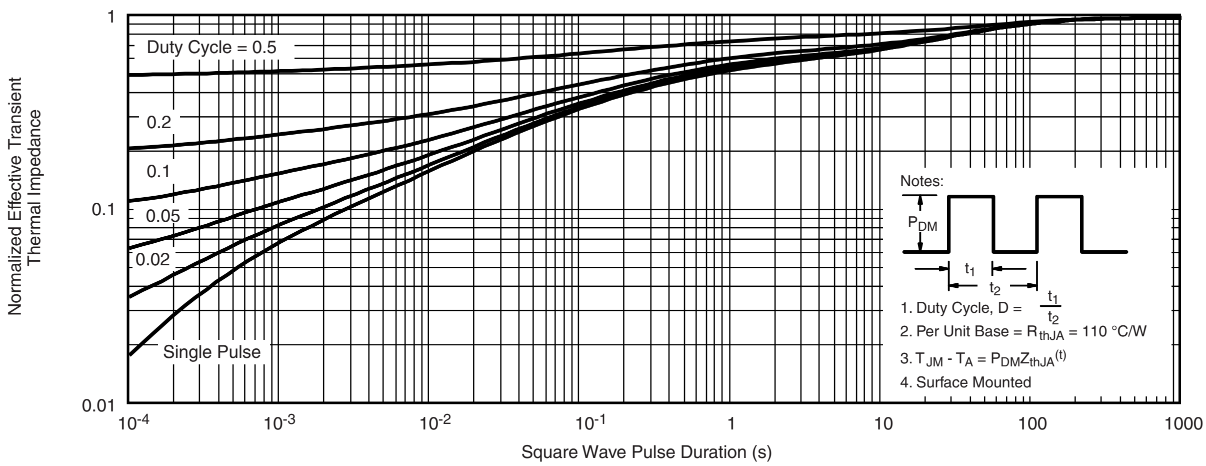
Current Derating*



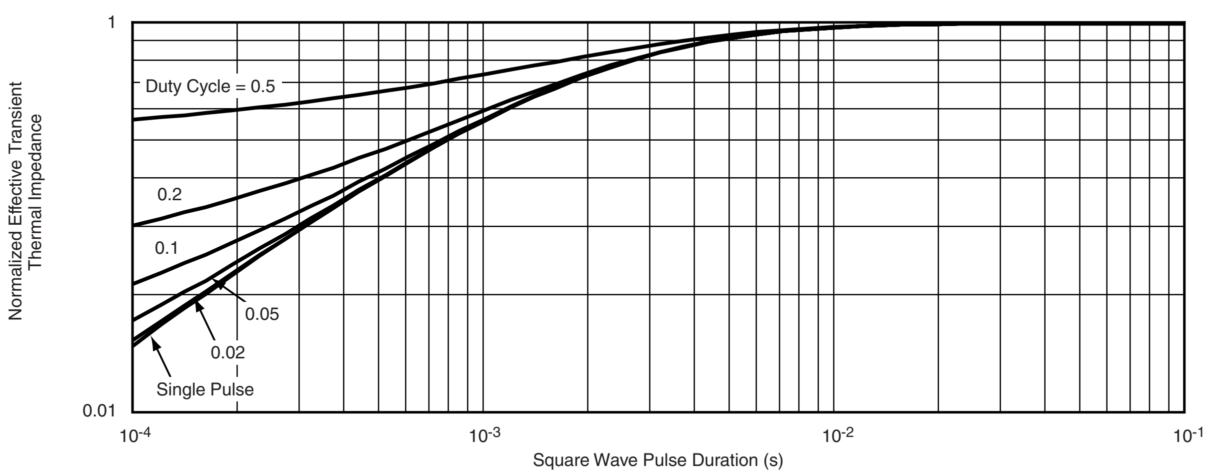
Power Derating

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

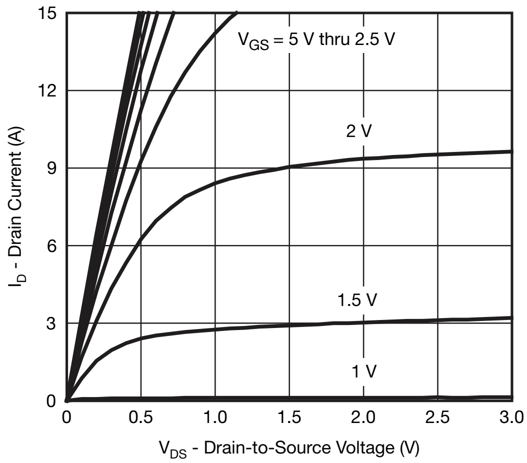


Normalized Thermal Transient Impedance, Junction-to-Ambient

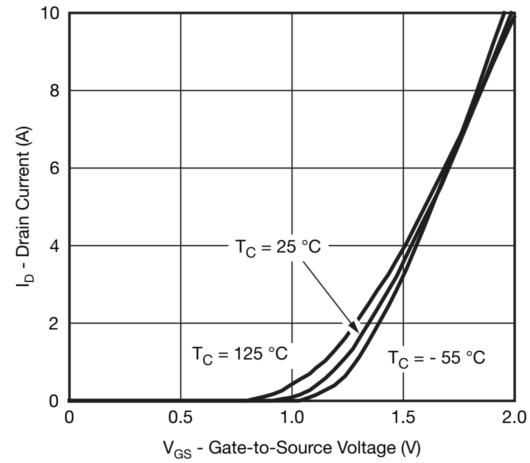


Normalized Thermal Transient Impedance, Junction-to-Case

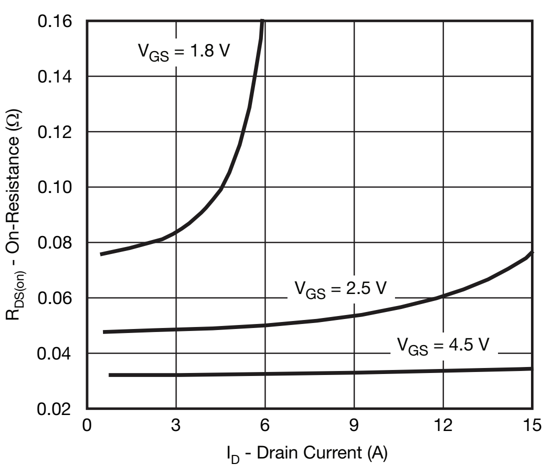
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



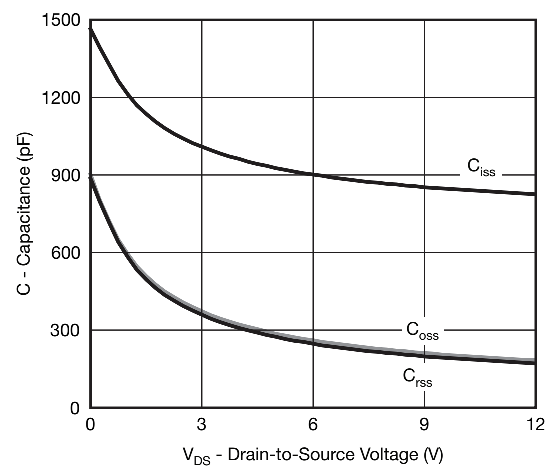
Output Characteristics



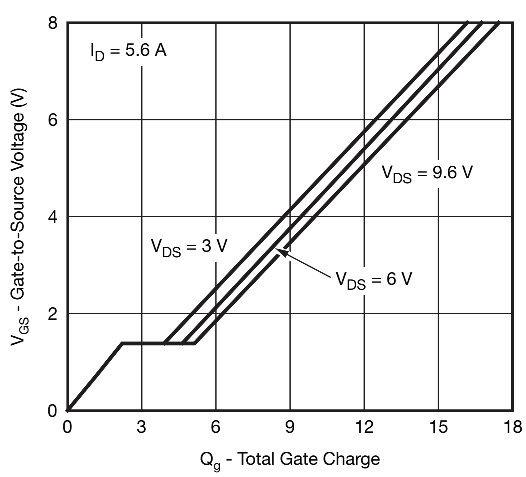
Transfer Characteristics



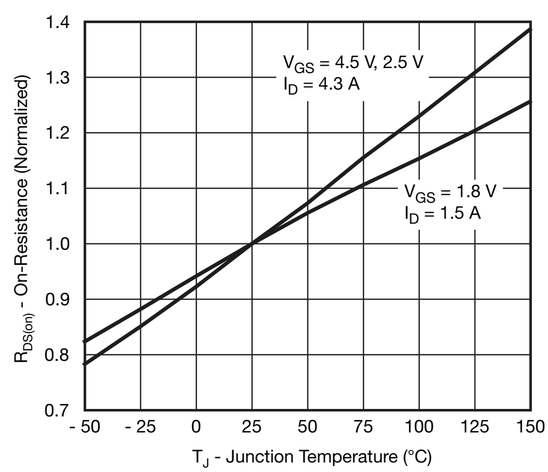
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

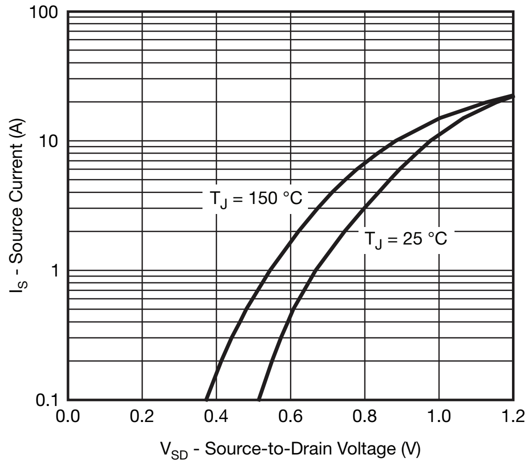


Gate Charge

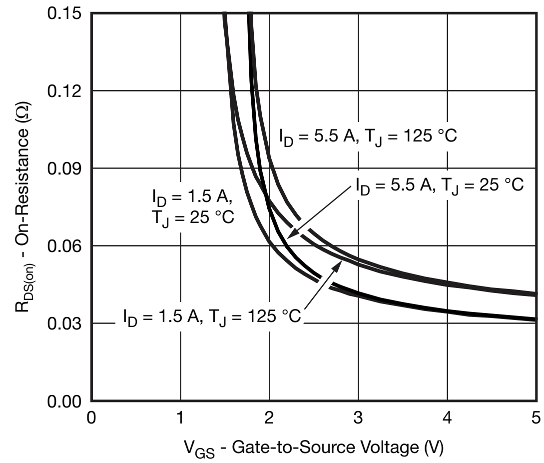


On-Resistance vs. Junction Temperature

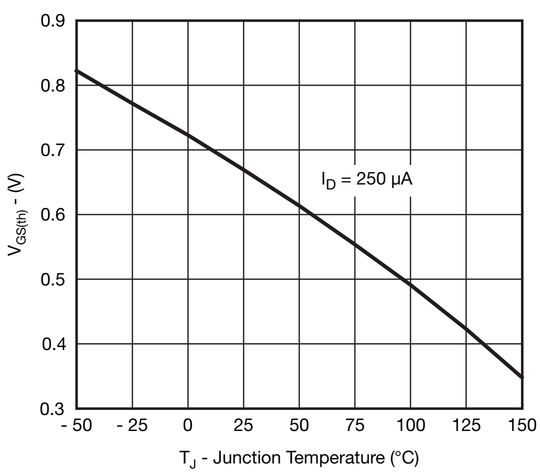
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



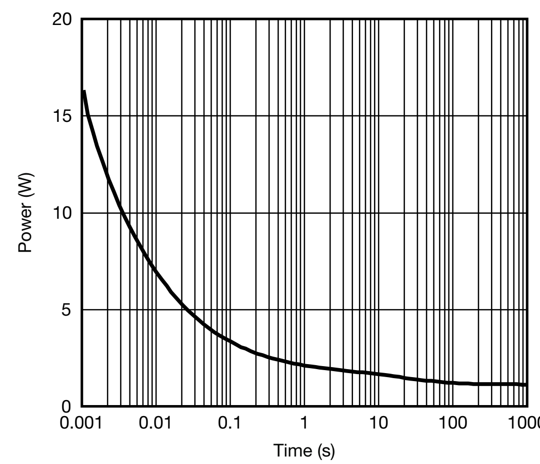
Soure-Drain Diode Forward Voltage



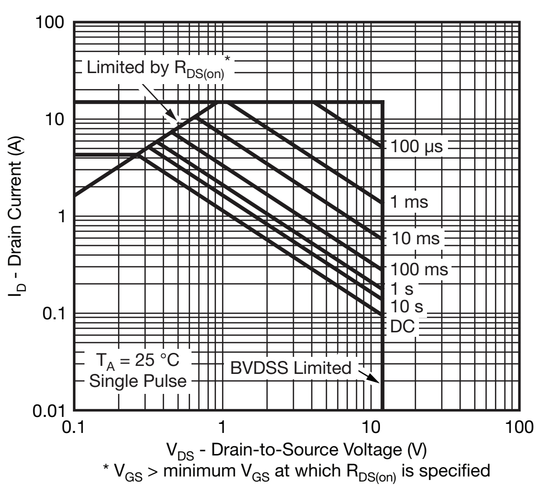
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

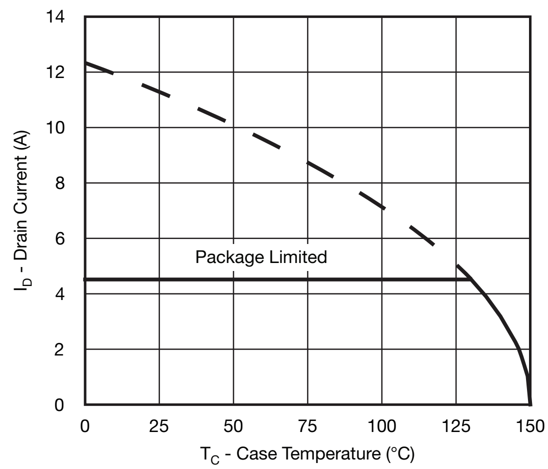


Single Pulse Power, Junction-to-Ambient

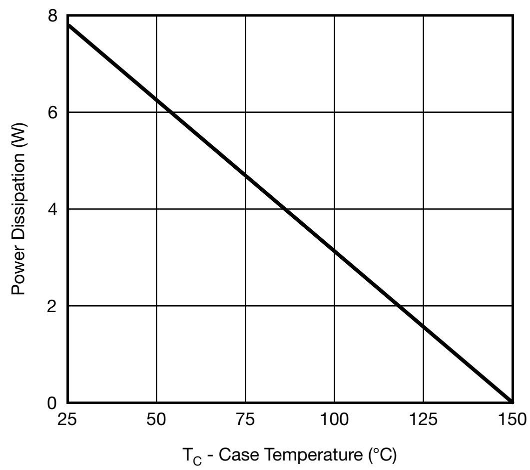


Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



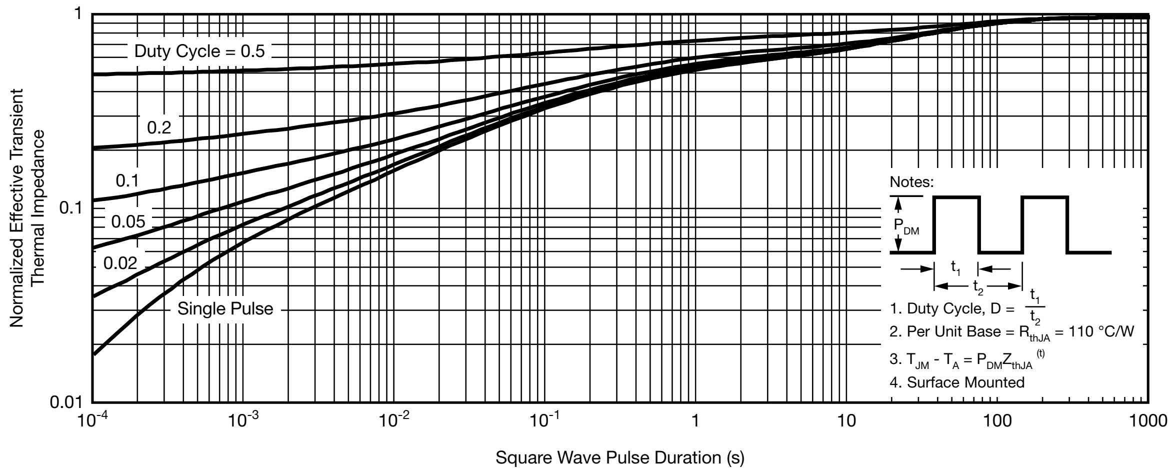
Current Derating*



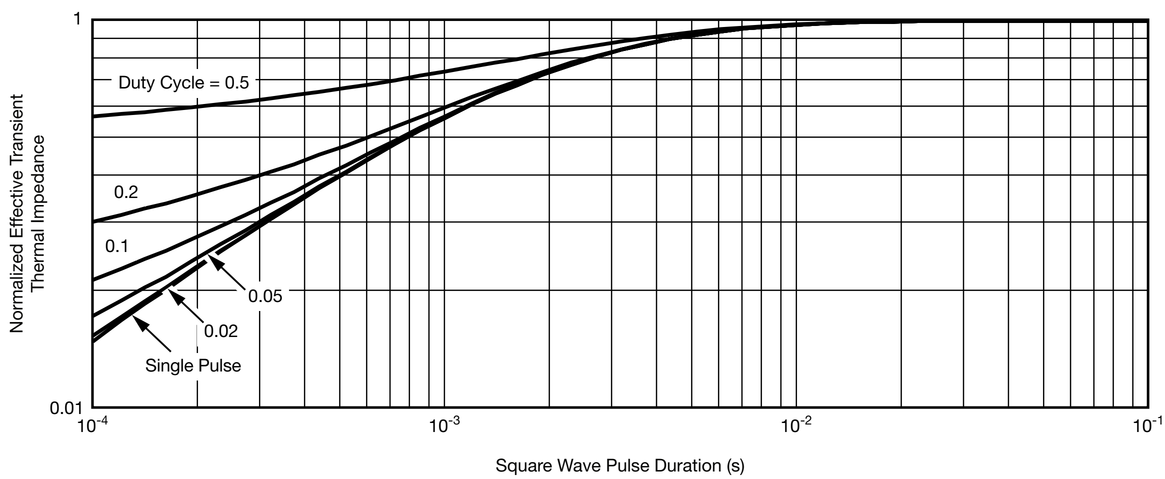
Power Derating

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



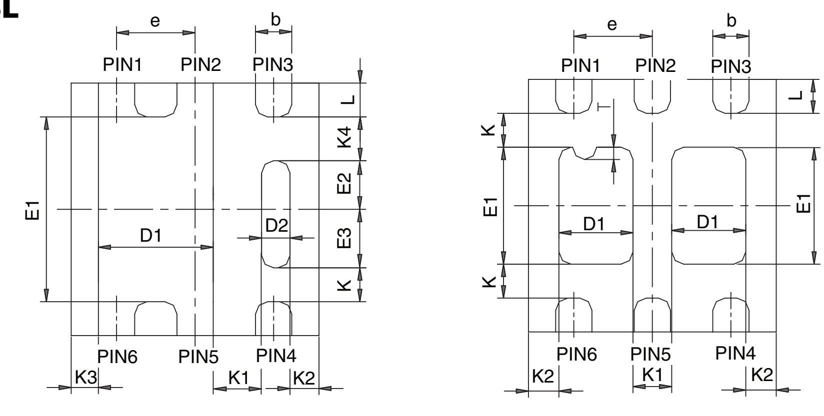
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

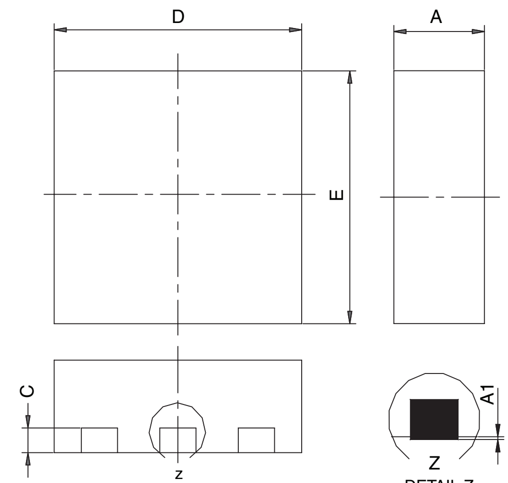
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?64162.

PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



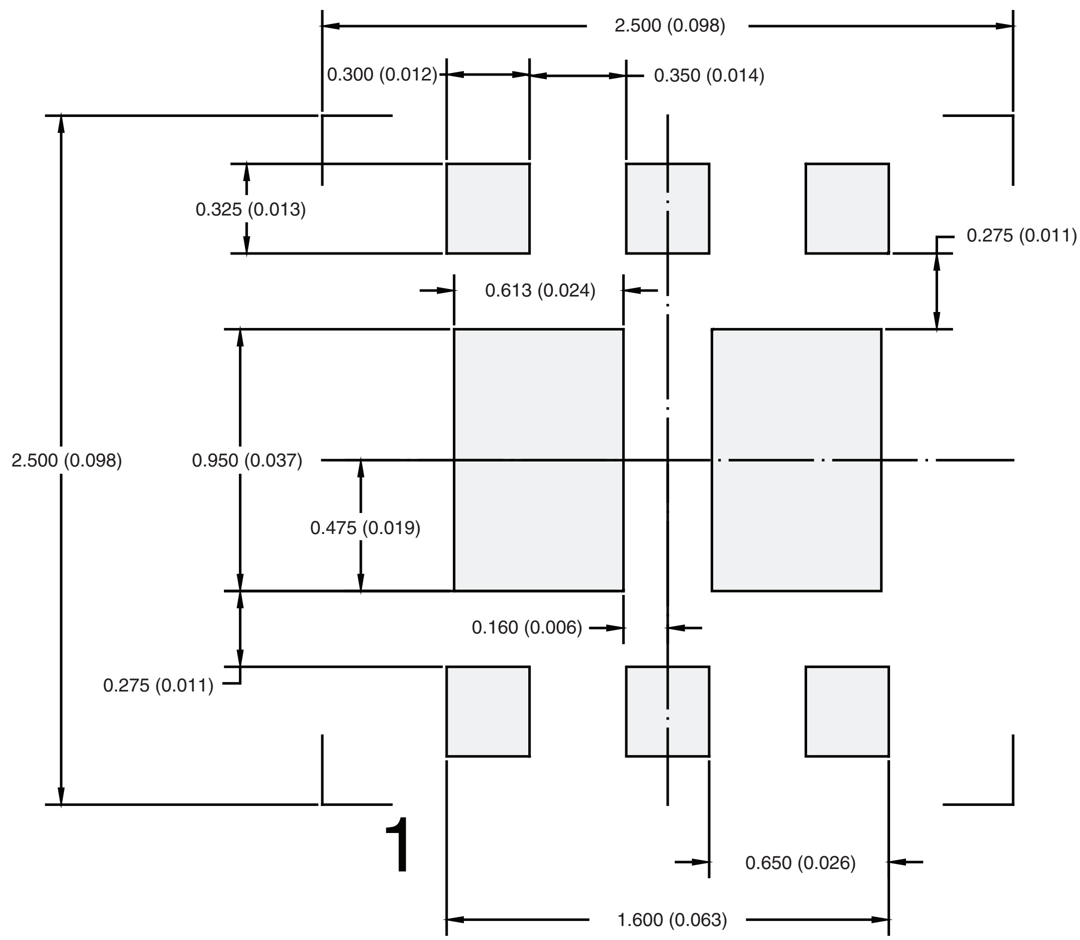
DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 − Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

Return to Index

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