8 Megapixel machine vision CMOS image sensor

Datasheet

Change record

Issue	Date	Modification
v1	13/12/2013	Origination
v1.1	12/05/2014	Added: - Descriptions for using the internal PLL - Warning about “channel_en” register, bit[3] should never be set to 1 - Pin list now lists the cap value for pins that need decoupling - VDDPLL should be connected to VDD18 - Values for programming the tmuxd1 and tmuxd2 registers - Recommended settings for registers are now listed in the overview and in Chapter 5.14 - Note: only the black reference columns on the left side should be used for row noise correction. - Registers in Chapter 5 now include their bit locations - Note about SPI clock in write operation: should have a final falling edge - New figures for angular response, spectral response and response curve Updated: - Spec sheet is now in accordance to test results - Power figures are now more accurate - Operating range is now -30°C to 70°C - For 12bit mode, all output channel modes are now listed - Corrected “slopes” register, is now 2bits long - Pin list is now sorted more logically - TDIG1/2 pins were wrongly listed as inputs - VRST_H was wrongly listed as a bias pin - Vres_h supply is renamed to VRST_H, to be consistent with the pin name - CMDP_ADC pin is renamed to CMDP_COMP - Settling time after sensor start-up is now more accurate - Necessary settings for 12bit are expanded - Overview in Chapter 4.4.5 now correctly lists disabled channels - Description for changing the output mode expanded - Minimum exposure time is now calculated with recommended settings Removed: - Names for registers that are of no use to users

Issue	Date	Modification
v1.2	28/08/2015	Updated to reflect engineering sample status Added: - Note saying that DVAL falling edge is one pixel period sooner than LVAL and FVAL - Description and pattern of column test mode - Specification for AR-coated D263 glass, this is the only version offered. - Note on avoiding excessive light - Engineering Status watermark, part numbers and description - ESD spec - RoHS/REACH status is to be confirmed - Baking condition added to Soldering chapter - Reference to defect specification Update: - Pin list was missing two pins - Dual integration mode register had the wrong address - Interleaved read-out works with columns, not rows - Training pattern description now correctly makes distinction between TP1 and TP2 - Dummy register recommendation is now “0” - MCLK signal is not needed for temperature sensor read out - New formula correctly calculates the exposure time, with updated minimum time - Default value for register 40 was wrong, it’s now “4” - SPI read now makes the distinction that SPI_OUT should be read on the rising edge only for fast SPI_CLK signals. - Frame rate calculation is updated using the new FOT formula - ADC gain doesn’t change with clock speed - Evaluation kit description - All specification values are typical, not minimum/maximum - Recommended VDD18 voltage is 1.98V - Reflow soldering profile is corrected - Register 90 default value was incorrect - 12bit mode setting now doesn’t require the 78[0] and 78[1] registers to be enabled Removed: - 1-channel mode: not supported on device - Wave soldering profile, was not recommended - Use of on-chip PLL, too unreliable - Confidentiality notice in footer

Disclaimer

CMOSIS reserves the right to change the product, specification and other information contained in this document without notice. Although CMOSIS does its best efforts to provide correct information, this is not warranted.

Table of Contents

1 INTRODUCTION

1.1 OVERVIEW

The CMV8000 is a high speed CMOS image sensor developed for machine vision and traffic applications, with 3360 by 2496 active pixels. The image array consists of 5.5µm by 5.5µm pipelined global shutter pixels which allow exposure during read-out, while performing CDS operation. The image data is read out serially through 16 LVDS channels, with 10 or 12 bit resolution. The sensor also integrates a programmable gain amplifier and offset regulation. Each LVDS output channel runs at 600 Mbps maximum which results in a frame rate of 103FPS at full image resolution with 10 bit color. Higher frame rates are possible when reading out a smaller frame or when subsampling is enabled. These modes are all programmable using the SPI interface. All internal exposure and read-out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- Capability to define up to 8 different windows
- Horizontal and vertical mirroring function
- Multiplexable output channels: 16, 8, 4 or 2 channel output possible
- LVDS control channel with read-out and frame information
- DDR LVDS output clock to sample data on the receiving end
- Selectable ADC Resolution: choose between maximum frame rate (10bit) or better image quality (12bit)
- Multiple High Dynamic Range options
- On-chip temperature sensor
- On-chip timing generation
- Sensor controllable via SPI-interface
- Available as panchromatic or with RGB Bayer-filter

1.3 SPECIFICATIONS

- Full well charge: 11.7Ke$^-$
- Sensitivity: 5.56V/lux.s (with microlenses @ 550nm)
- Dark noise: 8.6e$^-$ RMS
- Conversion gain: 0.077DN/e$^-$ (in 10bit mode) at unity gain
- Dynamic range: 61dB
- Parasitic light sensitivity: 1/20000
- Dark current: 41.2e$^-$/s (@ 25°C die temp)
- Fixed pattern noise: < 1LSB (in 10bit mode, < 0.1% of full swing, standard deviation on full image)
- Power consumption: 1200mW
- 3.3V signaling
- 3360 * 2496 active pixels on a 5.5µm pitch
- Maximum frame rate of 103FPS
- LVDS output clock of 125 to 300MHz
- Ceramic µPGA package (107 pins)

1.4 CONNECTION DIAGRAM

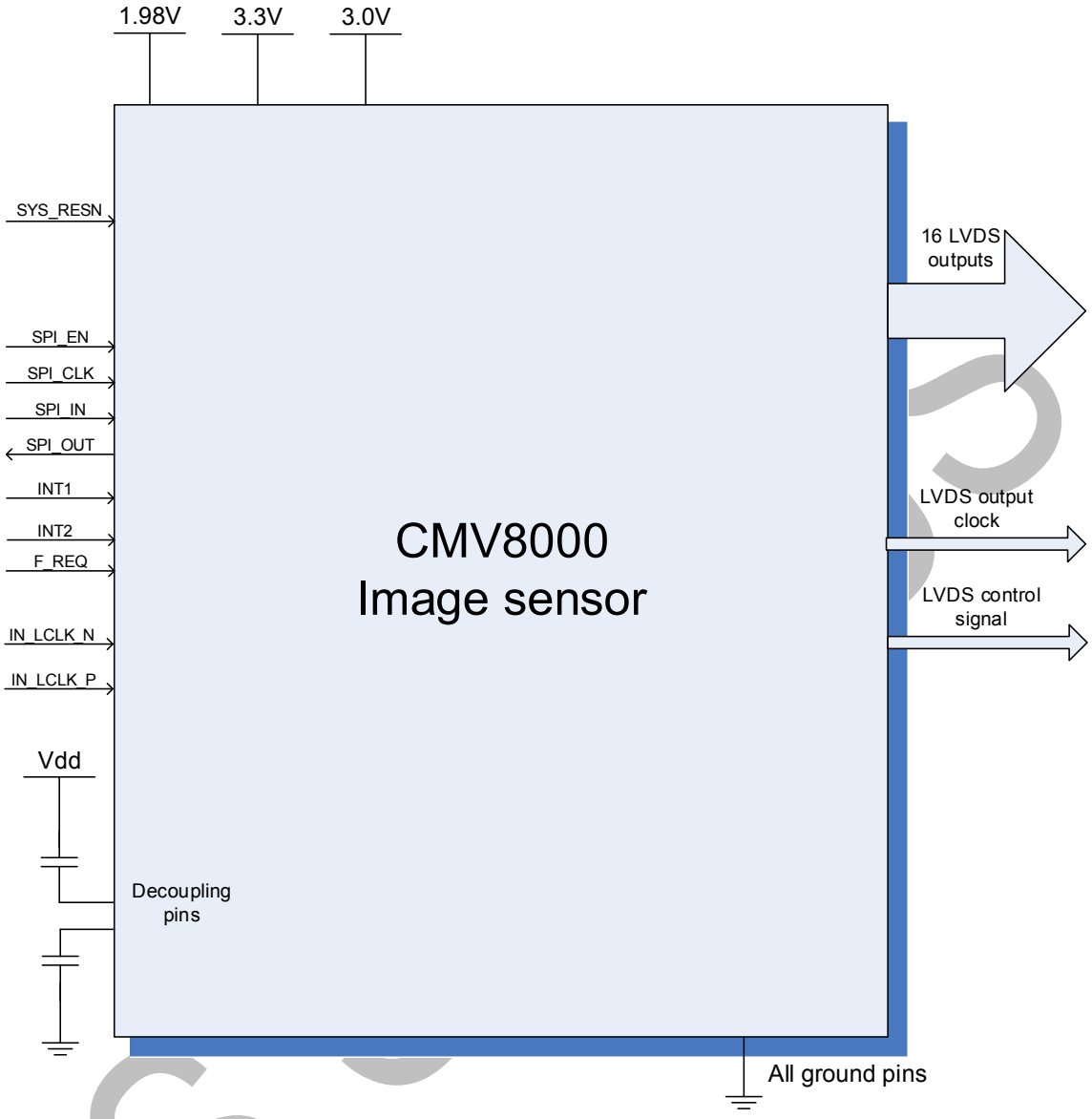

Figure 1: Sensor Connection diagram

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list in Chapter 11 and on the package drawing. The sensor has a default configuration on start-up that enables output over all 16 data channels, and uses 10 bits per pixel.

2 SENSOR ARCHITECTURE

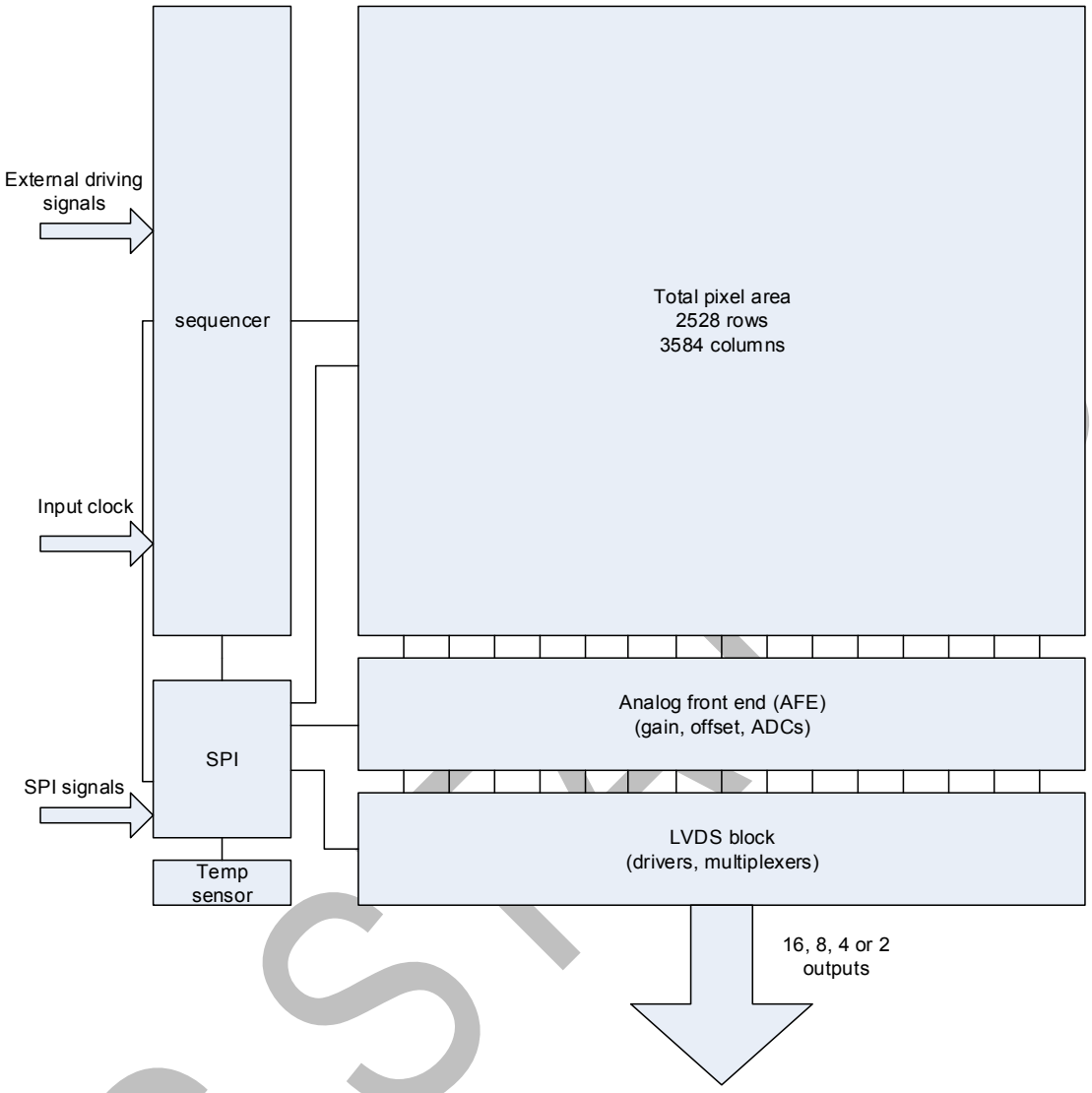

Figure 2: Sensor block diagram

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and is then read out sequentially, row-by-row. On the pixel output, an analog gain can be applied. The pixel values then pass through a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. In 16 channel mode, each LVDS channel reads out 224 adjacent columns of the array in bursts of 112 pixels to form a row of 3584 pixels, or 2*112*16. See Chapter 4.3 for more details. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface, visible in Figure 1. A temperature sensor, which can be read out over the SPI interface, is also included.

2.1 PIXEL ARRAY

The total pixel array consists of 3584 by 2528 pixels, each with a surface of 5.5µm by 5.5µm. As shown in the figure below, the outermost rows and columns black reference pixels and don't contain image data. These pixels will thus not contribute to the total image resolution, but they are still read out by the sensor to compensate for row and column noise. In total, there are 224 black reference columns (112 on each side) and 32 black reference rows at the top and bottom of the array. The maximum image resolution is thus 3360 by 2496 pixels, or 8.38 megapixel.

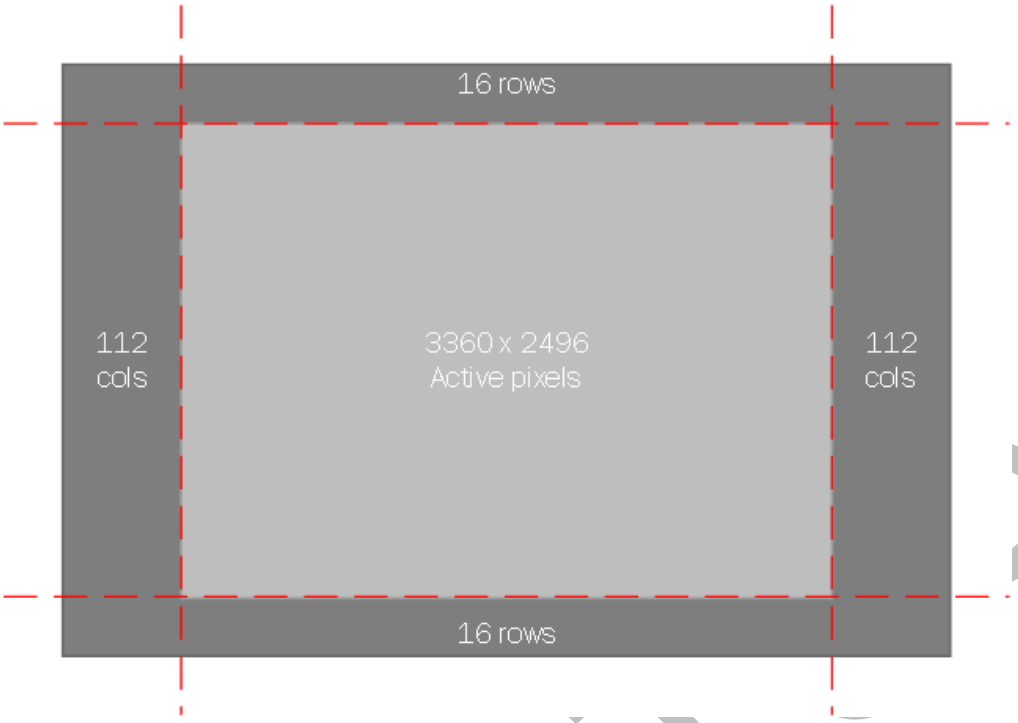

Figure 3 Physical layout of the active pixel array and black reference pixel

To assure that the dark reference rows are always read out first by the sequencer, these rows are assigned the 32 lowest logical addresses. When the image is mirrored in the Y-direction, the black reference rows will still be read out first, from row31 to row0, followed by the active pixels on row32 to row2527. In the image below, the pixel array is plotted according to the logical addresses, instead of the physical location.

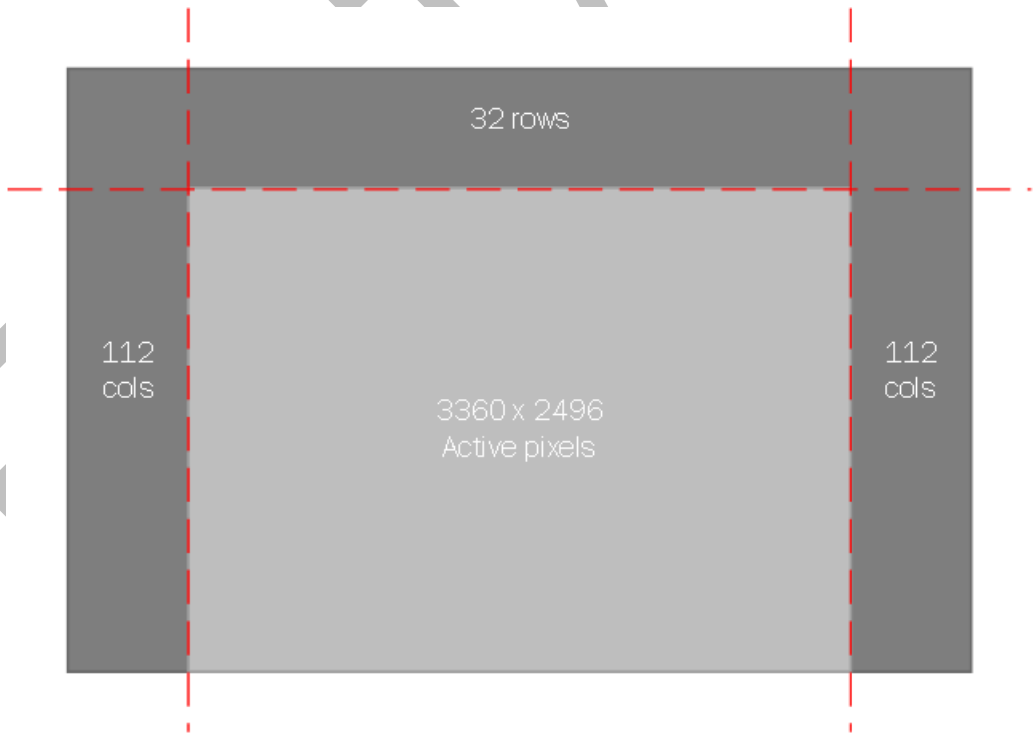

Figure 4 Logical organization of the pixel array

The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Microlenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%). When the black reference columns are used for row noise correction, it is best to only use the 112 reference columns to the left of the active pixel array.

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts: a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface).

The column ADC converts the analog pixel value to a 10 or 12 bit value. A digital offset can also be applied to the output of the column ADC's. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 600Mbps. The sensor has 18 LVDS output pairs:

- 16 Data channels
- 1 Control channel
- 1 Clock channel

The 16 data channels are used to transfer 10-bit or 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing can be found in Chapter 4.

LVDS requires parallel termination at the receiver side. So between IN_LCLK_P (pin T1) and IN_LCLK_N (pin U2) should be an external 100Ω resistor. Also all the LVDS outputs should all be externally terminated at the receiver side. See the TIA/EIA-644A standard for more details.

2.4 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface. A detailed description of the sensor (sequencer) programming can be found in Chapter 5 of this document.

2.5 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Chapter 3.9 contains more details on register programming and SPI timing.

2.6 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out the registers with address 88 and 89 (in burst mode, see Chapter 0 for more details on this mode).

A calibration of the temperature sensor is needed for absolute temperature measurements per device because the offset differs from device to device. The temperature sensor requires a running input clock and the other functions of the image sensor can be operational or in standby mode. The output value of the sensor is dependent on the input clock. A typical temperature sensor output vs. temperature curve at 200MHz can be found below. In most cases, the die temperature will be about 10°C to 15°C higher than ambient temperature. The ceramic package has about the same temperature as the die.

The typical offset value of the temperature sensor at 0°C is: $1000 \times \frac{f\,[MHz]}{200}$DN. This offset can differ per device. A typical slope would be around $0.3 \times \frac{200}{f[MHz]}$°C/DN.

For example, during the calibration of the temperature sensor, the register has the value of 1066 at 35°C and an input frequency of 200MHz. If after this the temperature rises and the value increases to 1184, the die temperature can be calculated back from that.

$$\left((1184 - 1066) \times 0.3 \times \frac{200}{200\text{MHz}}\right) + 35\text{°C} = 70.4\text{°C}$$

Or vice versa, if you want to know the temperature register value for a die temperature of -10°C at 200MHz:

$$\left((-10\text{°C} - 35\text{°C}) \times \frac{200\text{MHz}}{200} \times \frac{1}{0.3}\right) + 1066\text{DN} = 916\text{DN}$$

A more accurate calibration can be done by reading out the sensor at multiple temperatures, to determine the exact slope. For most devices this should be around 0.29 to 0.31.

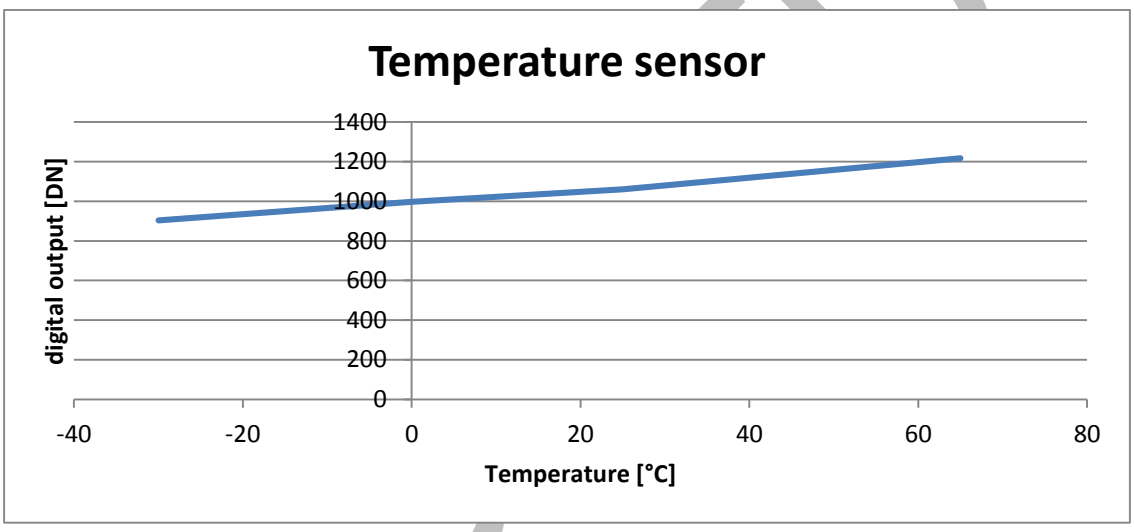

Figure 5: Typical output of the temperature sensor on the CMV8000

3 DRIVING THE CMV8000

3.1 SUPPLY SETTINGS

The CMV8000 image sensor has the following supply settings:

Supply name	Usage	Recommended value [V]	Range [V]	DC Power nominal [mW]	DC Current nominal [mA]	DC Current peak [mA]
VDD18	Digital blocks	1.98	1.8 – 1.98	740	410	410
VDD33	Sensitive analog blocks	3.3	3.0 - 3.6	415	125	125
VDDPIX	Pixel array power supply	3.0	2.3 - 3.6	60	20	150
VRST_H	Pixel reset pulse	3.3	3.0 - 3.6	1	0.3	50

See Chapter 11 for the exact pin numbers for every supply. Analog and digital ground can be tied together.

All variations on the VDD33 and VDDPIX can contribute to variations (noise) on the analog pixel signal, which is seen as noise in the image. During the camera design, precautions have to be taken to supply the sensor with very stable supply voltages to avoid this additional noise.

Because of the peak currents, decoupling is advised. Place large decoupling capacitors directly at the output of the voltage regulator to filter low noise and improve peak current supply. We advise 1x 330µF electrolytic, 1x 33µF tantalum and a 10µF ceramic capacitor per supply, directly at the output of the regulator.

Place small decoupling capacitors as close as possible to the sensor between supply pins and ground. We advise 1x 4.7µF and 1x 100nF ceramic capacitor per power supply pin and 1x 100µF ceramic capacitor per power supply plane (VDD18, VDDPIX, VDD33). VRST_H doesn't need a 100µF capacitor.

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor. The digital signals are sampled on the rising edge of the LVDS input clock. Therefore, when applied to an input, all of these signals should last at least 1 clock cycle to assure it has been detected. All digital I/O's have a capacitance of 2pF max.

Pin name	Description
IN_LCLK_N/P	High speed LVDS input clock, frequency range between 125 and 300 MHz
SYS_RESN	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up.
F_REQ	Frame request pin. When a rising edge is detected on this pin the programmed number of frames is captured and sent by the sensor.
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 60 MHz)
INT1	Input pin which can be used to program the exposure time externally. Optional
INT2	Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. Optional

3.4 ELECTRICAL I/O SPECIFICATIONS

3.4.1 DIGITAL I/O CMOS/TTL DC SPECIFICATIONS

See pin list for specific pins.

Parameter	Description	Conditions	min	typical	max	Units
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3V I_{OH}=-2mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3V I_{OL}=2mA			0.4	V

3.4.2 TIA/EIA-644A[1] LVDS DRIVER SPECIFICATIONS

Specifications for all output LVDS channels: OUTx_N/P, OUT_CLK_N/P and OUT_CTR_N/P.

Parameter	Description	Conditions	Min	typical	max	Units
V_{OD}	Differential output voltage	Steady State, RL = 100Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100Ω			50	mV
V_{OC}	Common mode voltage	Steady State, RL = 100Ω	1.26	1.37	1. 50	V
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

3.4.3 TIA/EIA-644A LVDS RECEIVER SPECIFICATIONS

Specifications for LVDS input clock IN_LCLK_N/P.

Parameter	Description	Conditions	min	typical	max	Units
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2V±50mV, 0≤ $V_{INP\|INN}$≤2.4V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

[1] V_{oc} is dependent on the 1.98V supply voltage, therefore these values differ from the TIA/EIA-644A spec.

3.5 INPUT CLOCK

A high speed LVDS clock has to be provided to drive the sensor. The speed of the output clock on which the pixel data can be sampled, will be equal to the speed of the input clock.

The speed of the input clock determines the data rate at the output. The maximum output clock speed is 300MHz. This puts the maximum data rate at 600Mbps, as the sensor has a DDR output clock. The minimum frequency for the IN_LCLK_N/P clock is 125MHz. Any frequency between the upper and lower limit can be applied by the user and will result in a corresponding output data rate. The following table displays the necessary clock speeds for a couple of data rates.

Range	IN_LCLK [MHz]	Data rate [Mbps]
Min	125	250
	150	300
Max	300	600

Note: Whenever the clock speed is changed, the clock gating register 123[0] always needs to be set to '1', before adjusting the clock speed. After the changes are made, register 123[0] can be set back to '0'.

3.6 FRAME RATE CALCULATION

The frame rate is defined by 2 main factors.

1. Exposure time
2. Read-out time

To simplify the calculation, we will assume that the exposure time is shorter than the read-out time and that the sensor is operating at default settings, taking a full resolution (3584 by 2528 pixels) 10-bit image at 600Mbps through 16 channels. This means that the frame rate will be defined only by the read-out time because the exposure happens in parallel with the read-out time. The read-out time is defined by:

1. Output clock speed: max 300MHz
2. ADC mode: 10 or 12 bit
3. Number of lines read-out
4. Number of LVDS outputs used: max 16 outputs

If any of these parameters are changed, it will have an impact on the frame rate. In default operation this will result in 104FPS. The total read-out time is composed of two parts: the frame overhead time (FOT) and the image read-out time.

The FOT is defined as:

$$FOT = \frac{\#bits}{2} \times T \times (224 \times \text{FOT\_LENGTH} + 1 + 112 + 2 \times 113 \times \frac{32}{\#\ outputs})$$

Where FOT_LENGTH is the value of the register, and T is the period of the input clock. With register FOT_LENGTH set to its recommended value of 50 and a clock speed of 300MHz, this results in 196.08µs frame overhead time.

The image read-out time is defined as:

$$Image\ readout\ time = ((\text{SLOT\_LENGTH} + 1) \times \frac{\#bits}{2} \times T \times \frac{32}{\#outputs}) \times \text{YSIZE\_TOT}$$

Where SLOT_LENGTH and YSIZE_TOT are the register values, and T is the period of the input clock. When reading out a full resolution image of 2528 lines in 10-bit mode with the recommended settings, this results in 9522.13µs of image read-out time.

The total read-out time is now the sum of the FOT and the image read-out time, which results in 196.08µs + 9522.13µs = 9718µs to read out a single full resolution image. The frame rate is thus 102.9FPS.

The table below gives some examples of how the frame rate increases when reading out a smaller frame in 10-bit mode.

Number of columns	Number of lines	Frame rate [FPS] fot_length = 50	Frame rate [FPS] fot_length = 40
3584	2528 (full frame)	103	103
3584	2496 (only active rows)	104	104
3584	1264 (half frame)	202	203
3584	100	1746	1868

In 12bit mode, these formulas are different. Here, FOT is defined as:

$$FOT = \frac{\#bits}{2} \times T \times (224 \times \text{FOT\_LENGTH} + 1 + 112 + 4 \times 125 \times \frac{32}{\#\ outputs})$$

And the read-out time is defined as:

$$Image\ readout\ time = (2 \times (\text{SLOT\_LENGTH} + 1) \times \frac{\#bits}{2} \times T \times \frac{32}{\#outputs}) \times \text{YSIZE\_TOT}$$

This leads to a reduced frame rate of 40FPS.

When the exposure time is longer than the read-out time, the frame rate is mostly defined by the exposure time itself because the exposure time would be much longer than the FOT.

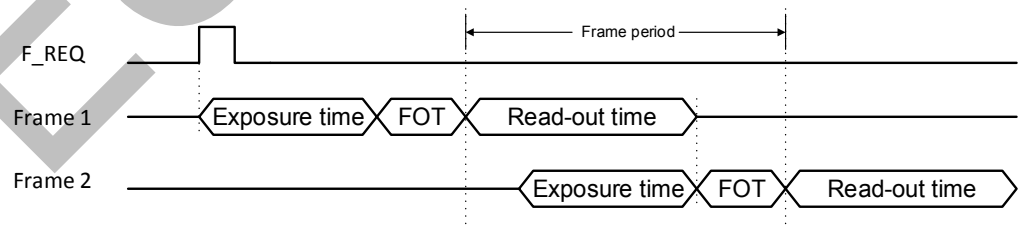

Figure 6: Frame period

3.7 START-UP SEQUENCE

The following sequence should be followed when the CMV8000 is started up in default output mode (600Mbps, 10bit resolution). There is no specific startup sequence for the power supplies needed.

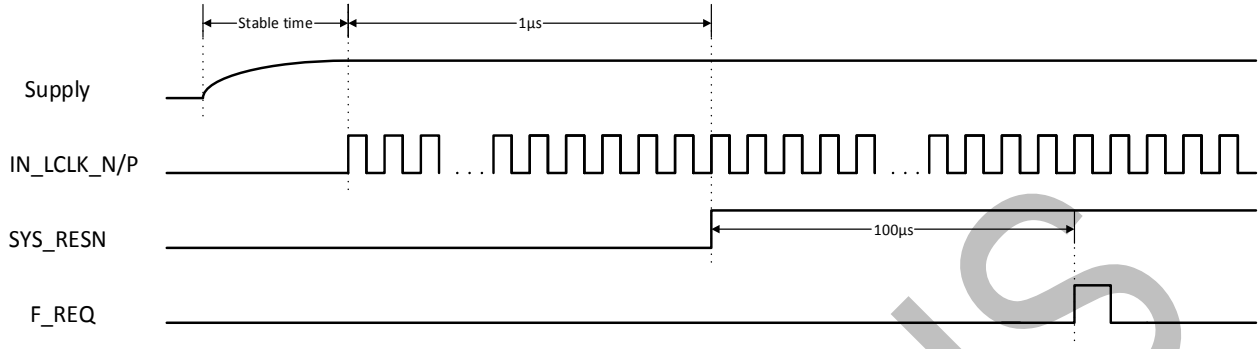

Figure 7: Start-up sequence for 600Mbps @ 10-bit

The input clock should start after the rise time of the supplies. The external reset pin should be released at least 1µs after the supplies are stable. The first frame can be requested 100µs after the reset pin has been released.

If the register settings need to be change (e.g. when using 12bit mode), this can be done through an SPI upload 100µs after the rising edge on the SYS_RESN pin, as described in Figure 8. In this case, the F_REQ pulse must not be sent until after the SPI upload is completed, plus a settling time. This settling time is to ensure that the changes programmed in the SPI upload have taken effect before an image is captured. The main factor that determines this settling time is a change in ADC gain, because the voltage over the ramp capacitor has to settle. For typical applications, where the ADC gain is changed from the default value of 32 to a value that saturates the ADC output (e.g. 39), the settling time is 8ms. In extreme cases, when the ADC gain would be increased to its maximum value of 63, the settling time can increase to 20ms.

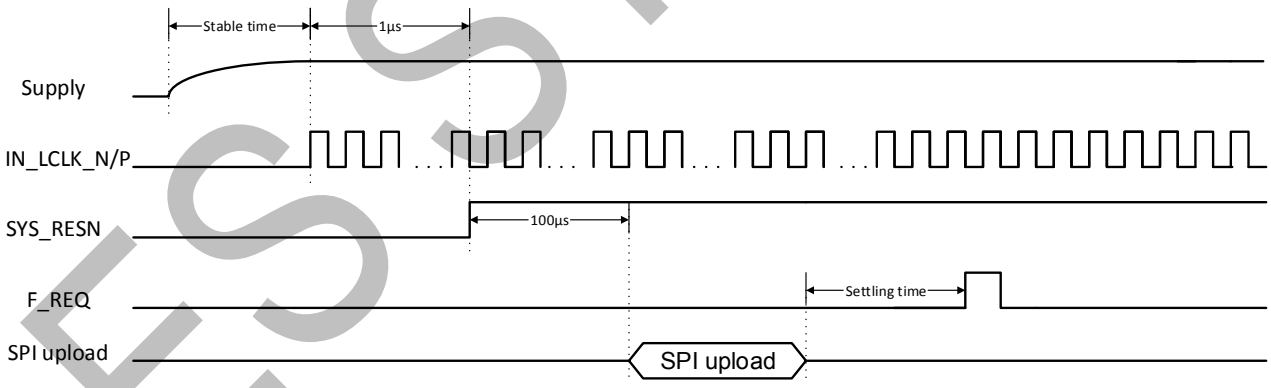

Figure 8: Start-up sequence for 12 bit mode

3.8 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running, the following sequence should be followed. The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RESN pin. After the reset there is a minimum time of 1µs needed before a F_REQ pulse can be sent.

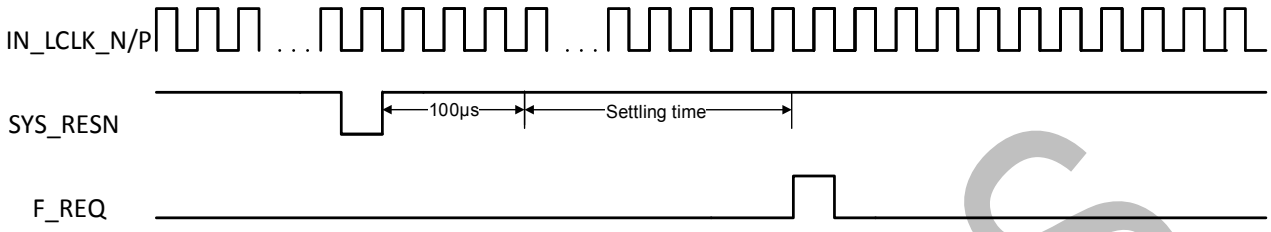

Figure 9: Reset sequence

When register settings are uploaded after the reset (e.g. when changing the bit mode), the following sequence should be followed.

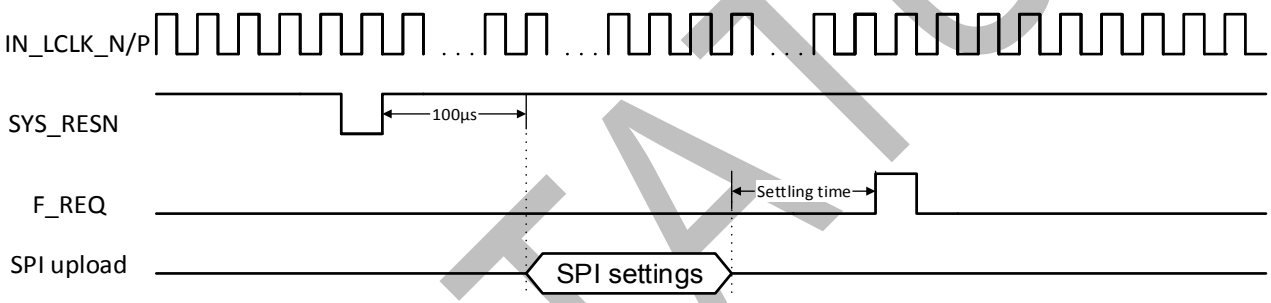

Figure 10: Reset sequence when changing bit mode

The details about how to program the sensor to change the bit mode can be found in Chapter5.10. As mentioned in Chapter 3.5, for a lower output data rate only the input clock need to be lowered.

3.9 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

3.9.1 SPI WRITE

The sensor samples the data on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 60MHz. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled and it has to remain high for 1 clock period after the last data bit is sent. SPI_EN has to remain high for 1 clock cycle and SPI_CLK has to receive a final falling edge to complete the write operation.

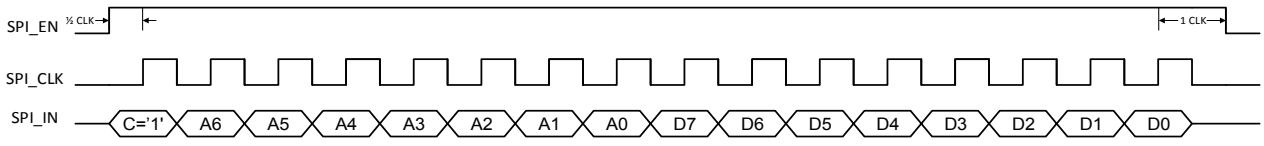

Figure 11: SPI write timing

One write action contains 16 bits in total:

- One control bit: First bit to be sent, indicates whether a read ('0') or write ('1') will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

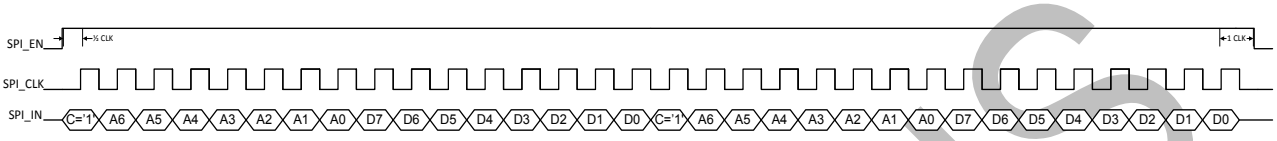

Figure 12: SPI write timing for 2 registers in burst

Most registers should be updated only during IDLE time. The sensor is not IDLE during a frame burst (between start of integration of first frame and read-out of last pixel of last frame).

Registers 35-38 (subsampling), 80 (ADC offset), 82[4:0] (ADC gain) and 118 (PGA gain) can be updated during IDLE or FOT. Registers 1 to 34 (windowing) and 54 (frames) can always be updated but it is recommended to update these during IDLE or FOT to minimize image effects. Registers 56-57 (LVDS training) can always be updated without disrupting the image process.

3.9.2 SPI READ

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin. For low-frequency clocks (< 30 MHz), the output can be sampled on the rising edge of the clock. For higher frequencies (up to 60 MHz), the data has to be sampled on the next falling edge. The data comes over the SPI_OUT with MSB first. When reading out the temperature sensor over the SPI, addresses 88 and 89 should be read out in burst mode (keep SPI_EN high).

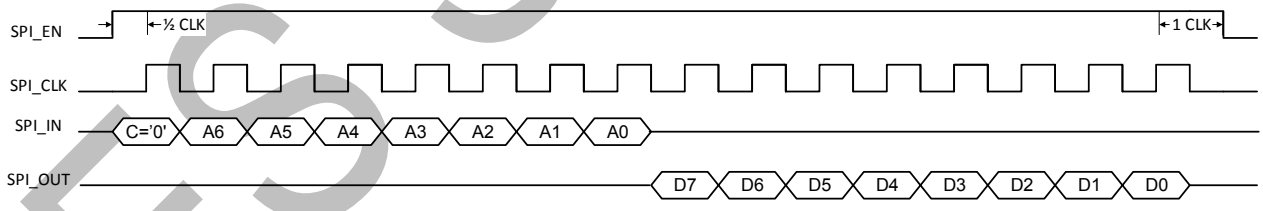

Figure 13: SPI read timing

3.10 REQUESTING A FRAME

After starting up the sensor (see 3.7), any number of frames can be requested by sending a F_REQ pulse. The number of frames can be set by programming the appropriate register (address 54). The default number of frames to be grabbed is 1.

In internal exposure mode, the exposure time will start after this F_REQ pulse. In the external exposure mode, the read-out will start after the F_REQ pulse. Both modes are explained into detail in the chapters below.

3.10.1 INTERNAL EXPOSURE CONTROL

In this mode, the exposure time is set by programming registers 41 to 43. After the high state of the F_REQ pulse is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the

pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one. See the diagram below for more details.

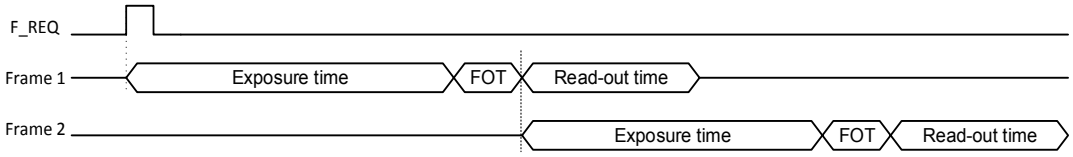

Figure 14: request for 2 frames in internal exposure mode

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame. Keep in mind that the next F_REQ pulse has to occur after the FOT of the current frame. For an exact calculation of the exposure time see Chapter 5.1.

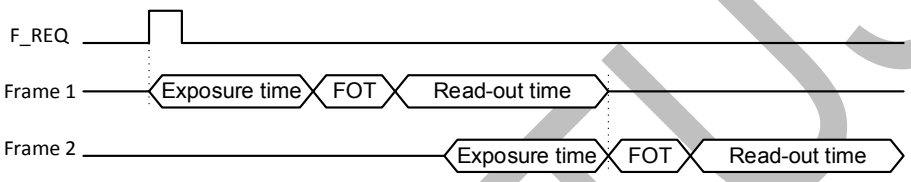

Figure 15: Request for 2 frames in internal exposure mode with exposure time < read-out time

If a next F_REQ pulse is applied during exposure time or FOT of the current frame, it will be ignored and no new frame is requested. A new frame request should occur during or after the read-out time of the current frame.

If the exposure time is shorter than the read-out time, keep in mind that when you apply a next F_REQ pulse during the read-out of the current frame, the exposure of that new frame will be delayed if necessary. When the next frame request is sent early in the read-out of the current frame, starting the exposure immediately would result in an overlap of the read-out time for two consecutive frames. To avoid this conflict, internally, the start of exposure is delayed so that the read-out of the current frame can finish and the read-out of the next frame can start immediately after. This is explained in the figure below.

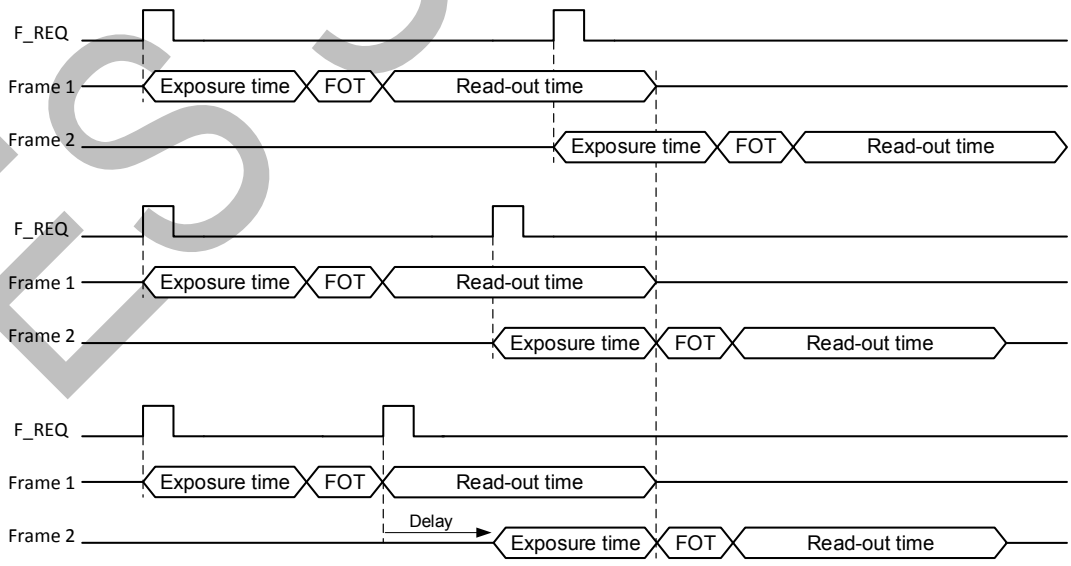

Figure 16: The timing effect of two requests for 1 frame in internal exposure mode

If the exposure time is longer than the read-out time, the start of exposure will never be delayed, because there is no chance of an overlap.

3.10.2 EXTERNAL EXPOSURE CONTROL

The exposure time can also be programmed externally by using the INT1 input pin. This mode needs to be enabled by setting the register 40[0]. In this case, the exposure starts when a high state is detected on the INT1 pin. When a high state is detected on the F_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the INT1 pin during or after the read-out of the previous frame. The minimum time between INT and F_REQ is 1 master clock cycle, the minimum time between F_REQ and INT1 pulse is FOT. For an exact calculation of the exposure time see Chapter 5.1.

Keep in mind that, if the exposure time is shorter than the read-out time, the F_REQ pulse should never be sent during the read-out time of the previous frame. Doing this will result in an incomplete frame read-out, as the sensor always starts the read-out immediately when a F_REQ edge is detected. This conflict between read-out times can be seen in the figure below as an incomplete read-out.

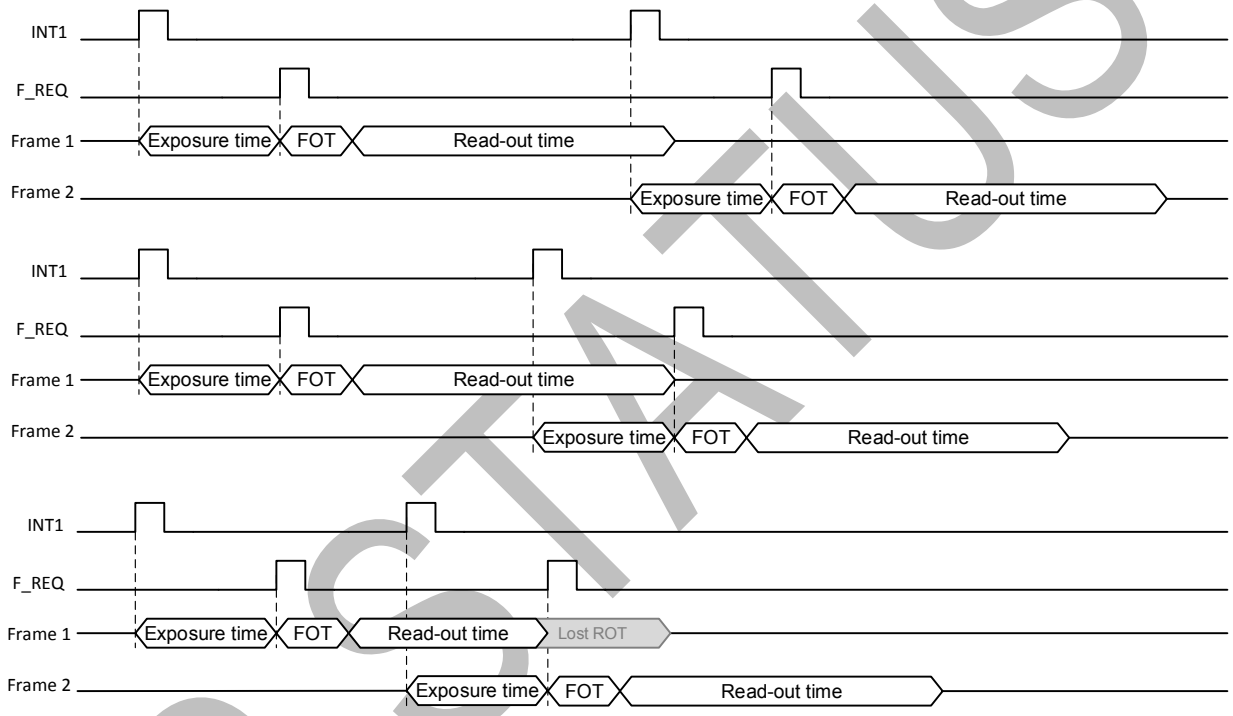

Figure 17: request for 2 frames using external exposure mode

In the interleaved read-out high-dynamic range mode, the INT2 input is used to control the exposure time of the odd columns.

4 READING OUT THE SENSOR

4.1 LVDS DATA OUTPUTS

The CMV8000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 16 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 18 LVDS output pairs (2 pins for each LVDS channel):

- 16 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 36 pins of the CMV8000 are used for the LVDS outputs (32 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs.

The 16 data channels are used to transfer the 10-bit or 12-bit pixel data from the sensor to the receiver in the surrounding system.

The output clock channel OUT_CLK transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the data rate will be double of the frequency. When 600Mbps output data rate is used, the LVDS output clock will be 300MHz.

The control channel contains status information of the data on the data channels. The data on the control channel is grouped in 10-bit or 12-bit words that are transferred synchronous to the 16 data channels.

4.2 LOW-LEVEL PIXEL TIMING

The figures below show the timing for the read-out of 10-bit and 12-bit pixel data over one LVDS output, together with the DDR output clock (OUT_CLK). To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the output clock.

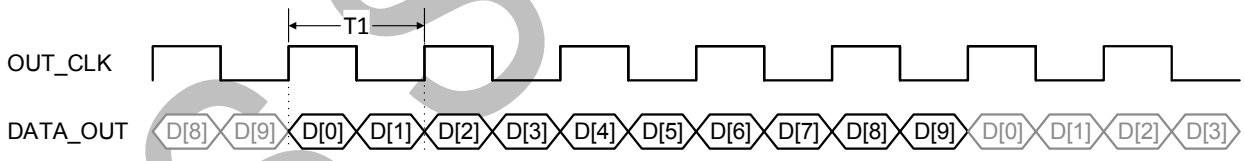

Figure 18: 10-bit pixel data on an LVDS channel

For 10-bit mode, the time 'T1' in Figure 18 will be equal to 1 clock cycle of the IN_LCLK input clock. When a frequency of 300MHz (max for 10bit mode) for IN_LCLK is used, this results in a 300MHz OUT_CLK.

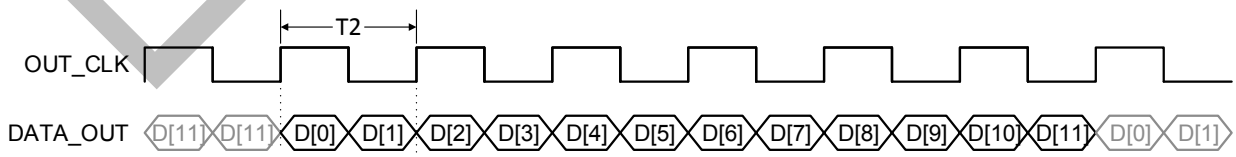

Figure 19: 12-bit pixel data on an LVDS channel

For 12-bit mode, the time 'T2' in Figure 19 will be equal to 1 clock cycle of the IN_LCLK input clock. When a frequency of 300MHz is used for IN_LCLK (max. in 12-bit mode), this results in a 300MHz OUT_CLK.

4.3 READ-OUT TIMING

The read-out of image data is always grouped in bursts of 112 pixels. Each pixel consists of 10 or 12 bits of data (see Chapter 4.2). For details on pixel remapping and pixel vs. channel location please see Chapter 4.4. Between every burst of 112 pixels, there is an overhead time that lasts for one pixel period.

Chapter 5.7 contains all the details about programming the sensor to use different output channels.

4.3.1 10 BIT MODE

In this section, the read-out timing for the default 10-bit mode is explained. In this mode the maximum frame rate of 104FPS can be reached when using 16 output channels.

4.3.1.1 16 OUTPUT CHANNELS

This is the default output mode. All 16 data output channels are used to transmit the image data. This means that reading out an entire row of image data takes 226 pixel periods. Next figure shows the timing for one LVDS channel.

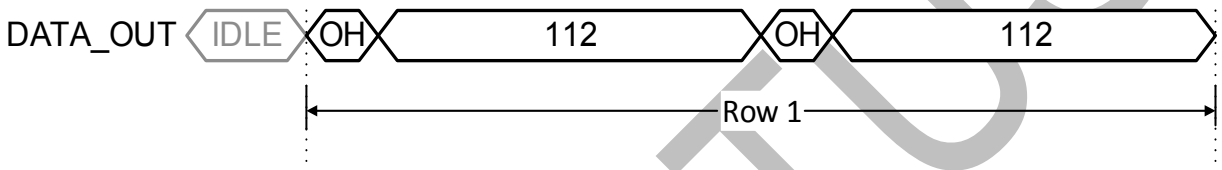

Figure 20: Output timing in default 16 channel mode

4.3.1.2 8 OUTPUT CHANNELS

Here, 8 data output channels are used to transmit the image data. This means that reading out an entire row of image data takes 452 pixel periods. Next figure shows the timing for one LVDS channel. In this mode, the maximum frame rate is reduced with a factor 2 compared to 16 channel mode.

Figure 21: Output timing in 8 channel mode

4.3.1.3 4 OUTPUT CHANNELS

Here, 4 data output channels are used to transmit the image data. This means that reading out an entire row of image data takes 904 pixel periods. Next figure shows the timing for one LVDS channel. In this mode, the maximum frame rate is reduced with a factor 4 compared to 16 channel mode.

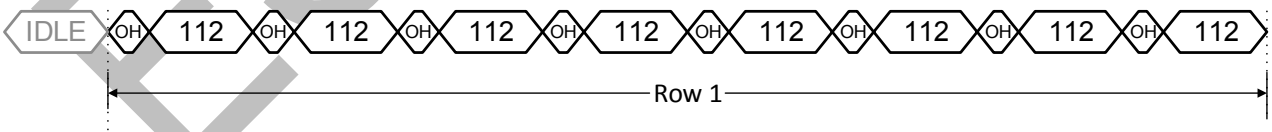

Figure 22: Output timing in 4 channel mode

4.3.1.4 2 OUTPUT CHANNELS

Here, 2 data output channels are used to transmit the image data. This means that reading out an entire row of image data takes 1808 pixel periods. Next figure shows the timing for one LVDS channel. In this mode, the maximum frame rate is reduced with a factor 8 compared to 16 channel mode.

Figure 23: Output timing in 2 channel mode

4.3.2 12 BIT MODE

In 12 bit mode, the analog-to-digital conversion takes longer to complete. This causes the frame rate to drop to 40FPS when running at the maximum bit rate.

4.3.2.1 16 OUTPUT CHANNELS

This is the default output mode. All 16 data output channels are used to transmit the image data. This means that reading out an entire row of image data takes 226 pixel periods. Next figure shows the timing for one LVDS channel.

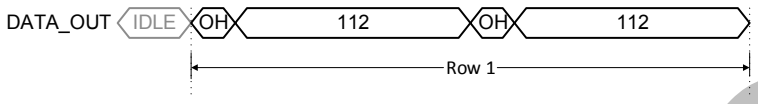

Figure 24: Output timing in default 16 channel mode

4.3.2.2 8 OUTPUT CHANNELS

Here, 8 data output channels are used to transmit the image data. This means that reading out an entire row of image data takes 452 pixel clock periods. Next figure shows the timing for one LVDS channel. In this mode, the maximum frame rate is reduced with a factor 2 compared to 16 channel mode.

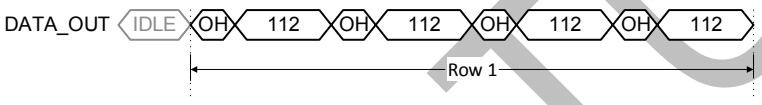

Figure 25: Output timing in 8 channel mode

4.3.2.3 4 OUTPUT CHANNELS

Here, 4 data output channels are used to transmit the image data. In this mode, the read-out of one row takes 904 pixel clock periods. Next figure shows the timing for one LVDS channel. The maximum frame rate is reduced with a factor 2 compared to 8 channel mode.

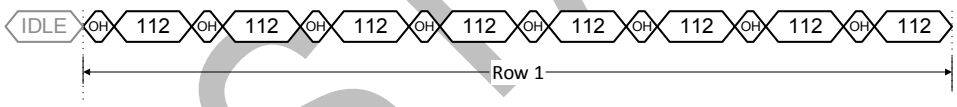

Figure 26: Output timing in 4 channel mode

4.3.2.4 2 OUTPUT CHANNELS

Here, 2 data output channels are used to transmit the image data. In this mode, the read-out of one row takes 1808 pixel clock periods. Next figure shows the timing for one LVDS channel. The maximum frame rate is reduced with a factor 2 compared to 4 channel mode.

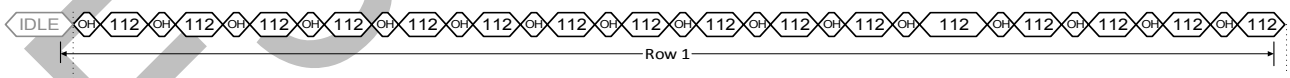

Figure 27: Output timing in 2 channel mode

4.4 PIXEL REMAPPING

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the user is able to remap the pixel values at the output to their correct location in the image array.

In each of the following figures, the timing for reading out one row is illustrated. The total amount of rows that are read out can be programmed, as explained in Chapter 5.3. By default, a full frame of 2528 rows is read out through 16 output channels. When the output is multiplexed to use less channels, the unused data channels are automatically turned off by the sensor to reduce power consumption, Chapter 5.7 explains this in more detail.

4.4.1 16 OUTPUTS

To read out one row, two bursts of 112 pixels are read out in parallel over all 16 data channels.

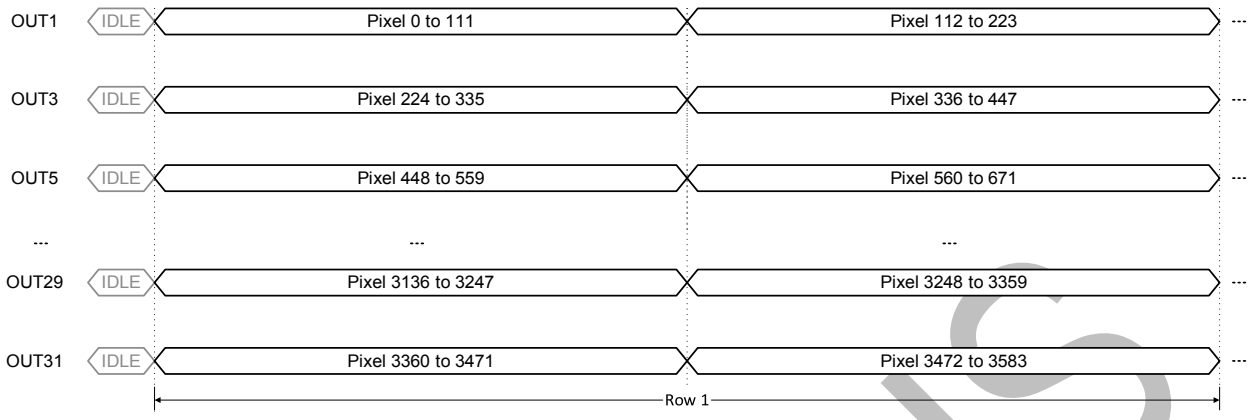

Figure 28: Pixel remapping for 16 output channels

4.4.2 8 OUTPUTS

To read out one row, four bursts of 112 pixels are read out in parallel over 8 data channels. The time it takes to read out one row, is doubled compared to when 16 data channels are used.

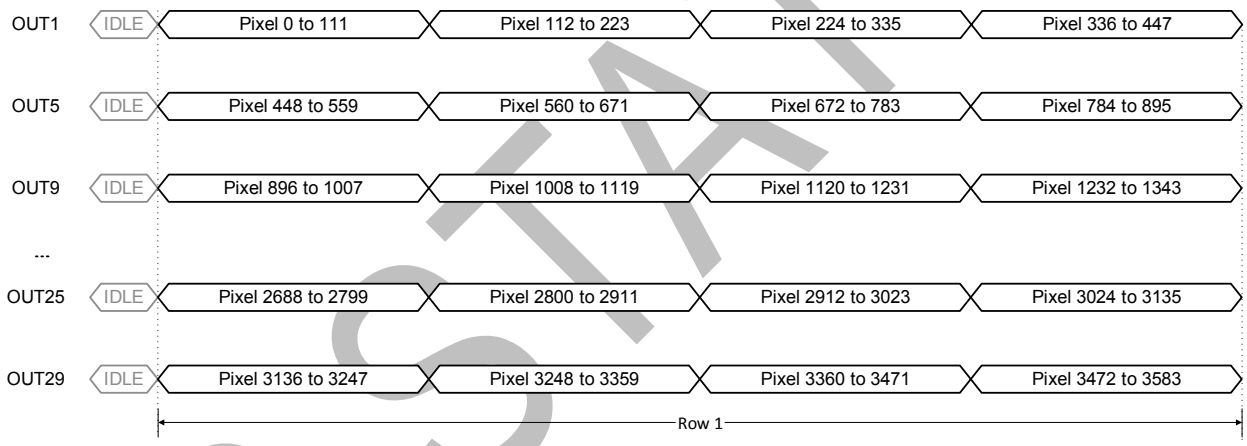

Figure 29: Pixel remapping for 8 output channels

4.4.3 4 OUTPUTS

To read out one row, eight bursts of 112 pixels are read out in parallel over 4 data channels. The time it takes to read out one row is four times as long compared to when 16 data channels are used.

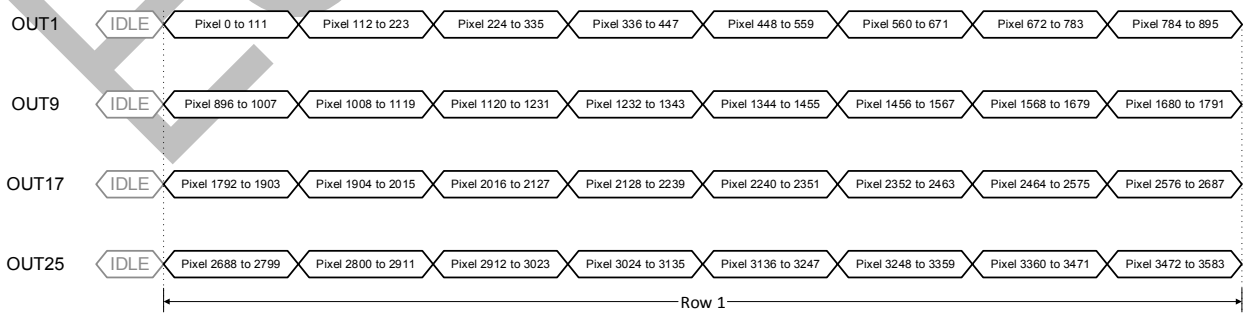

Figure 30: Pixel remapping for 4 output channels

4.4.4 2 OUTPUTS

To read out one row, sixteen bursts of 112 pixels are read out in parallel over 2 data channels. The time it takes to read out one row is eight times as long compared to when 16 data channels are used.

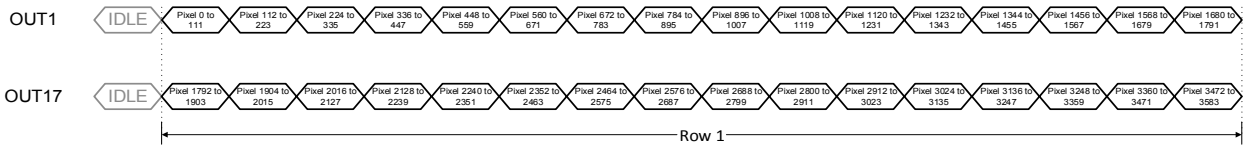

Figure 31: Pixel remapping for 2 output channels

4.4.5 Overview

When the sensor's output is multiplexed to less than 16 channels, the unused channels are automatically turned off. Therefore it's necessary to know on what channels to sample the data when multiplexing is used. The table below indicates the channels that send out data for different multiplexing options.

For example, when the output is multiplexed to 4 channels, the image data should be sampled on OUT1, OUT9, OUT17 and OUT25. All other data channels will be automatically turned off, and cannot be enabled for read-out. The same principle is valid for 8 and 2 channel multiplexing.

# OUTPUTS	OUT 1	OUT 3	OUT 5	OUT 7	OUT 9	OUT 11	OUT 13	OUT 15	OUT 17	OUT 19	OUT 21	OUT 23	OUT 25	OUT 27	OUT 29	OUT 31
16	OUT 1	OUT 3	OUT 5	OUT 7	OUT 9	OUT 11	OUT 13	OUT 15	OUT 17	OUT 19	OUT 21	OUT 23	OUT 25	OUT 27	OUT 29	OUT 31
8	OUT 1	OFF	OUT 5	OFF	OUT 9	OFF	OUT 13	OFF	OUT 17	OFF	OUT 21	OFF	OUT 25	OFF	OUT 29	OFF
4	OUT 1	OFF	OFF	OFF	OUT 9	OFF	OFF	OFF	OUT 17	OFF	OFF	OFF	OUT 25	OFF	OFF	OFF
2	OUT 1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OUT 17	OFF	OFF	OFF	OFF	OFF	OFF	OFF

4.5 Control Channel

4.5.1 Overview

The OUT_CTR LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 10-bit or 12-bit word format. Every bit of the word has a specific function, which is described in the table below.

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates validity of the read-out of a row
[2]	FVAL	Indicates the validity of the read-out of a frame
[3]	SLOT	Indicates the overhead period before 112-pixel bursts (*)
[4]	ROW	Indicates the overhead period before the read-out of a row (*)
[5]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels) (*)
[6]	INTE1	Indicates when pixels of integration block 1 are integrating (*)
[7]	INTE2	Indicates when pixels of integration block 2 are integrating (*)
[8]	'0'	Constant zero
[9]	'1'	Constant one
[10]	'0'	Constant zero
[11]	'0'	Constant zero

(*) Note: The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

The INTE signals will be low when FOT is high, so the part of exposure that overlaps with FOT is not accounted for in the INTE bits. Exposure time formulas are listed in Chapter 5.1.

Pins B2 (TDIG1) and C3 (TDIG2) can be programmed to map the state of the following control channel bits with registers 87[3:0] (tmuxd1) and 87[7:4] (tmuxd2):

tmuxd1 and tmuxd2	TDIG1	TDIG2
0	INTE1	INTE1
1	INTE2	INTE2
2	DVAL	DVAL
3	LVAL	LVAL
4	FVAL	FVAL

4.5.2 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the read-out status.

Next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the read-out of a frame of 2 rows (default is 2528 rows). This example uses the default mode of 16 outputs in 10 bit mode.

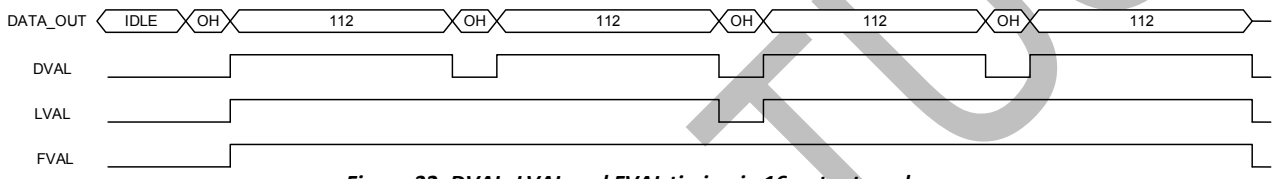

Figure 32: DVAL, LVAL and FVAL timing in 16 output mode

Note that at the end of the frame, the DVAL signal's last falling edge will occur 5 LVDS_CLK periods (=1 pixel period) sooner than the FVAL and LVAL signals. The pixel data ends at the falling edge of LVAL and FVAL though.

When only 8 outputs are used, the line read-out time is 2 times longer. The control channel takes this into account and the timing in this mode looks like the diagram below. The timing extrapolates identically for 4 and 2 outputs.

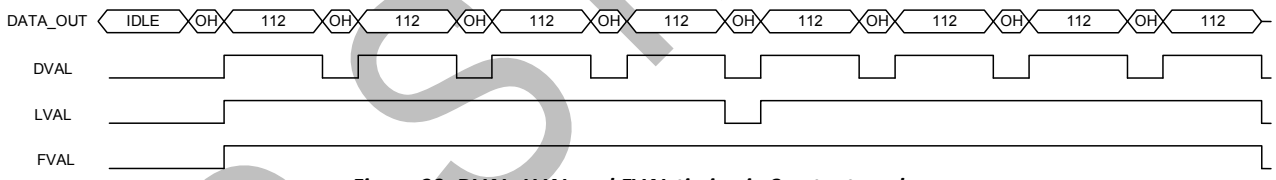

Figure 33: DVAL, LVAL and FVAL timing in 8 output mode

The figure below shows what happens on the control channel in more detail. Two frames are exposed and read out through 16 data channels, with 10 bits per pixel. The DVAL, LVAL and FVAL pulses show when the data is valid for one 112-pixel burst, one row, and one frame respectively, while the SLOT and ROW pulses signify the overhead periods between bursts and rows. On the last line, the status of all the signals on the control channel is presented in binary format as it is serially read out. Note how bits [8] and [9] always stay the same, as displayed in the table above. In 12 bit mode, the word on the control channel would be expanded with bit [10] and [11] that are continuously 0.

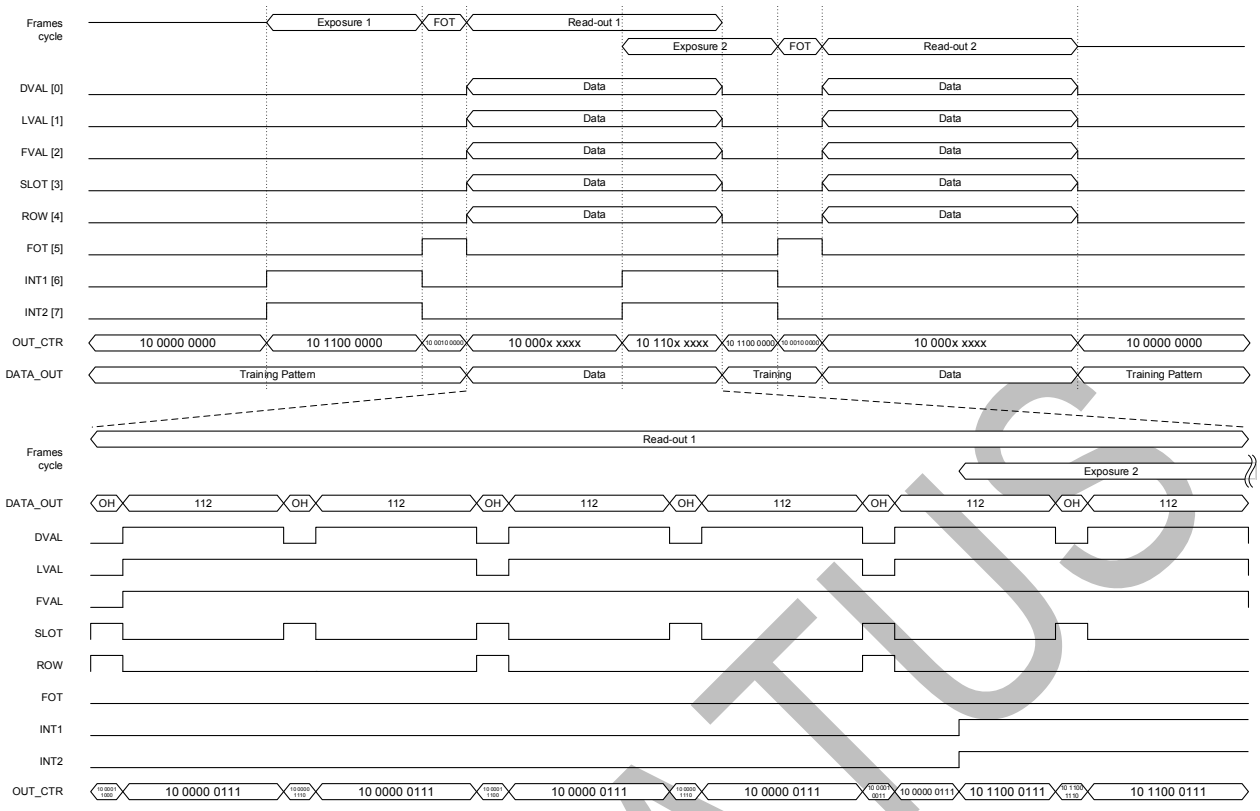

Figure 34: Detailed timings of the Control Channel (16 outputs, 10bits, 3 lines window)

4.6 TRAINING DATA

To synchronize the receiving side with the LVDS outputs of the CMV8000, a known bit pattern can be put on the output data channels. This pattern can be used to “train” the LVDS receiver of the surrounding system to achieve and maintain correct word alignment of the image data. Such a training pattern is put on all 16 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 112 pixels) in the form of a 10 or 12 bit word. The sensor has a 12-bit sequencer register (address 56) that can be loaded through the SPI to change the contents of the 12-bit training pattern TP1 for training during idle mode. TP2 equals TP1 with the 8 LSBs inverted and the 4 MSBs set to 0, and can be used for word alignment during overhead time (OH). TP2 will be put on the data channels for 1 LVDS_CLK period, and only for every LVAL. When there is more than one clock cycle of idle time between two LVAL’s, TP1 will be set on the outputs for the remaining time.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [9] (= 0010 0000 0000 or 512 decimal).

The figure below shows the location of the training pattern on the data channels and control channels when the sensor is in idle mode and when a frame of two rows is read out. The default mode of 16 outputs is used.

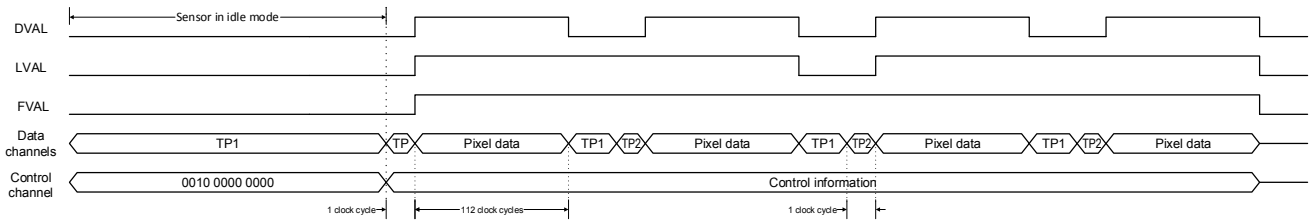

Figure 35: Training pattern location in the data and control channels.

5 IMAGE SENSOR PROGRAMMING

This section explains what functions and options are available on the sensor, and how they can be configured through the sequencer register.

5.1 EXPOSURE MODES

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of INT1 and the rising edge of F_REQ (see Chapter 3.10.2 for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

The table below gives an overview of the registers involved in the exposure mode.

Exposure time settings			
Register name	**Register address**	**Default value**	**Description of the value**
ext	40[0]	0	0: Value in EXP_LENGTH defines exposure time 1: Time between INT1 and F_REQ pulses define exposure time
EXP_LENGTH	41[7:0] 42[7:0] 43[7:0]	5056	If ext = 0: Set the exposure time according to the following formula: $\frac{\#bits}{2} \times T \times \left(\frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1) + (\text{SLOT\_LENGTH} + 1) \times \text{EXP\_LENGTH}\right)$ Where T is the period of the LVDS input clock and FOT_LENGTH is the value in register 77. SLOT_LENGTH is the value of register 61, and is different for each bit mode. If ext = 1: The exposure time is: $\frac{\#bits}{2} \times T \times \frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1) + external\ exposure\ time$ Where external exposure time is the time between INT1 and F_REQ.

To calculate the register value that is needed for a certain exposure time, in internal exposure mode, the following formula can be used. Exposure time and T should have the same time unit:

$$\text{EXP\_LENGTH} = \frac{\frac{exposure\ time}{\frac{\#bits}{5} \times T} - \frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1)}{\text{SLOT\_LENGTH} + 1}$$

The minimum value for the exposure register is 1. When the FOT_LENGTH register is at its recommended value of 50, the minimum exposure time in internal mode is 125µs for an input clock of 300MHz. With a lower FOT_LENGTH of 30, the shortest exposure time is 76µs.

In external mode, the minimum time between INT1 and F_REQ is 1 clock cycle. In this case, the minimum exposure time 123µs. With FOT_LENGTH lowered to 30 here, exposure time is 74µs.

5.2 HIGH DYNAMIC RANGE MODES

The sensor has two different ways to achieve high optical dynamic range in the grabbed image.

- Interleaved read-out: the odd and even columns have a different exposure time
- Piecewise linear response: pixels respond to light with a piecewise linear response curve.

All the HDR modes mentioned above can be used in both the internal and external exposure time mode. Note that a combination of the piecewise linear response and interleaved read-out is not possible.

5.2.1 INTERLEAVED READ-OUT

In this HDR mode, the odd and even columns of the image sensors will have a different exposure time. The table below gives an overview of the registers involved in the interleaved read-out when the internal exposure mode is selected.

Interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
INTE_DUAL	40[1]	0	0: interleaved exposure mode disabled 1: interleaved exposure mode enabled
EXP_LENGTH	41[7:0] 42[7:0] 43[7:0]	5056	If INTE_DUAL = 1 Set the exposure time for the even columns according following formula: $\frac{\#bits}{2} \times T \times \left(\frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1) + (\text{SLOT\_LENGTH} + 1) \times \text{EXP\_LENGTH}\right)$ Where T is the period of the LVDS input clock.
EXP_LENGTH2	44[7:0] 45[7:0] 46[7:0]	0	If INTE_DUAL = 1 Set the exposure time for the odd columns according following formula: $\frac{\#bits}{2} \times T \times \left(\frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1) + (\text{SLOT\_LENGTH} + 1) \times \text{EXP\_LENGTH2}\right)$ Where T is the period of the LVDS input clock.

The surrounding system can combine the image of the odd rows with the image of the even rows to a high dynamic rang image. In such an image very bright and very dark objects are made visible without clipping.

When the external exposure mode and interleaved read-out are selected, the different exposure times are achieved by using the INT1 and INT2 input pins. INT1 defines the exposure time for the even columns, while INT2 defines the exposure time for the odd columns. See the figure below for more details.

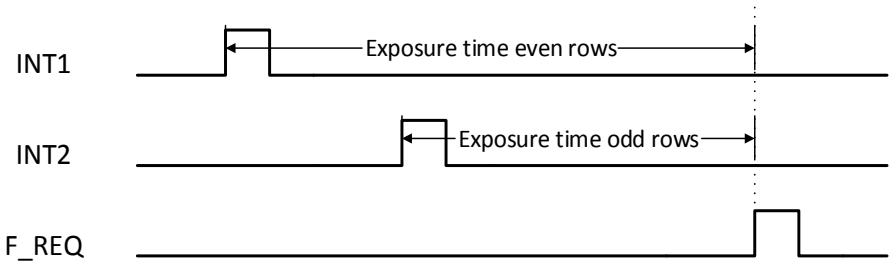

Figure 36: Interleaved read-out in external exposure mode

When a color sensor is used, the sequencer should be programmed to make sure it takes the Bayer pattern into account when doing interleaved read-out. This can be done by setting the appropriate register to '0'.

Color/mono			
Register name	**Register address**	**Default value**	**Description of the value**
MONO	121[0]	1	0: color sensor is used 1: monochrome sensor is used

5.2.2 PIECEWISE LINEAR RESPONSE

The CMV8000 has the possibility to achieve a high optical dynamic range by using a piecewise linear response. This feature will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched. The clipping level can be adjusted 2 times within one exposure time to achieve a maximum of 3 slopes in the response curve. More details can be found in the figure below.

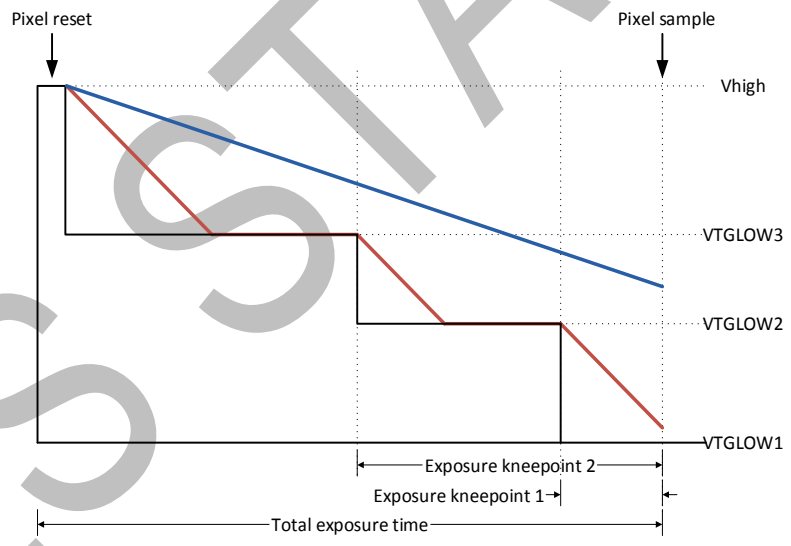

Figure 37: Programmable kneepoints

In the figure above, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. As shown in the figure, the bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to make sure that at the end of the exposure time the pixel is not saturated. The darker pixel is not influenced and will have a normal response. The VTGLOW voltages and different exposure times are programmable using the sequencer registers. Using this feature, a response as detailed in the figure below can be achieved. The placement of the knee points on the X-axis is controlled by the VTGLOW programming, while the slope of the segments is controlled by the programmed exposure times.

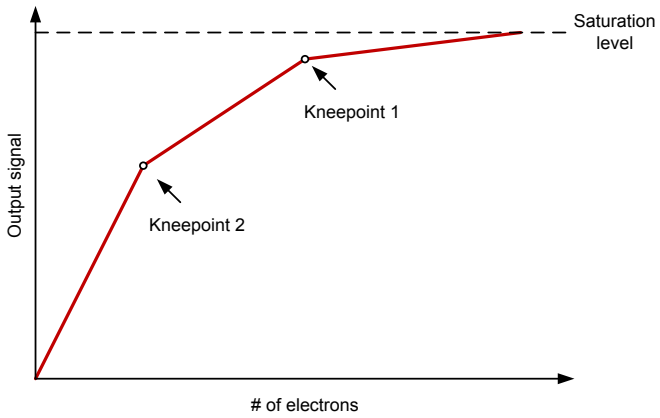

Figure 38: Piecewise linear response

5.2.2.1 INTERNAL EXPOSURE CONTROL

The following registers need to be programmed when a piecewise linear response in internal exposure mode is desired.

Piecewise linear response			
Register name	**Register address**	**Default value**	**Description of the value**
EXP_LENGTH	41[7:0] 42[7:0] 43[7:0]	5056	Set the total exposure time according to the following formula: $\frac{\#bits}{2} \times T \times \left(\frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1) + (\text{SLOT\_LENGTH} + 1) \times \text{EXP\_LENGTH}\right)$ Where T is the period of the LVDS input clock.
SLOPES	47[1:0]	1	Set the number of slopes (min=1, max=3).
EXP_K1	48[7:0] 49[7:0] 50[7:0]	0	Set the exposure time of kneepoint 1 according to the following formula: $\frac{\#bits}{2} \times T \times \left(\frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1) + (\text{SLOT\_LENGTH} + 1) \times \text{EXP\_K1}\right)$ Where T is the period of the LVDS input clock.
EXP_K2	51[7:0] 52[7:0] 53[7:0]	0	Set the exposure time of kneepoint 2 according to the following formula: $\frac{\#bits}{2} \times T \times \left(\frac{148}{224} \times (224 \times \text{FOT\_LENGTH} + 1) + (\text{SLOT\_LENGTH} + 1) \times \text{EXP\_K2}\right)$ Where T is the period of the LVDS input clock.
VTGLOW1	94[6:0]	64	Set the VTGLOW1 voltage (DAC setting). Bit [6] = enable Bit[5:0] = set voltage between 0 and 1.8V (linear)
VTGLOW2	95[6:0]	64	Set the VTGLOW2 voltage (DAC setting). Bit [6] = enable Bit[5:0] = set voltage between 0 and 1.8V (linear)
VTGLOW3	96[6:0]	64	Set the VTGLOW3 voltage (DAC) setting). Bit[6] = enable Bit[5:0] = set voltage between 0 and 1.8V (linear)

5.2.2.2 EXTERNAL EXPOSURE CONTROL

When external exposure time is used and a piecewise linear response is desired, the following registers should be programmed.

Piecewise linear response			
Register name	**Register address**	**Default value**	**Description of the value**
SLOPES	47[1:0]	1	Set the number of slopes (min=1, max=3).
VTGLOW1	94[6:0]	64	Set the VTGLOW1 voltage (DAC setting). Bit [6] = enable Bit[5:0] = set voltage between 0 and 1.8V (linear)
VTGLOW2	95[6:0]	64	Set the VTGLOW2 voltage (DAC setting). Bit [6] = enable Bit[5:0] = set voltage between 0 and 1.8V (linear)
VTGLOW3	96[6:0]	64	Set the VTGLOW3 voltage (DAC) setting). Bit[6] = enable Bit[5:0] = set voltage between 0 and 1.8V (linear)

The timing that needs to be applied in this external exposure mode looks like the one below.

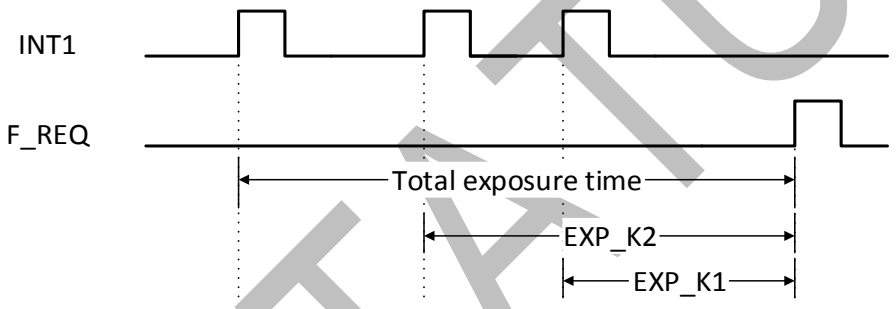

Figure 39: Piecewise linear response with external exposure time mode

5.3 WINDOWING

To limit the amount of data or to increase the frame rate of the sensor, windowing in Y direction is possible. The number of lines and start address can be set by programming the appropriate registers. The CMV8000 has the possibility to read-out multiple (max=8) predefined sub windows in one read-out cycle. The default mode is to read-out one window with the full frame size of 3584 by 2528 pixels.

5.3.1 SINGLE WINDOW

When a single window is read out, the start address and size can be uploaded in the corresponding registers. The default start address is 0 and the default size is 2528 (full frame).

Single window			
Register name	**Register address**	**Default value**	**Description of the value**
YADDR_0	3[7:0] 4[7:0]	0	Set the start address of the window in Y (min=0, max=2527)
YSIZE_TOT	1[7:0] 2[7:0]	2528	Set the number of lines read-out by the sensor (min=1, max=2528)

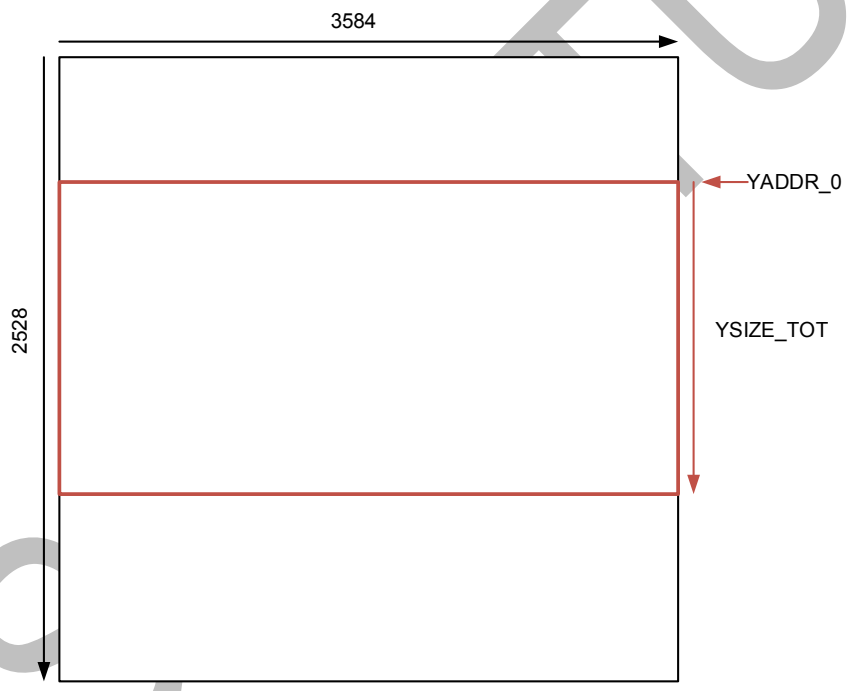

Figure 40: Single window settings

5.3.2 MULTIPLE WINDOWS

The CMV8000 can read out a maximum of 8 different sub windows in one read-out cycle. The location and length of these sub windows must be programmed in the correct registers. The total number of lines to be read-out (sum of all windows) needs to be specified in the YSIZE_TOT register. The registers which need to be programmed for the multiple windows can be found in the table below. The default values will result in one window with 2528 lines to be read-out.

Multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
YSIZE_TOT	1[7:0] 2[7:0]	2528	Set the total number of lines to read out (min=1, max=2528)
YADDR_0	3[7:0] 4[7:0]	0	Set the start address of the first window (min=0, max=2527)

Multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
YSIZE_0	19[7:0] 20[7:0]	0	Set the number of rows of the first window (min=1, max=2528)
YADDR_1	5[7:0] 6[7:0]	0	Set the start address of the second window in Y (min=0, max=2527)
YSIZE_1	21[7:0] 22[7:0]	0	Set the number of lines of the second window (min=1, max=2528)
YADDR_2	7[7:0] 8[7:0]	0	Set the start address of the third window in Y (min=0, max=2527)
YSIZE_2	23[7:0] 24[7:0]	0	Set the number of lines of the third window (min=1, max=2528)
YADDR_3	9[7:0] 10[7:0]	0	Set the start address of the fourth window in Y (min=0, max=2527)
YSIZE_3	25[7:0] 26[7:0]	0	Set the number of lines of the fourth window (min=1, max=2528)
YADDR_4	11[7:0] 12[7:0]	0	Set the start address of the fifth window in Y (min=0, max=2527)
YSIZE_4	27[7:0] 28[7:0]	0	Set the number of lines of the fifth window (min=1, max=2528)
YADDR_5	13[7:0] 14[7:0]	0	Set the start address of the sixth window in Y (min=0, max=2527)
YSIZE_5	29[7:0] 30[7:0]	0	Set the number of lines of the sixth window (min=1, max=2528)
YADDR_6	15[7:0] 16[7:0]	0	Set the start address of the seventh window in Y (min=0, max=2527)
YSIZE_6	31[7:0] 32[7:0]	0	Set the number of lines of the seventh window (min=1, max=2528)
YADDR_7	17[7:0] 18[7:0]	0	Set the start address of the eighth window in Y (min=0, max=2527)
YSIZE_7	33[7:0] 34[7:0]	0	Set the number of lines of the eighth window (min=1, max=2528)

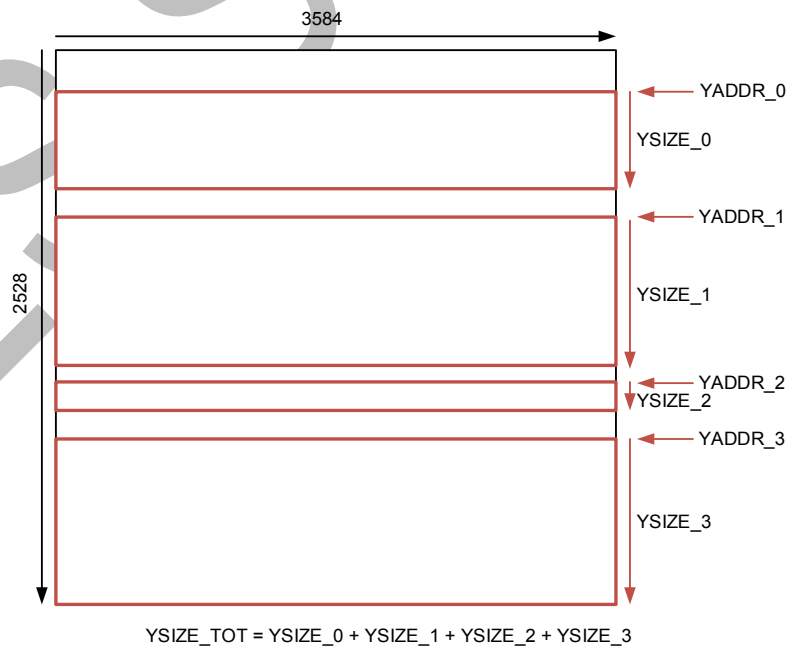

Figure 41: Example of multiple frame configuration

5.4 IMAGE MIRRORING

The image coming out of the image sensor can be mirrored, both in the X and Y direction. In the example below, 2 channel output mode is used to simplify the figure. When mirroring is disabled, the pixel in the upper left corner of the screen - pixel (0,0) - is read out first. When mirroring in Y is enabled, the bottom left pixel (0,2495) is read out first instead of the top left pixel (0,0). When mirroring in X is enabled, only the pixels within a channel are mirrored, not the channels themselves. Therefore, the first row to be read out is pixel (1679,0) to pixel (0,0) in channel 1 and pixel (3359,0) to pixel (1680,0) in channel 2.

Note: The black reference rows and columns are not pictured in the example below. When mirroring in the Y direction, the 32 reference rows are mirrored too, but are still read out first.

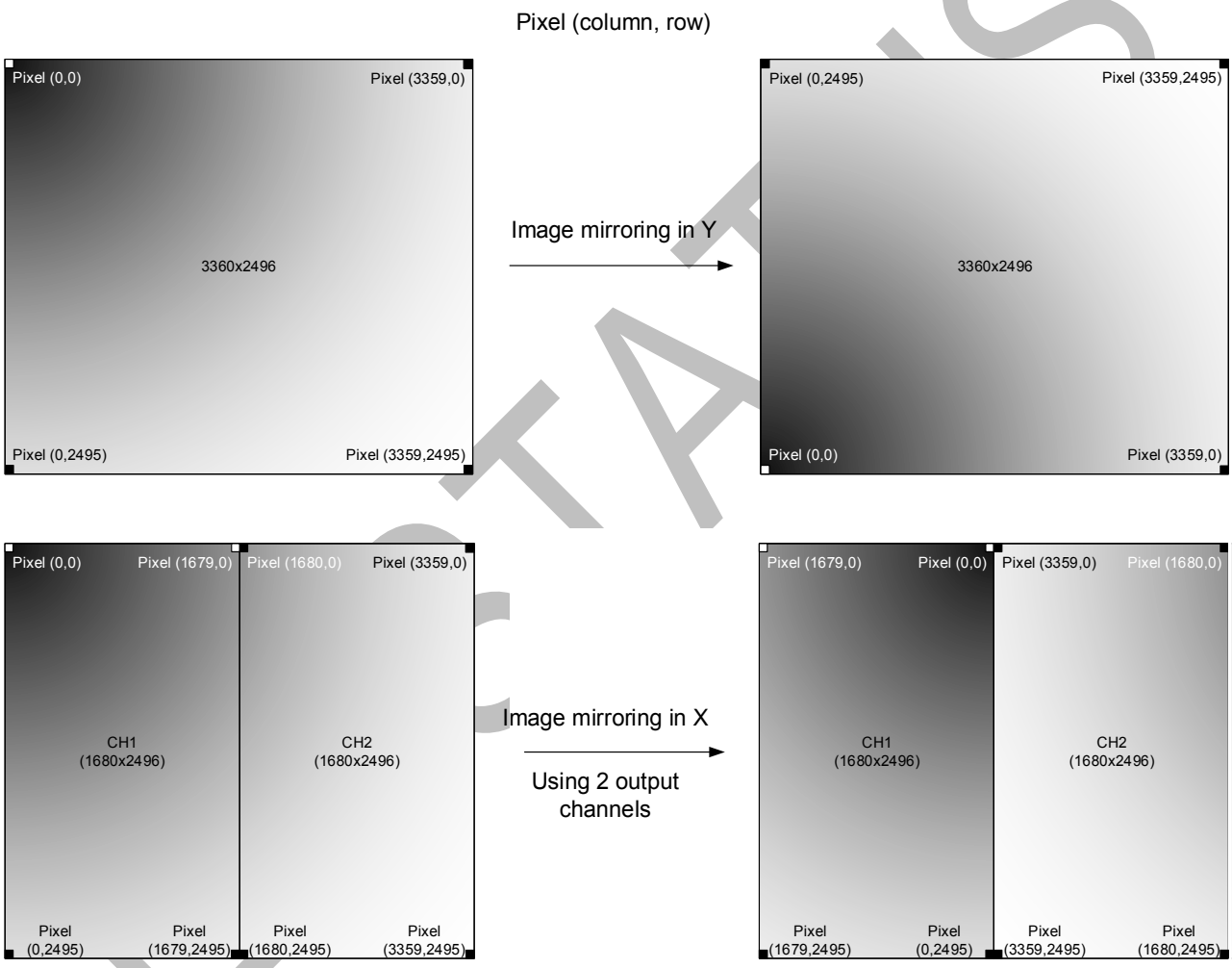

Figure 42: Image mirroring

The following registers are used for image mirroring:

Image mirroring			
Register name	**Register address**	**Default value**	**Description of the value**
MIRROR	39[1:0]	0	0: No image mirroring 1: Image mirroring in X 2: Image mirroring in Y 3: Image mirroring in X and Y

5.5 IMAGE SUBSAMPLING

To maintain the same field of view but reduce the amount of data coming out of the sensor, a subsampling mode is implemented on the chip. Different subsampling schemes can be programmed by setting the appropriate registers. These subsampling schemes can take into account whether a color or monochrome sensor is used to preserve the Bayer pattern information. The registers involved in subsampling are detailed below. A distinction is made between a simple and advanced mode (can be used for color devices). Subsampling can be enabled in every windowing mode.

5.5.1 SIMPLE SUBSAMPLING

Simple subsampling			
Register name	**Register address**	**Default value**	**Description of the value**
YSIZE_TOT	1[7:0] 2[7:0]	2528	Set the total number of lines read-out by the sensor (min=1, max=2528)
YSKIP1	35[7:0] 36[7:0]	0	Set the number of rows to skip (min=0, max=2528)
YSKIP2	37[7:0] 38[7:0]	0	Set to the same value as YSKIP1 (min=0, max=2528)

The figures below give two subsampling examples (skip 4x and skip 1x).

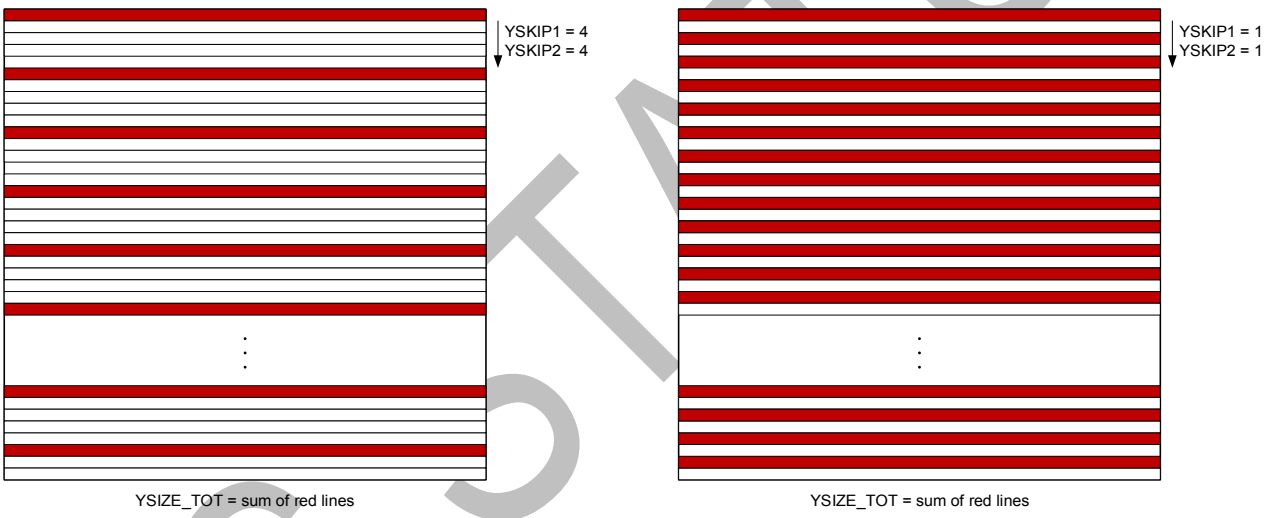

Figure 43: Subsampling examples (skip 4x and skip 1x)

5.5.2 ADVANCED SUBSAMPLING

When a color sensor is used, the subsampling scheme should take into account that a Bayer color filter is applied on the sensor. This Bayer pattern should be preserved when subsampling is used. This means that the number of rows to be skipped should always be a multiple of two. An advanced subsampling scheme can be programmed to achieve these requirements. Of course, this advanced subsampling scheme can also be programmed in a monochrome sensor. See the table of registers below for more details.

Advanced subsampling			
Register name	**Register address**	**Default value**	**Description of the value**
YSIZE_TOT	1[7:0] 2[7:0]	2528	Set the total number of lines read-out by the sensor (min=1, max=2528)
YSKIP1	35[7:0] 36[7:0]	0	Set to ‘0’ at all times
YSKIP2	37[7:0] 38[7:0]	0	Set the number of rows to skip, it should be an even number between (0 and 2528).

The figures below give two subsampling examples (skip 4x and skip 2x) in advanced mode.

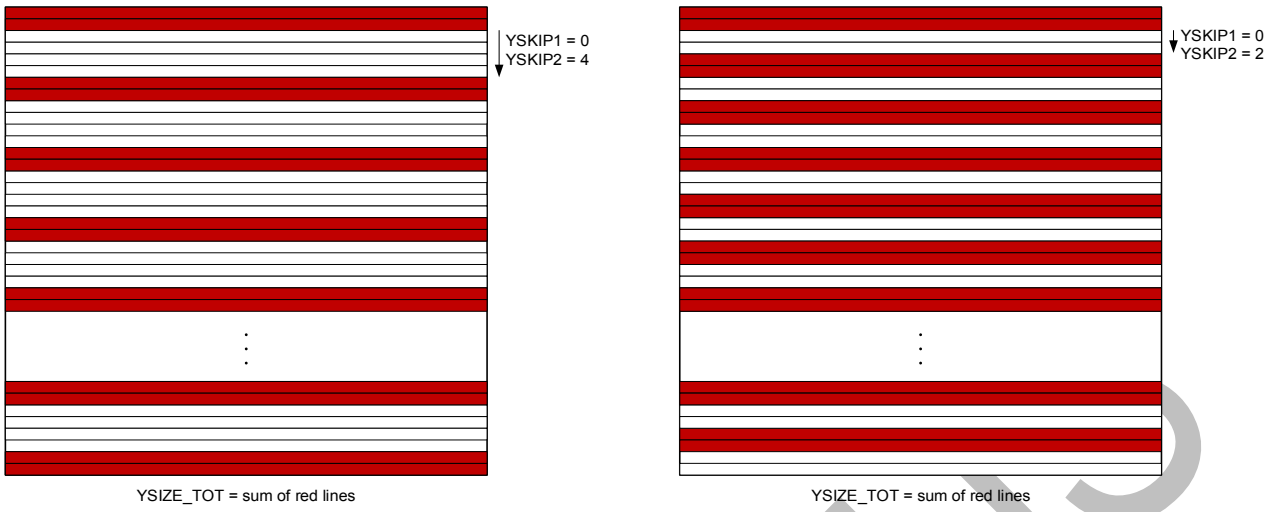

Figure 44: Subsampling examples in advanced mode (skip 4x and skip 2x)

5.6 NUMBER OF FRAMES

When internal exposure mode is selected, the number of frames sent by the sensor after a frame request can be programmed in the corresponding sequencer register.

Number of frames			
Register name	**Register address**	**Default value**	**Description of the value**
FRAMES	54[7:0] 55[7:0]	1	Set the number of frames grabbed and sent by the image sensor in internal exposure mode (min = 1, max = 65535)

5.7 OUTPUT MODE

The number of LVDS channels can be selected by programming the appropriate sequencer register. By selecting less than 16 outputs, the unused channels are turned off automatically. The pixel remapping scheme and the read-out timing for each mode can be found in Chapter 4.

Output mode				
Register name	**Register address**	**Default value**	**Description of the value**	
MUX	59[4:0]	1	0: unused 1: 16 outputs 3: 8 outputs 7: 4 outputs 15: 2 outputs	
ROW_LENGTH	62[6:0]	2	10bit mode 2: 16 outputs 4: 8 outputs 8 : 4 outputs 16: 2 outputs	12bit mode 4: 16 outputs 8: 8 outputs 16: 4 outputs 32: 2 outputs

5.8 TRAINING PATTERN

As detailed in Chapter 4.6, a training pattern is sent over the LVDS data channels whenever no valid image data is sent. This training pattern TP1 can be programmed using the sequencer register.

Training pattern			
Register name	**Register address**	**Default value**	**Description of the value**
LVDS_TRAIN	56[7:0] 57[3:0]	85	The 12 LSBs of this 16 bit word are sent in 12-bit mode. In 10 bit mode the 10 LSBs are sent.

5.9 BIT DEPTH

The CMV8000 has the possibility to send 12 bits or 10 bits per pixel. The end user can select the desired resolution by programming the corresponding sequencer register. Always keep the ADC tune and the LVDS Resolution register in the same bit mode.

Bit depth			
Register name	**Register address**	**Default value**	**Description of the value**
SLOT_LENGTH	61[7:0]	112	112: 10 bit mode 122: 12 bit mode
ROW_LENGTH	62[5:0]	2	2: 10 bit mode 4: 12 bit mode
SMP_LENGTH	65[7:0] 66[0]	96	96: 10 bit mode 231: 12 bit mode
ADC_RAMP_R_SIZE	71[7:0] 72[0]	41	29: 10 bit mode 54: 12 bit mode
ADC_INTERVAL	73[7:0]	1	19: 10bit mode 1: 12bit mode
ADC_RAMP_S_SIZE	74[7:0] 75[1:0]	144	120: 10 bit mode 397: 12 bit mode
DB_OFFSET_DATA	80[7:0] 81[3:0]	444	444: 10 bit mode 1966: 12 bit mode
DB_DIG_GAIN	82[4:0]	4	4: 10 bit mode 1: 12 bit mode
lvds	83[1]	1	1: 10 bit mode 0: 12 bit mode
div	84[4:0]	4	4: 10 bit mode 5: 12 bit mode
v_ramp_res	115[6:0]	94	70: 10bit mode 76: 12bit mode
V_ramp_sig	116[6:0]	94	70: 10bit mode 76: 12bit mode
tune	117[7:6]	0	0: 10 bit mode 3: 12 bit mode
gate parallel clock	123[0]	0	Set to 1 before adjusting clock speed settings

Whenever a change in clock frequency is needed, the clock gating register always needs to be set to ‘1’ before adjusting the SPI registers. After the changes are uploaded, this register can be set back to ‘0’.

5.10 DATA RATE

The CMV8000 has a maximum data rate of 600Mbps at the maximum IN_LCLK clock speed of 300MHz. This is because the output clock OUT_CLK on which the image data is sampled, is a double data rate clock. The data rate is thus always twice as high as the LVDS input clock frequency. If the data rate needs to be lowered, this can be done by simply lowering the speed of the LVDS input clock.

5.11 POWER CONTROL

The power consumption of the CMV8000 mostly depends on the amount of LVDS channels that are active. When the output mode is changed to less than 16 outputs, the sensor automatically disables the unused channels to decrease power consumption. The power will decrease per disabled channel is estimated at 18mW. So when reducing the outputs from 16 to 4, the power saving will be about 216mW or 33%. Other settings (such as bit rate, frame rate, temperature …) will have very little to no effect on the total power consumption.

Power control			
Register name	**Register address**	**Default value**	**Description of the value**
CHANNEL_EN	60[3:0]	7	60[0] 0: Disable the LVDS clock channel 1: Enable the LVDS clock channel 60[1] 0: Disable the LVDS control channel 1: Enable the LVDS control channel 60[2] 1: Only enable the active LVDS data channels (automatically changes with MUX setting). 0: Disable all data channels 60[3] **Never set this bit to '1'!** Doing so can severely damage the sensor.

Decreasing the input clock frequency (IN_LCLK) will also decrease power consumption, albeit little. Decreasing the IN_LCLK frequency by about 100MHz will decrease power consumption with about 10mW. All power savings will happen on the VDD18 supply. Other settings or factors have no significant effect on the power consumption.

5.12 OFFSET AND GAIN

5.12.1 OFFSET

A digital offset can be applied to the output signal. This dark level offset can be programmed by setting the desired value in the sequencer register. The 12 bit register value is a 2-complement number, allowing us to have a positive and a negative offset (from 2047 to -2048). The ADC itself has a fixed offset of -440.

So the dark-level @ output = -440 + Offset (in 2's complement). For example the default register value of 444 (0001 1011 1100) makes the default dark-level set at -440 + 444 = 4 digital numbers. For a register value larger than 2047, the value will be converted to a negative number, as described in the table below.

Offset			
Register name	**Register address**	**Default value**	**Description of the value**
DB_OFFSET_DATA	80[7:0] 81[3:0]	444	Set the dark level offset applied to the output signal (min = 0, max = 4095). The value is in 2's complement: **Decimal** — **Binary** — **2's Comp.** 0 — 0000 0000 0000 — 0 1 — 0000 0000 0001 — 1 … — … — … 2047 — 0111 1111 1111 — 2047 2048 — 1000 0000 0000 — -2048 2049 — 1000 0000 0001 — -2047 … — … — … 4095 — 1111 1111 1111 — -1

5.12.2 GAIN

An analog gain and ADC gain can be applied to the output signal. The analog gain is applied by a PGA in every column. The digital gain is applied by the ADC.

Gain			
Register name	**Register address**	**Default value**	**Description of the value**
PGA_GAIN	118[3:0]	7	Set the gain of the column amplifiers 7: x1 gain 15: x1.33 gain 14: x2 gain 5: x3 gain 13: x4 gain
adc_gain	117[5:0]	32	Set the gain of the ADC (min=0; max=63) 0: 0.5x gain 32: 1x gain 48: 2x gain

The ADC gain is not dependent on the LVDS input clock. If the input clock is slower, the adc_gain is automatically adjusted to give the same gain at the previous speed. Therefore, a setting of 32 will always yield a gain of x1, whatever the clock speed. Also at higher register values, the actual ADC gain will increase in bigger steps. So fine-tuning the ADC gain is easier at lower register values.

5.13 TEST MODE

The CMV8000 has a built in test mode that enables a test pattern that can be read out. This is digitally generated, and has no pixel or read noise in the signal. The brightness of this pattern can be controlled with the offset register.

The pattern starts at the first column with the grey value of DB_OFFSET_MODE and is incremented by 1 until 112 columns are reached. Then the pattern is repeated, this time starting at DB_OFFSET_MODE +1, and so on.

Test mode			
Register name	**Register address**	**Default value**	**Description of the value**
TEST_MODE	79[1:0]	0	3: enable test pattern
DB_OFFSET_MODE	80[7:0] 81[3:0]	444	Set the brightness, or offset of the test pattern.

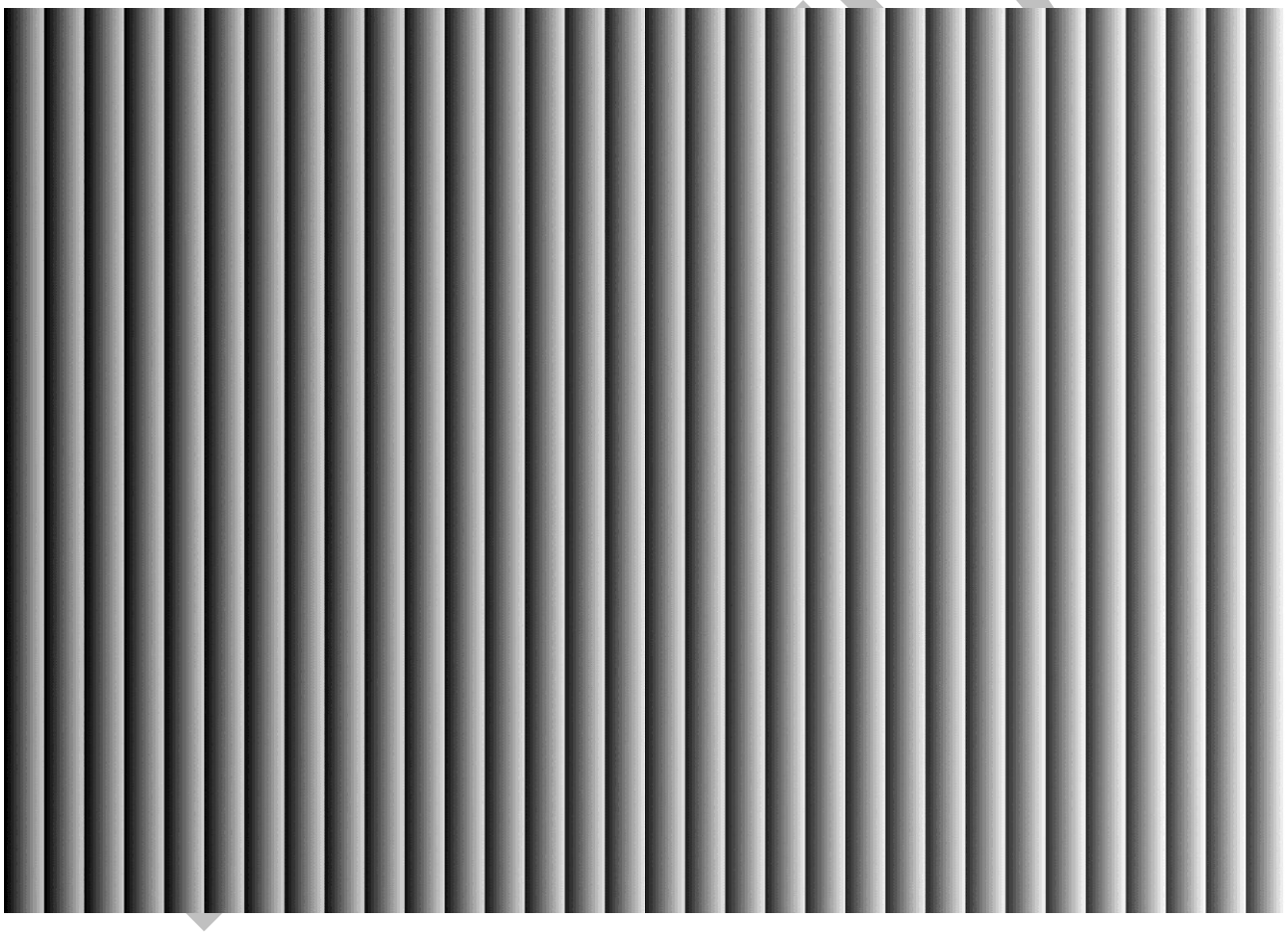

Figure 45 CMV8000 test pattern

5.14 Recommended Settings

The following table gives an overview of the registers which have a required value which is different from their default start-up value. We strongly recommend to load these register settings after start-up and before grabbing an image.

Address	Name		Required Value
68	clamp_sig	pc_disable	12
71	ADC_RAMP_R_SIZE		29
73	ADC_INTERVAL		19
74	ADC_RAMP_S_SIZE		120
76	no_ramp_ctrl		8
77	FOT_LENGTH		50
91	V_PC		200
92	V_PCHIGH		240
97	tg	rst	102
98	s2	s1	102
99	I_COL		8
103	V_CLAMP_RST		70
106	I_ADC		12
115	V_VRAMP_RES		70
116	V_VRAMP_SIG		70
118	PGA_GAIN		15

5.15 Adjusting Registers for Optimal Performance

Due to processing differences, the response and optical performance may differ slightly from sensor to sensor. To adjust this difference in response, the following registers should be tuned from sensor to sensor.

Address	Name	Default Value	Valid Range
117[5:0]	adc_gain	32	0-63
80[7:0]	DB_OFFSET_DATA	444	0-4095

Due to processing differences, the AFE (analog front end) of the sensor may differ from device to device. This means that the total gain value (bit/e) of the sensor may differ from sensor to sensor. The adc_gain register can be used to change the gain value (bit/e) from every sensor to match a desired value.

6 REGISTER OVERVIEW

The table below gives an overview of all the sensor registers. The registers that are not discussed in Chapter 5, should not be changed from their default value.

Register overview										
Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
0	0									Do not change
1	224	YSIZE_TOT[7:0]								
2	9	YSIZE_TOT[15:8]								
3	0	YADDR_0[7:0]								
4	0	YADDR_0[15:8]								
5	0	YADDR_1[7:0]								
6	0	YADDR_1[15:8]								
7	0	YADDR_2[7:0]								
8	0	YADDR_2[15:8]								
9	0	YADDR_3[7:0]								
10	0	YADDR_3[15:8]								
11	0	YADDR_4[7:0]								
12	0	YADDR_4[15:8]								
13	0	YADDR_5[7:0]								
14	0	YADDR_5[15:8]								
15	0	YADDR_6[7:0]								
16	0	YADDR_6[15:8]								
17	0	YADDR_7[7:0]								
18	0	YADDR_7[15:8]								
19	0	YSIZE_0[7:0]								
20	0	YSIZE_0[15:8]								
21	0	YSIZE_1[7:0]								
22	0	YSIZE_1[15:8]								
23	0	YSIZE_2[7:0]								
24	0	YSIZE_2[15:8]								
25	0	YSIZE_3[7:0]								
26	0	YSIZE_3[15:8]								
27	0	YSIZE_4[7:0]								
28	0	YSIZE_4[15:8]								
29	0	YSIZE_5[7:0]								
30	0	YSIZE_5[15:8]								
31	0	YSIZE_6[7:0]								
32	0	YSIZE_6[15:8]								
33	0	YSIZE_7[7:0]								
34	0	YSIZE_7[15:8]								
35	0	YSKIP1[7:0]								
36	0	YSKIP1[15:8]								
37	0	YSKIP2[7:0]								
38	0	YSKIP2[15:8]								
39	0							MIRROR[1:0]		
40	4						sync	dual	ext	
41	192	EXP_LENGTH[7:0]								
42	19	EXP_LENGTH[15:8]								
43	0	EXP_LENGTH[23:16]								
44	0	EXP_LENGTH2[7:0]								
45	0	EXP_LENGTH2[15:8]								
46	0	EXP_LENGTH2[23:16]								

Register overview										
Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
47	1							slopes		
48	0	EXP_K1[7:0]								
49	0	EXP_K1[15:8]								
50	0	EXP_K1[23:16]								
51	0	EXP_K2[7:0]								
52	0	EXP_K2[15:8]								
53	0	EXP_K2[23:16]								
54	1	FRAMES[7:0]								
55	0	FRAMES[15:8]								
56	85	LVDS_TRAIN[7:0]								
57	0					LVDS_TRAIN[11:8]				
58	1	DUMMY[7:0]								Set to 0
59	1				MUX[4:0]					
60	7					CHANNEL_EN[3:0]				
61	112	SLOT_LENGTH[7:0]								
62	2		ROW_LENGTH[6:0]							
63	0									
64	0									
65	96	SMP_LENGTH[7:0]								
66	0									
67	1									
68	24				clamp_sig		pc_disable			Set to 12
69	0									
70	0									
71	41	ADC_RAMP_R_SIZE[7:0]								Set to 29
72	0								ADC_RAMP_R_SIZE[8]	
73	1	ADC_INTERVAL[7:0]								Set to 19
74	144	ADC_RAMP_S_SIZE[7:0]								Set to 120
75	0							ADC_RAMP_S_SIZE[9:8]		
76	0					no_ramp_ctrl				Set to 8
77	40	FOT_LENGTH[7:0]								Set to 50
78	0							adc_cal	amp_cal	
79	0							TEST_MODE[1:0]		
80	188	DB_OFFSET_DATA[7:0]								Tune
81	1					DB_OFFSET_DATA[11:8]				
82	4				DB_DIG_GAIN[4:0]					
83	2							lvds	adc	
84	4				div[4:0]					
85	132									
86	3									
87	0	tmuxd2[3:0]				tmuxd1[3:0]				
88	0	TEMP_LO[7:0]								
89	0	TEMP_HI[7:0]								
90	129	REV_ID[7:0]								
91	224	V_PC[7:0]								Set to 200
92	224	V_PCHIGH[7:0]								Set to 240
93	64									

Register overview										
Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
94	64		V_TGLOW1[6:0]							
95	64		V_TGLOW2[6:0]							
96	64		V_TGLOW3[6:0]							
97	136	tg[3:0]				rst[3:0]				Set to 102
98	136	s2[3:0]				s1[3:0]				Set to 102
99	11					I_COL[3:0]				Set to 8
100	8									
101	0					TMUXANA[3:0]				
102	136	rec[3:0]				driv[3:0]				
103	84		V_CLAMP_RST[6:0]							Set to 70
104	84									
105	12									
106	14					I_ADC[3:0]				Set to 12
107	8									
108	8									
109	96									
110	75									
111	96									
112	96									
113	96									
114	96									
115	94		V_VRAMP_RES[6:0]							Set to 70
116	94		V_VRAMP_SIG[6:0]							Set to 70
117	32	tune[1:0]		adc_gain[5:0]						
118	7					PGA_GAIN[3:0]				Set to 15
119	255									
120	255									
121	25				lvds_rec				mono	
122	0									
123	0	RESERVED_1[6:0]							Gate parallel clock	
124	0	RESERVED_2[6:0]								
125	0	RESERVED_3[7:0]								
126	0	RESERVED_4[7:0]								
127	0	RESERVED_5[7:0]								

Note: Register 90 can be used to verify the sensor type. Bits [7:4] contain the product ID (8 for a CMV8000 sensor) and bits [3:0] contain the revision ID (1 for the first version).

7 MECHANICAL SPECIFICATIONS

7.1 PACKAGE DRAWING

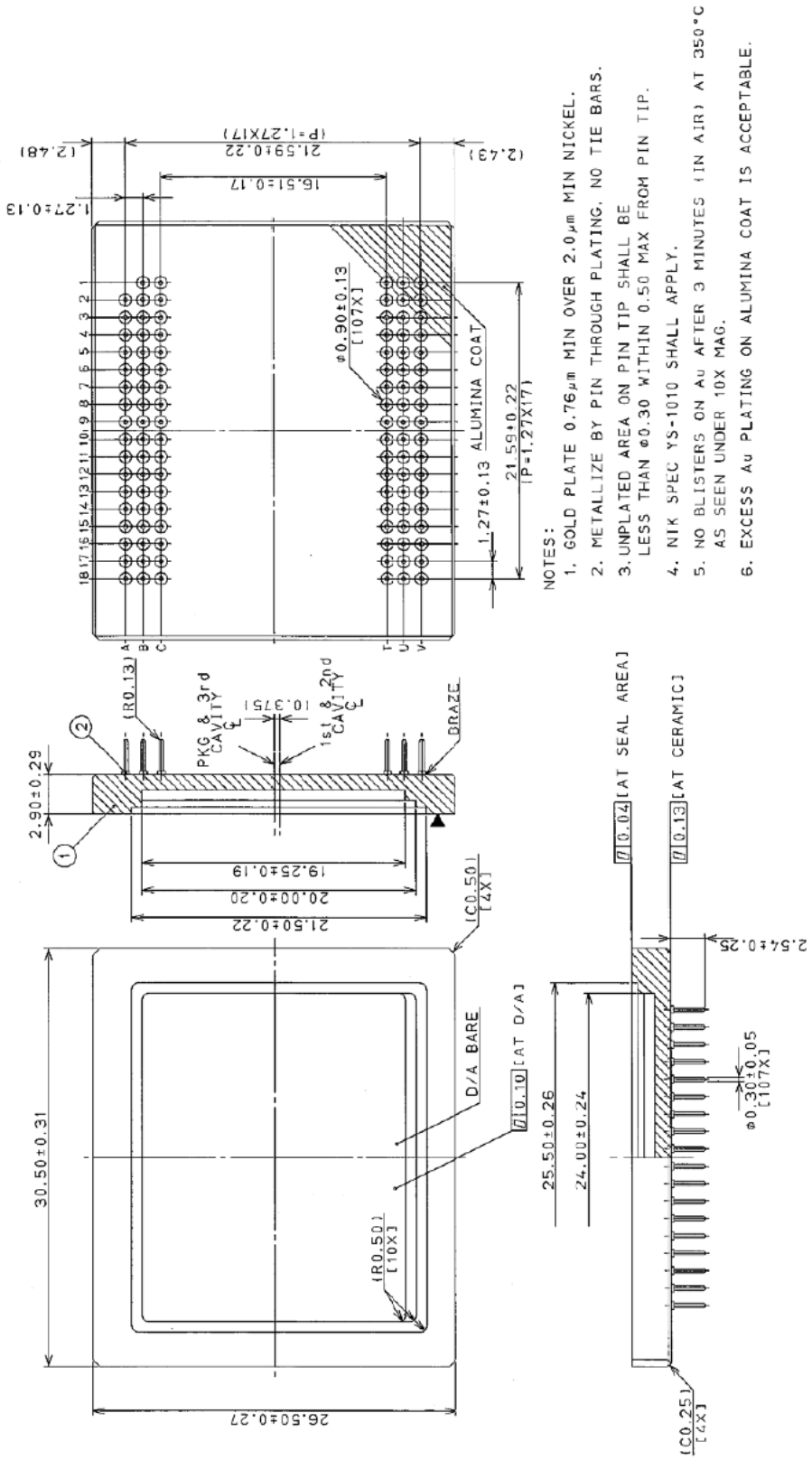

Figure 46: PGA package drawing of the CMV8000. All dimensions are in mm.

7.2 ASSEMBLY DRAWING

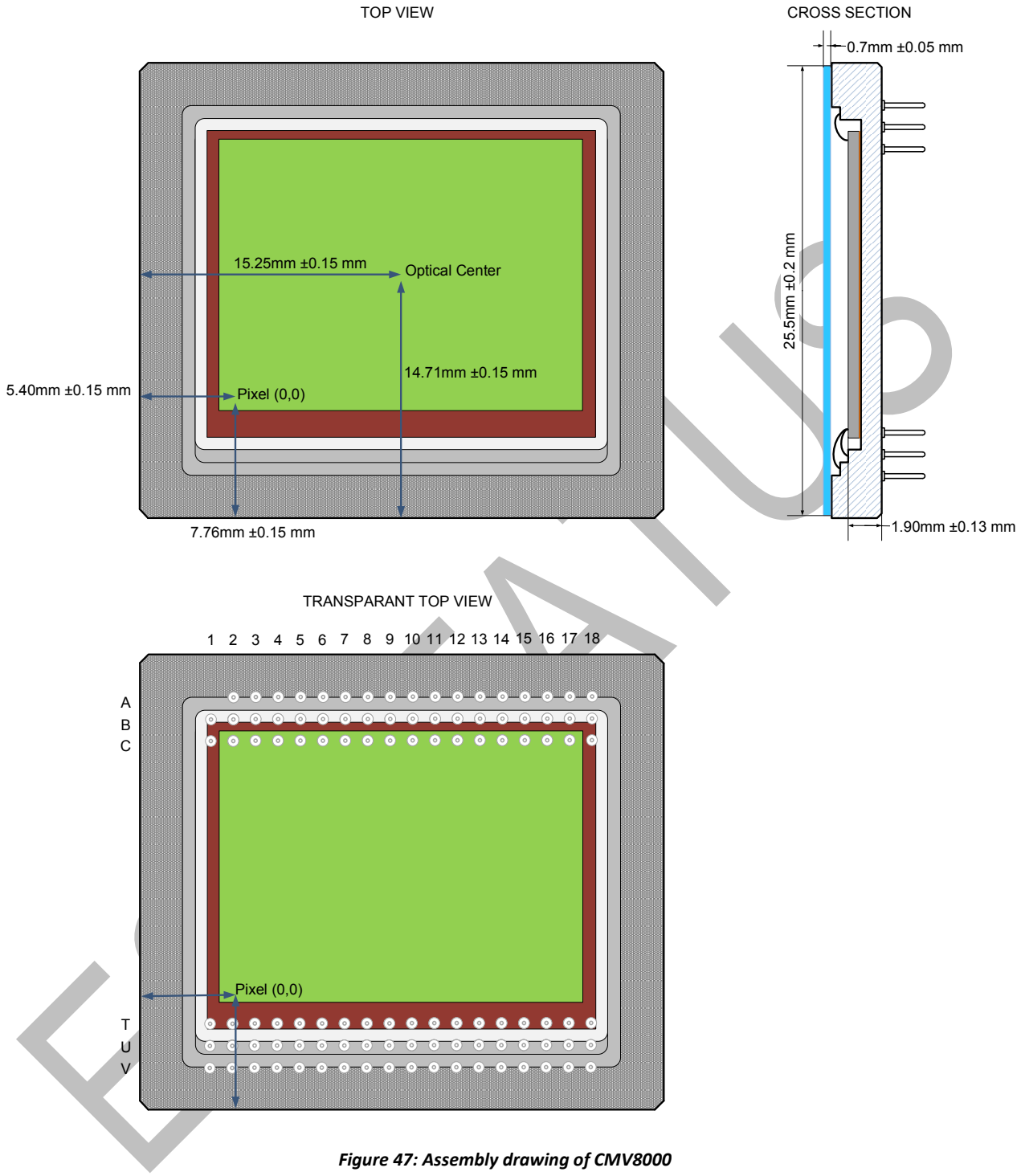

Figure 47: Assembly drawing of CMV8000

7.3 COVER GLASS

The cover glass of the CMV8000 is D263 glass coated with an anti-reflective coating to increase transmittance to at least 97% between 400nm and 900nm. The transmittance curve is shown in Figure 48. Refraction index of the glass is 1.52. Scratch, bubbles and digs shall be less than or equal to 0.02mm. When a color sensor is used, an IR-cutoff filter should be placed in the optical path of the sensor.

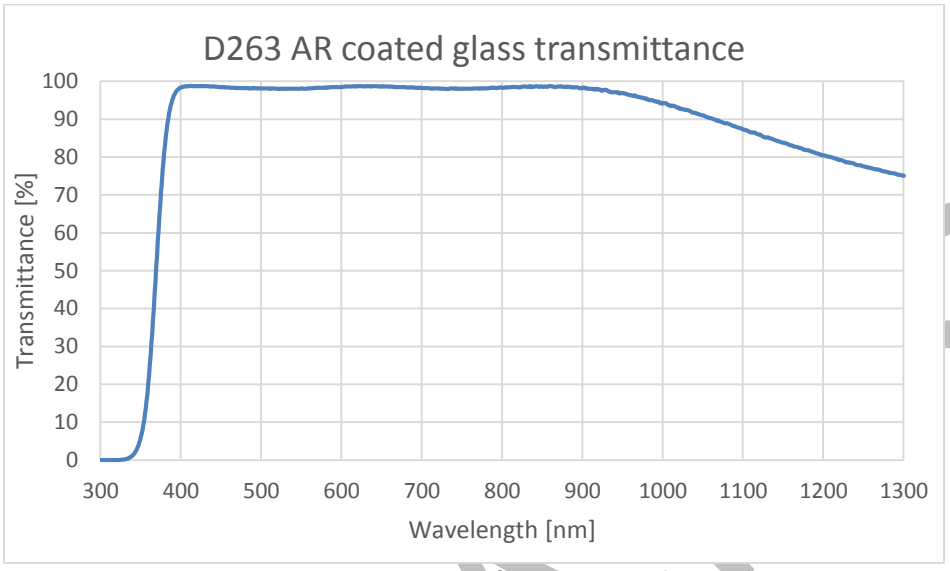

Figure 48: Transmittance curve of D263 AR-coated cover glass

7.4 COLOR FILTERS

When a color version of the CMV8000 is used, the color filters are applied in a Bayer pattern. The typical spectral response of the sensor with color filters and D263 cover glass can be found below. The use of an IR cut-off filter in the optical path of the CMV8000 image sensor is necessary to obtain good color separation when using light with an NIR component.

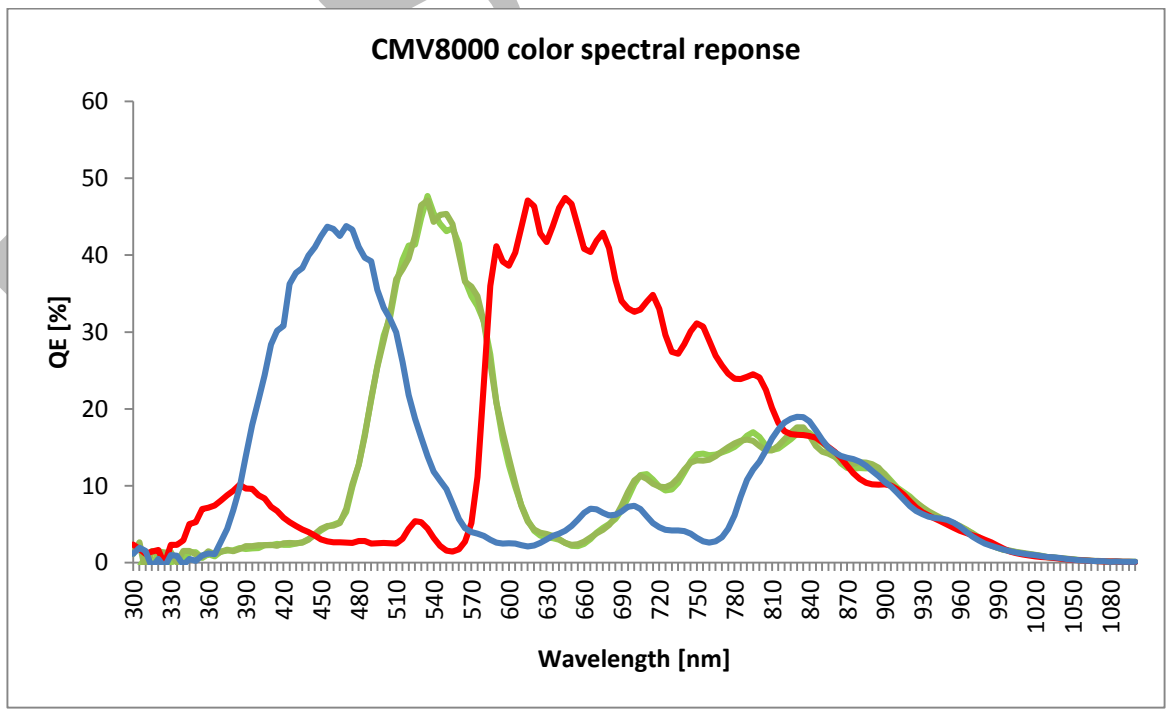

Figure 49: Typical spectral response of CMV8000 with RGB color filters and D263 cover glass

An RGB Bayer pattern is used on the CMV8000 image sensor. The order of the RGB filter can be found in the drawing below. With Y-mirroring off, pixel (0,0) at the top left is read out first and has a red filter. When Y-mirroring is on, pixel (0,2495) is read out first and has a green filter. For X- mirroring the address of the first read pixel depends on the output channels used, as described in Chapter 5.4.

The dark reference pixels are not pictured below as they don't contain image data.

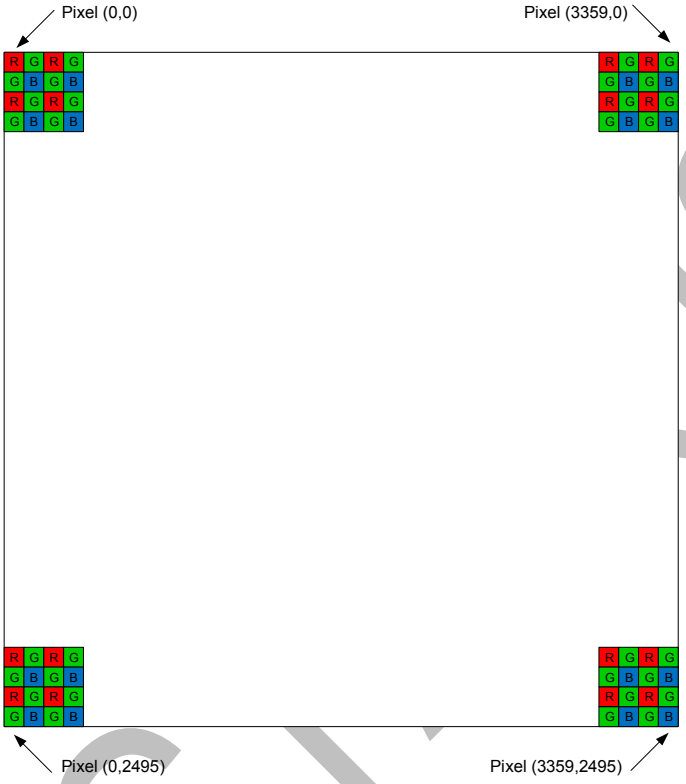

Figure 50: RGB Bayer pattern

8 RESPONSE CURVE

Below you can see a typical response curve of integration time (or light input) versus the average output value of the sensor.

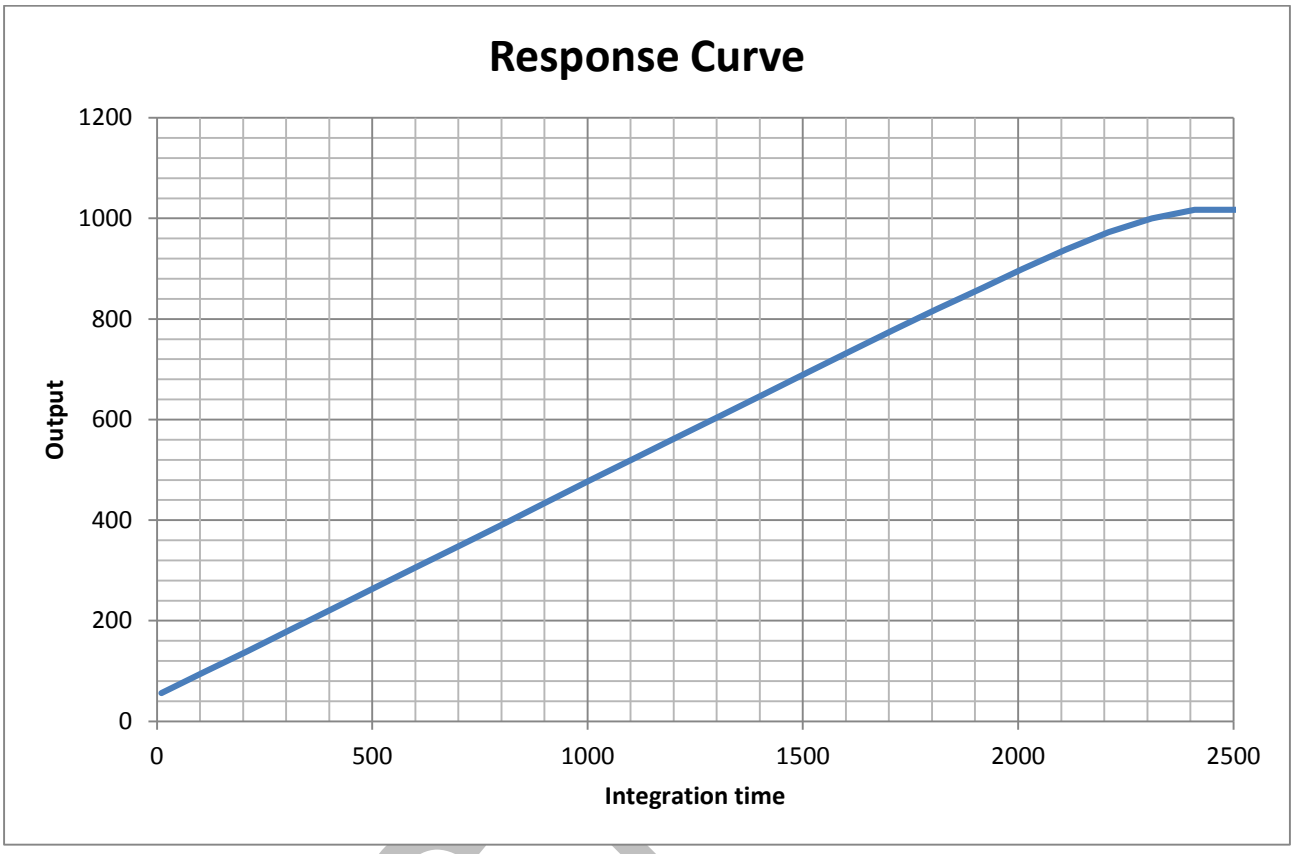

Figure 51: Typical response curve

9 SPECTRAL RESPONSE

The typical spectral response of a monochrome CMV8000 with microlenses can be found below.

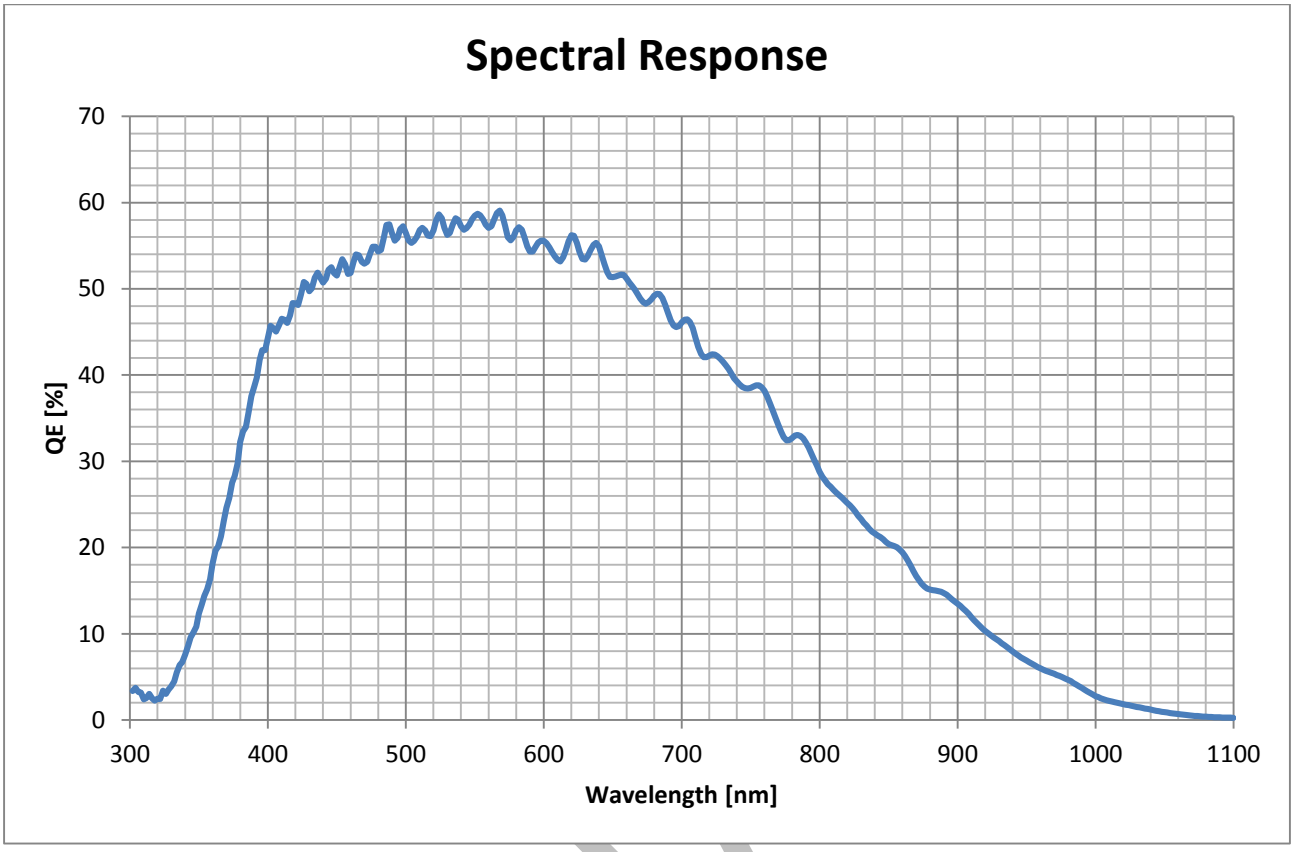

Figure 52: Typical spectral response

10 ANGULAR RESPONSE

The typical angular response for a CMV8000 sensor can be seen in the chart below, for a light wavelength of 650nm. The data includes the horizontal and vertical angles.

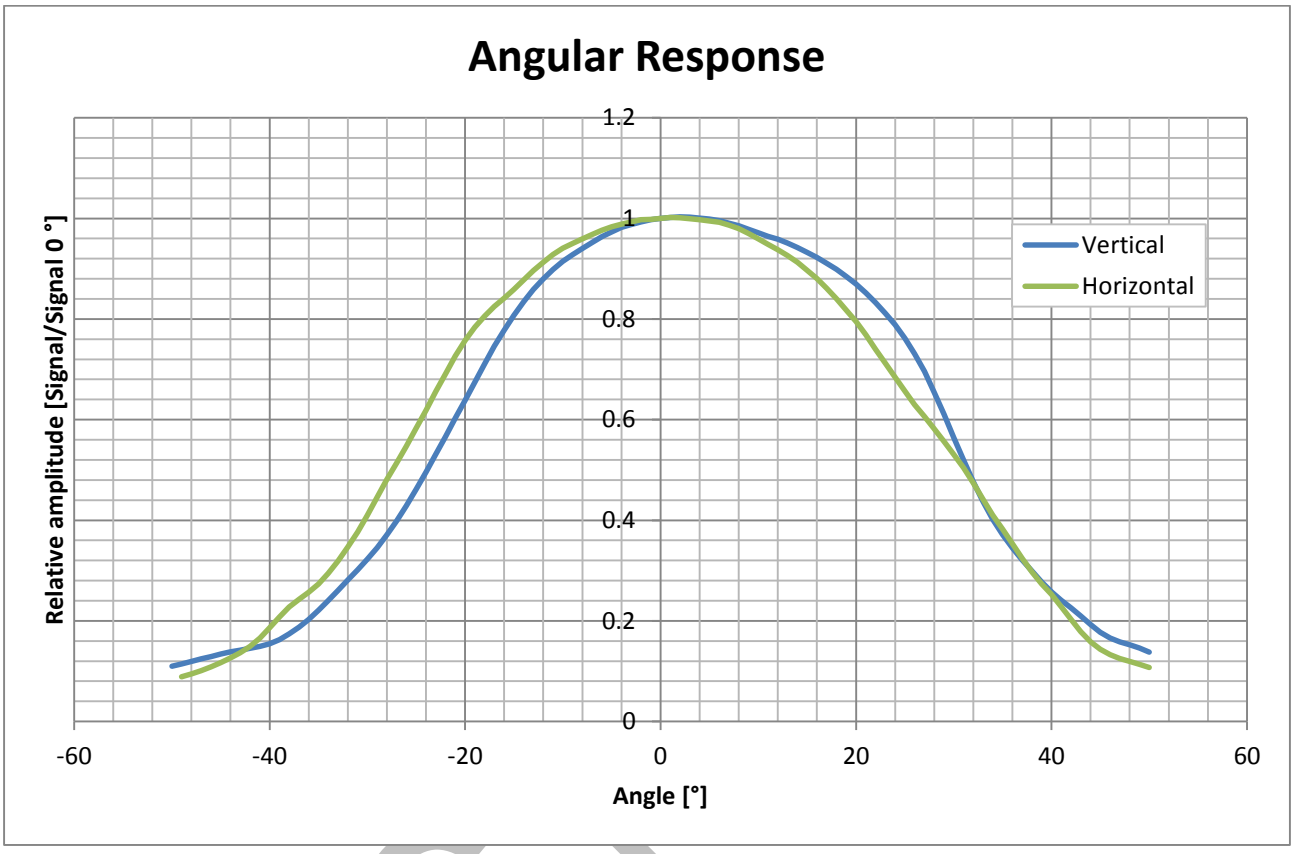

Figure 53: Horizontal and vertical angular response

11 PINNING

11.1 PIN LIST

The pin list of the CMV8000 can be found below. Analog and digital ground can be tied together.

Pin number	Pin name	Description	Type
A17	DNC	Do not connect!	\
B9	T_ANA	Analog test mux output	Analog output
A8	CMDN	Analog reference, decouple with 100nF to VSS33	Bias
A2	CMDN_COL_LOAD	Analog reference, decouple with 100nF to VSS33	Bias
B14	CMDN_COL_LOAD	Analog reference, decouple with 100nF to VSS33	Bias
A13	CMDN_COL_AMPL	Analog reference, decouple with 100nF to VSS33	Bias
A14	CMDN_COL_PC	Analog reference, decouple with 100nF to VSS33	Bias
B12	VTF_LOW1	Analog reference, decouple with 100nF to VSS33	Bias
A12	VTF_LOW2	Analog reference, decouple with 100nF to VSS33	Bias
B13	VTF_LOW3	Analog reference, decouple with 100nF to VSS33	Bias
A16	VBGAP	Analog reference, decouple with 100nF to VSS33	Bias
A9	VPC_L	Analog reference, decouple with 100nF to VSS33	Bias
B8	VPC_H	Analog reference, decouple with 100nF to VSS33	Bias
C16	VPC_COMP	Analog reference, decouple with 100nF to VSS33	Bias
B16	VREF	Analog reference, decouple with 100nF to VSS33	Bias
B17	VRAMP_SIG	Analog reference, decouple with 100nF to VSS33	Bias
C17	VRAMP_RES	Analog reference, decouple with 100nF to VSS33	Bias
B10	VRST_L	Analog reference, decouple with 100nF to VSS33	Bias
A7	CMDP	Analog reference, decouple with 100nF to VDD33	Bias
C15	CMDP_COMP	Analog reference, decouple with 100nF to VDD33	Bias
B7	CMDP_INV	Analog reference, decouple with 100nF to VDD33	Bias
B15	CMDP_RAMP	Analog reference, decouple with 100nF to VDD33	Bias
A15	CMDN_LVDS	Analog reference, decouple with 100nF to VSS18	Bias
C6	SYS_RESN	50Ω single ended, global sensor reset (active low)	Digital input
A3	F_REQ	50Ω single ended, frame request	Digital input
C4	INT2	50Ω single ended, used to set integration time externally	Digital input
B3	INT1	50Ω single ended, used to set integration time externally	Digital input
B5	SPI_ENABLE	50Ω single ended, SPI enable signal	Digital input
B4	SPI_CLK	50Ω single ended, SPI clock	Digital input
A4	SPI_IN	50Ω single ended, SPI input data	Digital input
A5	SPI_OUT	50Ω single ended, SPI output data	Digital output
B2	TDIG1	50Ω single ended, digital test mux 1	Digital output
C3	TDIG2	50Ω single ended, digital test mux 2	Digital output
T1	IN_LCLK_P	100Ω differential pairs	LVDS input
U1	IN_LCLK_N	100Ω differential pairs	LVDS input
T17	OUT_CLK_P	100Ω differential pairs	LVDS output
U17	OUT_CLK_N	100Ω differential pairs	LVDS output
U2	OUT_CTR_P	100Ω differential pairs	LVDS output
T2	OUT_CTR_N	100Ω differential pairs	LVDS output
U3	OUT1_P	100Ω differential pairs	LVDS output
T3	OUT1_N	100Ω differential pairs	LVDS output

Pin number	Pin name	Description	Type
T5	OUT3_P	100Ω differential pairs	LVDS output
T4	OUT3_N	100Ω differential pairs	LVDS output
V4	OUT5_P	100Ω differential pairs	LVDS output
U4	OUT5_N	100Ω differential pairs	LVDS output
V5	OUT7_P	100Ω differential pairs	LVDS output
U5	OUT7_N	100Ω differential pairs	LVDS output
T8	OUT9_P	100Ω differential pairs	LVDS output
T7	OUT9_N	100Ω differential pairs	LVDS output
V7	OUT11_P	100Ω differential pairs	LVDS output
U7	OUT11_N	100Ω differential pairs	LVDS output
V8	OUT13_P	100Ω differential pairs	LVDS output
U8	OUT13_N	100Ω differential pairs	LVDS output
V9	OUT15_P	100Ω differential pairs	LVDS output
U9	OUT15_N	100Ω differential pairs	LVDS output
V10	OUT17_P	100Ω differential pairs	LVDS output
U10	OUT17_N	100Ω differential pairs	LVDS output
T10	OUT19_P	100Ω differential pairs	LVDS output
T9	OUT19_N	100Ω differential pairs	LVDS output
T13	OUT21_P	100Ω differential pairs	LVDS output
T12	OUT21_N	100Ω differential pairs	LVDS output
V12	OUT23_P	100Ω differential pairs	LVDS output
U12	OUT23_N	100Ω differential pairs	LVDS output
V13	OUT25_P	100Ω differential pairs	LVDS output
U13	OUT25_N	100Ω differential pairs	LVDS output
V14	OUT27_P	100Ω differential pairs	LVDS output
U14	OUT27_N	100Ω differential pairs	LVDS output
V15	OUT29_P	100Ω differential pairs	LVDS output
U15	OUT29_N	100Ω differential pairs	LVDS output
T15	OUT31_P	100Ω differential pairs	LVDS output
T14	OUT31_N	100Ω differential pairs	LVDS output
T18	VDD18	Supply for ADC counters and on-chip logic	Supply
U6	VDD18	Supply for ADC counters and on-chip logic	Supply
U11	VDD18	Supply for ADC counters and on-chip logic	Supply
U16	VDD18	Supply for ADC counters and on-chip logic	Supply
V1	VDD18	Supply for ADC counters and on-chip logic	Supply
V17	VDD18	Supply for ADC counters and on-chip logic	Supply
B1	VDD18	Supply for ADC counters and on-chip logic	Supply
C1	VSS18	Ground for ADC counters and on-chip logic	Ground
V18	VSS18	Ground for ADC counters and on-chip logic	Ground
T6	VSS18	Ground for ADC counters and on-chip logic	Ground
T11	VSS18	Ground for ADC counters and on-chip logic	Ground
T16	VSS18	Ground for ADC counters and on-chip logic	Ground
U18	VSS18	Ground for ADC counters and on-chip logic	Ground
V3	VSS18	Ground for ADC counters and on-chip logic	Ground
V16	VSS18	Ground for ADC counters and on-chip logic	Ground
B11	VDDPIX	Supply for pixels	Supply

Pin number	Pin name	Description	Type
C7	VDDPIX	Supply for pixels	Supply
C10	VDDPIX	Supply for pixels	Supply
A6	VDDPIX	Supply for pixels	Supply
C14	VDDPIX	Supply for pixels	Supply
A10	VRST_H	Supply for reset drivers of pixels	Supply
B6	VDD33	Supply for sensitive analog circuits	Supply
C11	VDD33	Supply for sensitive analog circuits	Supply
C18	VDD33	Supply for sensitive analog circuits	Supply
V11	VDD33	Supply for sensitive analog circuits	Supply
V2	GND	Connect to ground	Ground
V6	VSS33	Ground for sensitive analog circuits and pixels	Ground
C12	VSS33	Ground for sensitive analog circuits and pixels	Ground
C13	VSS33	Ground for sensitive analog circuits and pixels	Ground
A11	VSS33	Ground for sensitive analog circuits and pixels	Ground
A18	VSS33	Ground for sensitive analog circuits and pixels	Ground
B18	VSS33	Ground for sensitive analog circuits and pixels	Ground
C2	VSS33	Ground for sensitive analog circuits and pixels	Ground
C5	VSS33	Ground for sensitive analog circuits and pixels	Ground
C8	VSS33	Ground for sensitive analog circuits and pixels	Ground
C9	VSS33	Ground for sensitive analog circuits and pixels	Ground

11.2 PIN LAYOUT

This is the pin layout seen from the top.

18	VSS33	VSS33	VDD33	VDD18	VSS18	VSS18
17	DNC	VRAMP_SIG	VRAMP_RES	OUT_CLK_P	OUT_CLK_N	VDD18
16	VBGAP	VREF	VPC_COMP	VSS18	VDD18	VSS18
15	CMDN_LVDS	CMDP_RAMP	CMDP_COMP	OUT31_P	OUT29_N	OUT29_P
14	CMDN_COL_PC	CMDN_COL_LOAD	VDDPIX	OUT31_N	OUT27_N	OUT27_P
13	CMDN_COL_AMPL	VTF_LOW3	VSS33	OUT21_P	OUT25_N	OUT25_P
12	VTF_LOW2	VTF_LOW1	VSS33	OUT21_N	OUT23_N	OUT23_P
11	VSS33	VDDPIX	VDD33	VSS18	VDD18	VDD33
10	VRST_H	VRST_L	VDDPIX	OUT19_P	OUT17_N	OUT17_P
9	VPC_L	T_ANA	VSS33	OUT19_N	OUT15_N	OUT15_P
8	CMDN	VPC_H	VSS33	OUT9_P	OUT13_N	OUT13_P
7	CMDP	CMDP_INV	VDDPIX	OUT9_N	OUT11_N	OUT11_P
6	VDDPIX	VDD33	SYS_RESN	VSS18	VDD18	VSS33
5	SPI_OUT	SPI_ENABLE	VSS33	OUT3_P	OUT7_N	OUT7_P
4	SPI_IN	SPI_CLK	INT2	OUT3_N	OUT5_N	OUT5_P
3	F_REQ	INT1	TDIG2	OUT1_N	OUT1_P	VSS18
2	CMDN_COL_LOAD	TDIG1	VSS33	OUT_CTR_N	OUT_CTR_P	GND
1		VDD18	VSS18	IN_LCLK_P	IN_LCLK_N	VDD18
	A	**B**	**C**	**T**	**U**	**V**

Figure 54: Pin layout

12 SPECIFICATION OVERVIEW

All values in the following table are typical.

Specification	Value	Comment
Total pixel array	2528 by 3584	Including black reference pixels
Active pixel array	2496 by 3360	Active pixels without black references
Pixel pitch	5.5 x 5.5 μm^2	
Optical format	1.43”	
Full well charge	11.7 Ke-	Pinned photodiode pixel
Conversion gain	0.077 LSB/e-	10 bit mode, unity gain
Sensitivity	5.56 V/lux.s 0.27 A/W	With microlenses @ 550nm
Temporal noise (analog domain)	8.6 e^-	Read-noise. Pipelined global shutter (GS) with correlated double sampling (CDS). Measured with high gain settings
Dynamic range	61 dB	
Pixel type	Global shutter pixel	Allows fixed pattern noise correction and reset (kTC) noise canceling through correlated double sampling.
Shutter type	Pipelined global shutter	Exposure of next image during read-out of the previous image.
Parasitic light sensitivity - Shutter efficiency	<1/20000 >99.995%	
Color filters	Optional	RGB Bayer pattern
Micro lenses	Yes	
Fill Factor	42%	w/o micro lens
QE * FF	60%	@ 550 nm with micro lenses.
Dark current signal	41.2 e^-/s	@ 25°C die temperature. The dark current doubles with every 6.5°C increase
DSNU	5.6 LSB/s	@ 25°C die temperature, in 10 bit mode.
Fixed pattern noise	<1 LSB RMS	<0.1% of full swing, 10 bit mode
PRNU	< 1% RMS of signal	
LVDS Output channels	16	Each data output running @ 600 Mbit/s. 8, 4 and 2 outputs selectable at reduced frame rate
Frame rate	103 frames/s	Using a 10bit/pixel and 600 Mbit/s data rate. Higher frame rate is possible in row windowing mode.
Timing generation	On-chip	Possibility to control exposure time through external pin.
PGA	Yes	5 analog gain settings
Programmable Registers	Sensor parameters	Window coordinates, Timing parameters, Gain & offset, Exposure time, mirrored read-out in X and Y direction …
Supported HDR modes	Interleaved integration times Piecewise linear response	Interleaved exposure times for different columns: Odd columns (double columns for color) have a different exposure compared to even columns (double columns for color). Final image is a combination of the two (through interpolation). Response curve with two knee points.
ADC	10 bit/12bit	Column ADC
Interface	LVDS	Serial output data + synchronization signals
I/O logic levels	LVDS = 1.8V Dig. I/O = 3.3V	
Supply voltages	1.98V 3.0V 3.3V	LVDS, ADC Pixel array supply Dig. I/O, SPI, PGA
Clock inputs	IN_LCLK_N/P SPI_CLK	Between 125 and 300MHz, LVDS Max. 60MHz

Specification	Value	Comment
Power	1200mW	Maximum over whole operating range
Package	Ceramic package	Custom ceramic µPGA (107-pins)
Operating range	-30°C to 70°C	Dark current and noise performance will degrade at higher temperature
Cover glass	D263	AR-coated glass, no IR cut-off filter on color devices
ESD	HBM Class 1C	JS-001-2012
RoHS/REACH	-	To be confirmed

13 ORDERING INFO

Part Number	Epi Thickness	Chroma	Microlens	Package	Glass
CMV8000ES-1E5M1PA	5 µm	Monochrome	Yes	Ceramic 107-pins µPGA	AR-coated
CMV8000ES-1E5C1PA	5 µm	RGB Bayer	Yes	Ceramic 107-pins µPGA	AR-coated

On request the package and cover glass can be customized. For options, pricing and delivery time please contact info@cmosis.com

13.1 ES QUALIFICATION

In the part number above, the letters “ES” stand for “engineering sample”.

The sensors with such an “ES” suffix are being delivered as “Engineering Sample” until the full qualification is performed. This includes all the reliability, quality and life cycle tests for all the variants of a product. Once this qualification is done, the “ES” label will be removed from the part number and the part will be in the “mass production” stage.

If the qualification tests are successfully concluded, the sensors with the “ES” label can be considered to be identical to the production devices in any mechanical and electro-optical way. There is no difference in defect specification between “ES” and “MP” devices and the same outgoing final test applies to both.

13.2 DEFECT SPECIFICATION

The defect specification for CMV8000 is available on demand. This document contains the criteria to which the CMV8000 sensors are tested prior to being shipped.

14 HANDLING AND SOLDERING PROCEDURE

14.1 SOLDERING

It is advised to bake the sensors prior to soldering. The bake condition would be 12h at +125°C. Afterwards, the sensors need to be soldered within the next 48hours (stored at <30°C and <60% RH).

14.1.1 MANUAL SOLDERING

Use partial heating method and use a soldering iron with temperature control. The soldering iron tip temperature is not to exceed 350°C with 270°C maximum pin temperature, 2 seconds maximum duration per pin. Avoid global heating of the ceramic package during soldering. Failure to do so may alter device performance and reliability.

14.1.2 REFLOW SOLDERING

The figure below shows the maximum recommended thermal profile for a reflow soldering system. If the temperature or time profile exceeds these recommendations, damage to the image sensor can occur. This reflow profile is based on Standard J-STD-020.

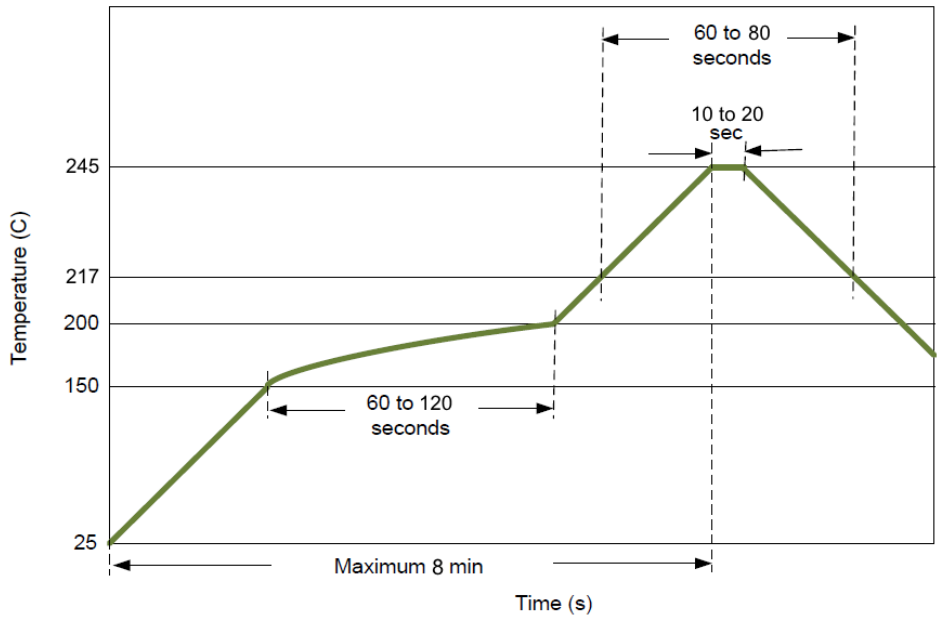

Figure 55: Reflow solder profile

14.1.3 SOLDERING RECOMMENDATIONS

Image sensors with filter arrays (CFA) and micro-lens are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. Best solution will be flow soldering or manual soldering of a socket (through hole or BGA) and plug in the sensor at latest stage of the assembly/test process. The BGA solution allows more flexibility for the routing of the camera PCB.

14.2 HANDLING IMAGE SENSORS

14.2.1 ESD

The CMV8000 has a HBM Class 1C ESD level. The following are the recommended minimum ESD requirements when handling image sensors.

1. Ground workspace (tables, floors…)
2. Ground handling personnel (wrist straps, special footwear…)
3. Minimize static charging (control humidity, use ionized air, and wear gloves…)

14.2.2 GLASS CLEANING

When cleaning of the cover glass is needed we recommend the following two methods.

1. Blowing off the particles with ionized nitrogen
2. Wipe clean using IPA (isopropyl alcohol) and ESD protective wipes.

14.2.3 IMAGE SENSOR STORING

Image sensors should be stored under the following conditions

1. Dust free
2. Temperature 20°C to 40°C
3. Humidity between 30% and 60%.
4. Avoid radiation, electromagnetic fields, ESD, mechanical stress

14.2.4 EXCESSIVE LIGHT

Excessive light falling on the sensor can cause heating up the micro lenses and color filters. This heat can cause deforming of the lenses and/or deterioration of the lenses and color filters by making them more opaque, increasing the heat up even more. Avoid shining high intensity light upon the sensors for extended periods of time. In case of lasers, they can cause heat up but can also damage the silicon die itself.

15 EVALUATION KIT

An evaluation kit for the CMV8000 is available, which you can rent or buy. The kit consists of a small form factor camera with a C-mount lens holder, a C-mount to F-mount adapter, and a 50mm F-mount lens. It can be connected to a PC via USB (cable included) or CameraLink. All software and user manuals for use through either interface are included with the kit. The lens, CameraLink cables, frame grabber and PC are not included with the kit. For more details you can contact info@cmosis.com.

Figure 56 CMV8000 evaluation kit

16 ADDITIONAL INFORMATION

For any additional questions related to the operation and specification of the CMV8000 sensors or feedback about this datasheet, please contact techsupport@cmosis.com.

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А