NCV70522DQ

Micro-Stepping Motor Driver

Introduction

The NCV70522DQ is a micro−stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and a SPI interface with an external microcontroller. The NCV70522DQ features an internal *current−translation table*: it takes the next micro−step depending on the clock signal on the *stepping input pin* (NXT) and the status of the *direction register* or input pin (DIR). A reliable current control is achieved using an integrated proprietary PWM algorithm.

The NCV70522DQ includes a so−called "*Speed and Load Angle*" (SLA) output, allowing the creation of stall detection algorithms and control loops to adjust torque and speed based on the motor's back electromotive force (BEMF).

The NCV70522DQ is implemented in I2T100 technology, enabling both high voltage analog circuitry and digital functionality on the same chip. The device is fully compatible with automotive voltage and temperature requirements and suited to general purpose stepper motor applications in the automotive, industrial, medical and marine domains.

Features

- Dual H−Bridge for 2 Phase Stepper Motors
- Programmable Peak−Current up to 1.2 A Continuous (1.5 A Short Time), Using a 5−Bit Current DAC
- On−Chip Current Translator
- SPI Interface
- Speed and Load−Angle Output
- 7 Step Modes from Full−Step up to 32 Micro−Steps
- Fully Integrated Current−Sense
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Active Fly−back Diodes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Digital IO's Compatible with 5 V and 3.3 V Microcontrollers
- Integrated 5 V Voltage Regulator to Supply an External Microcontroller
- Integrated Reset Function to Reset External Microcontroller
- Integrated Watchdog Function
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These are Pb−Free Devices*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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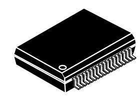
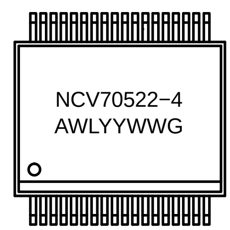


SSOP36 EP
DQ SUFFIX
CASE 940AB

MARKING DIAGRAM



NCV70522 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 27 of this data sheet.

February, 2015 − Rev. 2

Publication Order Number:
NCV70522DQ/D

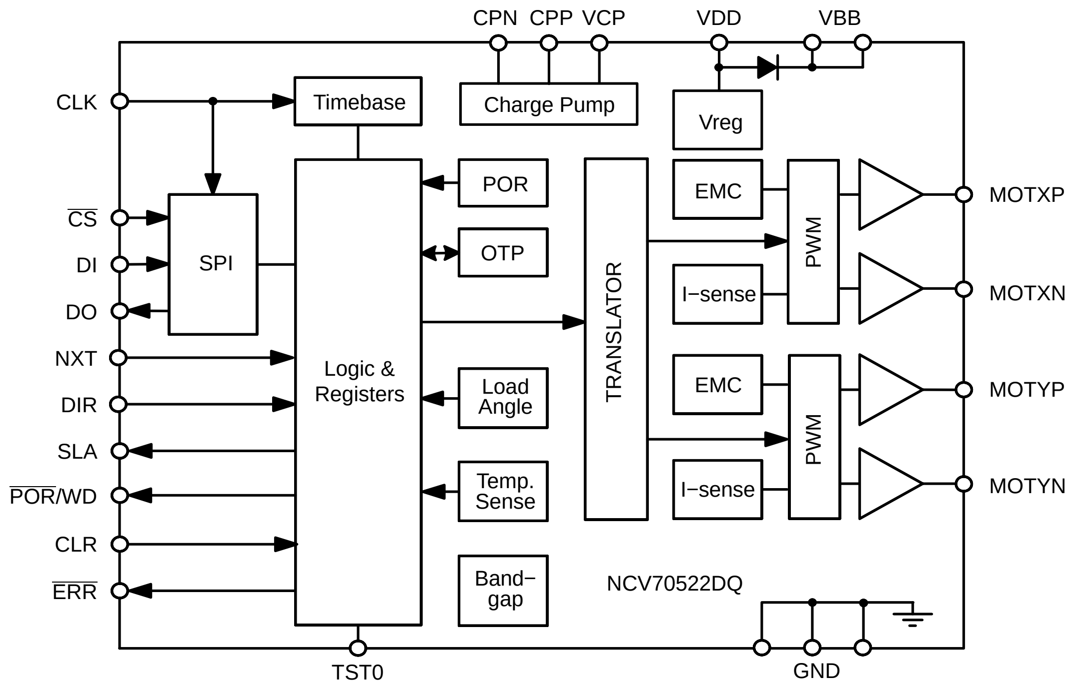


Figure 1. Block Diagram NCV70522DQ

Table 1. PIN DESCRIPTION

Name	Pin	Description	Type	Equivalent Schematic
$\overline{POR}$/WD	1	Power On Reset and Watchdog Reset Output	Digital Output	Type 4
TST0	2	Test Pin Input (to be Tied to Ground in Normal Operation)	Digital Input	
/	3, 19, 36	No Function (to be Tied to Ground)		
DO	4	SPI Data Output (Open Drain)	Digital Output	Type 4
VDD	5	Logic Supply Output (Needs External Decoupling Capacitor)	Supply	Type 3
GND	6	Ground	Supply	
DI	7	SPI Data In	Digital Input	Type 2
CLK	8	SPI Clock Input	Digital Input	Type 2
NXT	9	Next Micro−Step Input	Digital Input	Type 2
DIR	10	Direction Input	Digital Input	Type 2
$\overline{ERR}$	11	Error Output (Open Drain)	Digital Output	Type 4
SLA	12	Speed Load Angle Output	Analog Output	Type 5
/	13	No Function (to be Tied to Ground)		
CPN	14	Negative Connection of Charge Pump Capacitor	High Voltage	
CPP	15	Positive Connection of Charge Pump Capacitor	High Voltage	
VCP	16	Charge−Pump Filter−Capacitor	High Voltage	
CLR	17	"Clear" = Chip Reset Input	Digital Input	Type 1
$\overline{CS}$	18	SPI Chip Select Input	Digital Input	Type 2
VBB	20, 21	High Voltage Supply Input	Supply	Type 3
MOTYP	22, 23	Positive End of Phase Y Coil Output	Driver Output	
GND	24, 25	Ground	Supply	
MOTYN	26, 27	Negative End of Phase Y Coil Output	Driver Output	
MOTXN	28, 29	Negative End of Phase X Coil Output	Driver Output	
GND	30, 31	Ground	Supply	
MOTXP	32, 33	Positive End of Phase X Coil Output	Driver Output	
VBB	34, 35	High Voltage Supply Input	Supply	Type 3

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC Supply Voltage (Note 1)	−0.3	+40	V
T_{ST}	Storage Temperature	−55	+160	°C
T_J	Junction Temperature (Note 2)	−50	+175	°C
V_{ESD}	Electrostatic Discharges on Component Level, All Pins (Note 3)	−2	+2	kV
V_{ESD}	Electrostatic Discharges on Component Level, HiV Pins (Note 4)	−8	+8	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For limited time < 0.5 s
2. Circuit functionality not guaranteed.
3. Human Body Model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B)
4. HiV = High Voltage Pins MOTxx, V_{BB}, GND; Human Body Model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B)

Table 3. THERMAL RESISTANCE

Package	Thermal Resistance	Unit
	Junction−to−Exposed Pad	
SSOP36−EP	3.5	K/W

EQUIVALENT SCHEMATICS

The following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

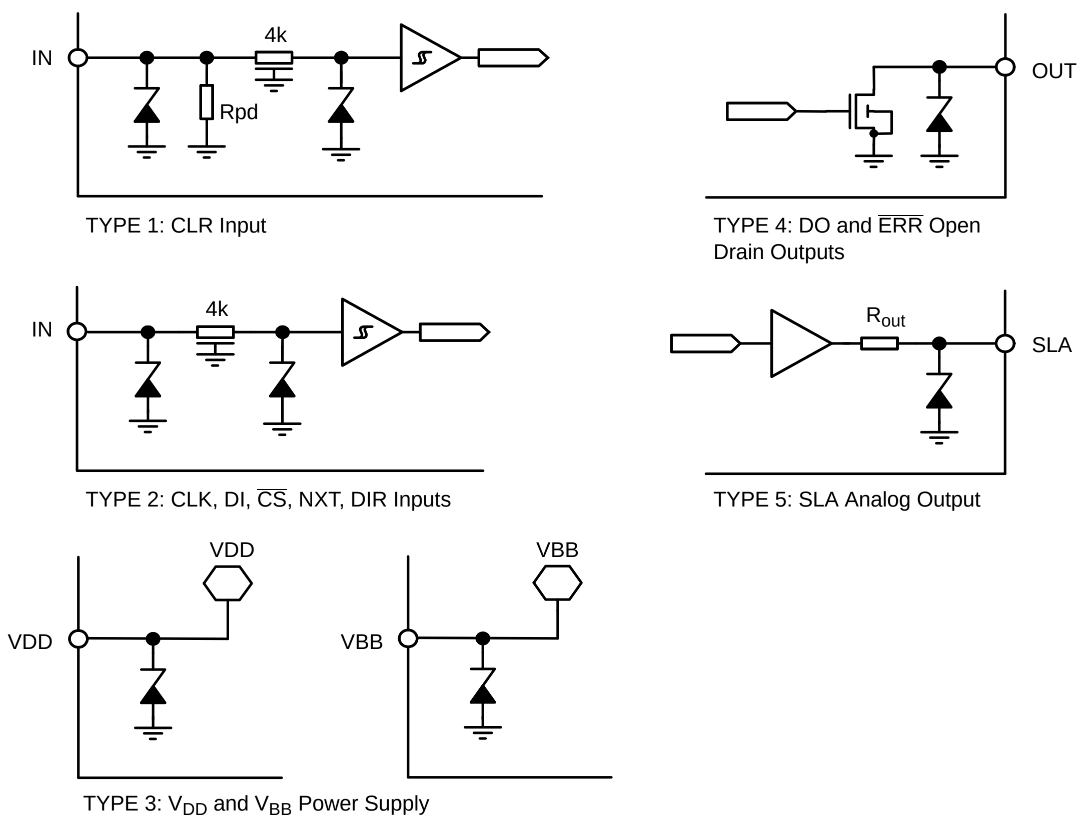
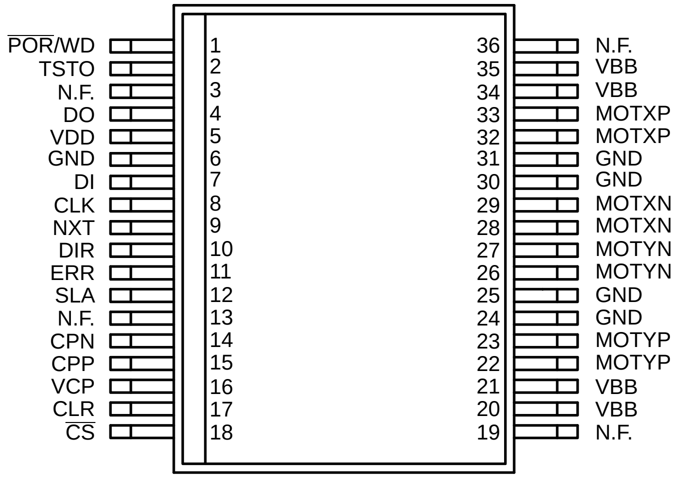


Figure 2. In− and Output Equivalent Diagrams

PACKAGE PIN DIAGRAM



ELECTRICAL SPECIFICATION

Recommended Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 5) is a substantial part of the operation conditions, hence the Customer must contact ON Semiconductor in order to mutually agree in writing on the allowed missions profile(s) in the application. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 4. OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC supply	+6	+30	V
T_J	Junction temperature	−40	+172 (Note 5)	°C

5. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.

Table 5. DC PARAMETERS
(The DC Parameters are Given for V_{BB} and Temperature in Their Operating Ranges Unless Otherwise Specified)
Convention: Currents Flowing in the Circuit are Defined as Positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
SUPPLY INPUTS							
V_{BB}	V_{BB}	Nominal Operating Supply Range		6		30	V
I_{BB}		Total Current Consumption	Unloaded Outputs			12	mA
I_{BBS}		Sleep Current in V_{BB} (Note 7)	Unloaded Outputs			400	µA
V_{DD}	V_{DD}	Logic Supply Output Voltage		4.5	5	5.5	V
I_{Load}		Maximum Output Current	6 V ≤ V_{BB} ≤ 8 V	15			mA
			8 V ≤ V_{BB} ≤ 30 V	40			mA
I_{DDLIM}		Current Limitation				150	mA
I_{Load_PD}		Output Current in Power Down Mode		1			mA
POWER ON RESET (POR) (Note 10)							
V_{DDH}	V_{DD}	Internal POR Comparator Threshold	V_{DD} Rising	3.6	4.20	4.5	V
V_{DDL}		Internal POR Comparator Threshold	V_{DD} Falling		3.85		V
V_{DDHYS}		Hysteresis Between V_{DDH} and V_{DDL}		0.10	0.35	0.60	V
MOTOR DRIVER							
$I_{MDmax,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max Peak Current Through Motor Coil	T_J = 125°C		1480		mA
$I_{MDmax,Peak}$		Max Peak Current Through Motor Coil	T_J = −40°C		1600		mA
I_{MDabs}		Absolute Error on Coil Current	T_J = 125°C and CUR[4:0] = 15...31	−10		10	%
I_{MDrel}		Error On Current Ratio I_{coilx}/I_{coily}		−7		7	%
I_{SET_TC1}		Temperature Coefficient of Coil Current Set−Level, CUR[4:0] = 0...27	T_J ≤ 160°C		−240		ppm/K
I_{SET_TC2}		Temperature Coefficient of Coil Current Set−Level, CUR[4:0] = 28...31	T_J ≤ 160°C		−490		ppm/K
R_{HS}		On−Resistance High−Side Driver, (Note 9) CUR[4:0] = 0...31	V_{BB} = 12 V, T_J = 27°C		0.45		Ω
			V_{BB} = 12 V, T_J = 160°C		0.94	1.25	Ω
R_{LS3}		On−Resistance Low−Side Driver, (Note 9) CUR[4:0] = 23...31	V_{BB} = 12 V, T_J = 27°C		0.45		Ω
			V_{BB} = 12 V, T_J = 160°C		0.94	1.25	Ω
R_{LS2}		On−Resistance Low−Side Driver, (Note 9) CUR[4:0] = 16...22	V_{BB} = 12 V, T_J = 27°C		0.90		Ω
			V_{BB} = 12 V, T_J = 160°C		1.9	2.5	Ω
R_{LS1}		On−Resistance Low−Side Driver, (Note 9) CUR[4:0] = 9...15	V_{BB} = 12 V, T_J = 27°C		1.8		Ω
			V_{BB} = 12 V, T_J = 160°C		3.8	5.0	Ω
R_{LS0}		On−Resistance Low−Side Driver, (Note 9) CUR[4:0] = 0...8	V_{BB} = 12 V, T_J = 27°C		3.6		Ω
			V_{BB} = 12 V, T_J = 160°C		7.5	10	Ω
I_{Mpd}		Pulldown Current	HiZ Mode		1		mA
DIGITAL INPUTS							
I_{leak}	DI, CLK NXT, DIR CLR, $\overline{CS}$	Input Leakage (Note 8)	T_J = 160°C			0.5	µA
V_{IL}		Logic Low Threshold	Tested at 1 MHz frequency	0		0.6	V
V_{IH}		Logic High Threshold	Tested at 1 MHz frequency	2.4		V_{DD}	V
R_{pd_CLR}	CLR	Internal Pulldown Resistor		120		300	kΩ
R_{pd_TST}	TST0	Internal Pulldown Resistor		3		9	kΩ

6. Current with oscillator running, all analogue cells active, SPI communication and NXT pulses applied. No floating inputs. Guaranteed by design.
7. Current with all analogue cells in power down. Logic is powered but no clocks running. All outputs unloaded, no inputs floating.
8. Not valid for pins with internal Pulldown resistor
9. Characterization Data Only
10. POR is derived from V_{DD}. For proper POR operation V_{BB} needs to be minimal V_{BB_min}.

Table 5. DC PARAMETERS
(The DC Parameters are Given for V_{BB} and Temperature in Their Operating Ranges Unless Otherwise Specified)
Convention: Currents Flowing in the Circuit are Defined as Positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUTS							
V_{OL}	DO, $\overline{ERR}$	Logic Low Level Open Drain	I_{OL} = 5 mA			0.30	V
THERMAL WARNING AND SHUTDOWN							
T_{tw}		Thermal Warning		138	145	152	°C
T_{tsd} (Notes 11, 12)		Thermal Shutdown			T_{tw} + 20		°C
CHARGE PUMP							
V_{cp}	VCP	Output Voltage	6 V ≤ V_{BB} ≤ 14 V		2 * V_{BB} − 2.5		V
			14 V < V_{BB} ≤ 30 V	V_{BB} + 9		V_{BB} + 16	
C_{buffer}		External Buffer Capacitor		180	220	470	nF
C_{pump}	CPP CPN	External Pump Capacitor		180	220	470	nF
SPEED AND LOAD ANGLE OUTPUT							
V_{out}	SLA	Output Voltage Range		0.2		V_{DD} − 0.2	V
V_{off}		Output Offset SLA Pin	SLAG = 0	−50		50	mV
			SLAG = 1	−50		50	mV
G_{sla}		Gain of SLA Pin = V_{BEMF} / V_{COIL}	SLAG = 0		0.5		
			SLAG = 1		0.25		
R_{out}		Output Resistance SLA Pin			0.23	1.0	kΩ
C_{load}		Load Capacitance SLA Pin				50	pF

11. No more than 100 cumulative hours in life time above T_{tw}
12. Thermal shutdown is derived from Thermal Warning

Table 6. AC PARAMETERS (The AC Parameters are Given for V_{BB} and Temperature in Their Operating Ranges)

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
INTERNAL OSCILLATOR							
f_{osc}		Frequency of Internal Oscillator		3.6	4.0	4.4	MHz
MOTORDRIVER							
f_{PWM}	MOTxx	PWM Frequency	Frequency Depends Only on Internal Oscillator	20.8	22.8	24.8	kHz
		Double PWM Frequency		41.6	45.6	49.6	kHz
f_d		PWM Jitter Depth (Note 13)			10		% f_{PWM}
tb_{rise}	MOTxx	Turn−On Voltage Slope, 10% to 90% (Note 13)	EMC[1:0] = 00		150		V/μs
			EMC[1:0] = 01		100		V/μs
			EMC[1:0] = 10		50		V/μs
tb_{fall}	MOTxx	Turn−off Voltage Slope, 90% to 10% (Note 13)	EMC[1:0] = 00		150		V/μs
			EMC[1:0] = 01		100		V/μs
			EMC[1:0] = 10		50		V/μs
DIGITAL OUTPUTS							
t_{H2L}	DO $\overline{ERR}$	Output Falltime from V_{inH} to V_{inL}	Capacitive Load 400 pF and Pullup Resistor of 1.5 kΩ			50	ns
CHARGE PUMP							
f_{CP}	CPN CPP	Charge Pump Frequency			250		kHz
t_{CPU}	MOTxx	Startup Time of Charge Pump (Note 14)	Spec External Components			5.0	ms
CLR FUNCTION							
t_{CLR}	CLR	Minimum Time for Hard Reset		100			μs
NXT FUNCTION							
t_{NXT_HI}	NXT	NXT Minimum, High Pulse Width	See Figure 3	2.0			μs
t_{NXT_LO}		NXT Minimum, Low Pulse Width	See Figure 3	2.0			μs
t_{DIR_SET}		NXT Hold Time, Following Change of DIR	See Figure 3		2.0		μs
t_{DIR_HOLD}		NXT Hold Time, Before Change of DIR	See Figure 3		2.0		μs
POWER UP							
t_{PU}	PORB/ WD	Power−Up Time	V_{BB} = 12 V, I_{LOAD} = 50 mA, C_{LOAD} = 220 nF			110	μs
t_{POR}		Reset Duration			100		ms
t_{RF}		Reset Filter Time			1.0		μs
WATCHDOG							
t_{WDTO}		Watchdog Time Out Interval		32		512	ms
t_{WDPR}		Prohibited Watchdog Acknowledge Delay			2.0		ms

13. Characterization Data Only
14. Guaranteed by design.

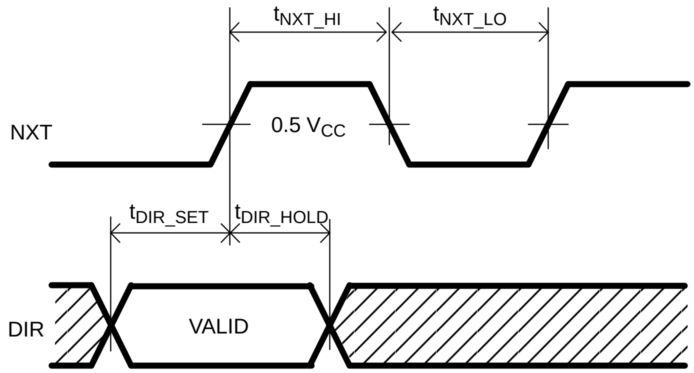


Figure 3. NXT−Input Timing Diagram

Table 7. SPI TIMING PARAMETERS

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}	SPI Clock Period	1			μs
t_{CLK_HIGH}	SPI Clock High Time	100			ns
t_{CLK_LOW}	SPI Clock Low Time	100			ns
t_{SET_DI}	DI Setup Time, Valid Data Before Rising Edge of CLK	50			ns
t_{HOLD_DI}	DI Hold Time, Hold Data After Rising Edge of CLK	50			ns
t_{CSB_HIGH}	$\overline{CS}$ High Time	2.5			μs
t_{SET_CSB}	$\overline{CS}$ Setup Time, $\overline{CS}$ Low Before Rising Edge of CLK	100			ns
t_{SET_CLK}	CLK Setup Time, CLK Low Before Rising Edge of $\overline{CS}$	100			ns

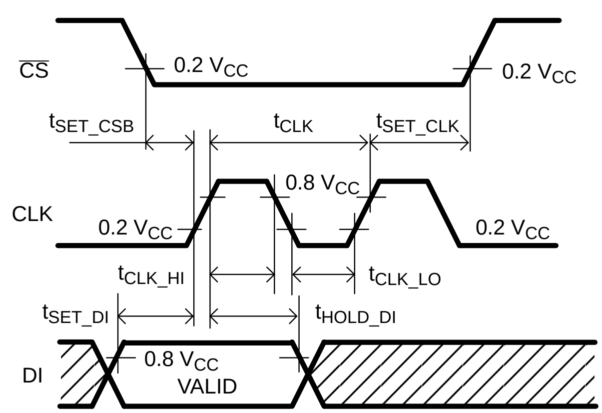


Figure 4. SPI Timing

TYPICAL APPLICATION SCHEMATIC

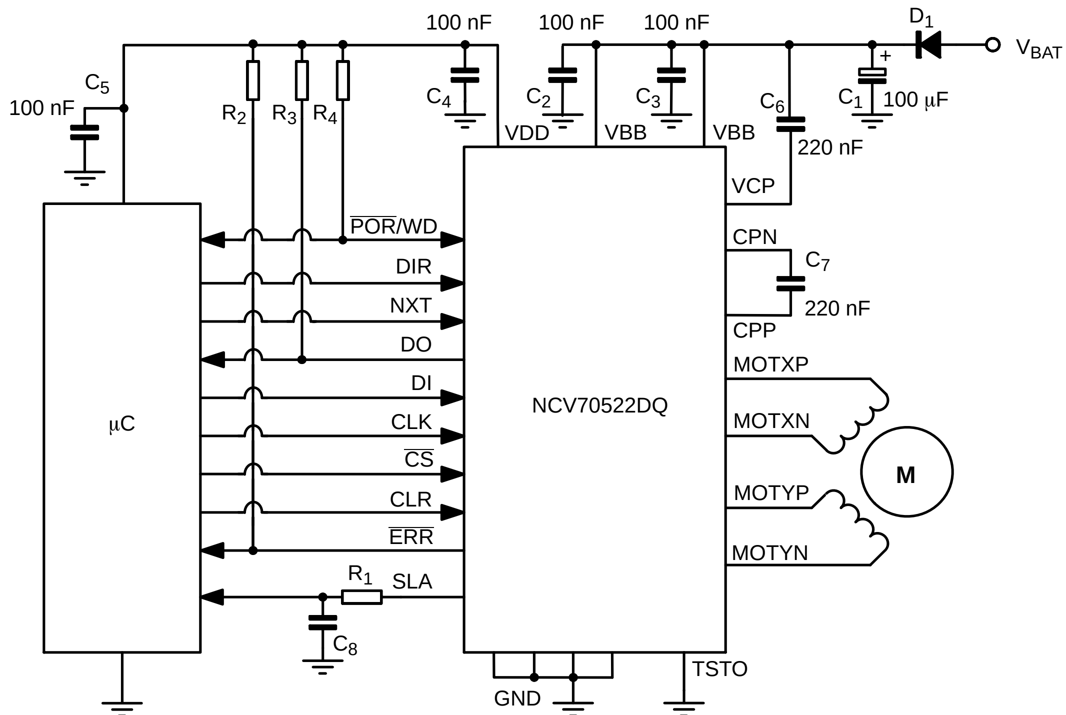


Figure 5. Typical Application Schematic NCV70522DQ

Table 8. EXTERNAL COMPONENTS LIST AND DESCRIPTION

Component	Function	Typ. Value	Tolerance	Unit
C_1	V_{BB} Buffer Capacitor (Low ESR < 1 Ω)	100	−20 +80%	μF
C_2, C_3	V_{BB} Decoupling Block Capacitor	100	−20 +80%	nF
C_4	V_{DD} Buffer Capacitor	220	± 20%	nF
C_5	V_{DD} Buffer Capacitor	100	± 20%	nF
C_6	Charge−Pump Buffer Capacitor	220	± 20%	nF
C_7	Charge−Pump Pumping Capacitor	220	± 20%	nF
C_8	Low Pass Filter SLA	1	± 20%	nF
R_1	Low Pass Filter SLA	5.6	± 1%	kΩ
R_2, R_3	Pullup Resistor Open Drain Output	4.7	± 1%	kΩ
D_1	Reverse Protection Diode	MURD530		

FUNCTIONAL DESCRIPTION

H−Bridge Drivers

A full H−bridge is integrated for each of the two stator windings. Each H−bridge consists of two low−side and two high−side N−type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (High−Impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H−bridge switches, it is guaranteed that the top− and bottom switches of the same half−bridge are never conductive simultaneously (interlock delay).

A two−stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched−off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate−drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (See Table 12 SPI Control Parameter Overview EMC[1:0]).

The power transistors are equipped with so−called “active diodes”: when a current is forced through the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain−bulk diode of the transistor.

Depending on the desired current range and the micro−step position at hand, the $R_{DS(on)}$ of the low−side transistors will be adapted such that excellent current−sense accuracy is maintained. The $R_{DS(on)}$ of the high−side transistors remain unchanged, see also the DC−parameter table for more details.

PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H−bridge switches. The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock.

The frequency of the PWM controller can be doubled to reduce the over−all current−ripple with a factor of two.

To further reduce the emission, an artificial jitter can be added to the PWM frequency. (see Table 12, SPI Control Register 1). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

Automatic Forward & Slow−Fast Decay

The PWM generation is in steady−state using a combination of forward and slow−decay. The absence of fast−decay in this mode, guarantees the lowest possible current−ripple “by design”. For transients to lower current levels, fast−decay is automatically activated to allow high−speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

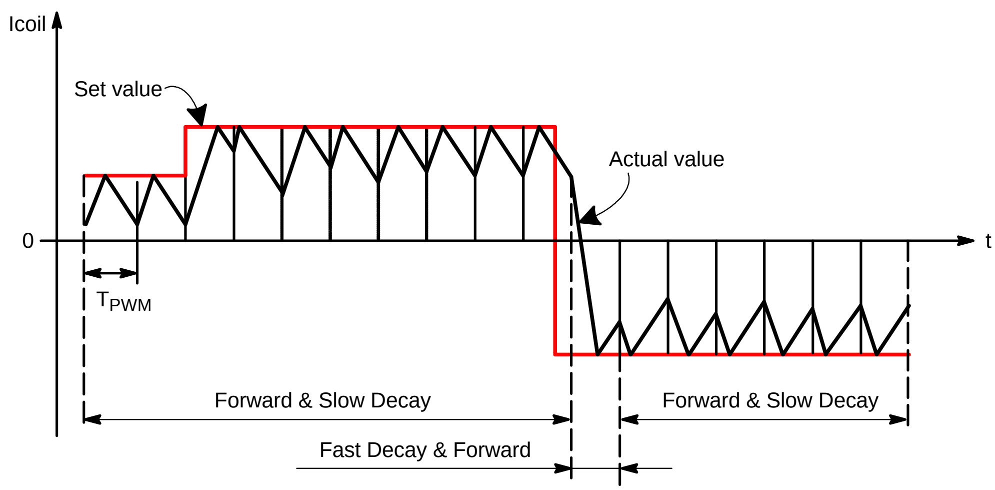


Figure 6. Forward & Slow/Fast Decay PWM

Automatic Duty Cycle Adaptation

In case the supply voltage is lower than 2*Bemf, then the duty cycle of the PWM is adapted automatically to >50% to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation.

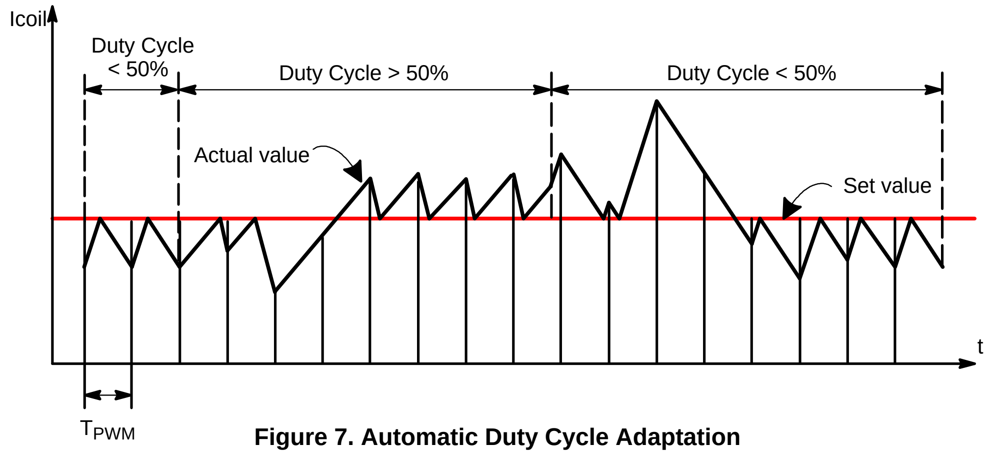


Figure 7. Automatic Duty Cycle Adaptation

Step Translator

Step Mode

The Step Translator provides the control of the motor by means of SPI register Stepmode: SM[2:0], SPI register DIRCNTRL and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given stepmode.

One out of 7 possible stepping modes can be selected through SPI−bits SM[2:0] (Table 12).

After power−on or hard reset, the coil−current translator is set to the default 1/32 micro−stepping at position '0'. Upon changing the Step Mode, the translator jumps to position 0* of the corresponding stepping mode. When remaining in the same Step Mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 10 lists the output current vs. the translator position.

As shown in Figure 8 the output current−pairs can be projected approximately on a circle in the (I_x,I_y) plane. There are however two exceptions: uncompensated half step and full step. In these stepmodes the currents are not regulated to a fraction of I_{max} but are in all intermediate steps regulated at 100%. In the (I_x,I_y) plane the current−pairs are projected on a square. Table 9 lists the output current vs. the translator position for these cases.

Table 9. SQUARE TRANSLATOR TABLE FOR FULL STEP AND UNCOMPENSATED HALF STEP

MSP[6:0]	Stepmode (SM[2:0])		% of I_{max}	
	101	110		
	Uncompensated Half−Step	Full Step	Coil x	Coil y
000 0000	0*	−	0	100
001 0000	1	1	100	100
010 0000	2	−	100	0
011 0000	3	2	100	−100
100 0000	4	−	0	−100
101 0000	5	3	−100	−100
110 0000	6	−	−100	0
111 0000	7	0	−100	100

Table 10. CIRCULAR TRANSLATOR TABLE

MSP[6:0]	Stepmode (SM[2:0])					% of I_{max}	
	000	001	010	011	100		
	1/32	1/16	1/8	1/4	1/2	Coil x	Coil y
000 0000	'0'	0*	0*	0*	0*	0	100
000 0001	1	–	–	–	–	3.5	98.8
000 0010	2	1	–	–	–	8.1	97.7
000 0011	3	–	–	–	–	12.7	96.5
000 0100	4	2	1	–	–	17.4	95.3
000 0101	5	–	–	–	–	22.1	94.1
000 0110	6	3	–	–	–	26.7	93
000 0111	7	–	–	–	–	31.4	91.8
000 1000	8	4	2	1	–	34.9	89.5
000 1001	9	–	–	–	–	38.3	87.2
000 1010	10	5	–	–	–	43	84.9
000 1011	11	–	–	–	–	46.5	82.6
000 1100	12	6	3	–	–	50	79
000 1101	13	–	–	–	–	54.6	75.5
000 1110	14	7	–	–	–	58.1	72.1
000 1111	15	–	–	–	–	61.6	68.6
001 0000	16	8	4	2	1	65.1	65.1
001 0001	17	–	–	–	–	68.6	61.6
001 0010	18	9	–	–	–	72.1	58.1
001 0011	19	–	–	–	–	75.5	54.6
001 0100	20	10	5	–	–	79	50
001 0101	21	–	–	–	–	82.6	46.5
001 0110	22	11	–	–	–	84.9	43
001 0111	23	–	–	–	–	87.2	38.3
001 1000	24	12	6	3	–	89.5	34.9
001 1001	25	–	–	–	–	91.8	31.4
001 1010	26	13	–	–	–	93	26.7
001 1011	27	–	–	–	–	94.1	22.1
001 1100	28	14	7	–	–	95.3	17.4
001 1101	29	–	–	–	–	96.5	12.7
001 1110	30	15	–	–	–	97.7	8.1
001 1111	31	–	–	–	–	98.8	3.5
010 0000	32	16	8	4	2	100	0
010 0001	33	–	–	–	–	98.8	−3.5
010 0010	34	17	–	–	–	97.7	−8.1
010 0011	35	–	–	–	–	96.5	−12.7
010 0100	36	18	9	–	–	95.3	−17.4
010 0101	37	–	–	–	–	94.1	−22.1
010 0110	38	19	–	–	–	93	−26.7
010 0111	39	–	–	–	–	91.8	−31.4
010 1000	40	20	10	5	–	89.5	−34.9
010 1001	41	–	–	–	–	87.2	−38.3
010 1010	42	21	–	–	–	84.9	−43
010 1011	43	–	–	–	–	82.6	−46.5
010 1100	44	22	11	–	–	79	−50
010 1101	45	–	–	–	–	75.5	−54.6
010 1110	46	23	–	–	–	72.1	−58.1
010 1111	47	–	–	–	–	68.6	−61.6
011 0000	48	24	12	6	3	65.1	−65.1
011 0001	49	–	–	–	–	61.6	−68.6
011 0010	50	25	–	–	–	58.1	−72.1
011 0011	51	–	–	–	–	54.6	−75.5
011 0100	52	26	13	–	–	50	−79
011 0101	53	–	–	–	–	46.5	−82.6
011 0110	54	27	–	–	–	43	−84.9
011 0111	55	–	–	–	–	38.3	−87.2
011 1000	56	28	14	7	–	34.9	−89.5
011 1001	57	–	–	–	–	31.4	−91.8
011 1010	58	29	–	–	–	26.7	−93
011 1011	59	–	–	–	–	22.1	−94.1
011 1100	60	30	15	–	–	17.4	−95.3
011 1101	61	–	–	–	–	12.7	−96.5
011 1110	62	31	–	–	–	8.1	−97.7

Table 10. CIRCULAR TRANSLATOR TABLE

	Stepmode (SM[2:0])					% of I_{max}	
	000	001	010	011	100		
MSP[6:0]	1/32	1/16	1/8	1/4	1/2	Coil x	Coil y
011 1111	63	−	−	−	−	3.5	−98.8
100 0000	64	32	16	8	4	0	−100
100 0001	65	−	−	−	−	−3.5	−98.8
100 0010	66	33	−	−	−	−8.1	−97.7
100 0011	67	−	−	−	−	−12.7	−96.5
100 0100	68	34	17	−	−	−17.4	−95.3
100 0101	69	−	−	−	−	−22.1	−94.1
100 0110	70	35	−	−	−	−26.7	−93
100 0111	71	−	−	−	−	−31.4	−91.8
100 1000	72	36	18	9	−	−34.9	−89.5
100 1001	73	−	−	−	−	−38.3	−87.2
100 1010	74	37	−	−	−	−43	−84.9
100 1011	75	−	−	−	−	−46.5	−82.6
100 1100	76	38	19	−	−	−50	−79
100 1101	77	−	−	−	−	−54.6	−75.5
100 1110	78	39	−	−	−	−58.1	−72.1
100 1111	79	−	−	−	−	−61.6	−68.6
101 0000	80	40	20	10	5	−65.1	−65.1
101 0001	81	−	−	−	−	−68.6	−61.6
101 0010	82	41	−	−	−	−72.1	−58.1
101 0011	83	−	−	−	−	−75.5	−54.6
101 0100	84	42	21	−	−	−79	−50
101 0101	85	−	−	−	−	−82.6	−46.5
101 0110	86	43	−	−	−	−84.9	−43
101 0111	87	−	−	−	−	−87.2	−38.3
101 1000	88	44	22	11	−	−89.5	−34.9
101 1001	89	−	−	−	−	−91.8	−31.4
101 1010	90	45	−	−	−	−93	−26.7
101 1011	91	−	−	−	−	−94.1	−22.1
101 1100	92	46	23	−	−	−95.3	−17.4
101 1101	93	−	−	−	−	−96.5	−12.7
101 1110	94	47	−	−	−	−97.7	−8.1
101 1111	95	−	−	−	−	−98.8	−3.5
110 0000	96	48	24	12	6	−100	0
110 0001	97	−	−	−	−	−98.8	3.5
110 0010	98	49	−	−	−	−97.7	8.1
110 0011	99	−	−	−	−	−96.5	12.7
110 0100	100	50	25	−	−	−95.3	17.4
110 0101	101	−	−	−	−	−94.1	22.1
110 0110	102	51	−	−	−	−93	26.7
110 0111	103	−	−	−	−	−91.8	31.4
110 1000	104	52	26	13	−	−89.5	34.9
110 1001	105	−	−	−	−	−87.2	38.3
110 1010	106	53	−	−	−	−84.9	43
110 1011	107	−	−	−	−	−82.6	46.5
110 1100	108	54	27	−	−	−79	50
110 1101	109	−	−	−	−	−75.5	54.6
110 1110	110	55	−	−	−	−72.1	58.1
110 1111	111	−	−	−	−	−68.6	61.6
111 0000	112	56	28	14	7	−65.1	65.1
111 0001	113	−	−	−	−	−61.6	68.6
111 0010	114	57	−	−	−	−58.1	72.1
111 0011	115	−	−	−	−	−54.6	75.5
111 0100	116	58	29	−	−	−50	79
111 0101	117	−	−	−	−	−46.5	82.6
111 0110	118	59	−	−	−	−43	84.9
111 0111	119	−	−	−	−	−38.3	87.2
111 1000	120	60	30	15	−	−34.9	89.5
111 1001	121	−	−	−	−	−31.4	91.8
111 1010	122	61	−	−	−	−26.7	93
111 1011	123	−	−	−	−	−22.1	94.1
111 1100	124	62	31	−	−	−17.4	95.3
111 1101	125	−	−	−	−	−12.7	96.5
111 1110	126	63	−	−	−	−8.1	97.7
111 1111	127	−	−	−	−	−3.5	98.8

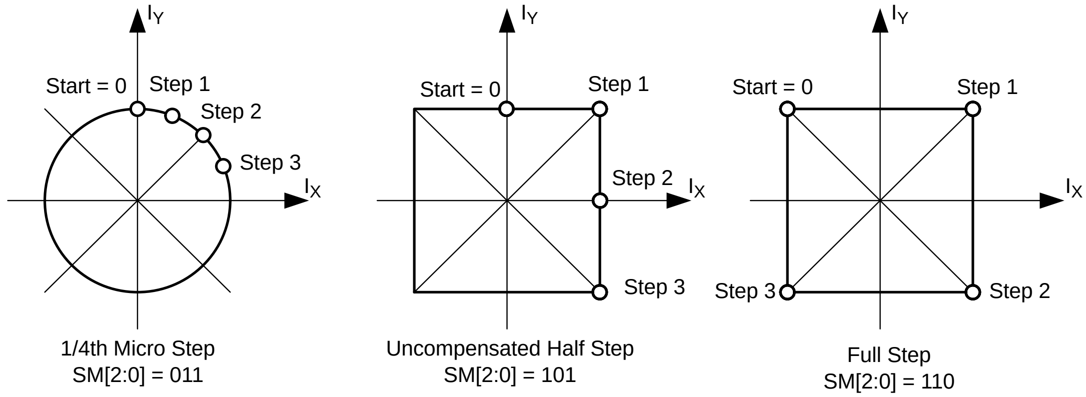


Figure 8. Translator Table: Circular and Square

Direction

The direction of rotation is selected by means of following combination of the DIR input pin and the SPI−controlled direction bit `<DIRCTRL>` as illustrated in Table 12.

NXT Input

Changes on the NXT input will move the motor current one step up/down in the translator table (even when the motor is disabled). Depending on the NXT−polarity bit `<NXTP>` (see Table 12), the next step is initiated either on the rising edge or the falling edge of the NXT input.

Translator Position

The translator position can be read in SPI Status Register 3. This is a 7−bit number equivalent to the 1/32th micro−step from Table 10: “Circular Translator Table” above. The translator position is updated immediately following a NXT trigger.

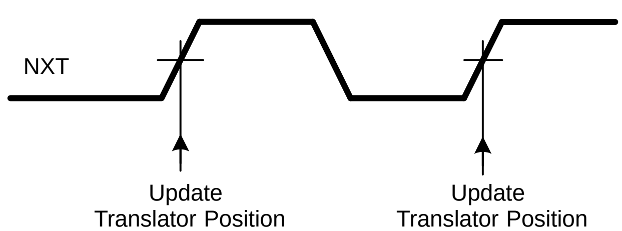


Figure 9. Translator Position Timing Diagram

Synchronization of Step Mode and NXT Input

When step mode is re−programmed to another resolution, (Figure 10), this is put in effect immediately upon the first arriving “NXT” input. If the micro−stepping resolution is increased, the coil currents will be regulated to the nearest micro−step, according to the fixed grid of the increased resolution. If however the micro−stepping resolution is decreased, then it is possible to introduce an offset (or phase shift) in the micro−step translator table.

If the step resolution is decreased at a translator table position that is shared both by the old and new resolution setting, then the offset is zero and micro−stepping proceeds according to the translator table.

If the translator position is **not** shared both by the old and new resolution setting, then the micro−stepping proceeds with an offset relative to the translator table (See Figure 10 right hand side).

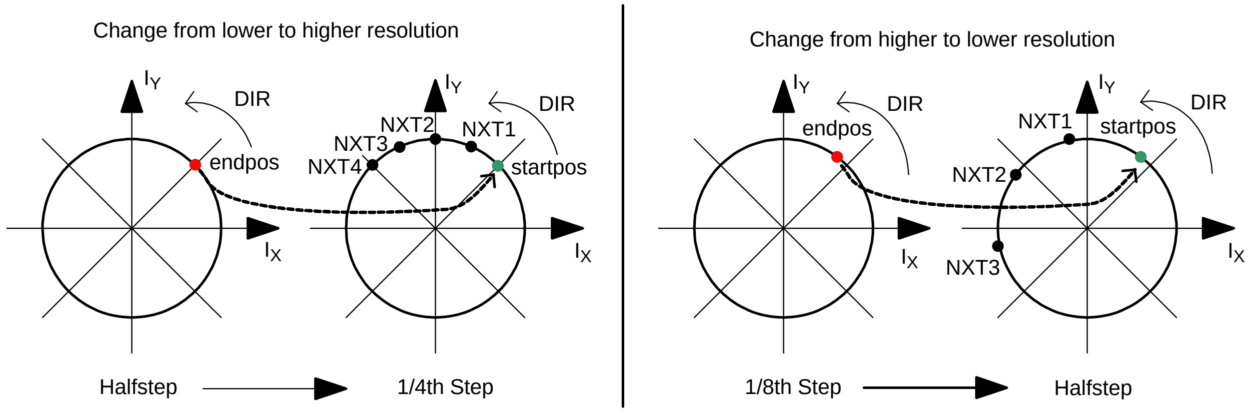


Figure 10. NXT−Step−Mode Synchronization

Left: change from lower to higher resolution. The left−hand side depicts the ending half−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the micro−step position.

Right: change from higher to lower resolution. The left−hand side depicts the ending micro−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the half−step position.

NOTE: It is advised to reduce the micro−stepping resolution only at micro−step positions that overlap with desired micro−step positions of the new resolution.

Programmable Peak−Current

The amplitude of the current waveform in the motor coils (coil peak current = I_{max}) is adjusted by means of an SPI parameter “CUR[4:0]” (Table 14). Whenever this parameter is changed, the coil−currents will be updated immediately at the next PWM period. Figure 11 presents the Peak−Current and Current Ranges in conjunction to the Current setting (CUR[4:0]).

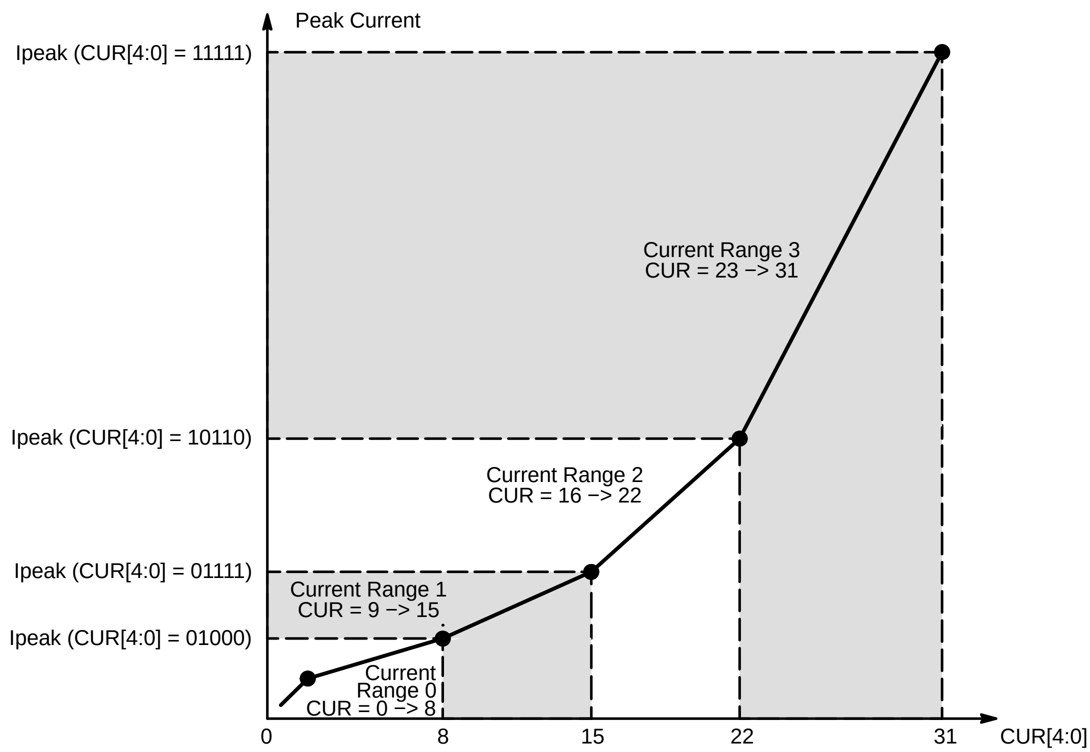


Figure 11. Programmable Peak−Current Overview

Speed and Load−Angle Output

The SLA−pin provides an output voltage that indicates the level of the Back−e.m.f. voltage of the motor. This Back−e.m.f. voltage is sampled during every so−called “coil current zero crossings”. Per coil, 2 zero−current positions exist per electrical period, yielding in total 4 zero−current observation points per electrical period.

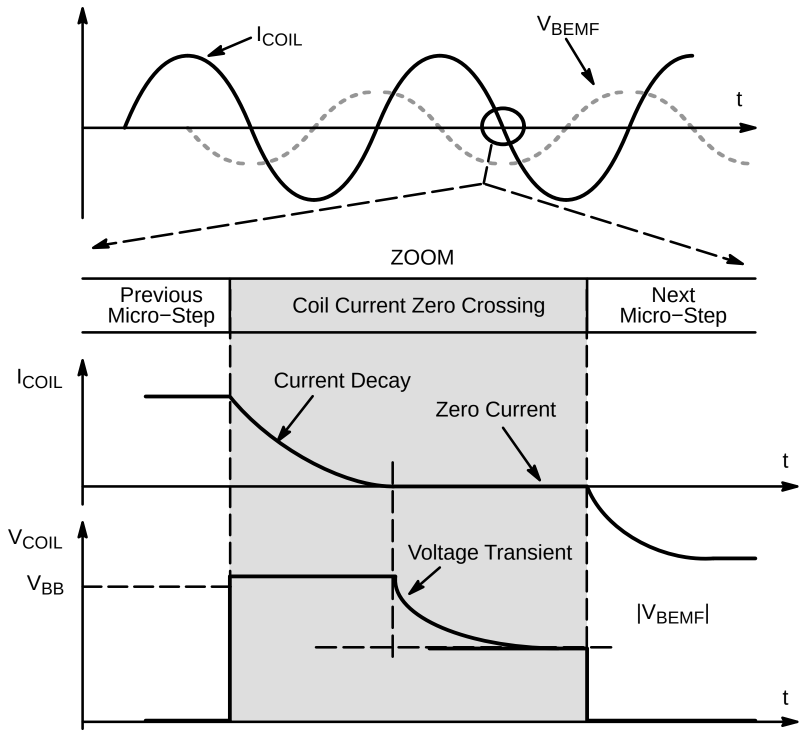


Figure 12. Principle of Bemf Measurement

Because of the relatively high re−circulation currents in the coil during current decay, the coil voltage V_{COIL} shows a transient behavior. As this transient is not always desired in application software, two operating modes can be selected by means of the bit <SLAT> (see “SLA−transparency” in Table 12). The SLA pin shows in “transparent mode” full visibility of the voltage transient behavior. This allows a sanity−check of the speed−setting versus motor operation and characteristics and supply voltage levels. If the bit “SLAT” is cleared, then only the voltage samples at the end of each coil current zero crossing are visible on the SLA−pin. Because the transient behavior of the coil voltage is not visible anymore, this mode generates smoother Back e.m.f. input for post−processing, e.g. by software.

In order to bring the sampled Back e.m.f. to a descent output level (0 V to 5 V), the sampled coil voltage V_{COIL} is divided by 2 or by 4. This divider is set through a SPI bit <SLAG>. (See Table 12)

The following drawing illustrates the operation of the SLA−pin and the transparency−bit. “PWMsh” and “Icoil=0” are internal signals that define together with SLAT the sampling and hold moments of the coil voltage.

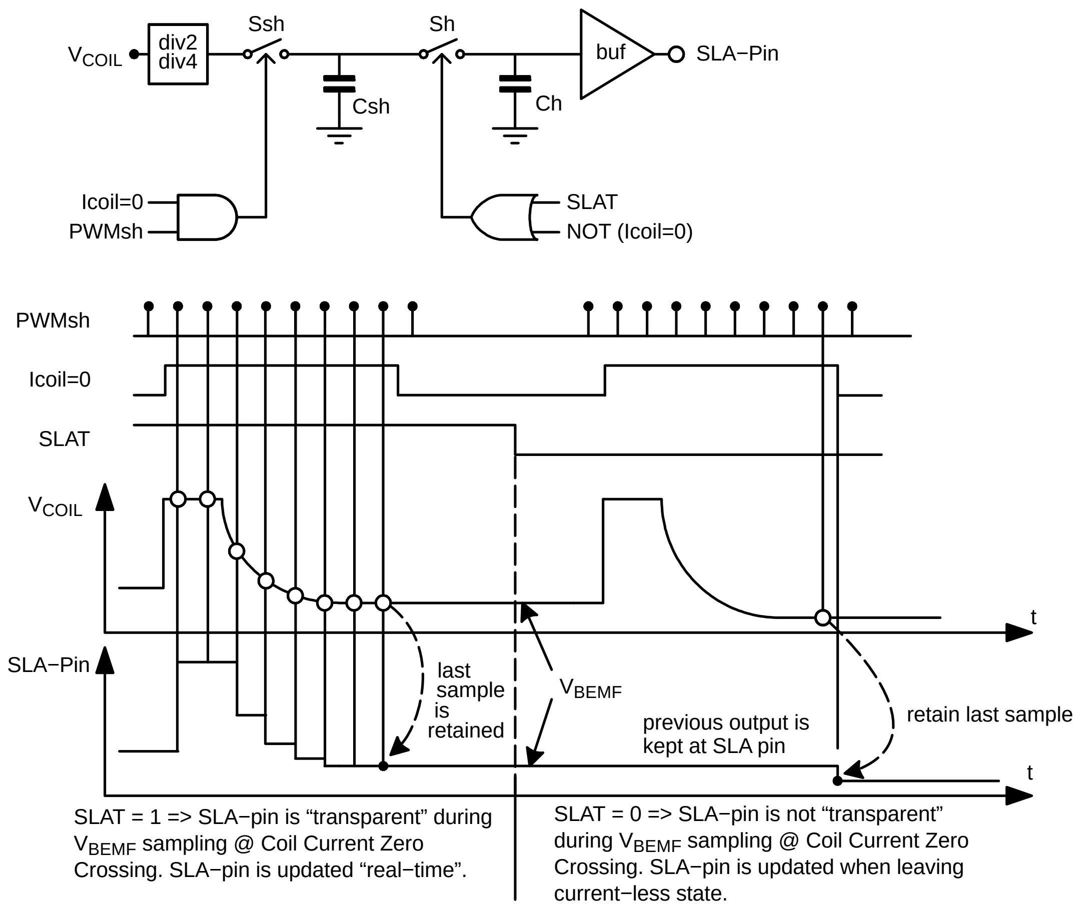


Figure 13. Timing Diagram of SLA−Pin

Warning, Error Detection and Diagnostics Feedback

Thermal Warning and Shutdown

When Junction temperature rises above T_{TW}, the thermal warning bit <TW> is set (Table 16 SPI Status Register 0). If junction temperature increases above thermal shutdown level, then the circuit goes in “Thermal Shutdown” mode (<TSD>) and all driver transistors are disabled (high impedance) (Table 16 SPI Status Register 2). The conditions to reset flag <TSD> is to be at a temperature lower than T_{TW} and to clear the <TSD> flag by reading it using any SPI read command.

Overcurrent Detection

The overcurrent detection circuit monitors the load current in each activated output stage. If the load current exceeds the overcurrent detection threshold, then the overcurrent flag is set and the drivers are switched off to reduce the power dissipation and to protect the integrated circuit. Each driver transistor has an individual detection bit in the Table 16 SPI Status Registers 1 and SPI Status Register 2 (<OVCXij> and <OVCYij>). Error condition is latched and the microcontroller needs to clear the status bits to reactivate the drivers.

Note: Successive reading the SPI Status Registers 1 and 2 in case of a short circuit condition, may lead to damage to the drivers.

Open Coil Detection

Open coil detection is based on the observation of 100% duty cycle of the PWM regulator. If in a coil 100% duty cycle is detected for longer than 32 ms the appropriate status bit in the SPI status register is set (<OPENX> or <OPENY>). (Table 16: SPI Status Register 0).

When the resistance of a motor coil is very large and the battery voltage is low, it can happen that the motor driver is not able to deliver the requested current to the motor. Under these conditions the PWM controller duty cycle will be 100% and after 32 ms, the error pin and <OPENX>, <OPENY> will flag this situation (motor current is kept alive). This feature can be used to test if the operating conditions (supply voltage, motor coil resistance) still allow reaching the requested coil−current or else the coil−current should be reduced.

Charge Pump Failure

The charge pump is an important circuit that guarantees low $R_{DS(on)}$ for all drivers, especially for low supply voltages. If the supply voltage is too low or external components are not properly connected to guarantee $R_{DS(on)}$ of the drivers, then the bit <CPFAIL> is set in the SPI Status Register 0. Also after power−on−reset the charge pump voltage will need some time to exceed the required threshold. During that time <CPFAIL> will be set to “1”.

Error Output

This is an open drain digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT($\overline{ERR}$) = <TW> OR <TSD> OR <OVCXij> OR <OVCYij> OR <OPENi> OR <CPFAIL>

Logic Supply Regulator

The NCV70522DQ has an on−chip 5 V low−drop regulator with external capacitor to supply the digital part of the chip, some low−voltage analog blocks and external circuitry. The voltage level is derived from an internal bandgap reference. To calculate the available drive−current for external circuitry, the specified I_{load} should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See Table 5.

Power−On Reset (POR) Function

The open drain output pin $\overline{POR}$/WD provides an “active low” reset for external purposes. At powerup of NCV70522DQ, this pin will be kept low for some time to reset for example an external microcontroller. A small analog filter avoids resetting due to spikes or noise on the V_{DD} supply.

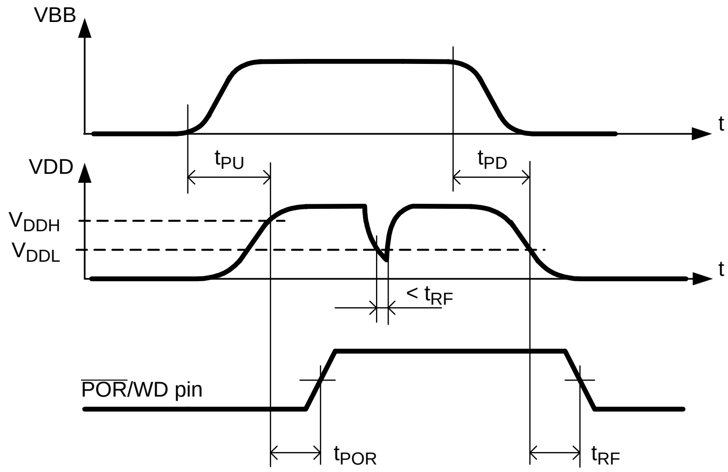


Figure 14. Power−on−Reset Timing Diagram

Watchdog Function

The watchdog function is enabled/disabled through <WDEN> bit (Table 13). Once this bit has been set to “1” (watchdog enable), the microcontroller needs to re−write this bit to clear an internal timer before the watchdog timeout interval expires. In case the timer is activated and WDEN is acknowledged too early (before t_{WDPR}) or not within the interval (after t_{WDTO}), then a reset of the microcontroller will occur through $\overline{POR}$/WD pin. In addition, a warm/cold boot bit <WD> is available in Table 16 for further processing when the external microcontroller is alive again.

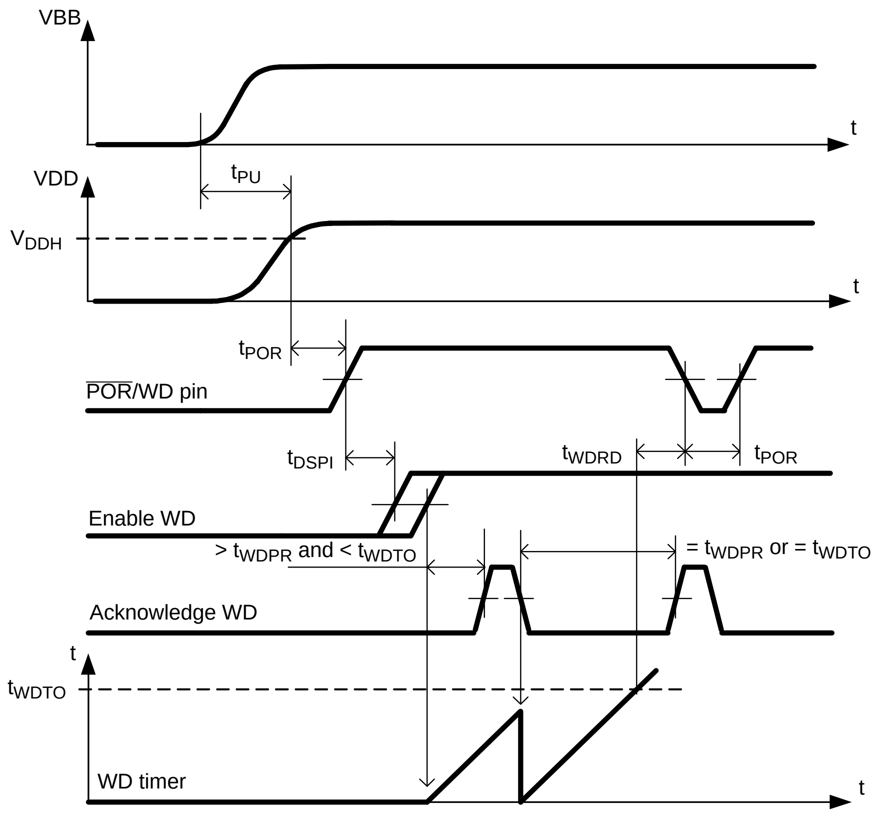


Figure 15. Watchdog Timing Diagram

Note: t_{DSPI} is the time needed by the external microcontroller to shift−in the <WDEN> bit after a power−up.

The duration of the watchdog timeout interval is programmable through the WDT[3:0] bits. The timing is given in Figure 15.

CLR Pin (=Hard Reset)

Logic 0 on CLR pin allows normal operation of the chip. To reset the complete digital inside the NCV70522DQ, the input CLR needs to be pulled to logic 1 during minimum time given by t_{CLR}. (See AC Parameters) This reset function clears all internal registers without the need of a power−cycle, except in sleep mode. The operation of all analog circuits is depending on the reset state of the digital, charge pump remains active. Logic 0 on CLR pin resumes normal operation again. The voltage regulator remains functional during and after the reset and the $\overline{\text{POR}}$/WD pin is not activated. Watchdog function is reset completely.

Sleep Mode

The bit <SLP> in SPI Control Register 2 is provided to enter a so−called "sleep mode". This mode allows reduction of current−consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low−power mode
- All internal registers are maintaining their logic content
- NXT and DIR inputs are ignored
- SPI communication remains possible (slight current increase during SPI communication)
- Oscillator and digital clocks are silent, except during SPI communication

Normal operation is resumed after writing logic '0' to bit <SLP>. A start−up time is needed for the charge pump to stabilize. After this time, NXT commands can be issued. When the device is in sleep mode and V_{BB} becomes lower than V_{BB_min} the device might reset.

SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with the NCV70522DQ. The implemented SPI block is designed to interface directly with numerous micro−controllers from several manufacturers. The NCV70522DQ acts always as a Slave and cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (NCV70522DQ), and DI signal is the output from the Master. A chip select line ($\overline{CS}$) allows individual selection of a Slave SPI device in a multiple− slave system. The $\overline{CS}$ line is active low. If the NCV70522DQ is not selected, DO is pulled up with the external pullup resistor. Since NCV70522DQ operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

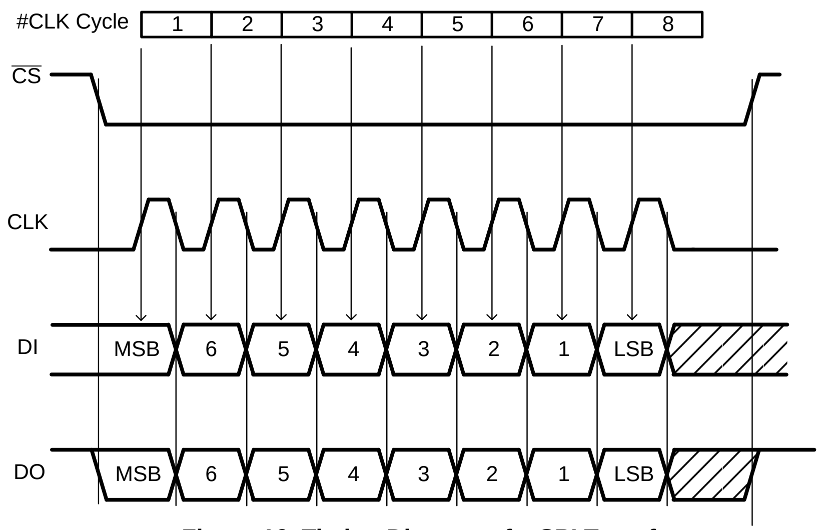


Figure 16. Timing Diagram of a SPI Transfer

NOTE: At the falling edge of the eighth clock pulse the data−out shift register is updated with the content of the addressed internal SPI register. The internal SPI registers are updated at the first rising edge of the NCV70522DQ system clock when $\overline{CS}$ = High.

Transfer Packet

Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more bytes.

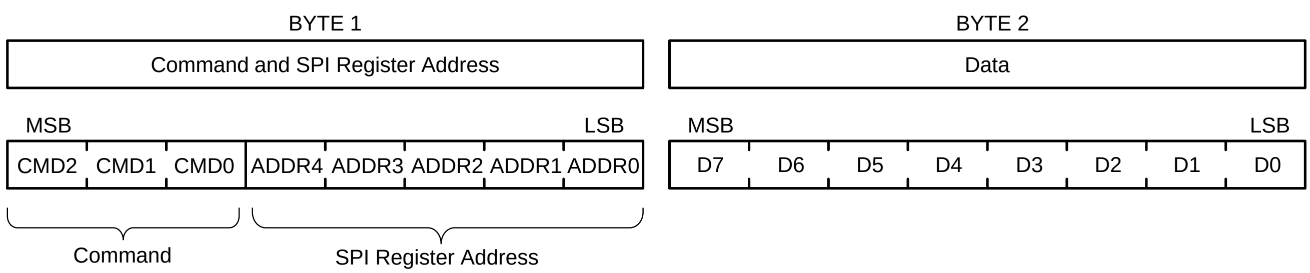


Figure 17. SPI Transfer Packet

Byte 1 contains the Command and the SPI Register Address and indicates to the NCV70522DQ the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from the NCV70522DQ in a READ operation.

Two command types can be distinguished in the communication between Master and NCV70522DQ:

- READ **from** SPI Register with address ADDR[4:0]: **CMD[2:0]** = “000”
- WRITE **to** SPI Register with address ADDR[4:0]: **CMD[2:0]** = “100”

READ Operation

If the Master wants to read data from Status or Control Registers, it initiates the communication by sending a READ command. This READ command contains the address of the SPI register to be read out. At the falling edge of the eighth clock pulse the data−out shift register is updated with the content of the corresponding internal SPI register. In the next 8−bit clock pulse train this data is shifted out via DO pin. At the same time the data shifted in from DI (Master) should be interpreted as the following successive command or dummy data.

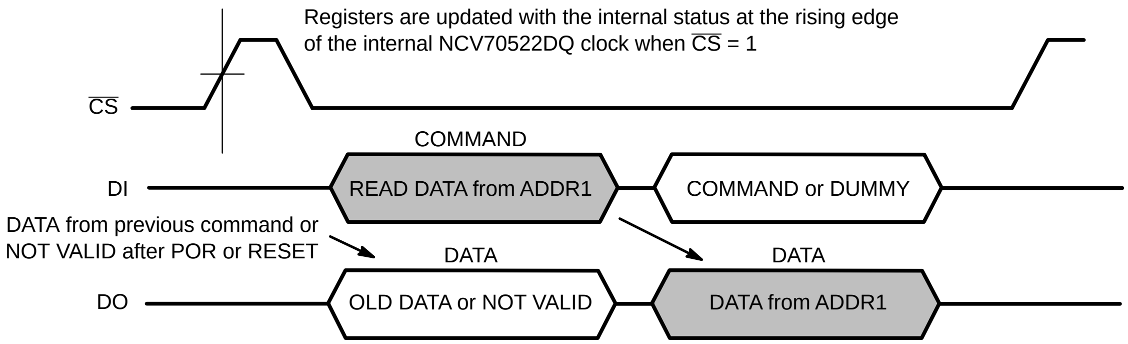


Figure 18. Single READ Operation where DATA from SPI Register with Address 1 is Read by the Master

All 4 Status Registers (see SPI Registers) contain 7 data bits and an even parity check bit. The most significant bit (D7) represents a parity of D[6:0]. If the number of logical ones in D[6:0] is odd, the parity bit D7 equals "1". If the number of logical ones in D[6:0] is even then the parity bit D7 equals "0". This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

Also the Control Registers can be read out following the same routine. Control Registers don't have a parity check.

The $\overline{CS}$ line is active low and may remain low between successive READ commands as illustrated in Figure 20. There is however one exception. In case an error condition is latched in one of Status Registers (see SPI Registers) the $\overline{ERR}$ pin is activated. (See the "Error Output" Section). This signal flags a problem to the external microcontroller. By reading the Status Registers information, the root cause of the problem can be determined. After this READ operation the Status Registers are cleared. Because the Status Registers and $\overline{ERR}$ pin (see SPI Registers) are only updated by the internal system clock when the $\overline{CS}$ line is high, the Master should force $\overline{CS}$ high immediately after the READ operation. For the same reason it is recommended to keep the $\overline{CS}$ line high always when the SPI bus is idle.

WRITE Operation

If the Master wants to write data to a Control Register it initiates the communication by sending a WRITE command. This contains the address of the SPI register to write to. The command is followed with a data byte. This incoming data will be stored in the corresponding Control Register after $\overline{CS}$ goes from low to high! NCV70522DQ responds on every incoming byte by shifting out via DO the data stored in the last received address.

It is important that the writing action (command − address and data) to the Control Register is exactly 16 bits long. If more or less bits are transmitted the complete transfer packet is ignored.

A WRITE command executed for a read−only register (e.g. Status Registers) will not affect the addressed register and the device operation.

Because after a power−on−reset the initial address is unknown the data shifted out via DO is not valid.

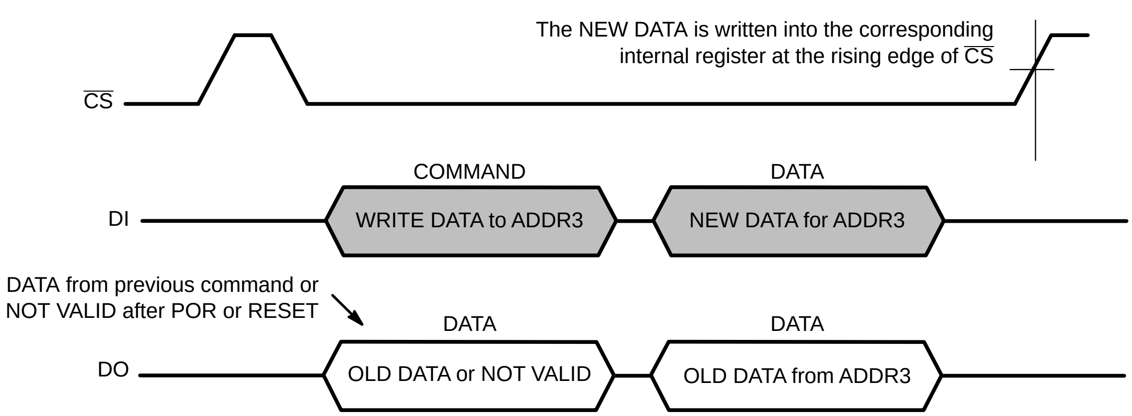


Figure 19. Single WRITE Operation where DATA from the Master is Written in SPI Register with Address 3

Examples of Combined READ and WRITE Operations

In the following examples successive READ and WRITE operations are combined. In Figure 20 the Master first reads the status from Register at ADDR4 and at ADDR5 followed by writing a control byte in Control Register at ADDR2. Note that during the write command (in Figures 19 and 20) the old data of the pointed register is returned at the moment the new data is shifted in.

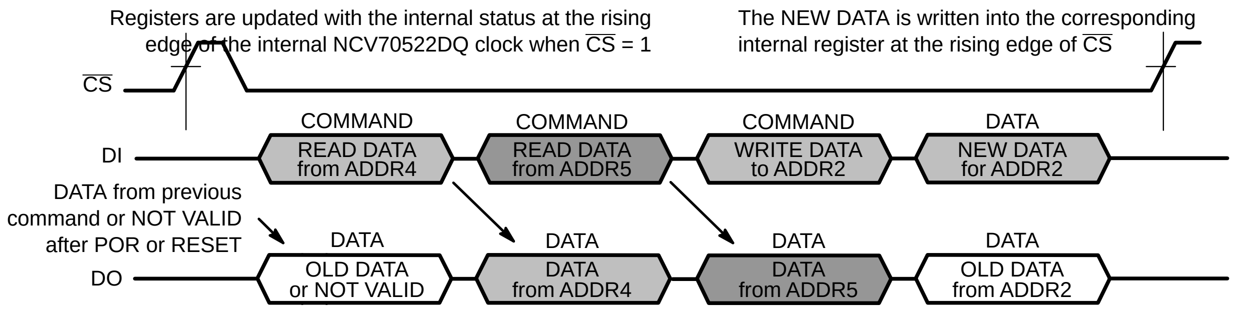


Figure 20. Two Successive READ Commands Followed by a WRITE Command

After the write operation the Master could initiate a read back command in order to verify if the data is correctly written, as illustrated in Figure 21. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is transmitted. This rule also applies when the master device wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when $\overline{CS}$ line is high, the first read out byte might represent old status information.

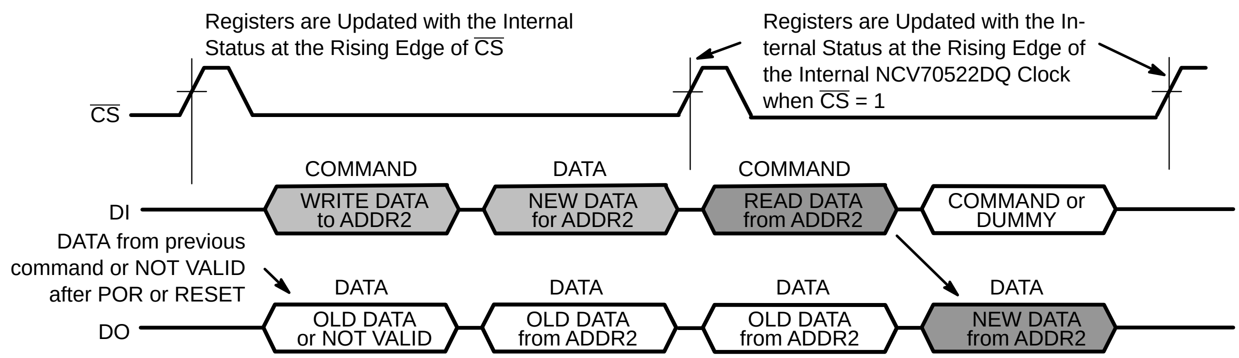


Figure 21. A WRITE Operation where DATA from the Master is Written in SPI Register with Address 2 Followed by a READ Back Operation to Verify a Correct WRITE Operation

NOTE: The internal data−out shift buffer of the NCV70522DQ is updated with the content of the selected SPI register only at the last (every eighth) falling edge of the CLK signal (see SPI Transfer Format and Pin Signals). As a result, new data for transmission cannot be written to the shift buffer at the beginning of the transfer packet and the first byte shifted out might represent old data.

Table 11. SPI CONTROL REGISTERS

(All SPI Control Registers have Read/Write Access and default to “0” after Power−on or hard reset)

Address		Structure							
	Content	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Access	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
	Reset	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
CRWD (00h)	Data	WDEN	WDT[3:0]				0	0	0
CR0 (01h)	Data	SM[2:0]			CUR[4:0]				
CR1 (02h)	Data	DIRCTRL	NXTP	−	−	PWMF	PWMJ	EMC[1:0]	
CR2 (03h)	Data	MOTEN	SLP	SLAG	SLAT	−	−	−	−

Where:

R/W: Read and Write access
Reset: Status after Power−On or hard reset
WDEN: Watchdog enable. Writing “0” to this bit will clear WD bit (see SPI Status Register 0)
WDT[3:0]: Watchdog timeout interval

Table 12. SPI CONTROL PARAMETER OVERVIEW

Symbol	Description	Status		Value
WDEN	Watchdog enable.	<WDEN> = 1	Writing “1” to this bit will enable the watchdog timer (if not enabled yet) or will clear this timer (if already enabled)	
		<WDEN> = 0	Writing “0” to this bit will disable the Watchdog	
DIRCTRL	Controls the Direction of Rotation (in Combination with Logic Level on Input DIR)	<DIR> = 0	<DIRCTRL> = 0	CW Motion
			<DIRCTRL> = 1	CCW Motion
		<DIR> = 1	<DIRCTRL> = 0	CCW Motion
			<DIRCTRL> = 1	CW Motion
EMC[1:0]	Turn On− and Turn−off Slopes (Note 15)	00	Very Fast	
		01	Fast	
		10	Slow	
		11	Very Slow	
MOTEN	Activates the Motor Driver Outputs	<MOTEN> = 0	Drivers Disabled	
		<MOTEN> = 1	Drivers Enabled	
NXTP	Selects if NXT triggers on Rising or Falling Edge	<NXTP> = 0	Trigger on Rising Edge	
		<NXTP> = 1	Trigger on Falling Edge	
PWMF	Enables Doubling of the PWM Frequency (Note 15)	<PWMF> = 0	Default Frequency	
		<PWMF> = 1	Double Frequency	
PWMJ	Enables Jitter PWM	<PWMJ> = 0	Jitter Disabled	
		<PWMJ> = 1	Jitter Enabled	
SM[2:0]	Stepmode	000	1/32 Micro Step	
		001	1/16 Micro Step	
		010	1/8 Micro Step	
		011	1/4 Micro Step	
		100	1/2 Compensated Half Step	
		101	1/2 Uncompensated Half Step	
		110	Full Step	
		111	n.a.	
SLAG	Speed Load Angle Gain Setting	<SLAG> = 0	Gain = 0.5	
		<SLAG> = 1	Gain = 0.25	
SLAT	Speed Load Angle Transparency Bit	<SLAT> = 0	SLA is NOT Transparent	
		<SLAT> = 1	SLA is Transparent	
SLP	Enables Sleep Mode	<SLP> = 0	Active Mode	
		<SLP> = 1	Sleep Mode	

15. The typical values can be found in Table 5: DC Parameters and Table 6: AC Parameters

WDT[3:0] Selects the watchdog timeout interval.

Table 13. WATCHDOG TIMEOUT INTERVAL AS FUNCTION OF WDT[3:0]

Index	WDT[3:0]				t_{WDTO} (ms)	Index	WDT[3:0]				t_{WDTO} (ms)
0	0	0	0	0	32	8	1	0	0	0	288
1	0	0	0	1	64	9	1	0	0	1	320
2	0	0	1	0	96	A	1	0	1	0	352
3	0	0	1	1	128	B	1	0	1	1	384
4	0	1	0	0	160	C	1	1	0	0	416
5	0	1	0	1	192	D	1	1	0	1	448
6	0	1	1	0	224	E	1	1	1	0	480
7	0	1	1	1	256	F	1	1	1	1	512

CUR[4:0] Selects IMCmax peak. This is the peak or amplitude of the regulated current waveform in the motor coils.

Table 14. SPI CONTROL PARAMETER OVERVIEW: CURRENT AMPLITUDE CUR[4:0]

Current Range (Note 17)	Index CUR[4:0]	Current (mA) (Note 16)	Current Range (Note 17)	Index CUR[4:0]	Current (mA) (Note 16)
0	0 00000	33	2	16 10000	365
	1 00001	64		17 10001	400
	2 00010	95		18 10010	440
	3 00011	104		19 10011	485
	4 00100	115		20 10100	530
	5 00101	126		21 10101	585
	6 00110	138		22 10110	630
	7 00111	153	3	23 10111	750
	8 01000	166		24 11000	825
1	9 01001	190		25 11001	895
	10 01010	205		26 11010	975
	11 01011	230		27 11011	1065
	12 01100	250		28 11100	1155
	13 01101	275		29 11101	1245
	14 01110	300		30 11110	1365
	15 01111	325		31 11111	1480

16. Typical current amplitude at T_J = 125°C.
17. Reducing the current over different current ranges might trigger overcurrent detection, please refer to dedicated application note for solutions.

SPI Status Register Description

All 4 SPI Status Registers have Read Access and are default to “0” after Power−on or hard reset.

Table 15. SPI STATUS REGISTERS

Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
SR0 04h	Data Not Latched	PAR	TW	CPfail	WD	OPENX	OPENY	−	−
SR1 05h	Data is Latched	PAR	OVCXPT	OVCXPB	OVCXNT	OVCXNB	−	−	−
SR2 06h	Data is Latched	PAR	OVCYPT	OVCYPB	OVCYYNT	OVCYNB	TSD	−	−
SR3 07h	Data Not Latched	PAR	MSP[6:0]						

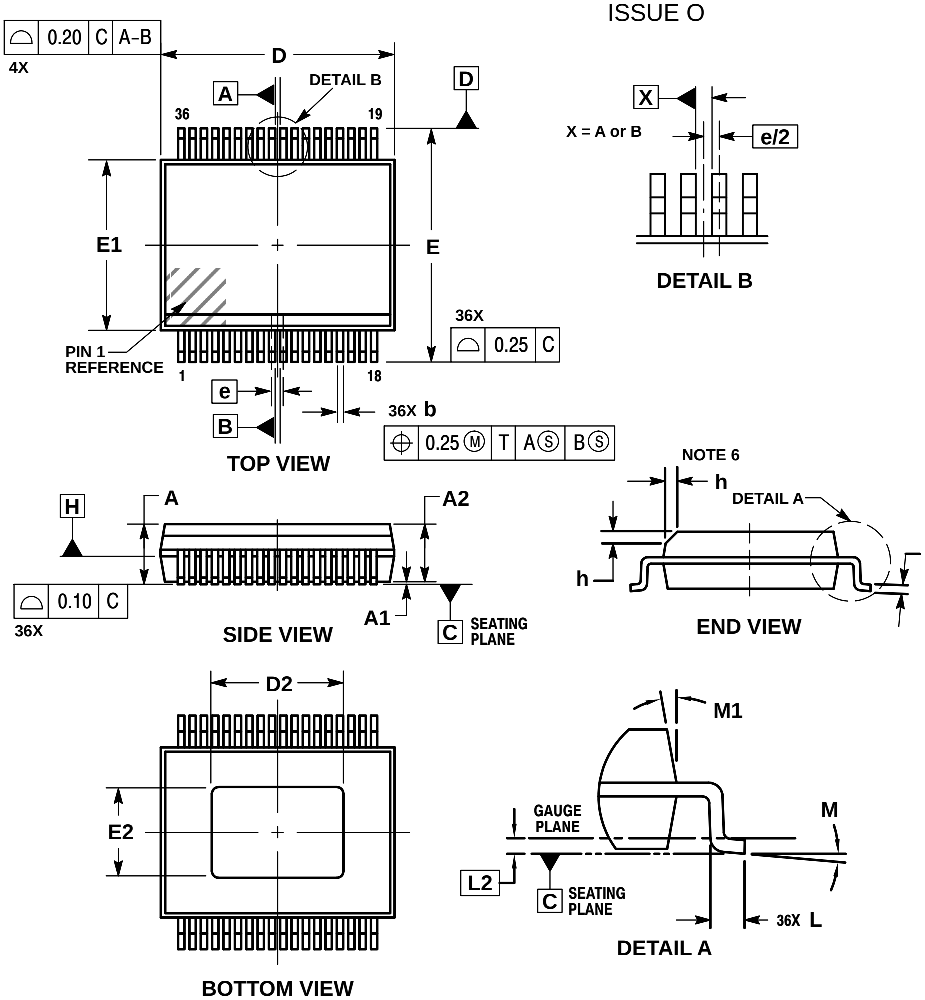
Where:
R: Read only mode access
Reset: Status after Power−On or hard reset
PAR: Parity check

Table 16. SPI STATUS FLAGS OVERVIEW

Mnemonic	Flag	Length (bit)	Related SPI Register	Comment	Reset State
CPFail	Charge Pump Failure	1	Status Register 0	'0' = no failure '1' = failure: indicates that the charge pump does not reach the required voltage level.	'0'
WD	Watchdog event	1	Status Register 0	This bit indicates the watchdog timer has not been cleared properly in time. If the master reads that WD is set to "1" after reset, it means that a watchdog re-set occurred (warm boot) instead of power−on−reset (cold boot). WD bit will be cleared only when the master writes "0" to WDEN bit.	'0'
MSP[6:0]	Micro Step Position	7	Status Register 3	Translator micro step position	'0000000'
OPENX	OPEN Coil X	1	Status Register 0	'1' = Open coil detected	'0'
OPENY	OPEN Coil Y	1	Status Register 0	'1' = Open coil detected	'0'
OVCXNB	Overcurrent at MOT**XN** Terminal; **B**ottom Transistor	1	Status Register 1	'0' = no failure '1' = failure: indicates that overcurrent is detected at bottom transistor XN−terminal	'0'
OVCXNT	Overcurrent at MOT**XN** Terminal; **T**op Transistor	1	Status Register 1	'0' = no failure '1' = failure: indicates that overcurrent is detected at top transistor XN−terminal	'0'
OVCXPB	Overcurrent at MOT**XP** Terminal; **B**ottom Transistor	1	Status Register 1	'0' = no failure '1' = failure: indicates that overcurrent is detected at bottom transistor XP−terminal	'0'
OVCXPT	Overcurrent at MOT**XP** Terminal; **T**op Transistor	1	Status Register 1	'0' = no failure '1' = failure: indicates that overcurrent is detected at top transistor XP−terminal	'0'
OVCYNB	Overcurrent at MOT**YN** Terminal; **B**ottom Transistor	1	Status Register 2	'0' = no failure '1' = failure: indicates that overcurrent is detected at bottom transistor YN−terminal	'0'
OVCYNT	Overcurrent at MOT**YN** Terminal; **T**op Transistor	1	Status Register 2	'0' = no failure '1' = failure: indicates that overcurrent is detected at top transistor YN−terminal	'0'
OVCYPB	Overcurrent at MOT**YP** Terminal; **B**ottom Transistor	1	Status Register 2	'0' = no failure '1' = failure: indicates that overcurrent is detected at bottom transistor YP−terminal	'0'
OVCYPT	Overcurrent at MOT**YP** Terminal; **T**op Transistor	1	Status Register 2	'0' = no failure '1' = failure: indicates that overcurrent is detected at top transistor YP−terminal	'0'
TSD	Thermal Shutdown	1	Status Register 2		'0'
TW	Thermal Warning	1	Status Register 0		'0'
WD	Watchdog event	1	Status Register 0	'0' = no watchdog reset '1' = watchdog reset occurred	'0'

PACKAGE DIMENSIONS

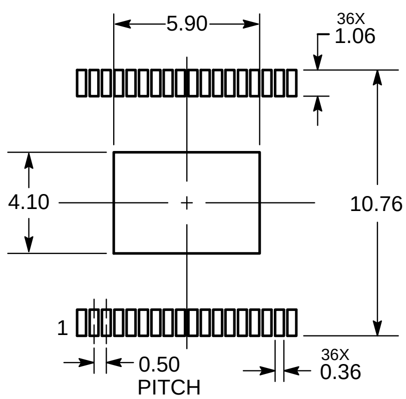
SSOP36 EP
CASE 940AB
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOACATED WITHIN THE INDICATED AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.65
A1	---	0.10
A2	2.35	2.60
b	0.18	0.36
c	0.23	0.32
D	10.30 BSC	
D2	5.70	5.90
E	10.30 BSC	
E1	7.50 BSC	
E2	3.90	4.10
e	0.50 BSC	
h	0.25	0.75
L	0.50	0.90
L2	0.25 BSC	
M	0°	8°
M1	5°	15°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DEVICE ORDERING INFORMATION

Part Number	Ambient Temperature Range	Package Type	Peak Current	Shipping†
NCV70522DQ004R2G	−40°C to +125°C	SSOP36−EP (Pb−Free)	1500 mA	1500 / Tape & Reel
NCV70522DQ004G	−40°C to +125°C	SSOP36−EP (Pb−Free)	1500 mA	47 / Tube / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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