



# PHPT61002NYCLH

100 V, 2 A NPN high power bipolar transistor

31 March 2017

Product data sheet

## 1. General description

NPN high power bipolar transistor in a SOT669 (LFPAK56) Surface-Mounted Device (SMD) power plastic package.

PNP complement: PHPT61002PYCLH

## 2. Features and benefits

- High thermal power dissipation capability
- High temperature applications up to 175 °C
- Reduced Printed Circuit Board (PCB) requirements comparing to transistors in DPAK
- High energy efficiency due to less heat generation

## 3. Applications

- Load switch
- Power management
- Linear mode voltage regulator
- Backlighting applications

## 4. Quick reference data

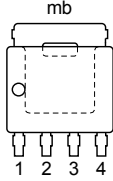
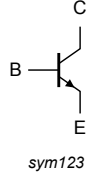
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CEO}$	collector-emitter voltage	open base	-	-	100	V
$I_C$	collector current		-	-	2	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	6	A
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = 2$ A; $I_B = 200$ mA; $T_{amb} = 25$ °C	[1]	80	150	mΩ

[1] pulsed;  $t_p \leq 300$  μs;  $\delta \leq 0.02$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E	emitter	 <p><b>LFPAK56; Power-SO8 (SOT669)</b></p>	
2	E	emitter		
3	E	emitter		
4	B	base		
mb	C	collector		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHPT61002NYCLH	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PHPT61002NYCLH	1002NCC

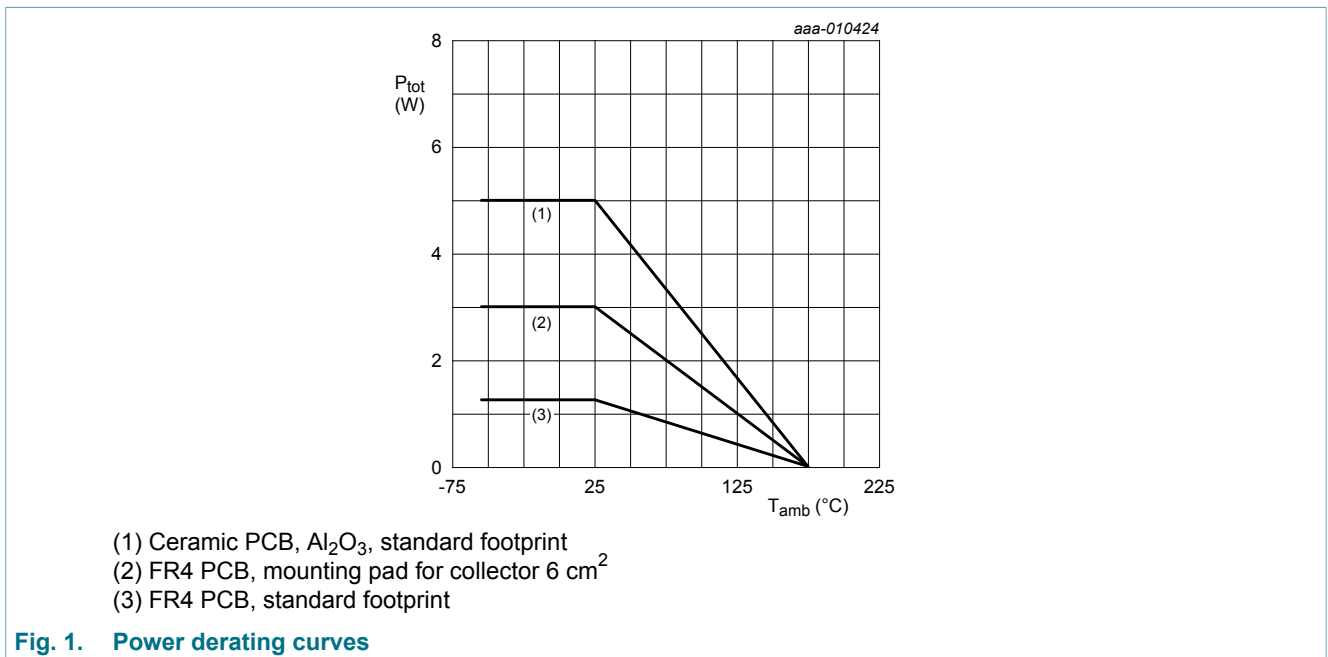
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter		-	100	V
$V_{CEO}$	collector-emitter voltage	open base		-	100	V
$V_{EBO}$	emitter-base voltage	open collector		-	7	V
$I_C$	collector current			-	2	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms		-	6	A
$I_B$	base current			-	0.5	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	1.25	W
			[2]	-	3	W
			[3]	-	5	W
			[4]	-	25	W
$T_j$	junction temperature			-	175	°C
$T_{amb}$	ambient temperature			-55	175	°C
$T_{stg}$	storage temperature			-65	175	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB); single-sided copper; tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB; single-sided copper; tin-plated mounting pad for collector 6 cm<sup>2</sup>.
- [3] Device mounted on an ceramic PCB; Al<sub>2</sub>O<sub>3</sub>; standard footprint.
- [4] Power dissipation from junction to mounting base.



**Fig. 1. Power derating curves**

## 9. Thermal characteristics

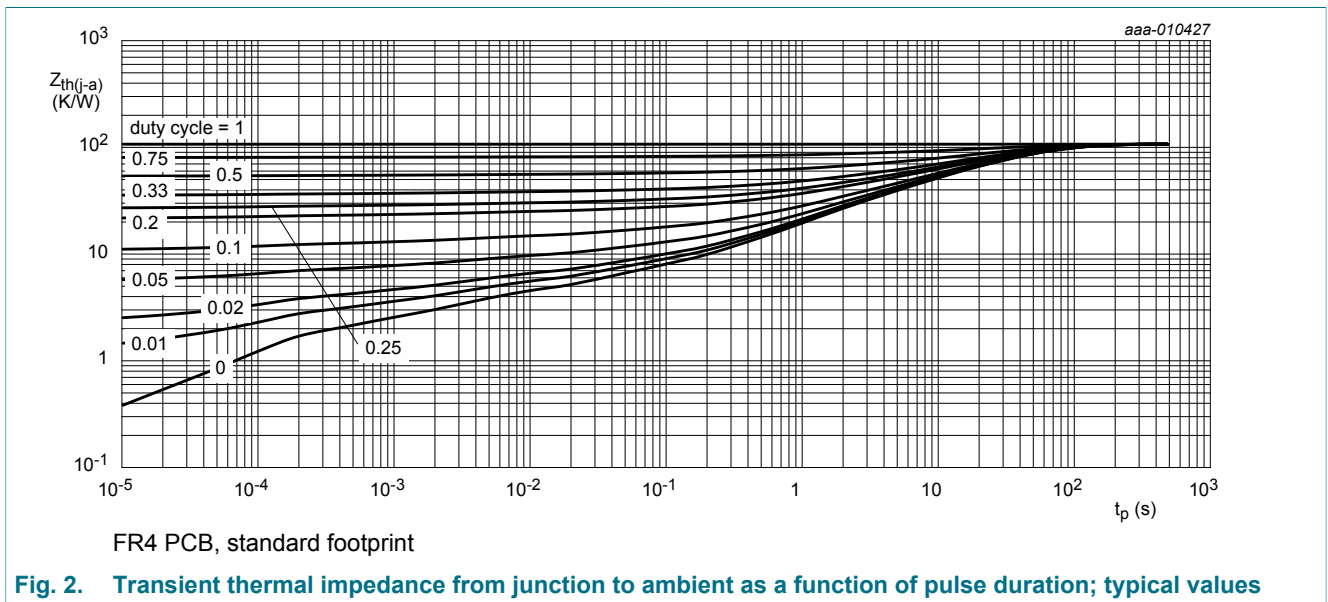
Table 6. Thermal characteristics

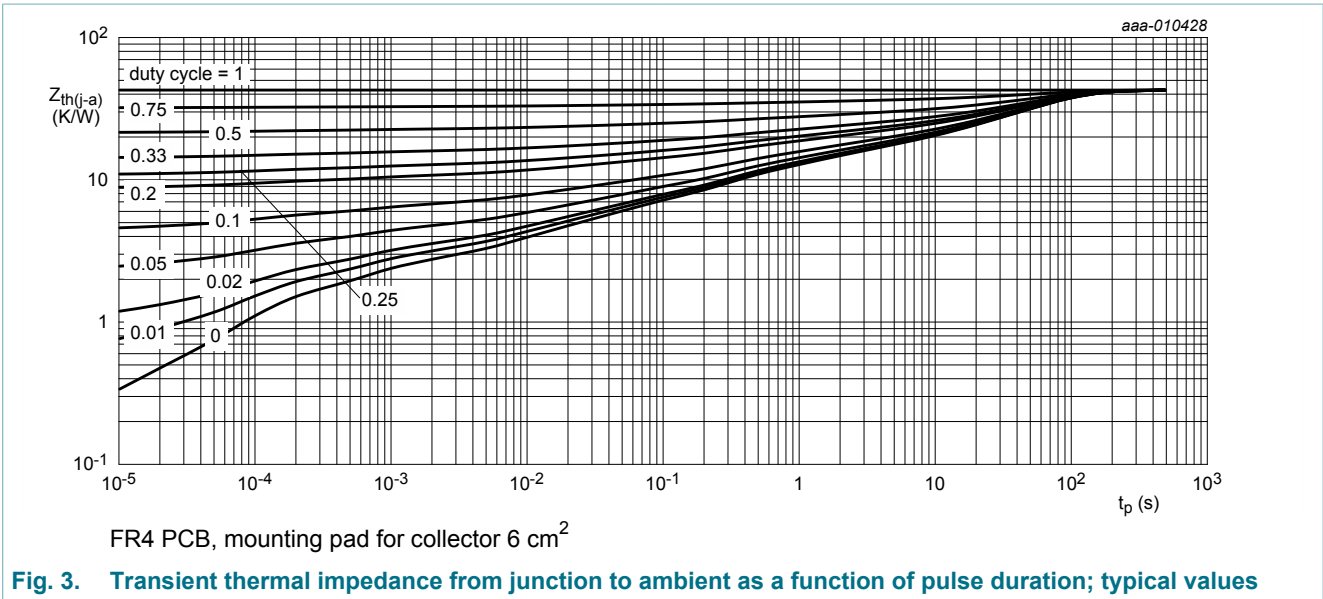
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	115	K/W
			[2]	-	-	50	K/W
			[3]	-	-	30	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	-	6	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB); single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB; single-sided copper; tin-plated and mounting pad for collector 6 cm<sup>2</sup>.

[3] Device mounted on an ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.





## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I <sub>CB0</sub>	collector-base cut-off current	V <sub>CB</sub> = 80 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
		V <sub>CB</sub> = 80 V; I <sub>E</sub> = 0 A; T <sub>J</sub> = 150 °C		-	-	50	μA
I <sub>CES</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 80 V; V <sub>BE</sub> = 0 V; T <sub>amb</sub> = 25 °C		-	-	100	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 7 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 1.5 V; I <sub>C</sub> = 500 mA; T <sub>amb</sub> = 25 °C	[1]	100	180	-	
		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 500 mA; T <sub>amb</sub> = 25 °C	[1]	120	220	-	
		V <sub>CE</sub> = 5 V; I <sub>C</sub> = 1 A; T <sub>amb</sub> = 25 °C	[1]	90	160	260	
		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 1 A; T <sub>amb</sub> = 25 °C	[1]	90	180	-	
		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 2 A; T <sub>amb</sub> = 25 °C	[1]	20	80	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 0.5 A; I <sub>B</sub> = 50 mA; T <sub>amb</sub> = 25 °C		-	50	75	mV
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 200 mA; T <sub>amb</sub> = 25 °C	[1]	-	160	300	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance		[1]	-	80	150	mΩ
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; T <sub>amb</sub> = 25 °C	[1]	-	0.92	1.05	V
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 200 mA; T <sub>amb</sub> = 25 °C	[1]	-	1.08	1.2	V
V <sub>BEon</sub>	base-emitter turn-on voltage	V <sub>CE</sub> = 2 V; I <sub>C</sub> = 0.1 A; T <sub>amb</sub> = 25 °C	[1]	-	0.68	0.85	V
t <sub>d</sub>	delay time	V <sub>CC</sub> = 12.5 V; I <sub>C</sub> = 1 A; I <sub>Bon</sub> = 0.05 A; I <sub>Boff</sub> = -0.05 A; T <sub>amb</sub> = 25 °C		-	20	-	ns
t <sub>r</sub>	rise time			-	300	-	ns
t <sub>on</sub>	turn-on time			-	320	-	ns
t <sub>s</sub>	storage time			-	800	-	ns
t <sub>f</sub>	fall time			-	420	-	ns
t <sub>off</sub>	turn-off time			-	1220	-	ns
f <sub>T</sub>	transition frequency		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 100 mA; f = 100 MHz; T <sub>amb</sub> = 25 °C		-	140	-
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz; T <sub>amb</sub> = 25 °C		-	11	-	pF

[1] pulsed; t<sub>p</sub> ≤ 300 μs; δ ≤ 0.02

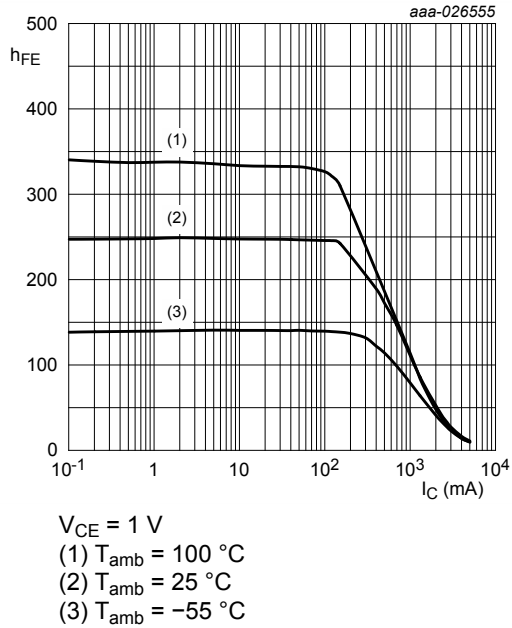


Fig. 4. DC current gain as a function of collector current; typical values

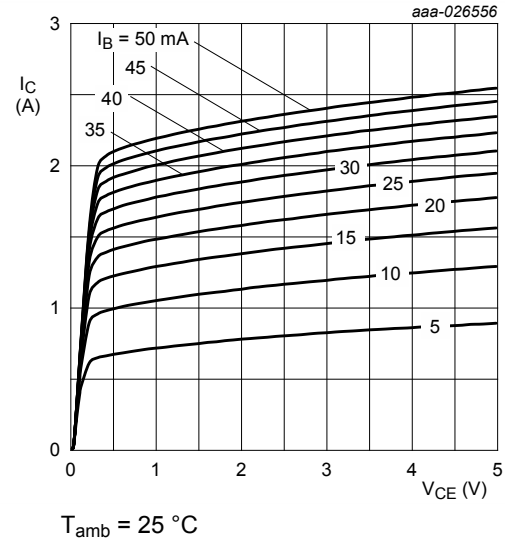


Fig. 5. Collector current as a function of collector-emitter voltage; typical values

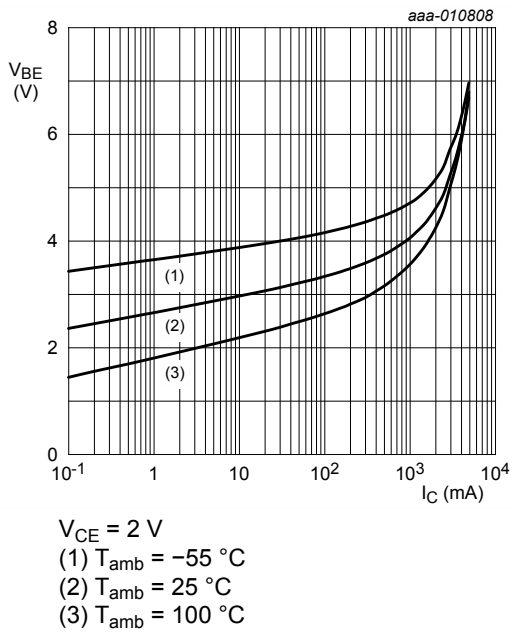


Fig. 6. Base-emitter voltage as a function of collector current; typical values

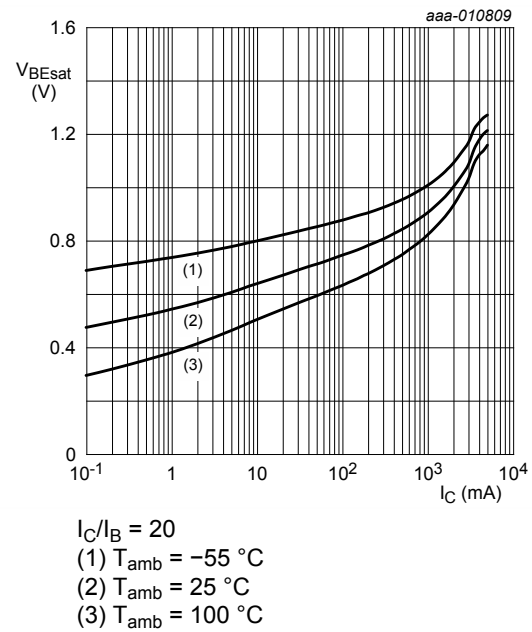
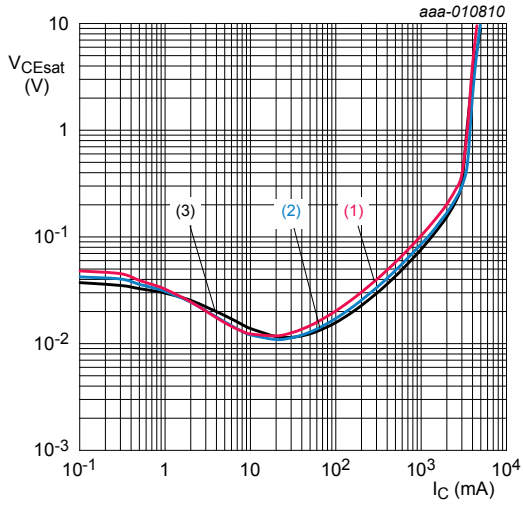
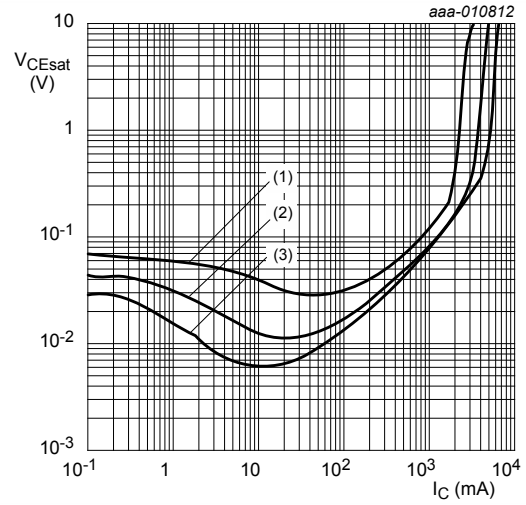


Fig. 7. Base-emitter saturation voltage as a function of collector current; typical values



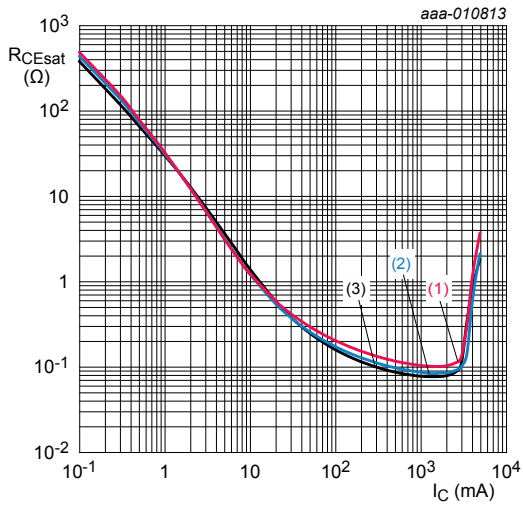
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values**



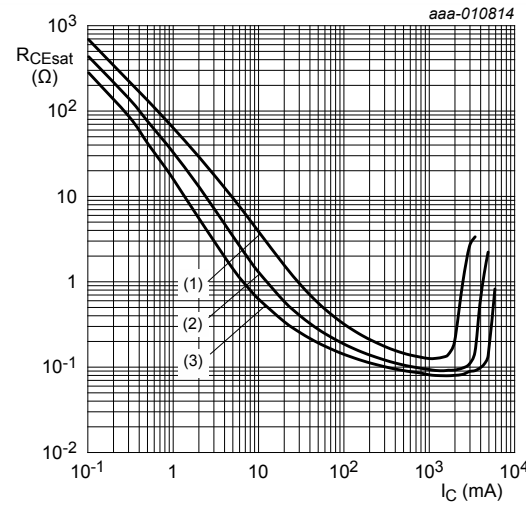
$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 50$   
 (2)  $I_C/I_B = 20$   
 (3)  $I_C/I_B = 10$

**Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 10. Collector-emitter saturation resistance as a function of collector current; typical values**



$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 50$   
 (2)  $I_C/I_B = 20$   
 (3)  $I_C/I_B = 10$

**Fig. 11. Collector-emitter saturation resistance as a function of collector current; typical values**



### 11. Test information

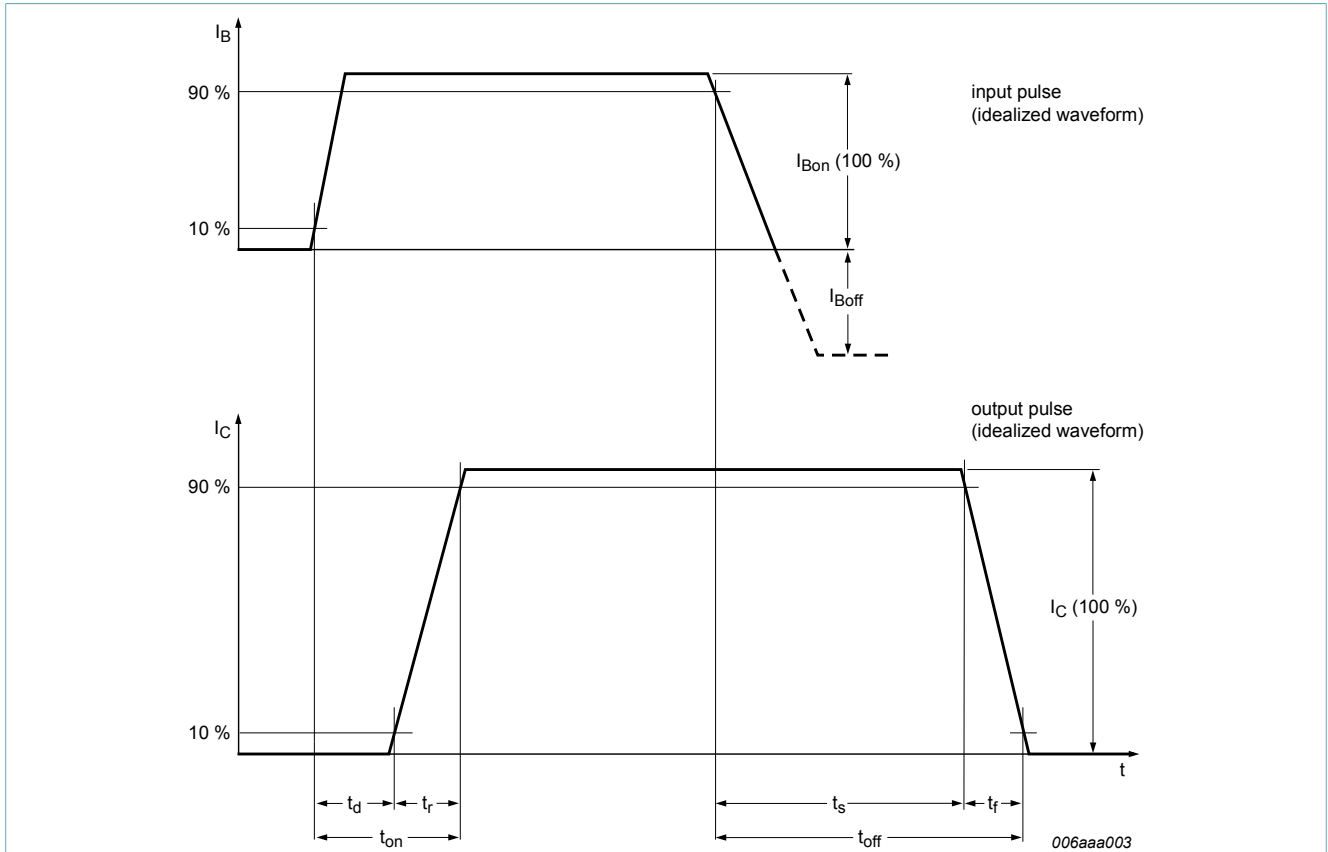


Fig. 12. BISS transistor switching time definition

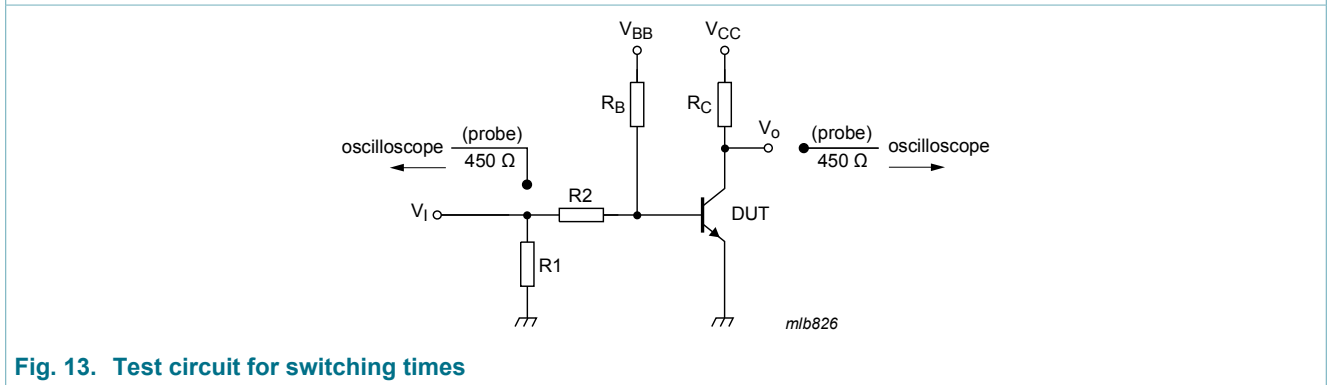


Fig. 13. Test circuit for switching times

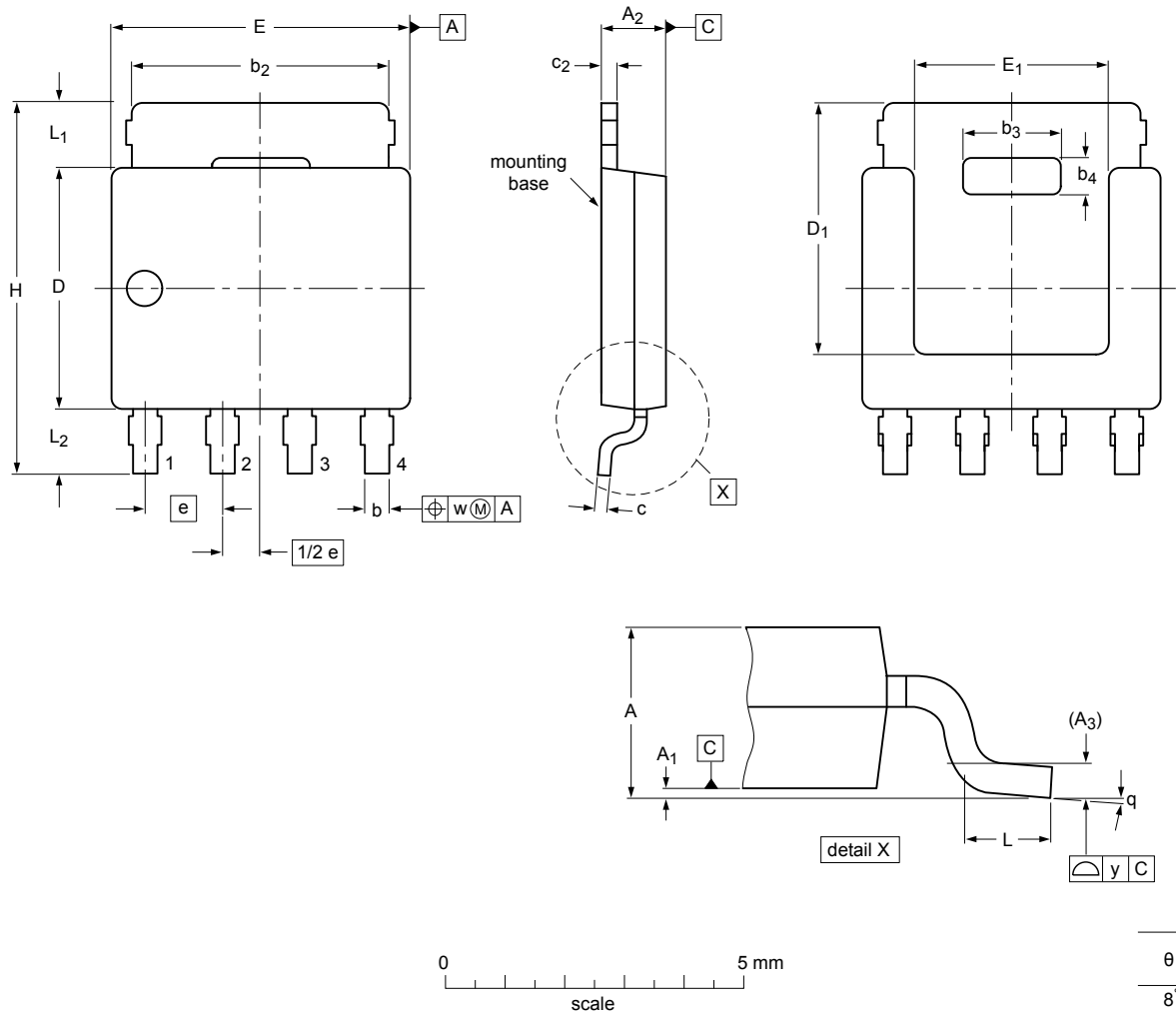
### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 12. Package outline

Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads

SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT669		MO-235			-11-03-25- 13-02-27

Fig. 14. Package outline LFAK56; Power-SO8 (SOT669)

### 13. Soldering

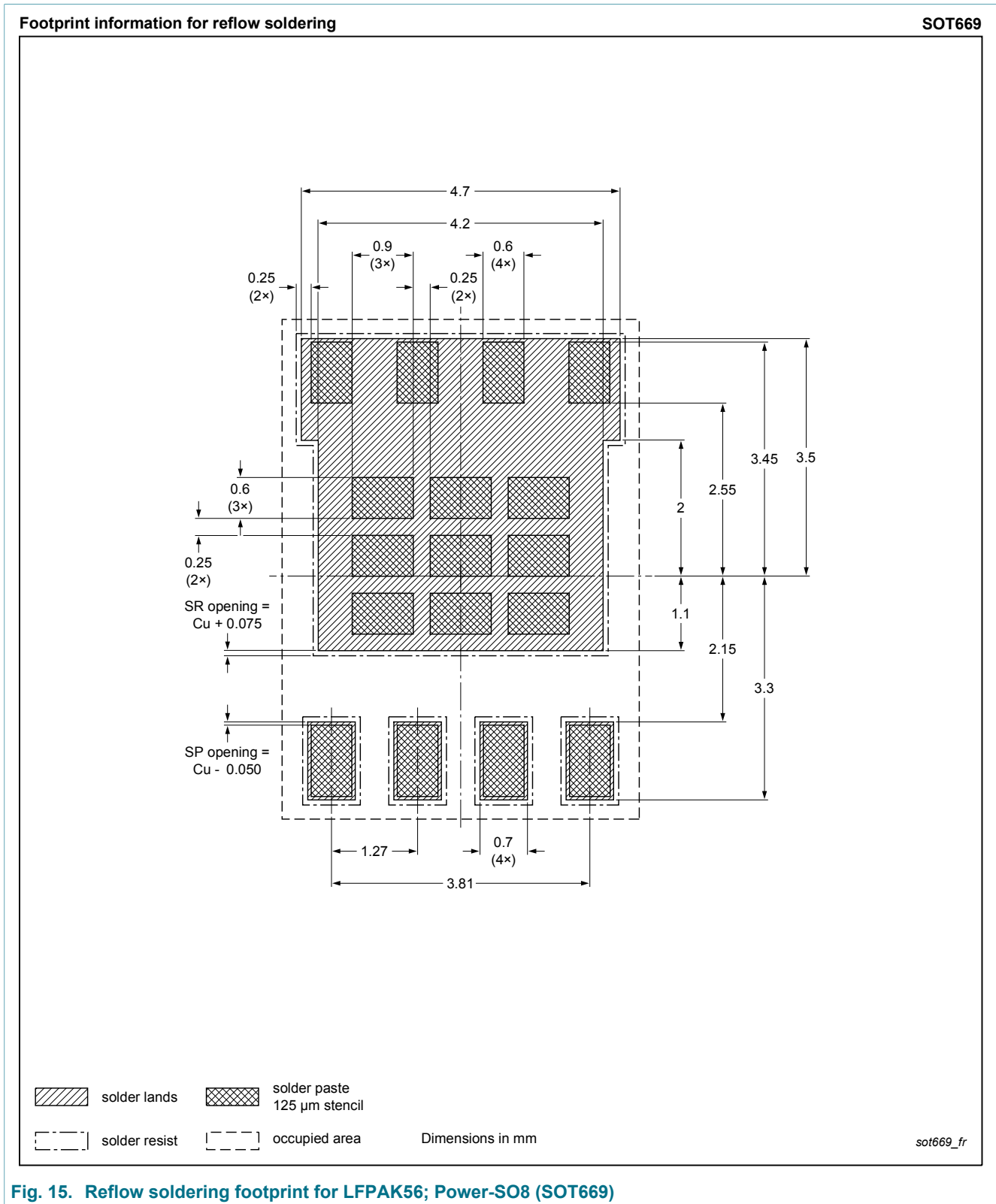


Fig. 15. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PHPT61002NYCLH v.1	20170331	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 31 March 2017

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