Features

- 3.0V to 5.5V Operation
- Industry-standard Architecture
  - Emulates Many 20-pin PALs®
  - Low-cost Easy-to-use Software Tools
- High-speed
  - 10 ns Maximum Pin-to-pin Delay
- Ultra-low Power
  - 5 µA (Max) Pin-controlled Power-down Mode Option
  - Typical 100 nA Standby
- CMOS and TTL Compatible Inputs and Outputs
  - I/O Pin-keeper Circuits
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High-reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Commercial and Industrial Temperature Ranges
- Dual-in-line and Surface Mount Packages in Standard Pinouts
- Inputs are 5V Tolerant
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available

High-performance EE PLD

ATF16LV8C

Description

The ATF16LV8C is a high-performance EECMOS programmable logic device that utilizes Atmel's proven electrically-erasable Flash memory technology. Speeds down to 10 ns and a 5 µA pin-controlled power-down mode option are offered. All speed

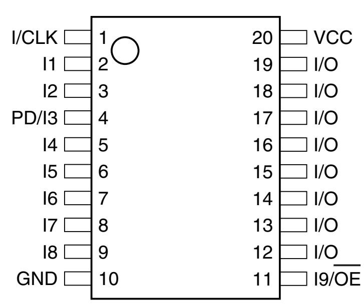
(continued)

Pin Configurations

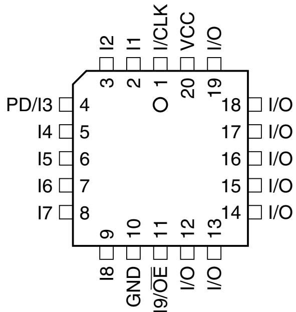
All Pinouts Top View

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bi-directional Buffers
OE	Output Enable
VCC	(+3V to 5.5V) Supply
PD	Programmable Power-down Option

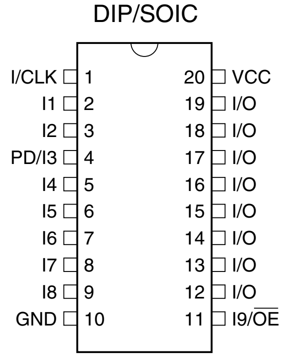
TSSOP



PLCC



DIP/SOIC



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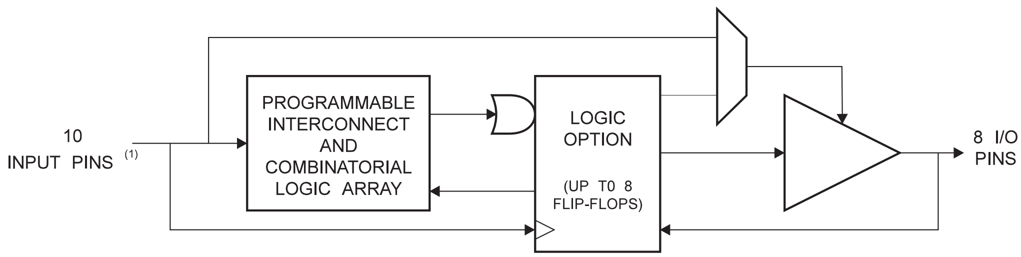
ranges are specified over the full 3.0V to 5.25V range for industrial and commercial temperature ranges.

The ATF16LV8C incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

The ATF16LV8C can significantly reduce total system power, thereby enhancing system reliability and reducing power supply costs. When pin 4 is configured as the power-down control pin, supply current drops to less than 5 µA whenever the pin is high. If the power-down feature isn't required for a particular application, pin 4 may be used as a logic input. Also, the pin keeper circuits eliminate the need for internal pull-up resistors along with their attendant power consumption.

Block Diagram



Note: 1. Includes optional PD control pin.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial
Operating Temperature (Ambient)	0°C - 70°C
V_{CC} Power Supply	3.0V to 5.5V

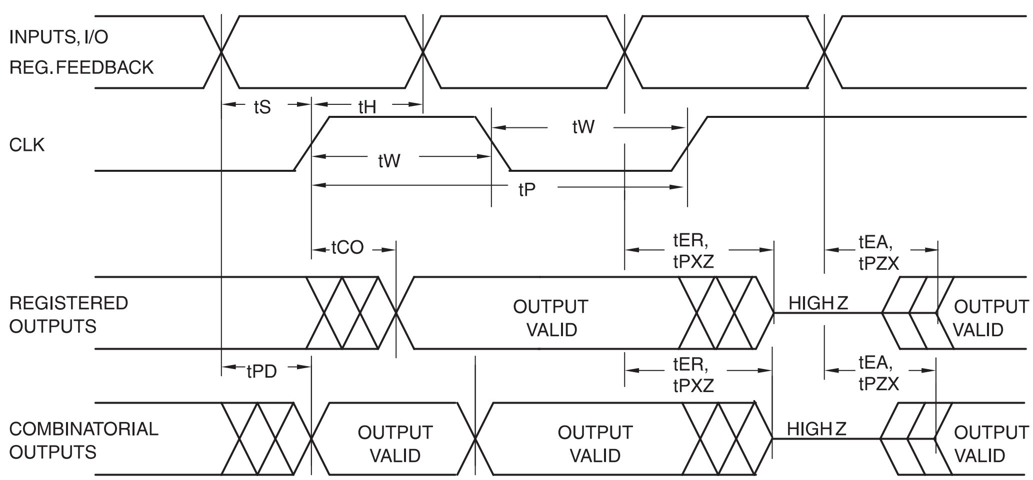
DC Characteristics

Symbol	Parameter	Condition(2)	Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(Max)			-10	µA
I_{IH}	Input or I/O High Leakage Current	$1.8 \le V_{IN} \le V_{CC}$			10	µA
I_{CC1}(1)	Power Supply Current	15 MHz, V_{CC} = Max, V_{IN} = 0, V_{CC}, Outputs Open		Com. Ind.	55 60	mA
I_{PD}(1)	Power Supply Current, Power-down Mode	V_{CC} = Max, V_{IN} = 0, V_{CC}		0.1	5	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V; V_{CC}= 3V; T_A = 25°C			-150	mA
V_{IL}	Input Low Voltage	MIN < V_{CC} < Max	-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = Min; All Outputs I_{OL} = 8 mA			0.5	V
V_{OH}	Output High Voltage	V_{CC} = Min I_{OH} = -4 mA	2.4			V
I_{OL}	Output Low Current	V_{CC} = Min	8			mA
I_{OH}	Output High Current	V_{CC} = Min	-4			mA

Note: 1. All I_{CC} parameters measured with outputs open.

2. For DC characteristics, the test condition of V_{CC} = Max corresponds to 3.6V.

AC Waveforms(1)



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics

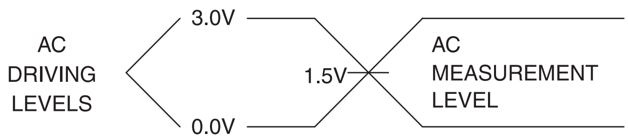
Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output	1	10	1	15	ns
t_{CF}	Clock to Feedback		5		8	ns
t_{CO}	Clock to Output	2	7	2	10	ns
t_S	Input or Feedback Setup Time	7		12		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	12		16		ns
t_W	Clock Width	6		8		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$		71.4		45.5	MHz
	Internal Feedback $1/(t_S + t_{CF})$		83.3		50	MHz
	No Feedback $1/(t_P)$		83.3		62.5	MHz
t_{EA}	Input to Output Enable — Product Term	3	10	3	15	ns
t_{ER}	Input to Output Disable — Product Term	2	10	2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable	2	8	2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable	1.5	8	1.5	15	ns

Power-down AC Characteristics(1)(2)(3)

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{IVDH}	Valid Input before PD High	10		15		ns
t_{GVDH}	Valid $\overline{OE}$ before PD High	0		0		ns
t_{CVDH}	Valid Clock before PD High	0		0		ns
t_{DHIX}	Input Don't Care after PD High		10		15	ns
t_{DHGX}	$\overline{OE}$ Don't Care after PD High		10		15	ns
t_{DHCX}	Clock Don't Care after PD High		10		15	ns
t_{DLIV}	PD Low to Valid Input		10		15	ns
t_{DLGV}	PD Low to Valid $\overline{OE}$		25		30	ns
t_{DLCV}	PD Low to Valid Clock		25		30	ns
t_{DLOV}	PD Low to Valid Output		30		35	ns

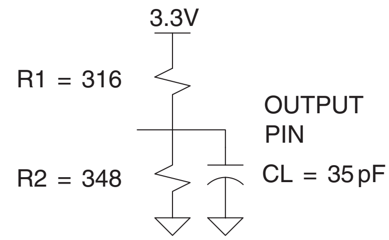
Notes: 1. Output data is latched and held.
2. High-Z outputs remain High-Z.
3. Clock and input transitions are ignored.

Input Test Waveforms and Measurement Levels:



t_R, t_F < 1.5ns (10% to 90%)

Output Test Loads: Commercial



Note: Similar devices are tested with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible devices.

Pin Capacitance

(f = 1 MHz, T = 25°C)[1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

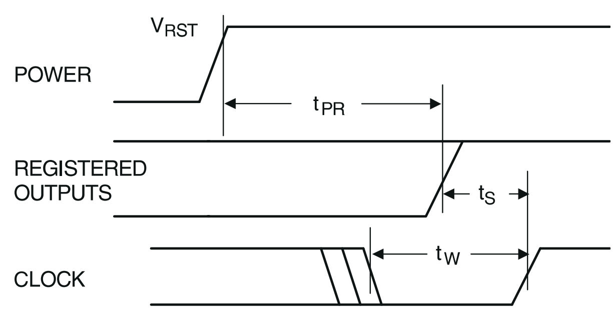
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power-up Reset

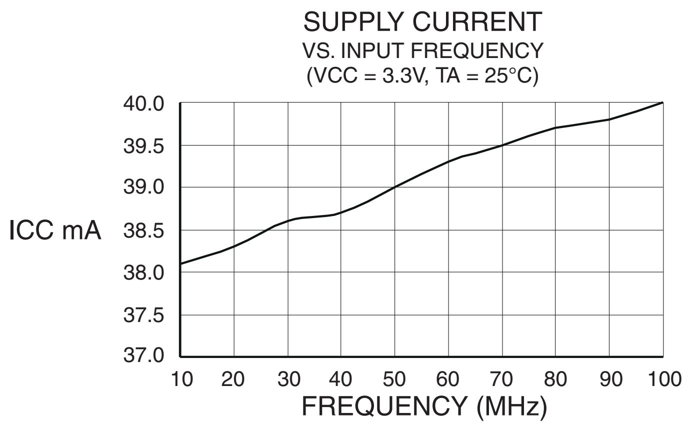
The ATF16LV8C's registers are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

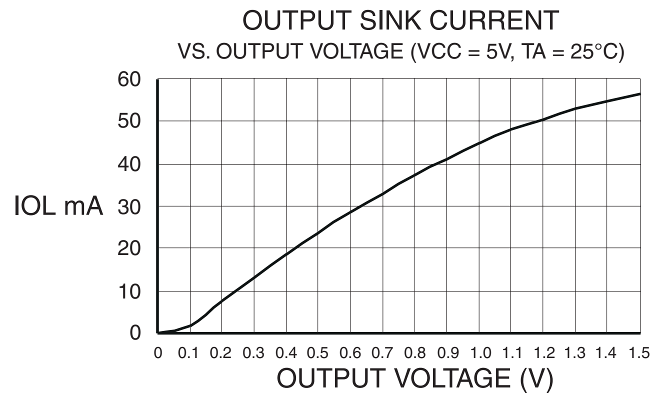
This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

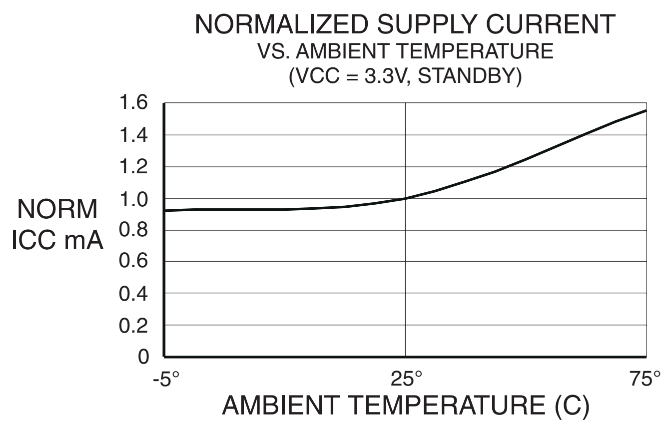
1. The V_{CC} rise must be monotonic from below 0.7V.
2. The signals from which the clock is derived must remain stable during T_{PR}.
3. After T_{PR}, all input and feedback setup times must be met before driving the clock term high.

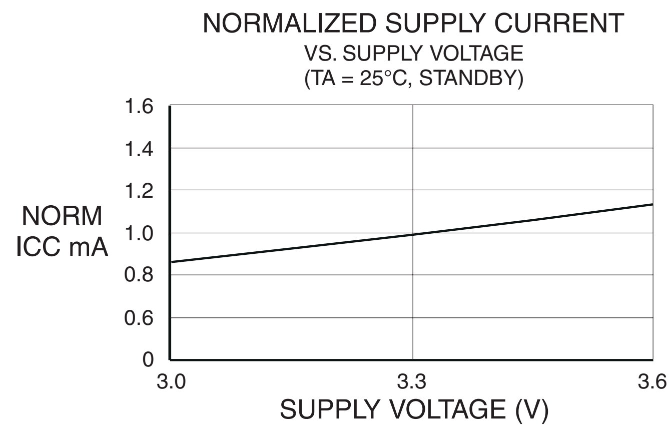


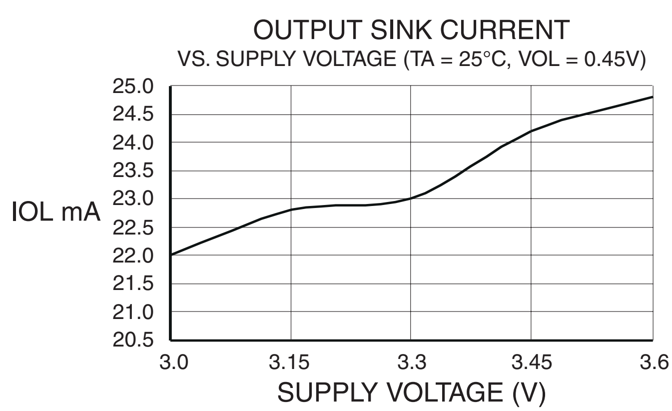
Parameter	Description	Typ	Max	Units
T_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	2.5	3.0	V

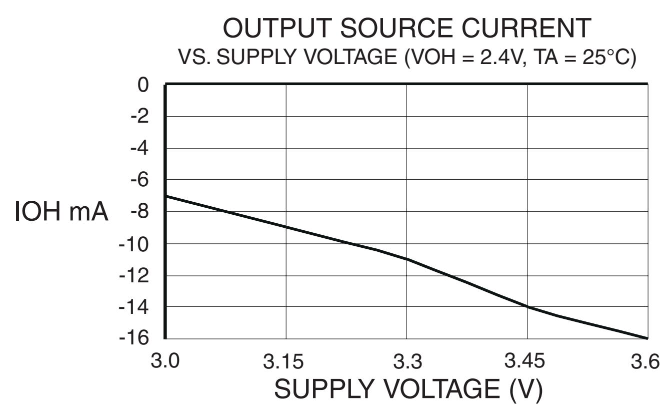

SUPPLY CURRENT
VS. INPUT FREQUENCY
(VCC = 3.3V, TA = 25°C)
ICC mA
40.0
39.5
39.0
38.5
38.0
37.5
37.0
10 20 30 40 50 60 70 80 90 100
FREQUENCY (MHz)

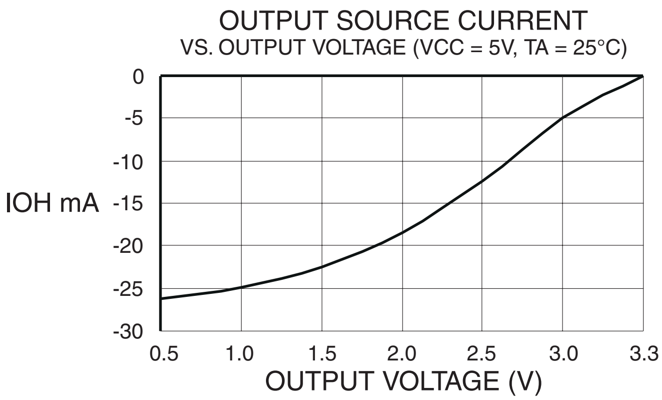

OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)
IOL mA
60
50
40
30
20
10
0
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5
OUTPUT VOLTAGE (V)

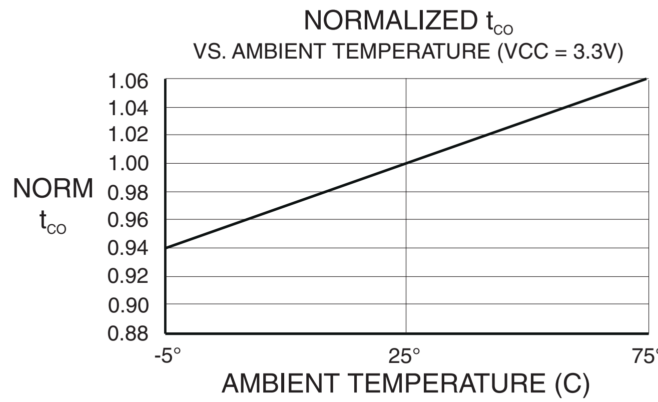

NORMALIZED SUPPLY CURRENT
VS. AMBIENT TEMPERATURE
(VCC = 3.3V, STANDBY)
NORM
ICC mA
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
-5° 25° 75°
AMBIENT TEMPERATURE (C)

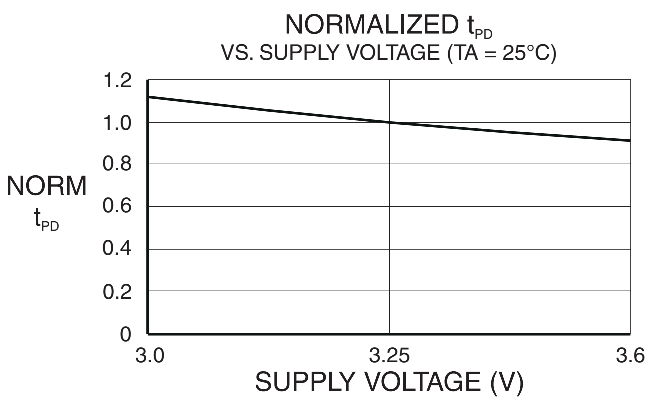

NORMALIZED SUPPLY CURRENT
VS. SUPPLY VOLTAGE
(TA = 25°C, STANDBY)
NORM
ICC mA
1.6
1.4
1.2
1.0
0.8
0.6
0
3.0 3.3 3.6
SUPPLY VOLTAGE (V)

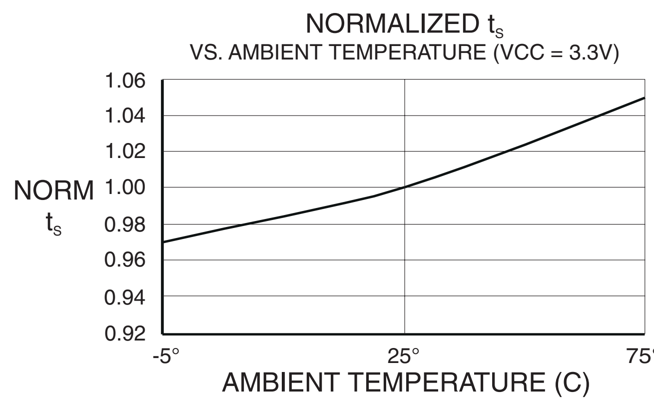

OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE (TA = 25°C, VOL = 0.45V)
IOL mA
25.0
24.5
24.0
23.5
23.0
22.5
22.0
21.5
21.0
20.5
3.0 3.15 3.3 3.45 3.6
SUPPLY VOLTAGE (V)

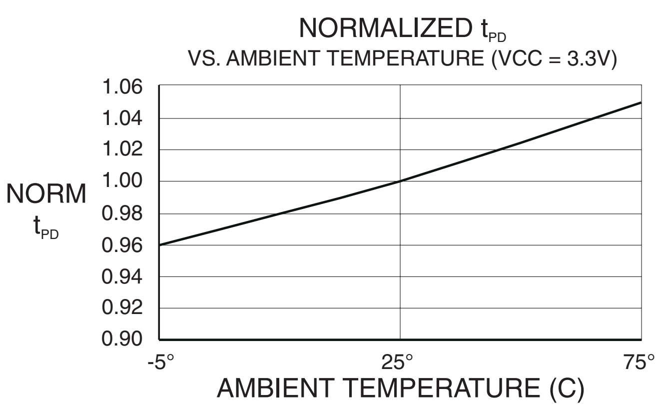

OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (VOH = 2.4V, TA = 25°C)
IOH mA
0
-2
-4
-6
-8
-10
-12
-14
-16
3.0 3.15 3.3 3.45 3.6
SUPPLY VOLTAGE (V)

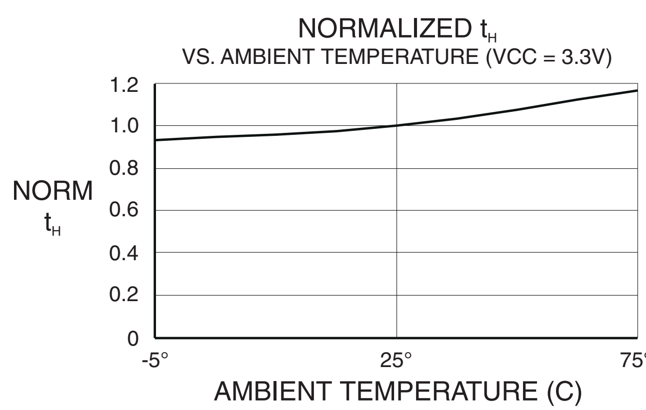

OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)
IOH mA
0
-5
-10
-15
-20
-25
-30
0.5
1.0
1.5
2.0
2.5
3.0
3.3
OUTPUT VOLTAGE (V)

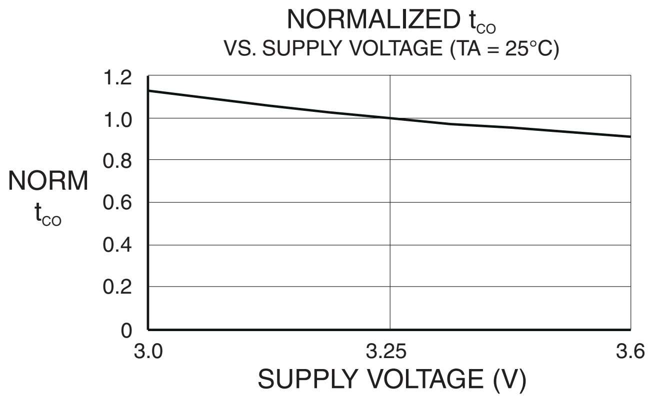

NORMALIZED t_{CO}
VS. AMBIENT TEMPERATURE (VCC = 3.3V)
NORM t_{CO}
1.06
1.04
1.02
1.00
0.98
0.96
0.94
0.92
0.90
0.88
-5°
25°
75°
AMBIENT TEMPERATURE (C)

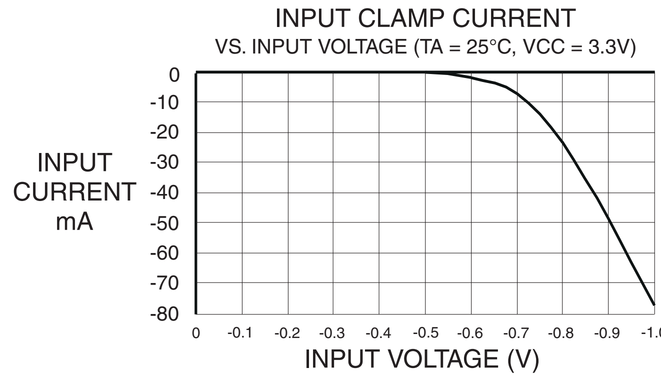

NORMALIZED t_{PD}
VS. SUPPLY VOLTAGE (TA = 25°C)
NORM t_{PD}
1.2
1.0
0.8
0.6
0.4
0.2
0
3.0
3.25
3.6
SUPPLY VOLTAGE (V)

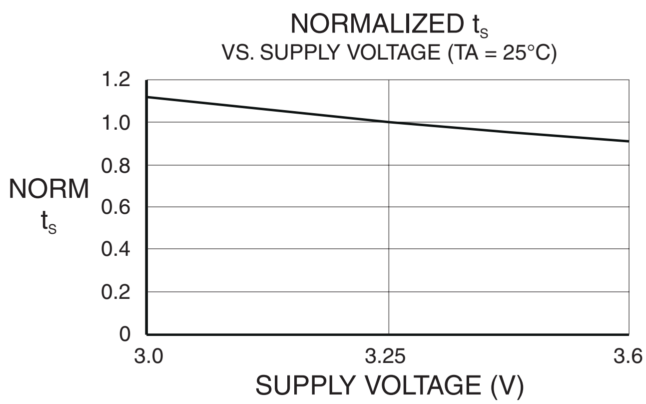

NORMALIZED t_S
VS. AMBIENT TEMPERATURE (VCC = 3.3V)
NORM t_S
1.06
1.04
1.02
1.00
0.98
0.96
0.94
0.92
-5°
25°
75°
AMBIENT TEMPERATURE (C)

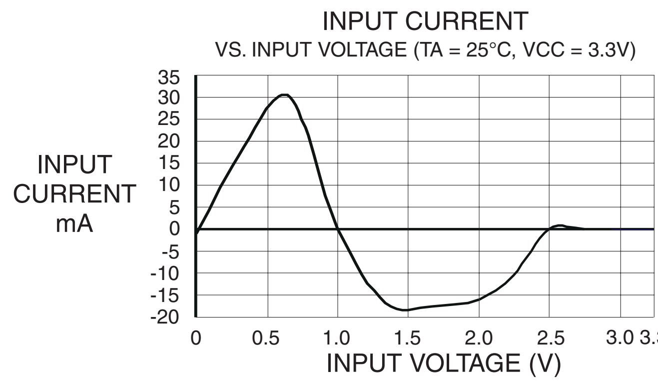

NORMALIZED t_{PD}
VS. AMBIENT TEMPERATURE (VCC = 3.3V)
NORM t_{PD}
1.06
1.04
1.02
1.00
0.98
0.96
0.94
0.92
0.90
-5°
25°
75°
AMBIENT TEMPERATURE (C)

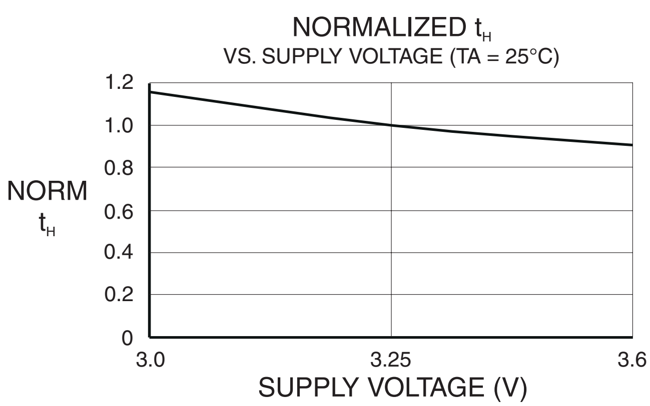

NORMALIZED t_H
VS. AMBIENT TEMPERATURE (VCC = 3.3V)
NORM t_H
1.2
1.0
0.8
0.6
0.4
0.2
0
-5°
25°
75°
AMBIENT TEMPERATURE (C)


NORMALIZED t_{CO}
VS. SUPPLY VOLTAGE (TA = 25°C)
1.2
1.0
0.8
0.6
0.4
0.2
0
NORM
t_{CO}
3.0
3.25
3.6
SUPPLY VOLTAGE (V)


INPUT CLAMP CURRENT
VS. INPUT VOLTAGE (TA = 25°C, VCC = 3.3V)
0
-10
-20
-30
-40
-50
-60
-70
-80
INPUT
CURRENT
mA
0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
-0.7
-0.8
-0.9
-1.0
INPUT VOLTAGE (V)


NORMALIZED t_S
VS. SUPPLY VOLTAGE (TA = 25°C)
1.2
1.0
0.8
0.6
0.4
0.2
0
NORM
t_S
3.0
3.25
3.6
SUPPLY VOLTAGE (V)


INPUT CURRENT
VS. INPUT VOLTAGE (TA = 25°C, VCC = 3.3V)
35
30
25
20
15
10
5
0
-5
-10
-15
-20
INPUT
CURRENT
mA
0
0.5
1.0
1.5
2.0
2.5
3.0
3.3
INPUT VOLTAGE (V)


NORMALIZED t_H
VS. SUPPLY VOLTAGE (TA = 25°C)
1.2
1.0
0.8
0.6
0.4
0.2
0
NORM
t_H
3.0
3.25
3.6
SUPPLY VOLTAGE (V)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7	7	ATF16LV8C-10JC ATF16LV8C-10PC ATF16LV8C-10SC ATF16LV8C-10XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
15	12	10	ATF16LV8C-15JC ATF16LV8C-15PC ATF16LV8C-15SC ATF16LV8C-15XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
10	7	7	ATF16LV8C-10JI ATF16LV8C-10PI ATF16LV8C-10SI ATF16LV8C-10XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)
15	12	10	ATF16LV8C-15JI ATF16LV8C-15PI ATF16LV8C-15SI ATF16LV8C-15XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)

Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7	7	ATF16LV8C-10JU ATF16LV8C-10SU ATF16LV8C-10XU	20J 20S 20X	Industrial (-40°C to 85°C)

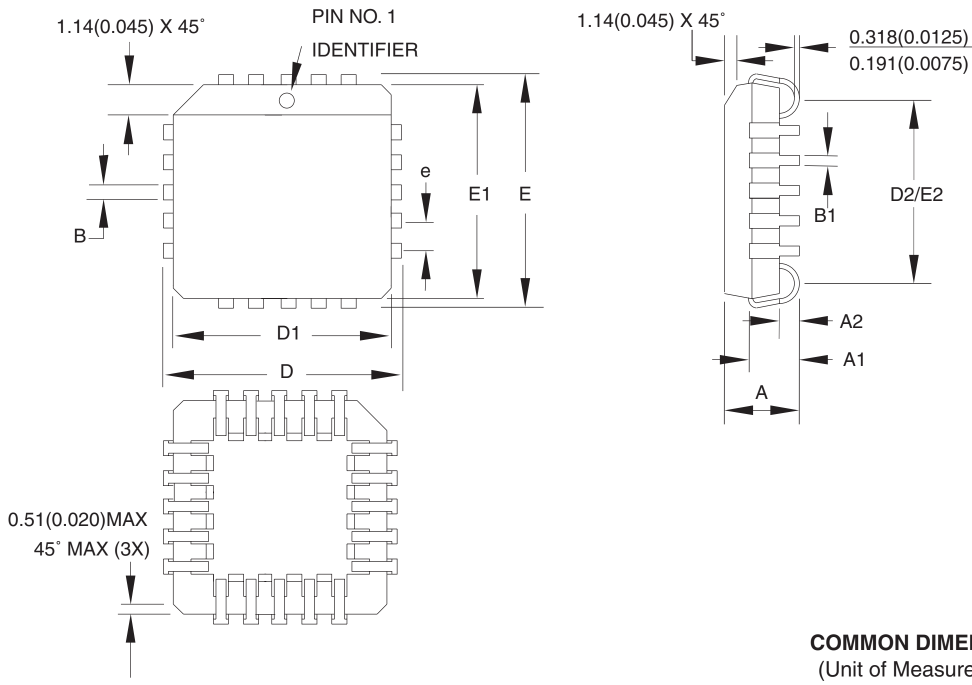
Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, simply de-rate I_{CC} by 15% on the “C” device. No speed de-rating is necessary.

Package Type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-wing Small Outline (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

Packaging Information

20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

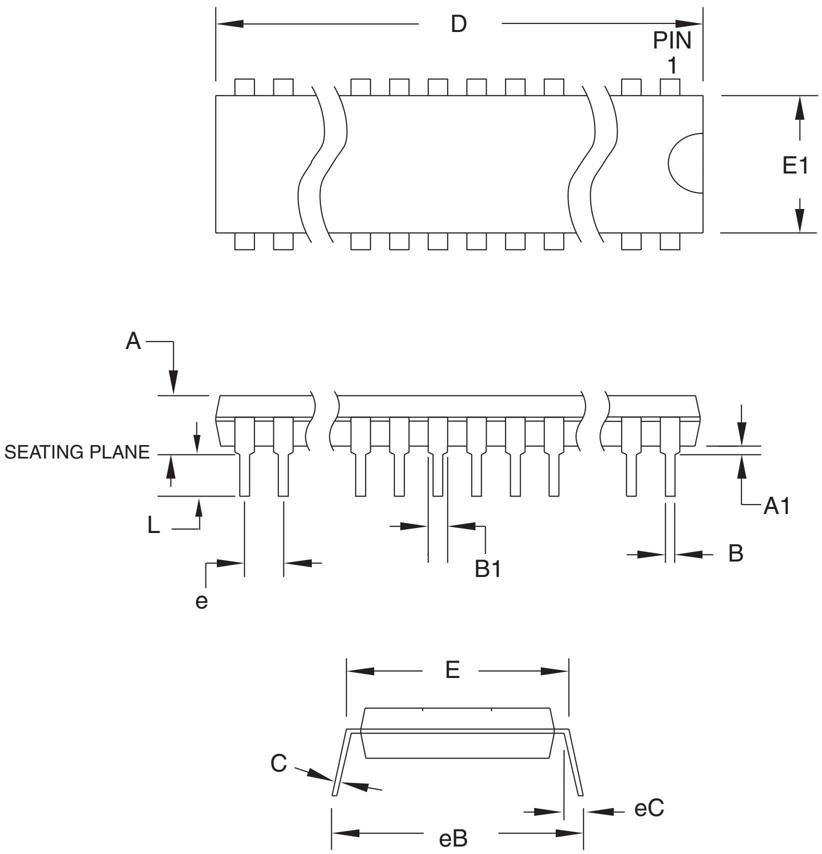
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

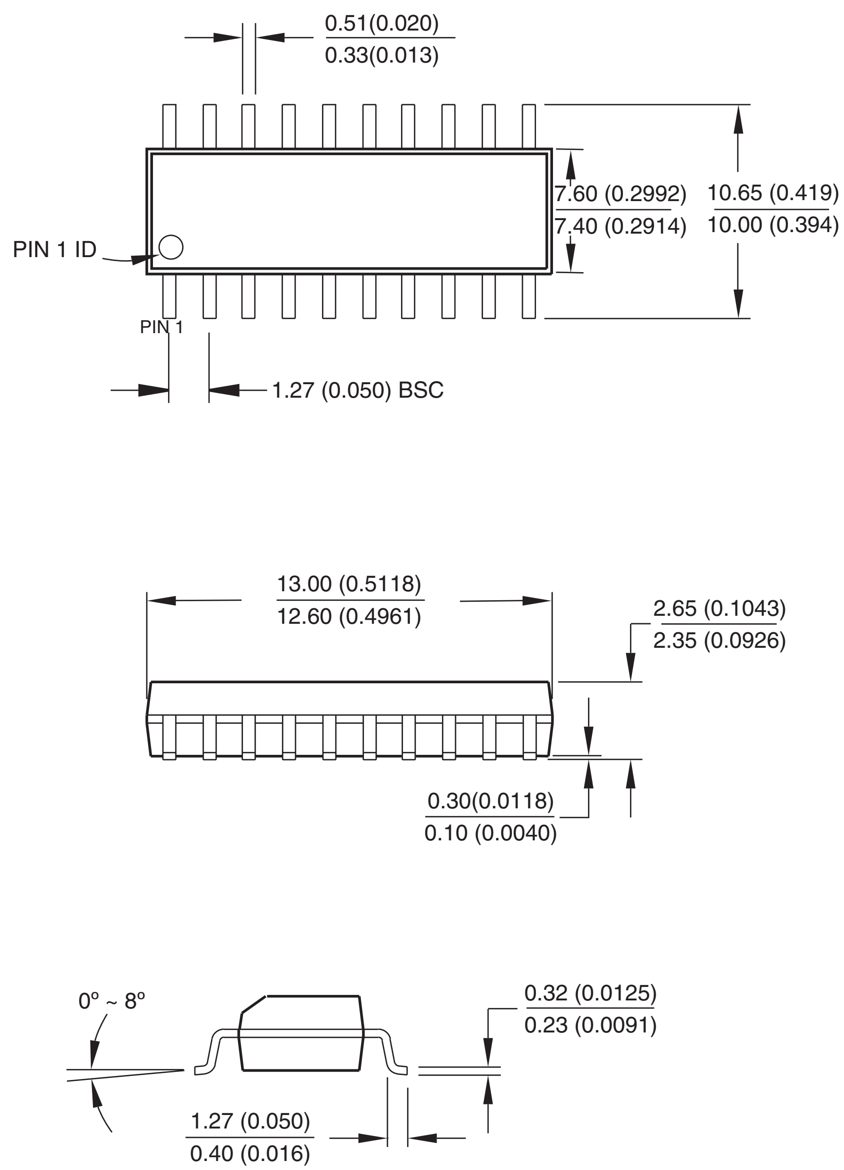
Notes:
1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/23/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

20S – SOIC

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
JEDEC Standard MS-013

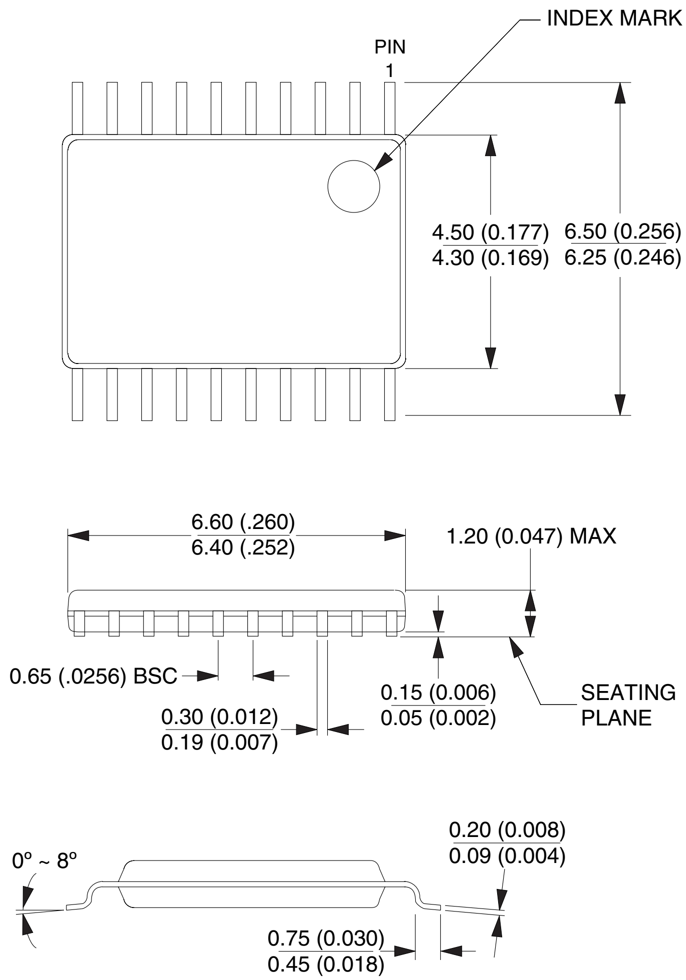


10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S**, 20-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC)	20S	B

20X – TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC



10/23/03

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

Revision History

Revision Level – Revision Date	History
H – June 2006	Added Green package options.

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