

# NLSV2T244

## 2-Bit Dual-Supply Non-Inverting Level Translator

The NLSV2T244 is a 2-bit configurable dual-supply voltage level translator. The input  $A_n$  and output  $B_n$  ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low-voltage translation from the input  $A_n$  to the output  $B_n$  port.

### Features

- Wide  $V_{CCA}$  and  $V_{CCB}$  Operating Range: 0.9 V to 4.5 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non-preferential  $V_{CCA}$  and  $V_{CCB}$  Sequencing
- Outputs at 3-State until Active  $V_{CC}$  is Reached
- Power-Off Protection
- Outputs Switch to 3-State with  $V_{CCB}$  at GND
- Small Packaging: UDFN8, SO-8, Micro8
- This is a Pb-Free Device

### Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

### Important Information

- ESD Protection for All Pins:  
HBM (Human Body Model) > 5000 V



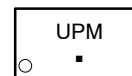
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAMS



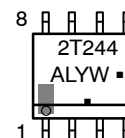
**UDFN8**  
**MU SUFFIX**  
**CASE 517AJ**



UP = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package



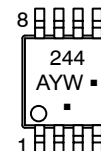
**SO-8**  
**D SUFFIX**  
**CASE 751**



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package



**Micro8**  
**DM SUFFIX**  
**CASE 846A**



A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NLSV2T244MUTAG	UDFN8 (Pb-Free)	3000/Tape & Reel
NLSV2T244DR2G	SO-8 (Pb-Free)	2500/Tape & Reel
NLSV2T244DMR2G	Micro8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NLSV2T244

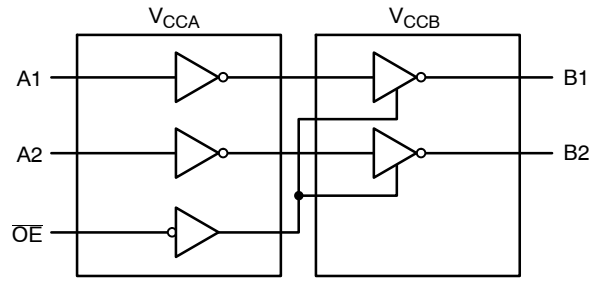
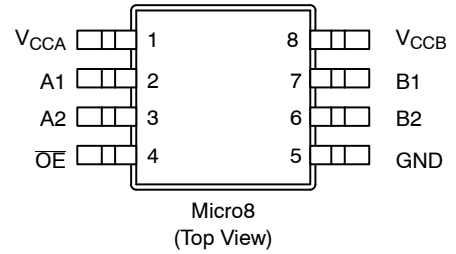
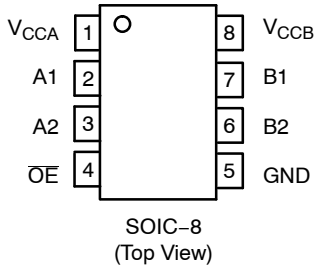
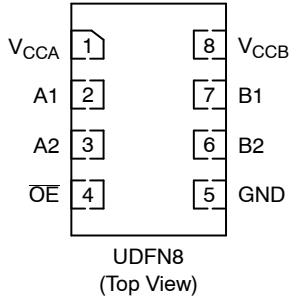


Figure 1. Logic Diagram

## PIN ASSIGNMENTS



## PIN ASSIGNMENT

PIN	FUNCTION
V <sub>CCA</sub>	Input Port DC Power Supply
V <sub>CCB</sub>	Output Port DC Power Supply
GND	Ground
A <sub>n</sub>	Input Port
B <sub>n</sub>	Output Port
$\overline{OE}$	Output Enable

## TRUTH TABLE

Inputs		Outputs
$\overline{OE}$	A <sub>n</sub>	B <sub>n</sub>
L	L	L
L	H	H
H	X	3-State

# NLSV2T244

## MAXIMUM RATINGS

Symbol	Rating	Value	Condition	Unit
$V_{CCA}, V_{CCB}$	DC Supply Voltage	-0.5 to +5.5		V
$V_I$	DC Input Voltage $A_n$	-0.5 to +5.5		V
$V_C$	Control Input $\overline{OE}$	-0.5 to +5.5		V
$V_O$	DC Output Voltage (Power Down) $B_n$	-0.5 to +5.5	$V_{CCA} = V_{CCB} = 0$	V
	(Active Mode) $B_n$	-0.5 to +5.5		V
	(Tri-State Mode) $B_n$	-0.5 to +5.5		V
$I_{IK}$	DC Input Diode Current	-20	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CCA}, I_{CCB}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CCA}, V_{CCB}$	Positive DC Supply Voltage	0.9	4.5	V
$V_I$	Bus Input Voltage	GND	4.5	V
$V_C$	Control Input $\overline{OE}$	GND	4.5	V
$V_{IO}$	Bus Output Voltage (Power Down Mode) $B_n$	GND	4.5	V
	(Active Mode) $B_n$	GND	$V_{CCB}$	V
	(Tri-State Mode) $B_n$	GND	4.5	V
$T_A$	Operating Temperature Range	-40	+85	$^{\circ}\text{C}$
$\Delta t / \Delta V$	Input Transition Rise or Rate $V_I$ , from 30% to 70% of $V_{CC}$ ; $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0	10	nS

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	-40°C to +85°C		Unit
					Min	Max	
V <sub>IH</sub>	Input HIGH Voltage (An, OE)		3.6 – 4.5	0.9 – 4.5	2.2	–	V
			2.7 – 3.6		2.0	–	
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		0.65 * V <sub>CCA</sub>	–	
			0.9 – 1.4		0.9 * V <sub>CCA</sub>	–	
V <sub>IL</sub>	Input LOW Voltage (An, OE)		3.6 – 4.5	0.9 – 4.5	–	0.8	V
			2.7 – 3.6		–	0.8	
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	0.35 * V <sub>CCA</sub>	
			0.9 – 1.4		–	0.1 * V <sub>CCA</sub>	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 μA; V <sub>I</sub> = V <sub>IH</sub>	0.9 – 4.5	0.9 – 4.5	V <sub>CCB</sub> - 0.2	–	V
		I <sub>OH</sub> = -0.5 mA; V <sub>I</sub> = V <sub>IH</sub>	0.9	0.9	0.75 * V <sub>CCB</sub>	–	
		I <sub>OH</sub> = -2 mA; V <sub>I</sub> = V <sub>IH</sub>	1.4	1.4	1.05	–	
		I <sub>OH</sub> = -6 mA; V <sub>I</sub> = V <sub>IH</sub>	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I <sub>OH</sub> = -12 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I <sub>OH</sub> = -18 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.7	–	
3.0	3.0		2.4	–			
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA; V <sub>I</sub> = V <sub>IL</sub>	0.9 – 4.5	0.9 – 4.5	–	0.2	V
		I <sub>OL</sub> = 0.5 mA; V <sub>I</sub> = V <sub>IL</sub>	1.1	1.1	–	0.3	
		I <sub>OL</sub> = 2 mA; V <sub>I</sub> = V <sub>IL</sub>	1.4	1.4	–	0.35	
		I <sub>OL</sub> = 6 mA; V <sub>I</sub> = V <sub>IL</sub>	1.65	1.65	–	0.3	
			2.3	2.3	–	0.4	
		I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IL</sub>	2.7	2.7	–	0.4	
			2.3	2.3	–	0.6	
		I <sub>OL</sub> = 18 mA; V <sub>I</sub> = V <sub>IL</sub>	3.0	3.0	–	0.4	
I <sub>OL</sub> = 24 mA; V <sub>I</sub> = V <sub>IL</sub>	3.0	3.0	–	0.55			
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = V <sub>CCA</sub> or GND	0.9 – 4.5	0.9 – 4.5	-1.0	1.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	OE = 0 V	0 0.9 – 4.5	0.9 – 4.5 0	-1.0 -1.0	1.0 1.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	1.0	μA
I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	1.0	μA
I <sub>CCA</sub> + I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
ΔI <sub>CCA</sub>	Increase in I <sub>CC</sub> per Input Voltage, Other Inputs at V <sub>CCA</sub> or GND	V <sub>I</sub> = V <sub>CCA</sub> - 0.6 V; V <sub>I</sub> = V <sub>CCA</sub> or GND	4.5	4.5	–	10	μA
			3.6	3.6	–	5.0	
ΔI <sub>CCB</sub>	Increase in I <sub>CC</sub> per Input Voltage, Other Inputs at V <sub>CCA</sub> or GND	V <sub>I</sub> = V <sub>CCA</sub> - 0.6 V; V <sub>I</sub> = V <sub>CCA</sub> or GND	4.5	4.5	–	10	μA
			3.6	3.6	–	5.0	
I <sub>OZ</sub>	I/O Tri-State Output Leakage Current	T <sub>A</sub> = 25°C, OE = 0 V	0.9 – 4.5	0.9 – 4.5	-1.0	1.0	μA

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## TOTAL STATIC POWER CONSUMPTION ( $I_{CCA} + I_{CCB}$ )

$V_{CCA}$ (V)	-40°C to +85°C										Unit
	$V_{CCB}$ (V)										
	4.5		3.3		2.8		1.8		0.9		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
4.5		2		2		2		2		< 1.5	$\mu$ A
3.3		2		2		2		2		< 1.5	$\mu$ A
2.8		< 2		< 1		< 1		< 0.5		< 0.5	$\mu$ A
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	$\mu$ A
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	$\mu$ A

NOTE: Connect ground before applying supply voltage  $V_{CCA}$  or  $V_{CCB}$ . This device is designed with the feature that the power-up sequence of  $V_{CCA}$  and  $V_{CCB}$  will not damage the IC.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	$V_{CCA}$ (V)	-40°C to +85°C										Unit
			$V_{CCB}$ (V)										
			4.5		3.3		2.8		1.8		1.2		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$ (Note 1)	Propagation Delay, $A_n$ to $B_n$	4.5		1.6		1.8		2.0		2.1		2.3	nS
		3.3		1.7		1.9		2.1		2.3		2.6	
		2.8		1.9		2.1		2.3		2.5		2.8	
		1.8		2.1		2.4		2.5		2.7		3.0	
		1.2		2.4		2.7		2.8		3.0		3.3	
$t_{PZH}$ , $t_{PZL}$ (Note 1)	Output Enable, $\overline{OE}$ to $B_n$	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
$t_{PHZ}$ , $t_{PLZ}$ (Note 1)	Output Disable, $\overline{OE}$ to $B_n$	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
$t_{OSHL}$ , $t_{OSLH}$ (Note 1)	Output to Output Skew, Time	4.5		0.15		0.15		0.15		0.15		0.15	nS
		3.3		0.15		0.15		0.15		0.15		0.15	
		2.5		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

1. Propagation delays defined per Figure 2.

## CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
$C_{IN}$	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	5.0	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA}$ , $f = 10$ MHz	20	pF

2. Typical values are at  $T_A = +25^\circ\text{C}$ .

3.  $C_{PD}$  is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:  
 $I_{CC(\text{operating})} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$  where  $I_{CC} = I_{CCA} + I_{CCB}$  and  $N_{SW}$  = total number of outputs switching.

# NLSV2T244

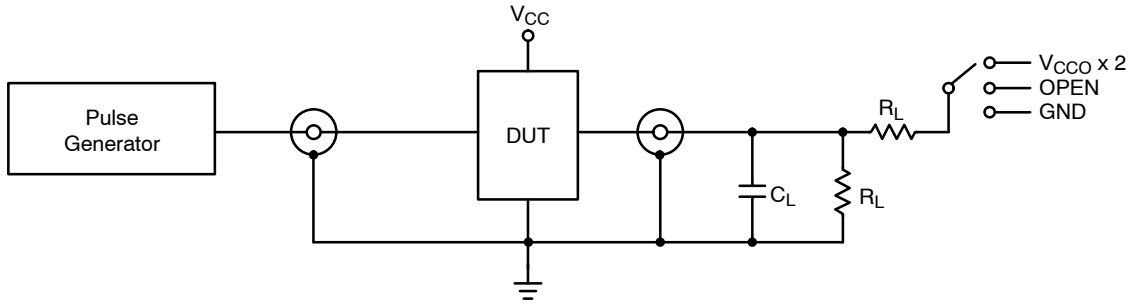
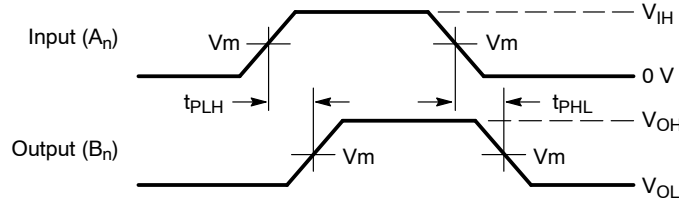


Figure 2. AC (Propagation Delay) Test Circuit

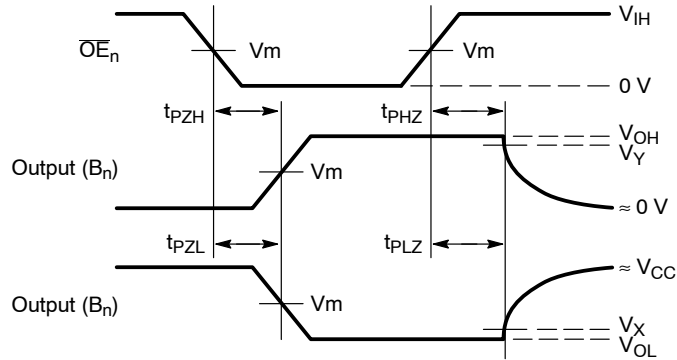
Test	Switch
$t_{PLH}$ , $t_{PHL}$	OPEN
$t_{PLZ}$ , $t_{PZL}$	$V_{CC} \times 2$
$t_{PHZ}$ , $t_{PZH}$	GND

$C_L = 15 \text{ pF}$  or equivalent (includes probe and jig capacitance)  
 $R_L = 2 \text{ k}\Omega$  or equivalent  
 $Z_{OUT}$  of pulse generator =  $50 \Omega$



Waveform 1 - Propagation Delays

$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$



Waveform 2 - Output Enable and Disable Times

$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

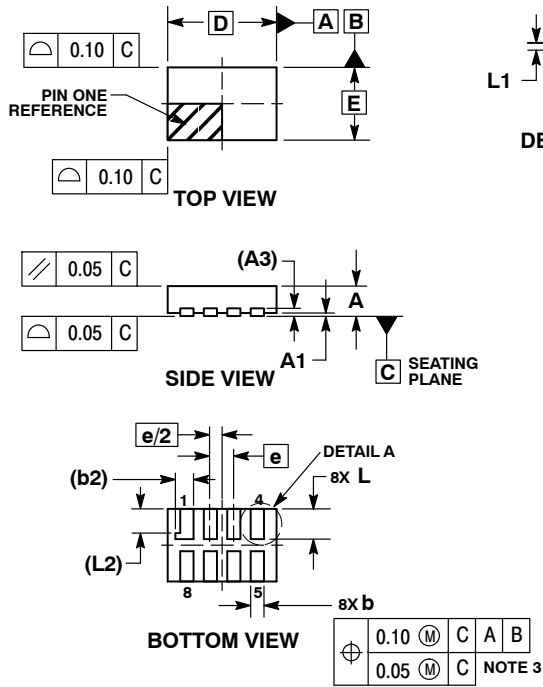
Figure 3. AC (Propagation Delay) Test Circuit Waveforms

Symbol	$V_{CC}$				
	3.0 V - 4.5 V	2.3 V - 2.7 V	1.65 V - 1.95 V	1.4 V - 1.6 V	0.9 V - 1.3 V
$V_{mA}$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$
$V_{mB}$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$
$V_X$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$
$V_Y$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$

# NLSV2T244

## PACKAGE DIMENSIONS

UDFN8 1.8 x 1.2, 0.4P  
CASE 517AJ  
ISSUE O

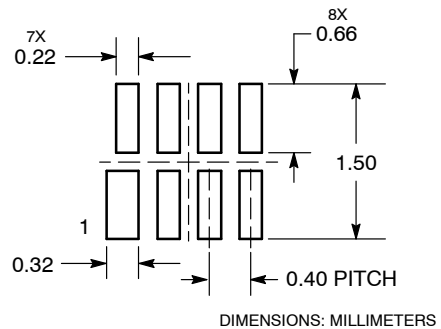


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
b2	0.30	REF
D	1.80	BSC
E	1.20	BSC
e	0.40	BSC
L	0.45	0.55
L1	0.00	0.03
L2	0.40	REF

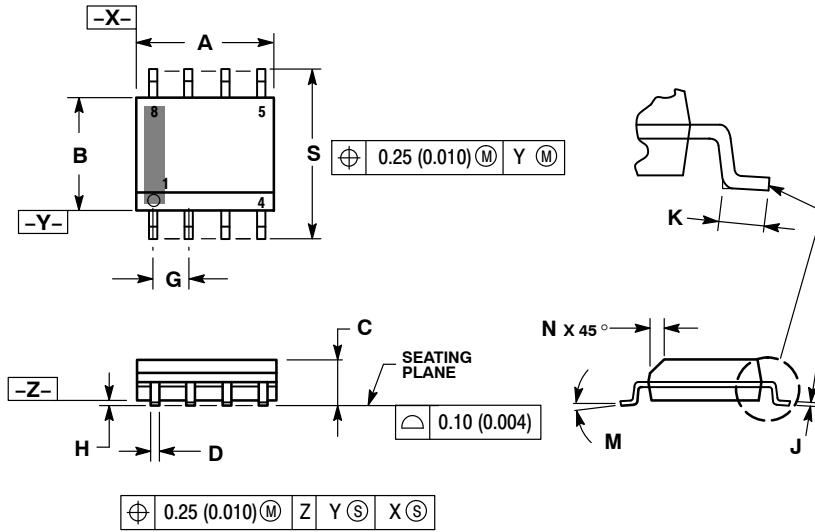
**MOUNTING FOOTPRINT  
SOLDERMASK DEFINED**



# NLSV2T244

## PACKAGE DIMENSIONS

SO-8  
CASE 751-07  
ISSUE AJ

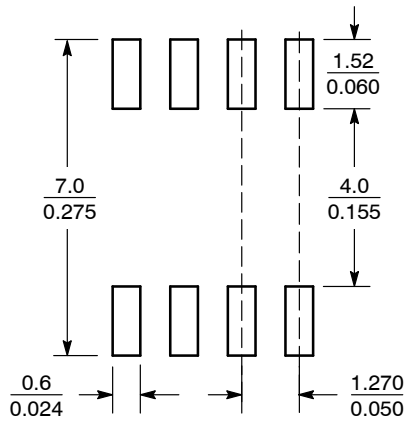


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

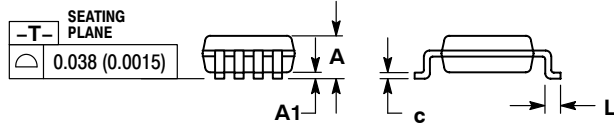
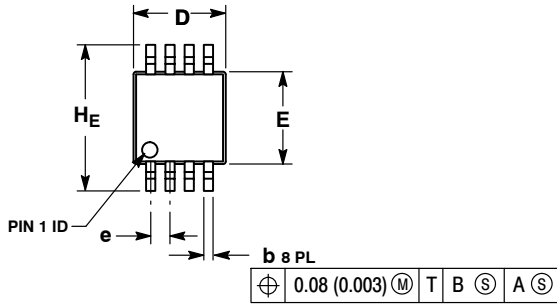
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



# NLSV2T244

## PACKAGE DIMENSIONS

Micro8™  
CASE 846A-02  
ISSUE H

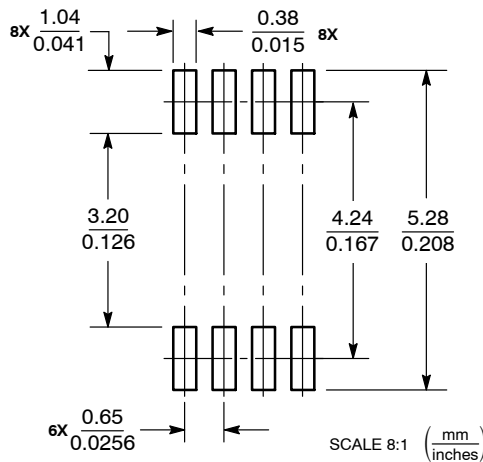


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
HE	4.75	4.90	5.05	0.187	0.193	0.199

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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