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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

February 2011

74AC14, 74ACT14
Hex Inverter with Schmitt Trigger Input

Features

- I_{CC} reduced by 50%
- Outputs source/sink 24mA
- 74ACT14 has TTL-compatible inputs

General Description

The 74AC14 and 74ACT14 contain six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

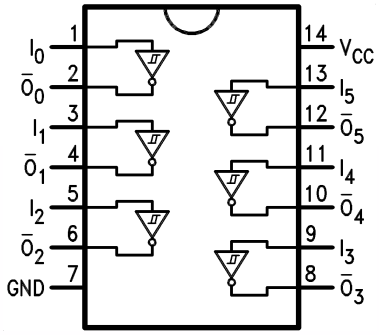
The 74AC14 and 74ACT14 have hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Ordering Information

Order Number	Package Number	Package Description
74AC14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

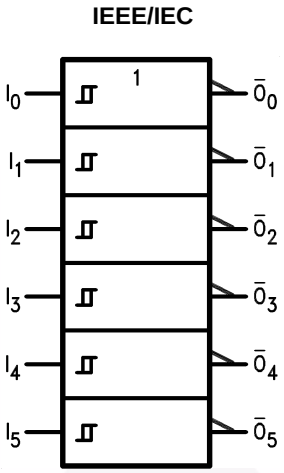
Connection Diagram



Pin Description

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Logic Symbol



Function Table

Input	Output
A	$\overline{\mathbf{O}}$
L	H
H	L

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = –0.5V$	–20mA
	$V_I = V_{CC} + 1.5$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 1.5V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = –50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	I_{OH} = 12mA		2.56	2.46	
		4.5	I_{OH} = 24mA		3.86	3.76	
		5.5	I_{OH} = 24mA(1)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	I_{OL} = 12mA		0.36	0.44	
		4.5	I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA(1)		0.36	0.44	
I_{IN}(3)	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	µA
V_{t+}	Maximum Positive Threshold	3.0	T_A = Worst Case		2.2	2.2	V
		4.5			3.2	3.2	
		5.5			3.9	3.9	
V_{t-}	Minimum Negative Threshold	3.0	T_A = Worst Case		0.5	0.5	V
		4.5			0.9	0.9	
		5.5			1.1	1.1	
$V_{H(MAX)}$	Maximum Hysteresis	3.0	T_A = Worst Case		1.2	1.2	V
		4.5			1.4	1.4	
		5.5			1.6	1.6	
$V_{H(MIN)}$	Minimum Hysteresis	3.0	T_A = Worst Case		0.3	0.3	V
		4.5			0.4	0.4	
		5.5			0.5	0.5	
I_{OLD}	Minimum Dynamic	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}	Output Current(2)	5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}(3)	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		2.0	20.0	µA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = –50µA	4.49	4.34	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA		3.86	3.76	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA(4)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50µA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA		0.36	0.44	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA(4)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
$V_{H(MAX)}$	Maximum Hysteresis	4.5	T_A = Worst Case		1.4	1.4	V
		5.5			1.6	1.6	
$V_{H(MIN)}$	Minimum Hysteresis	4.5	T_A = Worst Case		0.4	0.4	V
		5.5			0.5	0.5	
V_{t+}	Maximum Positive Threshold	4.5	T_A = Worst Case		2.0	2.0	V
		5.5			2.0	2.0	
$V_{t–}$	Minimum Negative Threshold	4.5	T_A = Worst Case		0.8	0.8	V
		5.5			0.8	0.8	
I_{CCT}	Maximum I_{CC}/Input	5.5	V_I = V_{CC} – 2.1V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current(5)	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		2.0	20.0	µA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.5	15.0	ns
		5.0	1.5	7.0	10.0	1.5	11.0	
t_{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.5	13.0	ns
		5.0	1.5	6.0	8.5	1.5	9.5	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

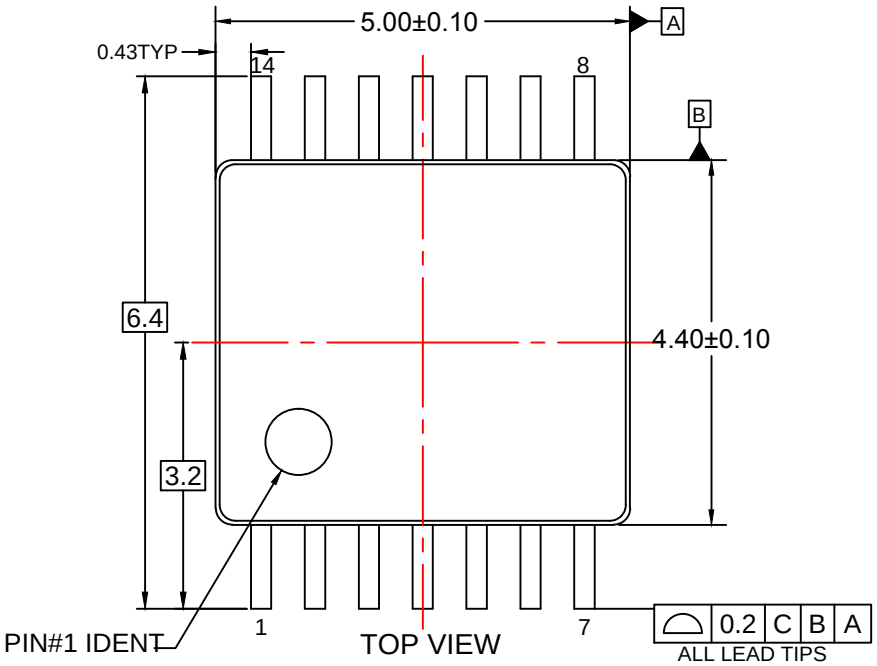
Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay	5.0	3.0	8.0	10.0	3.0	11.0	ns
t_{PHL}	Propagation Delay	5.0	3.0	8.0	10.0	3.0	11.0	ns

Note:

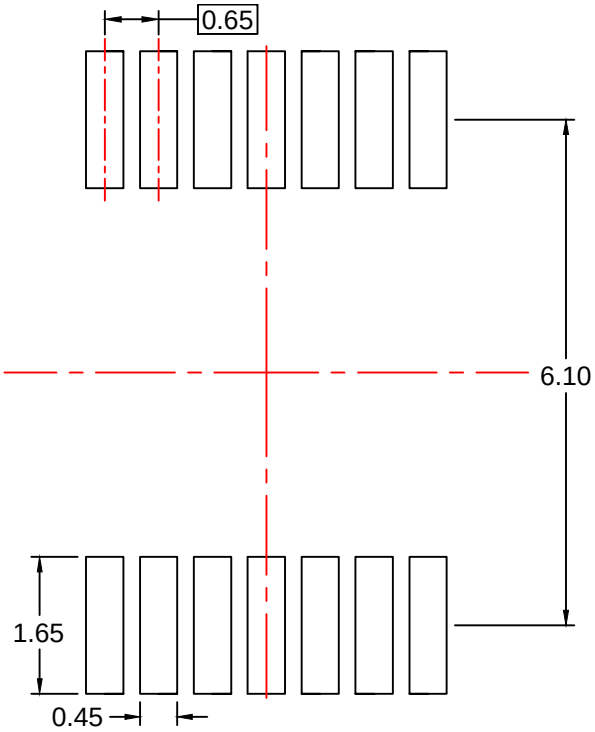
7. Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

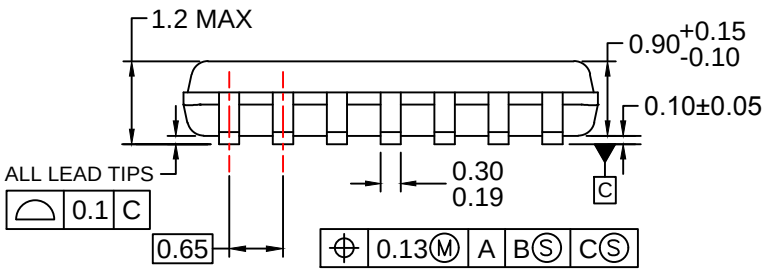
Symbol	Parameter	Conditions	Typ	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V		
	AC		25.0	pF
	ACT		80	



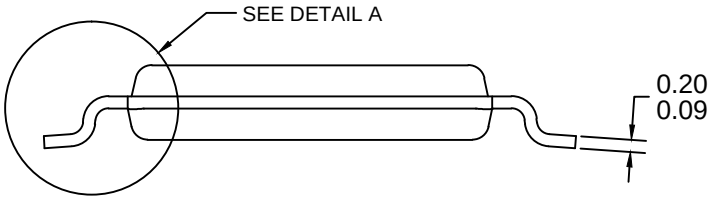
TOP VIEW

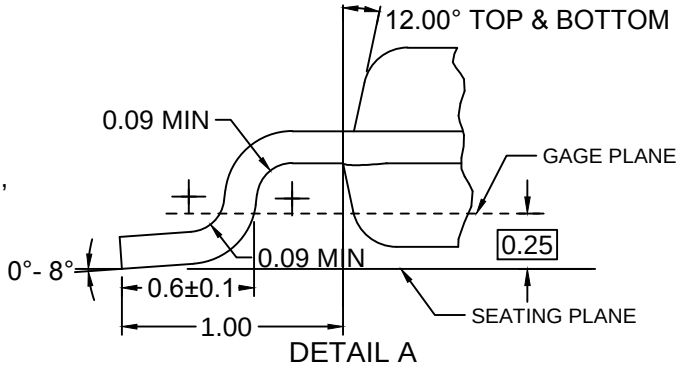


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

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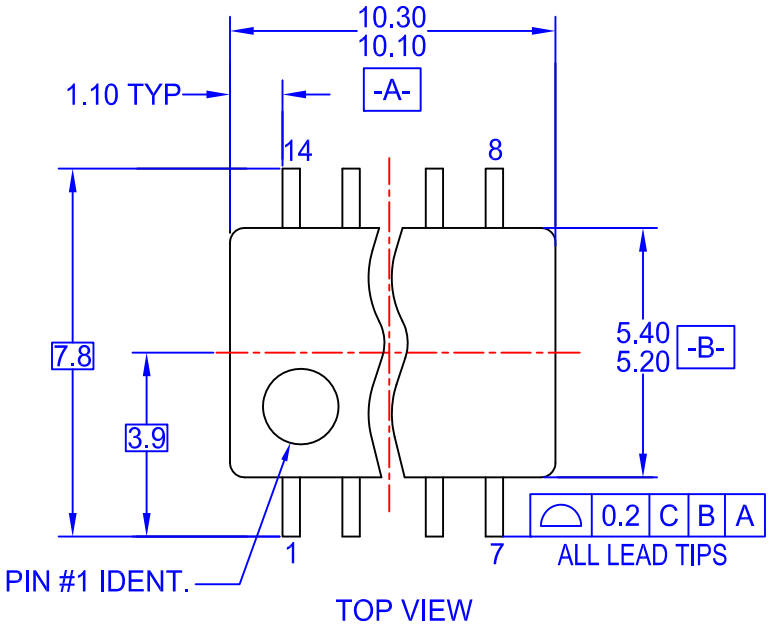
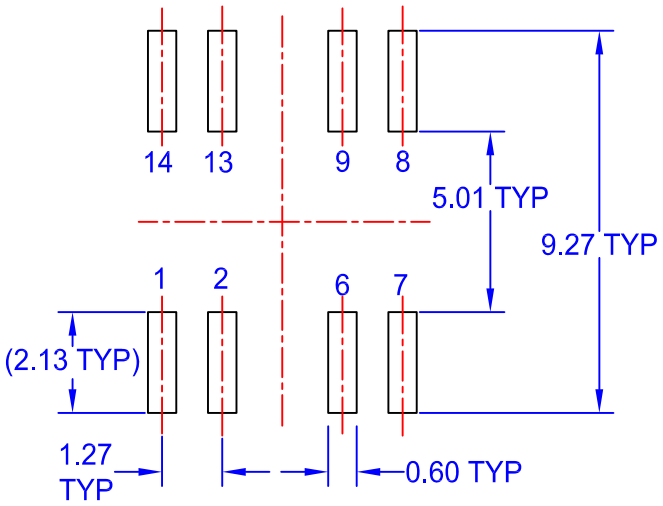


TOP VIEW



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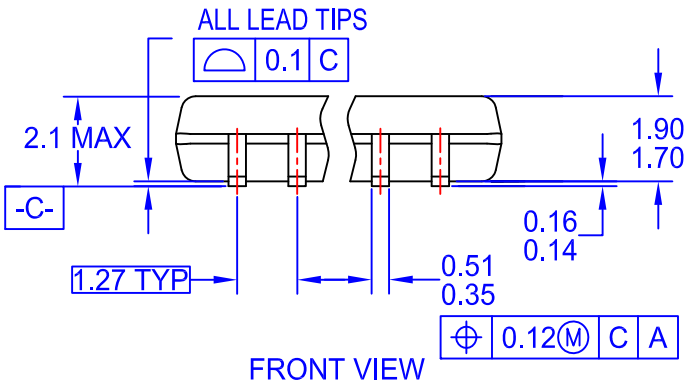
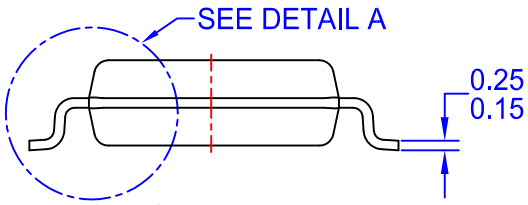
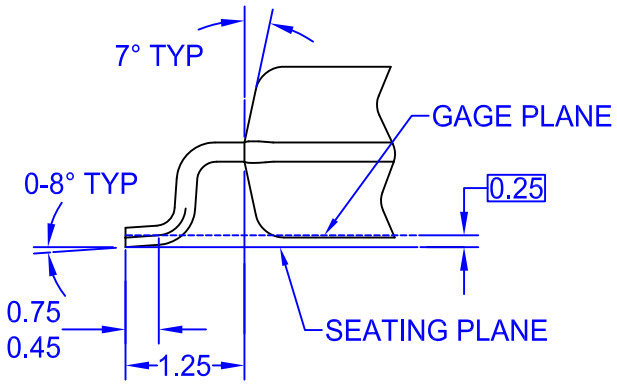


FRONT VIEW



SIDE VIEW

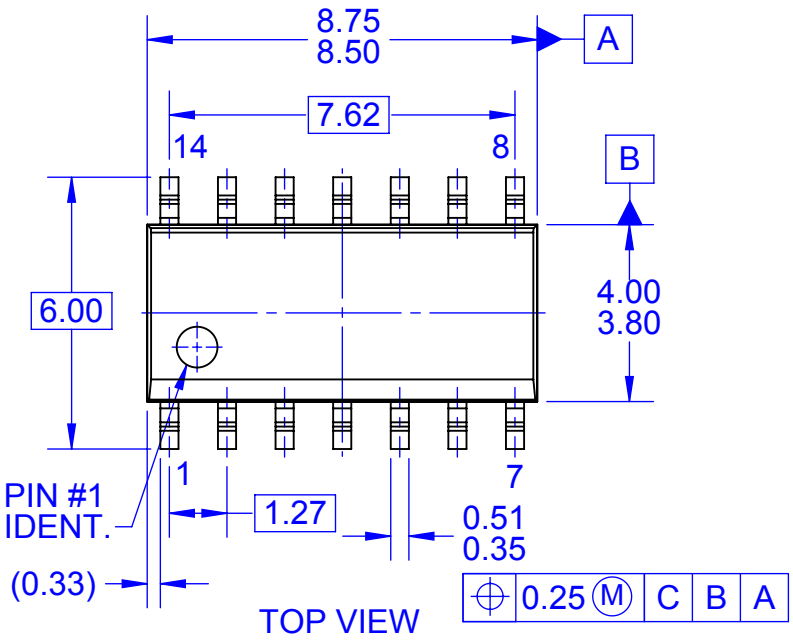


DETAIL A

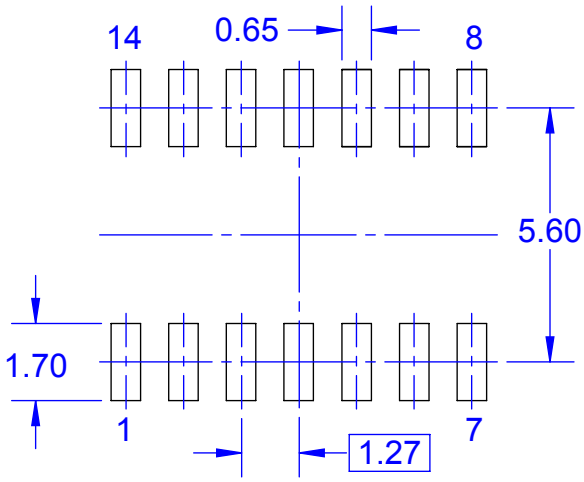
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DRAWING FILENAME: MKT-M14Drev4.

FAIRCHILD ™



TOP VIEW



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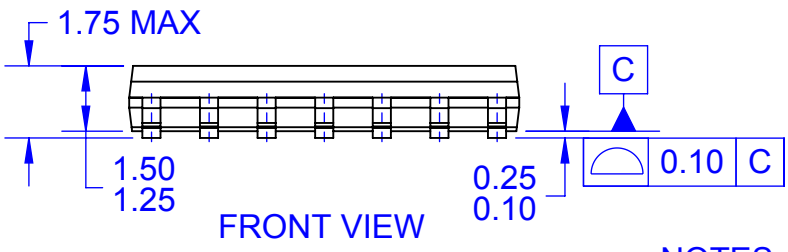

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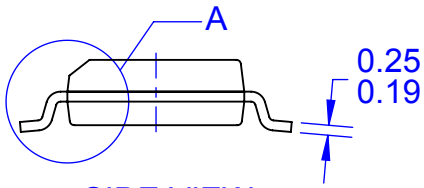
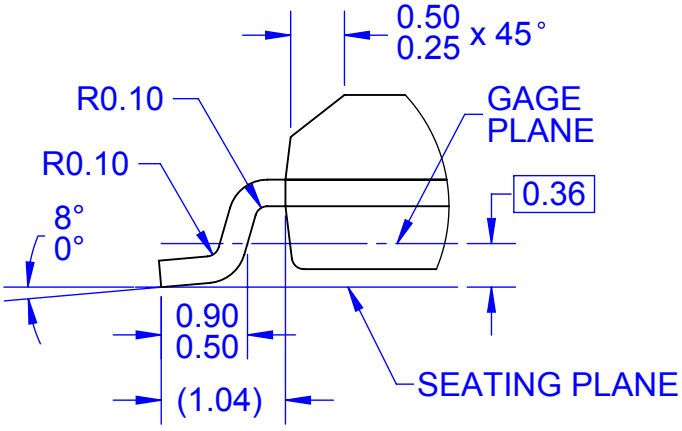


SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14



DETAIL A
SCALE 16 : 1

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