

RX24T Group Renesas MCUs

R01DS0257EJ0200

Rev.2.00

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80-MHz 32-bit RX MCUs, on-chip FPU, 153.6 DMIPS, power supply 5 V, 12-bit ADC (equipped with 3-channel synchronous S/H circuits, double data registers, operating amplifiers, comparator) 3 units, Simultaneous sampling up to ADC 5 channels, CAN, 80-MHz PWM (three-phase complementary output × 2 channels + single-phase complementary output × 4 channels or three-phase complementary × 3 channels + single-phase complementary × 1 channel)

Features

■ 32-bit RXv2 CPU core

- Max. operating frequency: 80 MHz
Capable of 153.6 DMIPS in operation at 80 MHz
- Enhanced DSP: 32-bit multiply-accumulate and 16-bit multiply-subtract instructions supported
- Built-in FPU: 32-bit single-precision floating point (compliant to IEEE754)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported

■ Low power design and architecture

- Operation from a single 2.7-V to 5.5-V supply
- Three low power consumption modes

■ On-chip code flash memory

- 512-/384-/256-/128-Kbyte capacities
- On-board or off-board user programming
- For instructions and operands

■ On-chip data flash memory

- 8-Kbyte (Number of erase/write cycles: 1,000,000 (typ))
- BGO (Back Ground Operation)

■ On-chip SRAM, no wait states

- 32-/16-Kbytes of SRAM

■ Data transfer functions

- DTC: Four transfer modes

■ Reset and supply management

- Seven types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- Main clock oscillator frequency: 1 to 20 MHz
- External clock input frequency: Up to 20 MHz
- PLL circuit input: 4 MHz to 12.5 MHz
- On-chip low-speed oscillators, On-chip high-speed oscillators, dedicated on-chip oscillator for the IWDT
- Clock frequency accuracy measurement circuit (CAC)

■ Independent watchdog timer

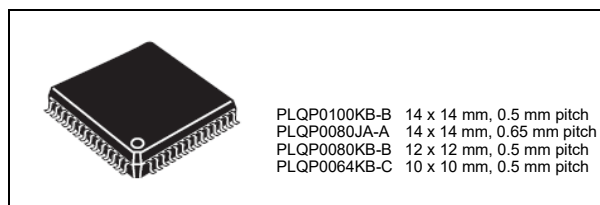
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance

- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ MPC

- Multiple locations are selectable for I/O pins of peripheral functions



■ Up to 6 communications channels

- CAN (compliant with ISO11898-1), incorporating 16 message boxes (1 channel)
- SCI with many useful functions (3 channels)
Asynchronous mode, clock synchronous mode, smart card interface mode, simplified SPI, simplified I²C, and extended serial mode.
- I²C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (1 channel)
- RSPI capable of high speed connection Transfer at up to 20 Mbps (1 channel)

■ Up to 25 extended-function timers

- 16-bit MTU3: 80 MHz operation, input capture, output compare, three-phase complementary PWM × 2 channels output, CPU-efficient complementary PWM, phase counting mode (nine channels)
- 16-bit GPT: 80 MHz operation, input capture, output compare, PWM wave-form single-phase complementary × 4 channels output or three-phase × 1 channel + single-phase complementary × 1 channel output, comparator interlocking operation (count operation, PWM negate control) (4 channels)
- 8-bit TMRs (8 channels)
- 16-bit compare-match timers (4 channels)

■ 12-bit A/D converter: 22 channels in 3 units

- Incorporating sample-and-hold circuit 12 bits × 3 units (unit 0: 5 channels, unit 1: 5 channels, unit 2: 12 channels)
- Sampling time can be set for each channel
- Group scan priority control mode (3 levels)
- Self-diagnostic function and analog input disconnection detection assistance function (compliant to IEC60730)
- Input signal amplitude by the programmable gain amplifier (4 channels)
- ADC: 3-channel simultaneous sample-and-hold circuit (3 shunt method), double data register (1 shunt method), amplifier (4 channels), comparator (4 channels)

■ 8-bit D/A converter: 2 channels

- This can be used as reference voltage for a comparator

■ Register write protection function can protect values in important registers against overwriting.

■ Up to 81 pins for general I/O ports

- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Operating temperature range

- -40 to +85°C

■ Applications

- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 shows the outline of maximum specifications, and the numbers of peripheral modules and of channels of the modules differ depending on chip version and the pin number on the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/4)

| Classification | Module/Function | Description |
|-----------------------|--|---|
| CPU | CPU | <ul style="list-style-type: none"> Maximum operating frequency: 80 MHz 32-bit RX CPU (RX v2) Minimum instruction execution time: One instruction per clock cycle Address space: 4-Gbyte linear Register set <ul style="list-style-type: none"> General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers Basic instructions: 75 Variable-length instruction format Floating-point instructions: 11 DSP instructions: 23 Addressing modes: 11 Data arrangement <ul style="list-style-type: none"> Instructions: Little endian Data: Selectable as little endian or big endian On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit On-chip divider: 32-bit ÷ 32-bit → 32-bit Barrel shifter: 32 bits ROM cache: 2 Kbytes (disabled by default) |
| | FPU | <ul style="list-style-type: none"> Single precision (32-bit) floating point Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | ROM | <ul style="list-style-type: none"> Capacity: 128 K/256 K/384 K/512 Kbytes Up to 32 MHz, no-wait memory access 32 to 80 MHz: wait states Off-board programming Programming/erasing method: <ul style="list-style-type: none"> Serial programming (asynchronous serial communication), self-programming |
| | RAM | <ul style="list-style-type: none"> Capacity: 16 K/32 Kbytes 80 MHz, no-wait memory access |
| | E2 DataFlash | <ul style="list-style-type: none"> Capacity: 8 Kbytes Number of erase/write cycles: 1,000,000 (typ) |
| MCU operating mode | | Single-chip mode |
| Clock | Clock generation circuit | <ul style="list-style-type: none"> Main clock oscillator, low- and high-speed on-chip oscillators, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) <p>The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 80 MHz (at max.)</p> <p>The MTU3 and GPT modules run in synchronization with the PCLKA: 80 MHz (at max.)</p> <p>The peripheral modules other than MTU3 and GPT run in synchronization with the PCLKB: 40 MHz (at max.)</p> <p>ADCLK operated in S12AD runs in synchronization with the PCLKD: 40 MHz (at max.)</p> <p>The flash memory peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)</p> |
| Resets | | RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset |
| Voltage detection | Voltage detection circuit (LVDAb) | <ul style="list-style-type: none"> When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 9 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels |
| Low power consumption | Low power consumption functions | <ul style="list-style-type: none"> Module stop function Three low power consumption modes <ul style="list-style-type: none"> Sleep mode, deep sleep mode, and software standby mode |
| | Function for lower operating power consumption | <ul style="list-style-type: none"> Operating power control modes <ul style="list-style-type: none"> High-speed operating mode and middle-speed operating mode |

Table 1.1 Outline of Specifications (2/4)

| Classification | Module/Function | Description |
|-------------------------------------|---|--|
| Interrupt | Interrupt controller (ICUb) | <ul style="list-style-type: none"> • Interrupt vectors: 163 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDI interrupt) • 16 levels specifiable for the order of priority |
| DMA | Data transfer controller (DTCa) | <ul style="list-style-type: none"> • Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function |
| I/O ports | General I/O ports | 100-pin/80-pin/64-pin <ul style="list-style-type: none"> • I/O: 80/60/48 • Input: 1/1/1 • Pull-up resistors: 80/60/48 • Open-drain outputs: 60/45/37 • 5-V tolerance: 2/2/2 |
| Multi-function pin controller (MPC) | | Capable of selecting the input/output function from multiple pins |
| Timers | Multi-function timer pulse unit 3 (MTU3d) | <ul style="list-style-type: none"> • 9 units (16 bits × 9 channels) • Provides up to 28 pulse-input/output lines and three pulse-input lines • Select from among fourteen counter-input clock signals for each channel (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, PCLK/32, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) other than channel 1/3/4/6/7, for which only eleven signals are available, channel 2 for 12, channel 5 for 10 • 43 general registers including 28 output compare/input capture registers • Counter clear operation (with compare match- or input capture-sourced simultaneous counter clear capability) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffer operation • Cascaded operation • 45 interrupt sources • Automatic transfer of register data • Pulse output modes: Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode <ul style="list-style-type: none"> • 3-phase non-overlapping waveform output for inverter control • Automatic dead time setting • Adjustable PWM duty cycle: from 0 to 100% • A/D conversion request delaying function • Interrupt at crest/trough can be skipped • Double buffer function • Reset-synchronized PWM mode <ul style="list-style-type: none"> • Outputs three phases each for positive and negative PWM waveforms in user-specified duty cycle • Phase counting modes: 16-bit mode (channel 1 and 2)/32-bit mode (channel 1 and 2) • Dead time compensation counter function • A/D converter start trigger can be generated • A/D converter start triggers can be skipped • Signals from the input capture and external counter clock pins are input via a digital filter |
| | Port output enable 3 (POE3b, POE3A) | <ul style="list-style-type: none"> • POE3b <ul style="list-style-type: none"> • Control of the high-impedance state of the MTU3's waveform output pins • Startup by input from signal sources on 6 pins (POE0#, POE4#, POE8#, POE10#, POE11#, and POE12#) • Startup by detection of short-circuited outputs (detection of simultaneous PMW output at the active level) • Startup by detection of oscillation stopping or by a comparator, or under software control • Control of addition of pins for output control is programmable • POE3A (The following functions are added to the POE3b) <ul style="list-style-type: none"> • Control of the high-impedance state of GPT's waveform output pins • Control of the MTU3/GPT waveform output pins and switching them to operate as general I/O ports • A comparator detection interrupt source can be set for each output pin group |

Table 1.1 Outline of Specifications (3/4)

| Classification | Module/Function | Description |
|----------------|--|--|
| Timers | General PWM timer (GPTB) | <ul style="list-style-type: none"> • 16 bits × 4 channels • Two channels can be cascaded and used as a 32-bit timer • Counting up or down (saw waves), or counting up and down (triangle waves) is selectable for each counter. • A count clock is selectable from 13 types (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, PCLK/32, PCLK/64, PCLK/256, PCLK/1024, GTECLKA, GTECLKB, GTECLKC, and GTECLKD) for each channel. • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronous operation of the several counters • Modes of synchronous operation (synchronized or displaced by a desired time to obtain relative phase shifts) • Generation of dead times in PWM operation • Through combination of three counters, generation of three-phased PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the comparator detection, MTU3 count start, software, compare match • Noise filter function for signals on the Input capture, external trigger pins, and the external count clock pins • A/D converter start triggers can be generated |
| | Compare match timer (CMT) | <ul style="list-style-type: none"> • (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Independent watchdog timer (IWDtA) | <ul style="list-style-type: none"> • 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDtA-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256 |
| | 8-bit timer (TMR) | <ul style="list-style-type: none"> • (8 bits × 2 channels) × 4 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer • Generates A/D conversion start trigger • Generates baud rate clock for the SCI5 and SCI6 |
| | Communication functions | Serial communications interfaces (SCIg) |
| | I ² C bus interface (RIICa) | <ul style="list-style-type: none"> • 1 channel • Communications formats: I²C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode |
| | CAN module (RSCAN) | <ul style="list-style-type: none"> • Single channel • ISO11898-1 specifications compliant (standard and extended frames) • 16 message boxes |
| | Serial peripheral interface (RSPIb) | <ul style="list-style-type: none"> • 1 channel • Transfer facility <p>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)</p> <ul style="list-style-type: none"> • Capable of handling serial transfer as a master or slave • Data formats <p>Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)</p> <ul style="list-style-type: none"> • Double buffers for both transmission and reception |

Table 1.1 Outline of Specifications (4/4)

| Classification | Module/Function | Description |
|---|--|--|
| 12-bit A/D converter (S12ADF) | | <ul style="list-style-type: none"> • 12 bits (5 channels × 2 units/12 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 μs per channel when the ADCLK is operating at 40 MHz • Operating modes <ul style="list-style-type: none"> Scan mode (single scan mode, continuous scan mode, and 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sampling variable <ul style="list-style-type: none"> Sampling time can be set up for each channel • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Assist on analog input disconnection detection • A/D conversion start conditions <ul style="list-style-type: none"> A software trigger, a trigger from a timer (MTU3, GPT, TMR), or an external trigger signal • Sample-and-hold function <ul style="list-style-type: none"> Sample-and-hold circuit included (3 channels for unit 1) • Amplification of input signals by a programmable gain amplifier (1 channel for unit 0, 3 channels for unit 1) <ul style="list-style-type: none"> Amplification rate: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times (total of 6 steps) |
| Comparator C (CMPC) | | <ul style="list-style-type: none"> • 4 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage: Select from among two voltages • Analog input voltage is selectable from 4 inputs |
| 8-bit D/A converter (DA, DAa) | | <ul style="list-style-type: none"> • DA <ul style="list-style-type: none"> 1 channel 8-bit resolution Output voltage: 0 V to VREF Dedicated for generating comparator C reference voltage • DAa <ul style="list-style-type: none"> 2 channels 8-bit resolution Output voltage: 0 V to VREF Can be output externally and used as comparator C reference voltage |
| Safety | Memory protection unit (MPU) | <ul style="list-style-type: none"> • Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area. |
| | Register write protection function | <ul style="list-style-type: none"> • Protects important registers from being overwritten for in case a program runs out of control. |
| | CRC calculator (CRC) | <ul style="list-style-type: none"> • CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| | Main clock oscillation stop function | <ul style="list-style-type: none"> • Main clock oscillation stop detection: Available |
| | Clock frequency accuracy measurement circuit (CAC) | <ul style="list-style-type: none"> • Monitors the clock output from the main clock oscillator, high-speed on-chip oscillator, low-speed on-chip oscillator, the PLL frequency synthesizer, IWDG-dedicated on-chip oscillator, and PCLKB. |
| | Data operation circuit (DOC) | The function to compare, add, or subtract 16-bit data |
| Power supply voltages/Operating frequencies | | VCC = 2.7 to 5.5 V: 80 MHz |
| Packages | | 100-pin LQFP 0.5 mm pitch 80-pin LQFP 0.65 mm pitch 80-pin LQFP 0.5 mm pitch 64-pin LQFP 0.5 mm pitch |
| On-chip debugging system | | E1 emulator (FINE interface) |

Table 1.2 Comparison of Functions for Different Packages

| Module/Functions | | RX24T Group | | | |
|---|--|--|--|--|--------|
| | | Chip Version B | Chip Version A | | |
| | | 100 Pins | 100 Pins | 80 Pins | 64Pins |
| Memory | ROM | 512 K/384 K/ 256 Kbytes | 256 K/128 Kbytes | | |
| | RAM | 32 Kbytes | 16 Kbytes | | |
| | E2 DataFlash | 8 Kbytes | | | |
| Interrupts | External interrupts | NMI, IRQ0 to IRQ7 | | | |
| DTC | Data transfer controller (DTCa) | Available | | | |
| Timers | Multi-function timer pulse unit 3 (MTU3d) | 9 channels | | | |
| | General PWM timer (GPTB) | 4 channels | Not supported | | |
| | Port output enable 3 (POE3b) | Not supported | Available | | |
| | Port output enable 3 (POE3A) | Available | Not supported | | |
| | 8-bit timer (TMR) | 2 channels × 4 units | | | |
| | Compare match timer (CMT) | 2 channels × 2 units | | | |
| | Independent watchdog timer (IWDTa) | Available | | | |
| Communications | Serial communications interfaces (SCIg) [including simple I ² C and simple SPI] | 3 channels (SCI1, SCI5, SCI6) | | | |
| | I ² C bus interface (RIICa) | 1 channel | | | |
| | Serial peripheral interface (RSP1b) | 1 channel | | | |
| | CAN module (RSCAN) | 1 channel | Not supported | | |
| 12-bit A/D converter (S12ADF) (Internal high-precision channel) | | 5 channels × 2 units, 12 channels × 1 unit (4 channels × 2 units, 12 channels × 1 unit) | 5 channels × 2 units, 7 channels × 1 unit (4 channels × 2 units, 7 channels × 1 unit) | 3 channels × 1 unit, 4 channels × 1 unit, 5 channels × 1 unit (3 channels × 1 unit, 3 channels × 1 unit, 5 channels × 1 unit) | |
| | 3 channels simultaneous sampling | 3 channels/unit 1 | | | |
| | Programmable gain amplifier | 1 channel/unit 0, 3 channels/unit 1 | | | |
| Comparator C (CMPC) | | 4 channels | | | |
| | | Without reference voltage external input | With reference voltage external input | | |
| 8-bit D/A converter (DA) | Not supported | Available | | | |
| 8-bit D/A converter (DAa) | Available | Not supported | | | |
| CRC calculator (CRC) | Available | | | | |
| Packages | 100-pin LQFP | 100-pin LQFP | 80-pin LQFP/LQFP | 64-pin LQFP | |

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

| Group | Part No. | Part No. (for Orders) | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Operating Frequency (max.) | Chip Version | |
|-------|--------------|-----------------------|--------------|--------------|--------------|--------------|----------------------------|--------------|------------|
| RX24T | R5F524TEADFP | R5F524TEADFP#31 | PLQP0100KB-B | 512 Kbytes | 32 Kbytes | 8 Kbytes | 80 MHz | B | |
| | R5F524TCADFP | R5F524TCADFP#31 | PLQP0100KB-B | 384 Kbytes | | | | | |
| | R5F524TBADFP | R5F524TBADFP#31 | PLQP0100KB-B | 256 Kbytes | | | | | |
| | R5F524TAADFP | R5F524TAADFP#31 | PLQP0100KB-B | 256 Kbytes | 16 Kbytes | 8 Kbytes | 80 MHz | A | |
| | R5F524TAADFF | R5F524TAADFF#31 | PLQP0080JA-A | | | | | | |
| | R5F524TAADFN | R5F524TAADFN#31 | PLQP0080KB-B | | | | | | |
| | R5F524TAADFM | R5F524TAADFM#31 | PLQP0064KB-C | | | | | | |
| | R5F524T8ADFP | R5F524T8ADFP#31 | PLQP0100KB-B | | | | | | 128 Kbytes |
| | R5F524T8ADFF | R5F524T8ADFF#31 | PLQP0080JA-A | | | | | | |
| | R5F524T8ADFN | R5F524T8ADFN#31 | PLQP0080KB-B | | | | | | |
| | R5F524T8ADFM | R5F524T8ADFM#31 | PLQP0064KB-C | | | | | | |

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.

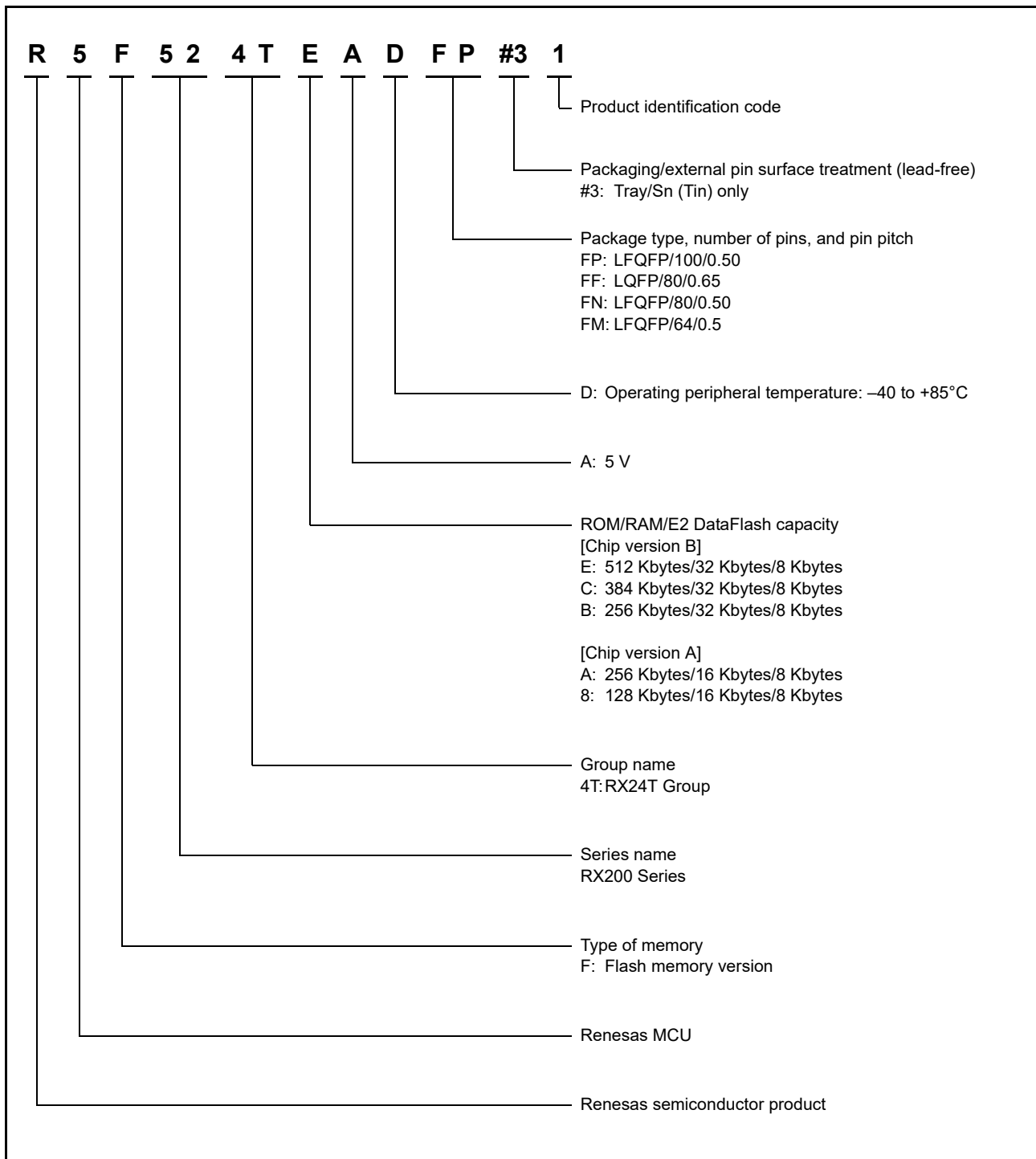


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

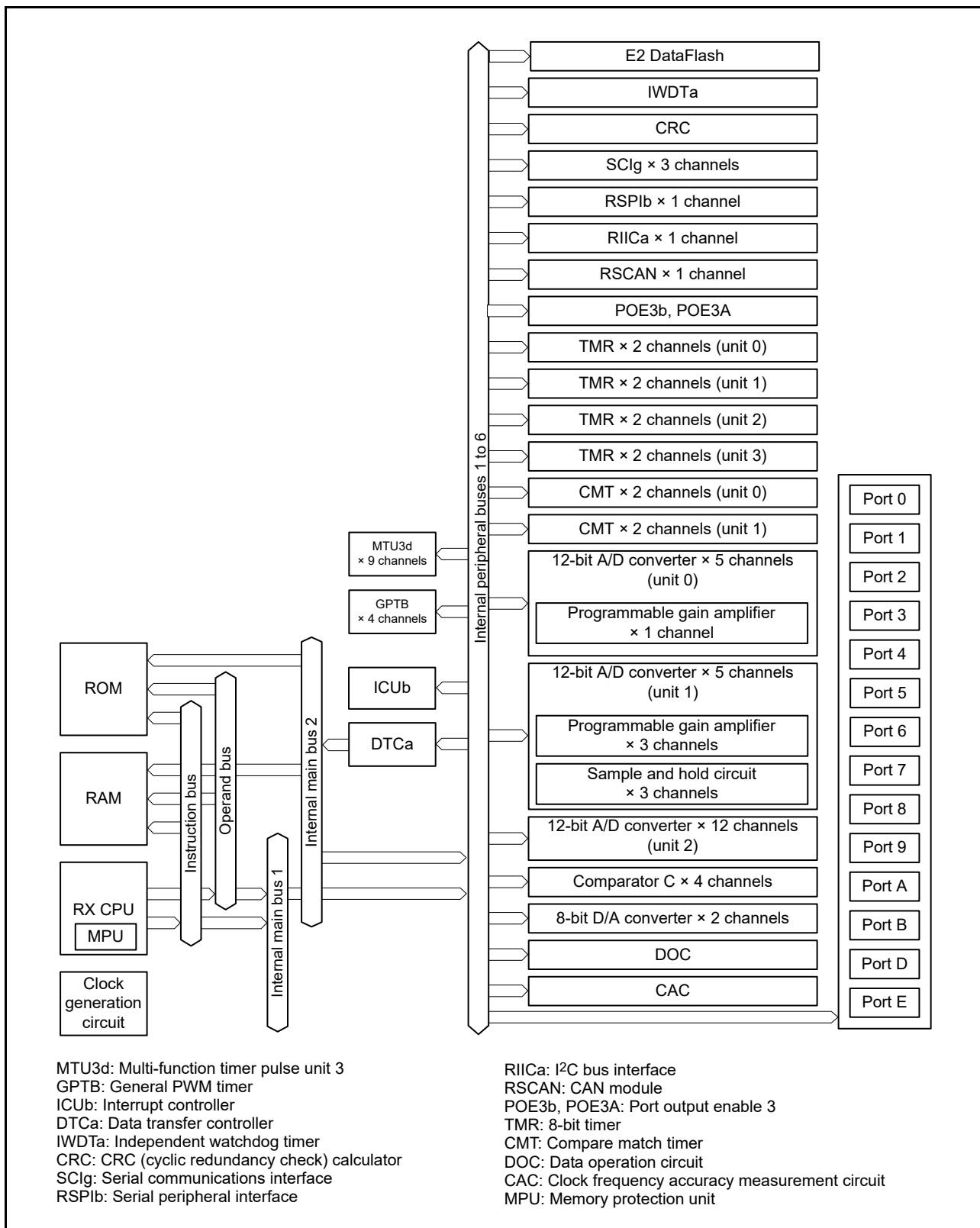


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/4)

| Classifications | Pin Name | I/O | Description |
|---|--|--|--|
| Power supply | VCC | — | Power supply pin. Connect it to the system power supply. |
| | VCL | — | Connect this pin to the VSS pin via the 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VSS | — | Ground pin. Connect it to the system power supply (0 V). |
| Clock | XTAL | Output | Pins for connecting a crystal. An external clock can be input through the EXTAL pin. |
| | EXTAL | Input | |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal levels on this pin must not be changed during operation. |
| System control | RES# | Input | Reset pin. This MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Input pin for the clock frequency accuracy measurement circuit. |
| On-chip emulator | FINED | I/O | FINE interface pin. |
| Interrupts | NMI | Input | Non-maskable interrupt request pin. |
| | IRQ0 to IRQ7 | Input | Interrupt request pins. |
| Multi-function timer pulse unit 3 (MTU3d) | MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins. |
| | MTIOC0A#, MTIOC0B#, MTIOC0C#, MTIOC0D# | I/O | The TGRA0 to TGRD0 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins. |
| | MTIOC1A#, MTIOC1B# | I/O | The TGRA1 and TGRB1 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins. |
| | MTIOC2A#, MTIOC2B# | I/O | The TGRA2 and TGRB2 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins. |
| | MTIOC3A#, MTIOC3B#, MTIOC3C#, MTIOC3D# | I/O | The TGRA3 to TGRD3 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins. |
| | MTIOC4A#, MTIOC4B#, MTIOC4C#, MTIOC4D# | I/O | The TGRA4 to TGRD4 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIC5U, MTIC5V, MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins. |
| | MTIC5U#, MTIC5V#, MTIC5W# | Input | The TGRU5, TGRV5, and TGRW5 input capture inverted input/external pulse inverted input pins. |
| | MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D | I/O | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins. |
| | MTIOC6A#, MTIOC6B#, MTIOC6C#, MTIOC6D# | I/O | The TGRA6 to TGRD6 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D | I/O | The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins. | |
| MTIOC7A#, MTIOC7B#, MTIOC7C#, MTIOC7D# | I/O | The TGRA7 to TGRD7 input capture inverted input/output compare inverted output/PWM inverted output pins. | |
| MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D | I/O | The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins. | |

Table 1.4 Pin Functions (2/4)

| Classifications | Pin Name | I/O | Description |
|---|---|--|--|
| Multi-function timer pulse unit 3 (MTU3d) | MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D# | I/O | The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTCLKA, MTCLKB, MTCLKC, MTCLKD | Input | Input pins for the external clock. |
| | MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD# | Input | Inverted input pins for the external clock. |
| | ADSM0, ADSM1 | Output | A/D trigger output pins. |
| General PWM timer (GPTB) | GTIOC0A, GTIOC0B | I/O | The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins |
| | GTIOC0A#, GTIOC0B# | I/O | The GPT0.GTGRA and GPT0.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins |
| | GTIOC1A, GTIOC1B | I/O | The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins |
| | GTIOC1A#, GTIOC1B# | I/O | The GPT1.GTGRA and GPT1.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins |
| | GTIOC2A, GTIOC2B | I/O | The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins |
| | GTIOC2A#, GTIOC2B# | I/O | The GPT2.GTGRA and GPT2.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins |
| | GTIOC3A, GTIOC3B | I/O | The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins |
| | GTIOC3A#, GTIOC3B# | I/O | The GPT3.GTGRA and GPT3.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins |
| | GTETRG | Input | External trigger input pin for GPT0 to GPT3 |
| | GTECLKA, GTECLKB, GTECLKC, GTECLKD | Input | Input pins A to D for the external clock |
| 8-bit timer (TMR) | GTADSM0, GTADSM1 | Output | A/D conversion start request monitoring output pins |
| | TMO0 to TMO7 | Output | Compare match output pins. |
| | TMCi0 to TMCi7 | Input | Input pins for the external clock to be input to the counter. |
| Port output enable 3 (POE3b, POE3A) | TMRi0 to TMRi7 | Input | Counter reset input pins. |
| | POE0#, POE4#, POE8#, POE10#, POE11#, POE12# | Input | Input pins for request signals to switch the MTU and GPT pins between the high impedance state or operation as general I/O port pins |
| | Serial communications interface (SCiG) | • Asynchronous mode/clock synchronous mode | |
| SCK1, SCK5, SCK6 | | I/O | Input/output pins for the clock. |
| RXD1, RXD5, RXD6 | | Input | Input pins for received data. |
| TXD1, TXD5, TXD6 | | Output | Output pins for transmitted data. |
| CTS1#, CTS5#, CTS6# | | Input | Input pins for controlling the start of transmission and reception. |
| RTS1#, RTS5#, RTS6# | | Output | Output pins for controlling the start of transmission and reception. |
| • Simple I ² C mode | | | |
| SSCL1, SSCL5, SSCL6 | | I/O | Input/output pins for the I ² C clock. |
| SSDA1, SSDA5, SSDA6 | | I/O | Input/output pins for the I ² C data. |
| • Simple SPI mode | | | |
| SCK1, SCK5, SCK6 | | I/O | Input/output pins for the clock. |
| SMISO1, SMISO5, SMISO6 | | I/O | Input/output pins for slave transmit data. |
| SMOSI1, SMOSI5, SMOSI6 | | I/O | Input/output pins for master transmit data. |
| SS1#, SS5#, SS6# | Input | Chip-select input pins. | |

Table 1.4 Pin Functions (3/4)

| Classifications | Pin Name | I/O | Description |
|--|--|--------|---|
| I ² C bus interface (R1ICa) | SCL0 | I/O | Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the N-channel open drain output. |
| | SDA0 | I/O | Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output. |
| Serial peripheral interface (RSPIb) | RSPCKA | I/O | Input/output pin for the RSPI clock. |
| | MOSIA | I/O | Input/output pin for transmitting data from the RSPI master. |
| | MISOA | I/O | Input/output pin for transmitting data from the RSPI slave. |
| | SSLA0 | I/O | Input/output pin to select the slave for the RSPI. |
| | SSLA1 to SSLA3 | Output | Output pins to select the slave for the RSPI. |
| CAN module (RSCAN) | CRXD0 | Input | Input pin |
| | CTXD0 | Output | Output pin |
| 12-bit A/D converter (S12ADF) | AN000 to AN003, AN016, AN100 to AN103, AN116, AN200 to AN211 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ADST0, ADST1, ADST2 | Output | Output pins for A/D conversion status. |
| | ADTRG0#, ADTRG1#, ADTRG2# | Input | Input pins for the external trigger signals that start the A/D conversion. |
| 8-bit D/A converter (DAa) | DA0, DA1 | Output | Output pins for the analog signals to be processed by the D/A converter |
| Comparator C (CMPC) | COMP0 to COMP3 | Output | Comparator detection result output pins. |
| | CVREFC0, CVREFC1 | Input | Analog reference voltage supply pins for comparator C. |
| | CMPC00 to CMPC03 | Input | Analog input pin for CMPC0 |
| | CMPC10 to CMPC13 | Input | Analog input pin for CMPC1 |
| | CMPC20 to CMPC23 | Input | Analog input pin for CMPC2 |
| | CMPC30 to CMPC33 | Input | Analog input pin for CMPC3 |
| Analog power supply | AVCC0 | — | Analog power supply and reference power supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1, AVCC2, or VREF when 12-bit A/D converter unit 0 is not used. |
| | AVSS0 | — | Analog ground and reference ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used. |
| | AVCC1 | — | Analog power supply and reference power supply pin for 12-bit A/D converter unit 1. Connect the AVCC1 pin to AVCC0, AVCC2, or VREF when 12-bit A/D converter unit 1 is not used. |
| | AVSS1 | — | Analog ground and reference ground pin for 12-bit A/D converter unit 1. Connect the AVSS1 pin to AVSS0 or AVSS2 when 12-bit A/D converter unit 1 is not used. |
| | AVCC2 | — | Analog power supply and reference power supply pin for 12-bit A/D converter unit 2. Connect the AVCC2 pin to AVCC0, AVCC1, or VREF when 12-bit A/D converter unit 2 is not used. |
| | AVSS2 | — | Analog ground and reference ground pin for 12-bit A/D converter unit 2. Analog ground pin for comparator C and 8-bit D/A converter. Connect the AVSS2 pin to AVSS0 or AVSS1 when 12-bit A/D converter unit 2, comparator C and 8-bit D/A converter are not used. |
| | VREF | — | Analog power supply pin for comparator C and 8-bit D/A converter. For the 64-pin LFQFP package, the VREF pin is internally connected to AVCC2 and is shared. Connect the VREF pin to AVCC0, AVCC1, or AVCC2 when comparator C and 8-bit D/A converter are not used. |

Table 1.4 Pin Functions (4/4)

| Classifications | Pin Name | I/O | Description |
|-----------------|----------------------|-----|---------------------------------------|
| I/O ports | P00 to P02 | I/O | 3-bit input/output pins. |
| | P10, P11 | I/O | 2-bit input/output pins. |
| | P20 to P24 | I/O | 5-bit input/output pins. |
| | P30 to P33, P36, P37 | I/O | 6-bit input/output pins. |
| | P40 to P47 | I/O | 8-bit input/output pins. |
| | P50 to P55 | I/O | 6-bit input/output pins. |
| | P60 to P65 | I/O | 6-bit input/output pins. |
| | P70 to P76 | I/O | 7-bit input/output pins. |
| | P80 to P82 | I/O | 3-bit input/output pins. |
| | P90 to P96 | I/O | 7-bit input/output pins. |
| | PA0 to PA5 | I/O | 6-bit input/output pins. |
| | PB0 to PB7 | I/O | 8-bit input/output pins. |
| | PD0 to PD7 | I/O | 8-bit input/output pins. |
| | PE0 to PE5 | I/O | 6-bit input/output pins (PE2: input). |

Note: When the A/D converter, D/A converter, and comparator C are not used, connect the AVCC0, AVCC1, AVCC2, and VREF pins to VCC, and connect the AVSS0, AVSS1 and AVSS2 pins to VSS, respectively.

1.5 Pin Assignments

Figure 1.3 to Figure 1.6 shows the pin assignments. Table 1.5 to Table 1.8 shows the lists of pins and pin functions.

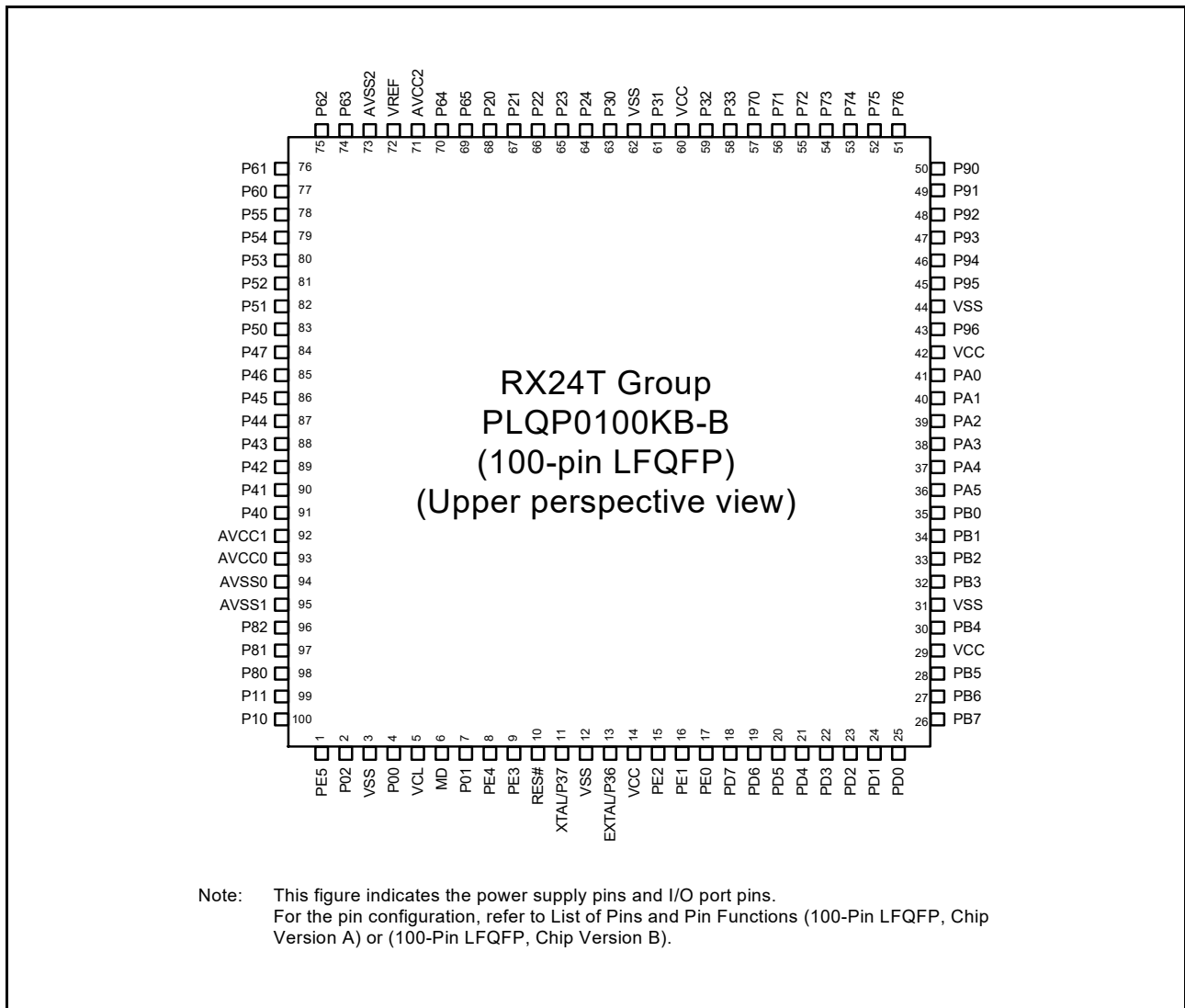


Figure 1.3 Pin Assignments of the 100-Pin LQFP (Chip Version A and B)

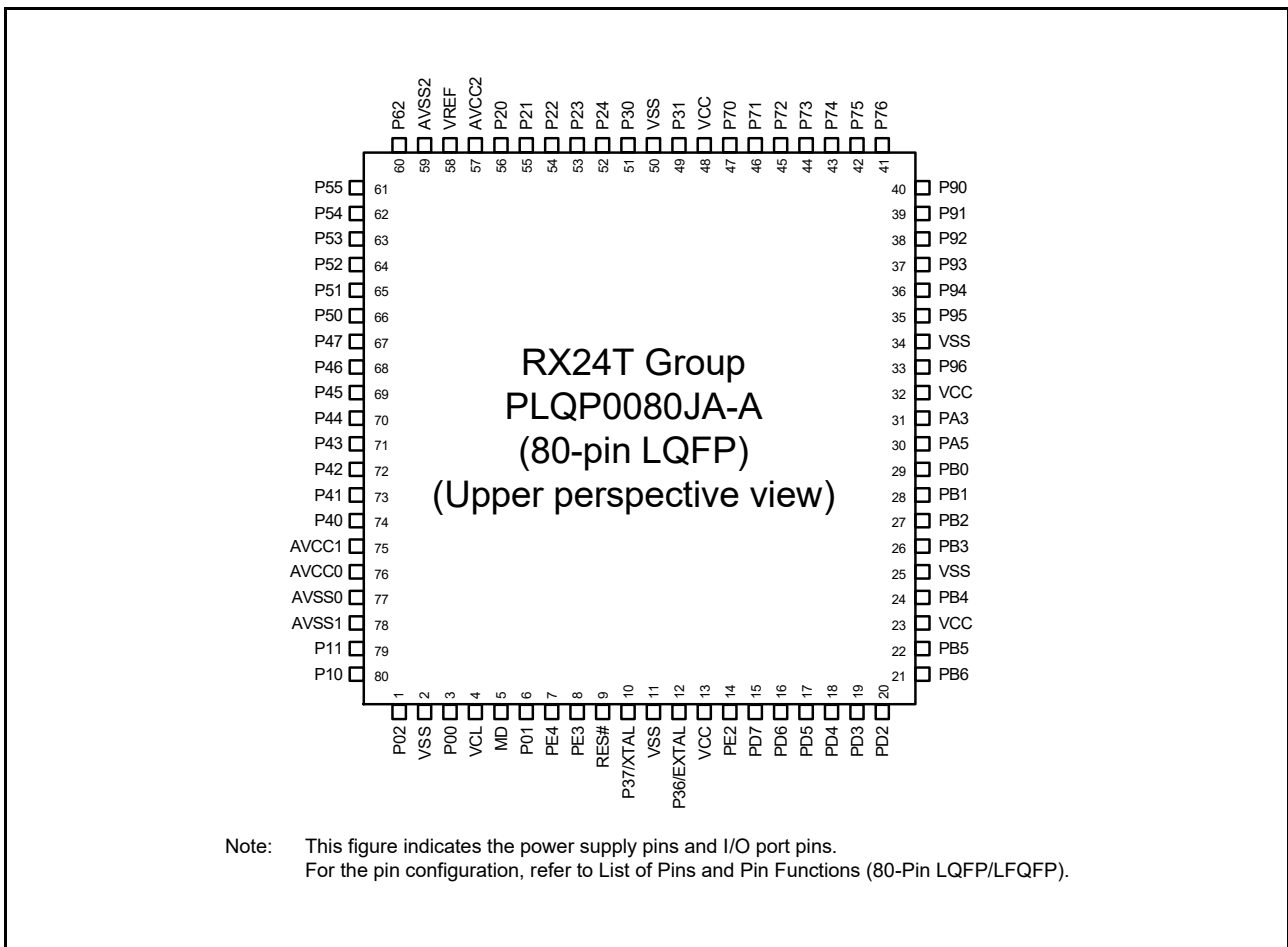


Figure 1.4 Pin Assignments of the 80-Pin LQFP

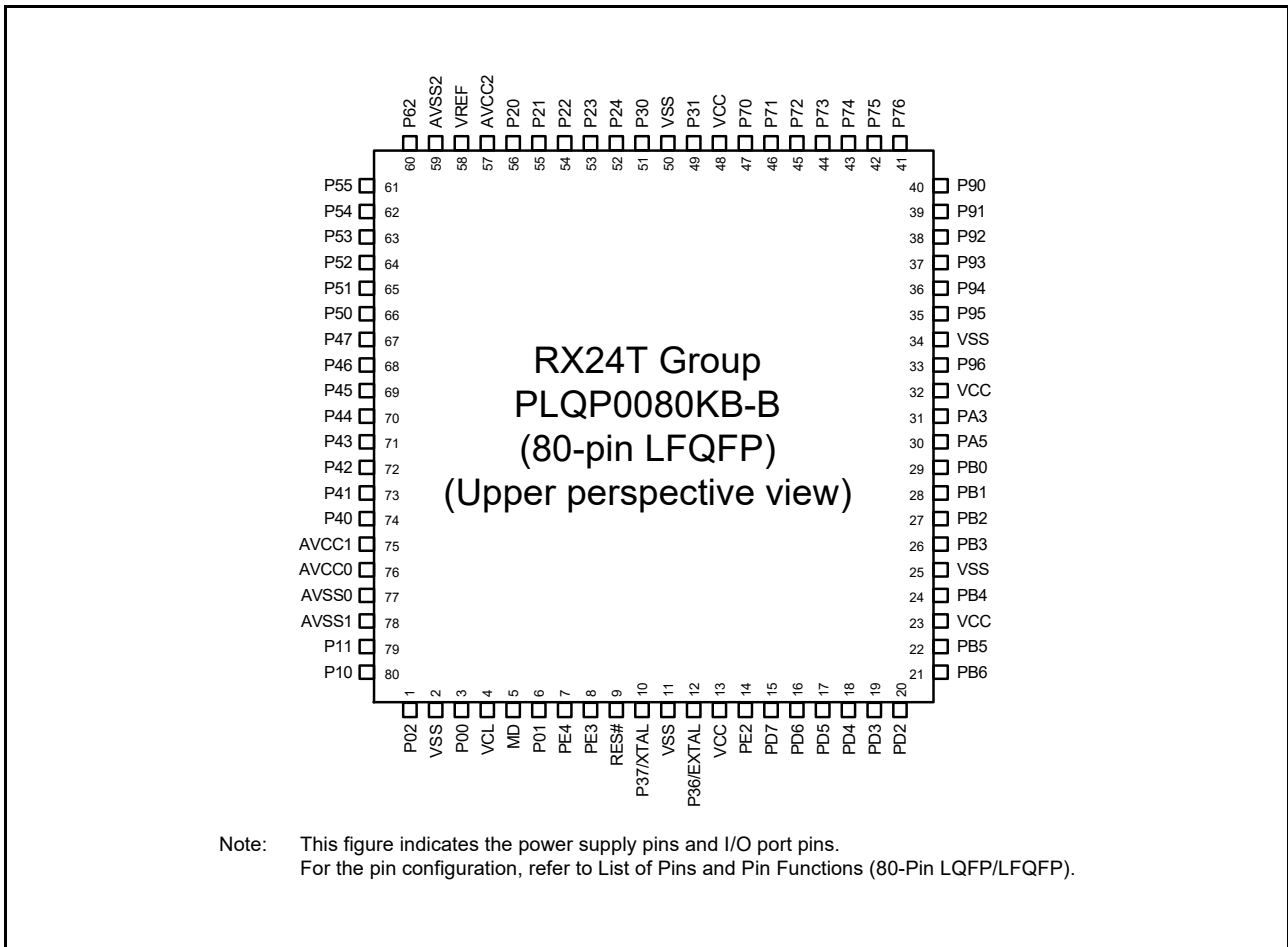


Figure 1.5 Pin Assignments of the 80-Pin LQFP

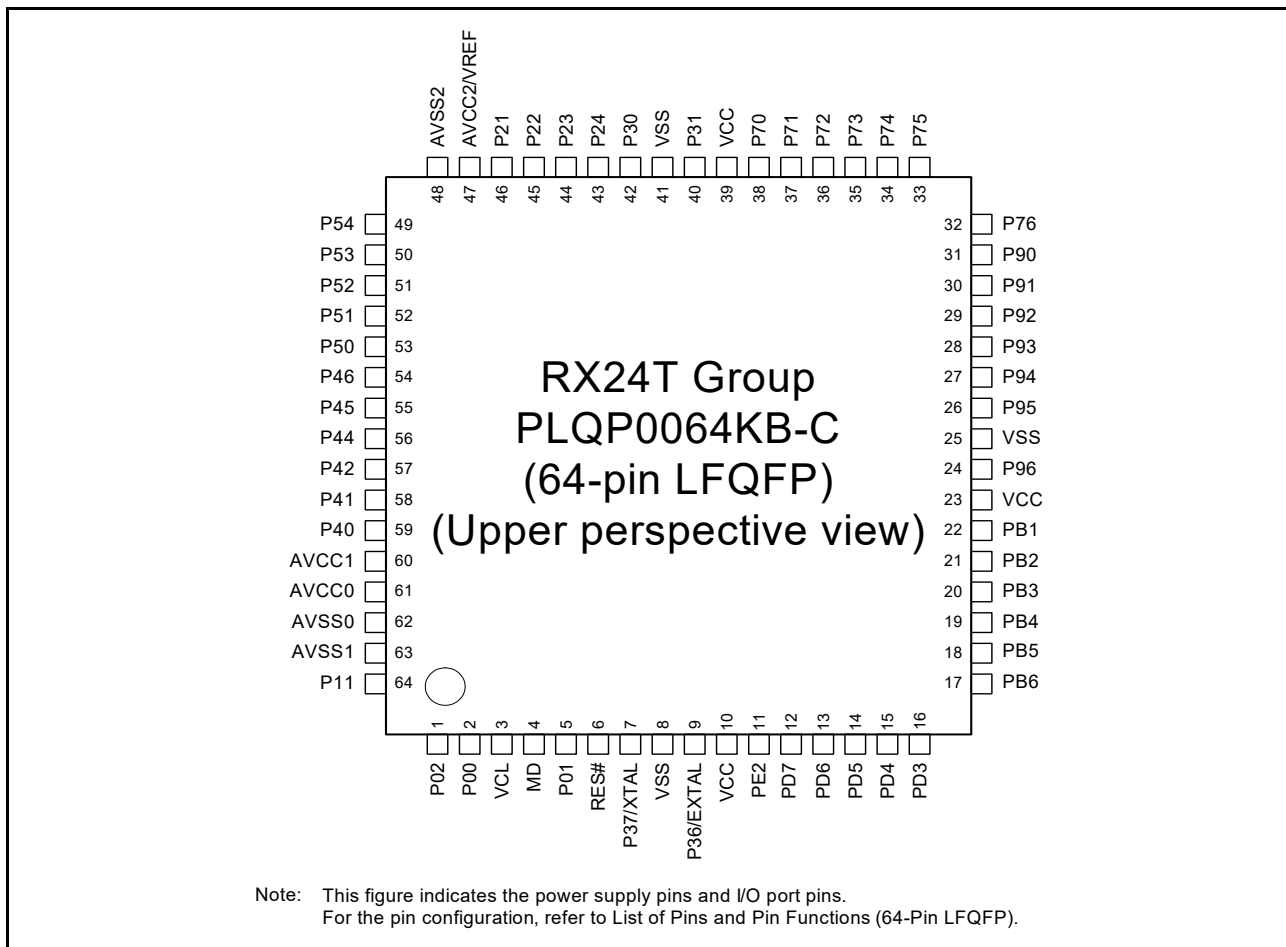


Figure 1.6 Pin Assignments of the 64-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (1/3)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (TMR, MTU, POE, CAC, GPT) | Communications (SCI, RSPI, RIIC, RSCAN) | Others |
|---------|-------------------------------------|----------|--|---|---------------|
| 1 | | PE5 | | | IRQ0 |
| 2 | | P02 | MTIOC9D, MTIOC9D# | CTS1#, RTS1#, SS1# | IRQ5, ADST0 |
| 3 | VSS | | | | |
| 4 | | P00 | | | IRQ2, ADST1 |
| 5 | VCL | | | | |
| 6 | MD | | | | FINED |
| 7 | | P01 | POE12# | | IRQ4, ADST2 |
| 8 | | PE4 | MTCLKC, MTCLKC#, POE10# | | IRQ1 |
| 9 | | PE3 | MTCLKD, MTCLKD#, POE11# | | IRQ2 |
| 10 | RES# | | | | |
| 11 | XTAL | P37 | | | |
| 12 | VSS | | | | |
| 13 | EXTAL | P36 | | | |
| 14 | VCC | | | | |
| 15 | | PE2 | POE10# | | NMI |
| 16 | | PE1 | MTIOC9D, MTIOC9D#, TMO5 | CTS5#, RTS5#, SS5#, SSLA3 | |
| 17 | | PE0 | MTIOC9B, MTIOC9B#, TMC11, TMC15 | RXD5, SMISO5, SSCL5, SSLA2 | |
| 18 | | PD7 | MTIOC9A, MTIOC9A#, TMR11, TMR15, GTIOC3A, GTIOC3A# | TXD5, SMOSI5, SSSA5, SSLA1 | |
| 19 | | PD6 | MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B# | CTS1#, RTS1#, SS1#, SSLA0 | IRQ5, ADST0 |
| 20 | | PD5 | TMRI0, TMRI6, GTECLKA | RXD1, SMISO1, SSCL1 | IRQ3 |
| 21 | | PD4 | TMC10, TMC16, GTECLKB | SCK1 | IRQ2 |
| 22 | | PD3 | TMO0, GTECLKC | TXD1, SMOSI1, SSSA1 | |
| 23 | | PD2 | TMC11, TMO4, GTIOC0A, GTIOC0A# | SCK5, MOSIA | |
| 24 | | PD1 | TMO2, GTIOC0B, GTIOC0B# | MISOA | |
| 25 | | PD0 | TMO6, GTIOC1A, GTIOC1A# | RSPCKA | |
| 26 | | PB7 | GTIOC1B, GTIOC1B# | SCK5 | |
| 27 | | PB6 | GTIOC2A, GTIOC2A# | RXD5, SMISO5, SSCL5 | IRQ5 |
| 28 | | PB5 | GTIOC2B, GTIOC2B# | TXD5, SMOSI5, SSSA5 | |
| 29 | VCC | | | | |
| 30 | | PB4 | POE8#, GTETRG, GTECLKD | CTS5#, RTS5#, SS5# | IRQ3 |
| 31 | VSS | | | | |
| 32 | | PB3 | MTIOC0A, MTIOC0A#, CACREF | SCK6, RSPCKA | |
| 33 | | PB2 | MTIOC0B, MTIOC0B#, TMR10, ADMS0 | TXD6, SMOSI6, SSSA6, SDA0 | |
| 34 | | PB1 | MTIOC0C, MTIOC0C#, TMC10, ADMS1 | RXD6, SMISO6, SSCL6, SCL0 | |
| 35 | | PB0 | MTIOC0D, MTIOC0D#, TMO0 | TXD6, SMOSI6, SSSA6, MOSIA | ADTRG2# |
| 36 | | PA5 | MTIOC1A, MTIOC1A#, TMC13 | RXD6, SMISO6, SSCL6, MISOA | IRQ1, ADTRG1# |
| 37 | | PA4 | MTIOC1B, MTIOC1B#, TMC17 | SCK6, RSPCKA | ADTRG0# |
| 38 | | PA3 | MTIOC2A, MTIOC2A#, TMR17, GTADSM0 | SSLA0 | |
| 39 | | PA2 | MTIOC2B, MTIOC2B#, TMO7, GTADSM1 | CTS6#, RTS6#, SS6#, SSLA1 | |
| 40 | | PA1 | MTIOC6A, MTIOC6A#, TMO4 | SSLA2, CRXD0 | ADTRG0# |
| 41 | | PA0 | MTIOC6C, MTIOC6C#, TMO2 | SSLA3, CTXD0 | |
| 42 | VCC | | | | |
| 43 | | P96 | POE4# | | IRQ4 |
| 44 | VSS | | | | |
| 45 | | P95 | MTIOC6B, MTIOC6B# | | |
| 46 | | P94 | MTIOC7A, MTIOC7A# | | |
| 47 | | P93 | MTIOC7B, MTIOC7B# | | |
| 48 | | P92 | MTIOC6D, MTIOC6D# | | |
| 49 | | P91 | MTIOC7C, MTIOC7C# | | |
| 50 | | P90 | MTIOC7D, MTIOC7D# | | |
| 51 | | P76 | MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B# | | |

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (2/3)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (TMR, MTU, POE, CAC, GPT) | Communications (SCI, RSPI, RIIC, RSCAN) | Others |
|---------|-------------------------------------|----------|---|---|---------------------------------------|
| 52 | | P75 | MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B# | | |
| 53 | | P74 | MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B# | | |
| 54 | | P73 | MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A# | | |
| 55 | | P72 | MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A# | | |
| 56 | | P71 | MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A# | | |
| 57 | | P70 | POE0# | | IRQ5 |
| 58 | | P33 | MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0 | SSLA3 | |
| 59 | | P32 | MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6 | SSLA2 | |
| 60 | VCC | | | | |
| 61 | | P31 | MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6 | SSLA1 | IRQ6 |
| 62 | VSS | | | | |
| 63 | | P30 | MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCi6 | SSLA0 | IRQ7, COMP3 |
| 64 | | P24 | MTIC5U, MTIC5U#, TMCi2, TMO6 | RSPCKA | COMP0, DA0 |
| 65 | | P23 | MTIC5V, MTIC5V#, TMO2, CACREF | MOSIA | COMP1, DA1 |
| 66 | | P22 | MTIC5W, MTIC5W#, TMRI2, TMO4 | MISOA | ADTRG2#, COMP2 |
| 67 | | P21 | MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCi4 | | IRQ6, ADTRG1#, AN116 |
| 68 | | P20 | MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4 | | IRQ7, ADTRG0#, AN016 |
| 69 | | P65 | | | AN205 |
| 70 | | P64 | | | AN204 |
| 71 | AVCC2 | | | | |
| 72 | VREF | | | | |
| 73 | AVSS2 | | | | |
| 74 | | P63 | | | AN203, IRQ7 |
| 75 | | P62 | | | AN202, IRQ6 |
| 76 | | P61 | | | AN201, IRQ5 |
| 77 | | P60 | | | AN200, IRQ4 |
| 78 | | P55 | | | AN211, IRQ3 |
| 79 | | P54 | | | AN210, IRQ2 |
| 80 | | P53 | | | AN209, IRQ1 |
| 81 | | P52 | | | AN208, IRQ0 |
| 82 | | P51 | | | AN207 |
| 83 | | P50 | | | AN206 |
| 84 | | P47 | | | AN103 |
| 85 | | P46 | | | AN102, CMPC12, CMPC13, CMPC30, CMPC31 |
| 86 | | P45 | | | AN101, CMPC02, CMPC03, CMPC20, CMPC21 |
| 87 | | P44 | | | AN100, CMPC10, CMPC11, CMPC32, CMPC33 |
| 88 | | P43 | | | AN003 |
| 89 | | P42 | | | AN002 |
| 90 | | P41 | | | AN001 |
| 91 | | P40 | | | AN000, CMPC00, CMPC01, CMPC22, CMPC23 |
| 92 | AVCC1 | | | | |
| 93 | AVCC0 | | | | |

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (3/3)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (TMR, MTU, POE, CAC, GPT) | Communications (SCI, RSPI, RIIC, RSCAN) | Others |
|---------|-------------------------------------|----------|---|---|--------|
| 94 | AVSS0 | | | | |
| 95 | AVSS1 | | | | |
| 96 | | P82 | MTIC5U, MTIC5U#, TMO4 | SCK6 | |
| 97 | | P81 | MTIC5V, MTIC5V#, TMC14 | TXD6, SMOS16, SSDA6 | |
| 98 | | P80 | MTIC5W, MTIC5W#, TMRI4 | RXD6, SMISO6, SSCL6 | |
| 99 | | P11 | MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3 | | IRQ1 |
| 100 | | P10 | MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12# | CTS6#, RTS6#, SS6# | IRQ0 |

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (1/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCI, RSPI, RIIC) | Others |
|---------|-------------------------------------|----------|-----------------------------|----------------------------------|---------------|
| 1 | | PE5 | | | IRQ0 |
| 2 | | P02 | MTIOC9D | CTS1#, RTS1#, SS1# | IRQ5, ADST0 |
| 3 | VSS | | | | |
| 4 | | P00 | | | IRQ2, ADST1 |
| 5 | VCL | | | | |
| 6 | MD | | | | FINED |
| 7 | | P01 | POE12# | | IRQ4, ADST2 |
| 8 | | PE4 | MTCLKC, POE10# | | IRQ1 |
| 9 | | PE3 | MTCLKD, POE11# | | IRQ2 |
| 10 | RES# | | | | |
| 11 | XTAL | P37 | | | |
| 12 | VSS | | | | |
| 13 | EXTAL | P36 | | | |
| 14 | VCC | | | | |
| 15 | | PE2 | POE10# | | NMI |
| 16 | | PE1 | MTIOC9D, TMO5 | CTS5#, RTS5#, SS5#, SSLA3 | |
| 17 | | PE0 | MTIOC9B, TMC11, TMC15 | SSLA2 | |
| 18 | | PD7 | MTIOC9A, TMR11, TMR15 | SSLA1 | |
| 19 | | PD6 | MTIOC9C, TMO1 | CTS1#, RTS1#, SS1#, SSLA0 | IRQ5, ADST0 |
| 20 | | PD5 | TMR10, TMR16 | RXD1, SMISO1, SSCL1 | IRQ3 |
| 21 | | PD4 | TMC10, TMC16 | SCK1 | IRQ2 |
| 22 | | PD3 | TMO0 | TXD1, SMOSI1, SSSA1 | |
| 23 | | PD2 | TMC11, TMO4 | SCK5, MOSIA | |
| 24 | | PD1 | TMO2 | MISOA | |
| 25 | | PD0 | TMO6 | RSPCKA | |
| 26 | | PB7 | | SCK5 | |
| 27 | | PB6 | | RXD5, SMISO5, SSCL5 | IRQ5 |
| 28 | | PB5 | | TXD5, SMOSI5, SSSA5 | |
| 29 | VCC | | | | |
| 30 | | PB4 | POE8# | CTS5#, RTS5#, SS5# | IRQ3 |
| 31 | VSS | | | | |
| 32 | | PB3 | MTIOC0A, CACREF | SCK6, RSPCKA | |
| 33 | | PB2 | MTIOC0B, TMR10, AD5M0 | TXD6, SMOSI6, SSSA6, SDA0 | |
| 34 | | PB1 | MTIOC0C, TMC10, AD5M1 | RXD6, SMISO6, SSCL6, SCL0 | |
| 35 | | PB0 | MTIOC0D, TMO0 | TXD6, SMOSI6, SSSA6, MOSIA | ADTRG2# |
| 36 | | PA5 | MTIOC1A, TMC13 | RXD6, SMISO6, SSCL6, MISOA | IRQ1, ADTRG1# |
| 37 | | PA4 | MTIOC1B, TMC17 | SCK6, RSPCKA | ADTRG0# |
| 38 | | PA3 | MTIOC2A, TMR17 | SSLA0 | |
| 39 | | PA2 | MTIOC2B, TMO7 | CTS6#, RTS6#, SS6#, SSLA1 | |
| 40 | | PA1 | MTIOC6A, TMO4 | SSLA2 | ADTRG0# |
| 41 | | PA0 | MTIOC6C, TMO2 | SSLA3 | |
| 42 | VCC | | | | |
| 43 | | P96 | POE4# | | IRQ4 |
| 44 | VSS | | | | |
| 45 | | P95 | MTIOC6B | | |
| 46 | | P94 | MTIOC7A | | |
| 47 | | P93 | MTIOC7B | | |
| 48 | | P92 | MTIOC6D | | |
| 49 | | P91 | MTIOC7C | | |
| 50 | | P90 | MTIOC7D | | |
| 51 | | P76 | MTIOC4D | | |
| 52 | | P75 | MTIOC4C | | |
| 53 | | P74 | MTIOC3D | | |
| 54 | | P73 | MTIOC4B | | |

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (2/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCI, RSPI, RIIC) | Others |
|---------|-------------------------------------|----------|--------------------------------|----------------------------------|---------------------------------------|
| 55 | | P72 | MTIOC4A | | |
| 56 | | P71 | MTIOC3B | | |
| 57 | | P70 | POE0# | | IRQ5 |
| 58 | | P33 | MTIOC3A, MTCLKA, TMO0 | SSLA3 | |
| 59 | | P32 | MTIOC3C, MTCLKB, TMO6 | SSLA2 | |
| 60 | VCC | | | | |
| 61 | | P31 | MTIOC0A, MTCLKC, TMRI6 | SSLA1 | IRQ6 |
| 62 | VSS | | | | |
| 63 | | P30 | MTIOC0B, MTCLKD, TMC16 | SSLA0 | IRQ7, COMP3 |
| 64 | | P24 | MTIC5U, TMC12, TMO6 | RSPCKA | COMP0 |
| 65 | | P23 | MTIC5V, TMO2, CACREF | MOSIA | COMP1 |
| 66 | | P22 | MTIC5W, TMRI2, TMO4 | MISOA | ADTRG2#, COMP2 |
| 67 | | P21 | MTCLKA, MTIOC9A, TMC14 | | IRQ6, ADTRG1#, AN116, CVREFC1 |
| 68 | | P20 | MTCLKB, MTIOC9C, TMRI4 | | IRQ7, ADTRG0#, AN016, CVREFC0 |
| 69 | | P65 | | | AN205 |
| 70 | | P64 | | | AN204 |
| 71 | AVCC2 | | | | |
| 72 | VREF | | | | |
| 73 | AVSS2 | | | | |
| 74 | | P63 | | | AN203, IRQ7 |
| 75 | | P62 | | | AN202, IRQ6 |
| 76 | | P61 | | | AN201, IRQ5 |
| 77 | | P60 | | | AN200, IRQ4 |
| 78 | | P55 | | | AN211, IRQ3 |
| 79 | | P54 | | | AN210, IRQ2 |
| 80 | | P53 | | | AN209, IRQ1 |
| 81 | | P52 | | | AN208, IRQ0 |
| 82 | | P51 | | | AN207 |
| 83 | | P50 | | | AN206 |
| 84 | | P47 | | | AN103 |
| 85 | | P46 | | | AN102, CMPC12, CMPC13, CMPC30, CMPC31 |
| 86 | | P45 | | | AN101, CMPC02, CMPC03, CMPC20, CMPC21 |
| 87 | | P44 | | | AN100, CMPC10, CMPC11, CMPC32, CMPC33 |
| 88 | | P43 | | | AN003 |
| 89 | | P42 | | | AN002 |
| 90 | | P41 | | | AN001 |
| 91 | | P40 | | | AN000, CMPC00, CMPC01, CMPC22, CMPC23 |
| 92 | AVCC1 | | | | |
| 93 | AVCC0 | | | | |
| 94 | AVSS0 | | | | |
| 95 | AVSS1 | | | | |
| 96 | | P82 | MTIC5U, TMO4 | SCK6 | |
| 97 | | P81 | MTIC5V, TMC14 | TXD6, SMOSI6, SSDA6 | |
| 98 | | P80 | MTIC5W, TMRI4 | RXD6, SMISO6, SSCL6 | |
| 99 | | P11 | MTIOC3A, MTCLKC, TMO3 | | IRQ1 |
| 100 | | P10 | MTIOC9B, MTCLKD, TMRI3, POE12# | CTS6#, RTS6#, SS6# | IRQ0 |

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP/LFQFP) (1/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCI, RSPI, RIIC) | Others |
|---------|-------------------------------------|----------|-----------------------------|----------------------------------|---------------|
| 1 | | P02 | MTIOC9D | CTS1#, RTS1#, SS1# | IRQ5, ADST0 |
| 2 | VSS | | | | |
| 3 | | P00 | | | IRQ2, ADST1 |
| 4 | VCL | | | | |
| 5 | MD | | | | FINED |
| 6 | | P01 | POE12# | | IRQ4, ADST2 |
| 7 | | PE4 | MTCLKC, POE10# | | IRQ1 |
| 8 | | PE3 | MTCLKD, POE11# | | IRQ2 |
| 9 | RES# | | | | |
| 10 | XTAL | P37 | | | |
| 11 | VSS | | | | |
| 12 | EXTAL | P36 | | | |
| 13 | VCC | | | | |
| 14 | | PE2 | POE10# | | NMI |
| 15 | | PD7 | MTIOC9A, TMR1, TMR15 | SSLA1 | |
| 16 | | PD6 | MTIOC9C, TMO1 | CTS1#, RTS1#, SS1#, SSLA0 | IRQ5, ADST0 |
| 17 | | PD5 | TMRI0, TMRI6 | RXD1, SMISO1, SSCL1 | IRQ3 |
| 18 | | PD4 | TMCI0, TMCI6 | SCK1 | IRQ2 |
| 19 | | PD3 | TMO0 | TXD1, SMOS1, SDA1 | |
| 20 | | PD2 | TMCI1, TMO4 | SCK5, MOSIA | |
| 21 | | PB6 | | RXD5, SMISO5, SSCL5 | IRQ5 |
| 22 | | PB5 | | TXD5, SMOS5, SDA5 | |
| 23 | VCC | | | | |
| 24 | | PB4 | POE8# | CTS5#, RTS5#, SS5# | IRQ3 |
| 25 | VSS | | | | |
| 26 | | PB3 | MTIOC0A, CACREF | SCK6, RSPCKA | |
| 27 | | PB2 | MTIOC0B, TMRI0, ADSM0 | TXD6, SMOS6, SDA6, SDA0 | |
| 28 | | PB1 | MTIOC0C, TMCI0, ADSM1 | RXD6, SMISO6, SSCL6, SCL0 | |
| 29 | | PB0 | MTIOC0D, TMO0 | TXD6, SMOS6, SDA6, MOSIA | ADTRG2# |
| 30 | | PA5 | MTIOC1A, TMCI3 | RXD6, SMISO6, SSCL6, MISOA | IRQ1, ADTRG1# |
| 31 | | PA3 | MTIOC2A, TMRI7 | SSLA0 | |
| 32 | VCC | | | | |
| 33 | | P96 | POE4# | | IRQ4 |
| 34 | VSS | | | | |
| 35 | | P95 | MTIOC6B | | |
| 36 | | P94 | MTIOC7A | | |
| 37 | | P93 | MTIOC7B | | |
| 38 | | P92 | MTIOC6D | | |
| 39 | | P91 | MTIOC7C | | |
| 40 | | P90 | MTIOC7D | | |
| 41 | | P76 | MTIOC4D | | |
| 42 | | P75 | MTIOC4C | | |
| 43 | | P74 | MTIOC3D | | |
| 44 | | P73 | MTIOC4B | | |
| 45 | | P72 | MTIOC4A | | |
| 46 | | P71 | MTIOC3B | | |
| 47 | | P70 | POE0# | | IRQ5 |
| 48 | VCC | | | | |

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP/LFQFP) (2/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCI, RSPI, RIIC) | Others |
|---------|-------------------------------------|----------|--------------------------------|----------------------------------|---------------------------------------|
| 49 | | P31 | MTIOC0A, MTCLKC, TMRI6 | SSLA1 | IRQ6 |
| 50 | VSS | | | | |
| 51 | | P30 | MTIOC0B, MTCLKD, TMC16 | SSLA0 | IRQ7, COMP3 |
| 52 | | P24 | MTIC5U, TMC12, TMO6 | RSPCKA | COMP0 |
| 53 | | P23 | MTIC5V, TMO2, CACREF | MOSIA | COMP1 |
| 54 | | P22 | MTIC5W, TMRI2, TMO4 | MISOA | ADTRG2#, COMP2 |
| 55 | | P21 | MTCLKA, MTIOC9A, TMC14 | | IRQ6, ADTRG1#, AN116, CVREFC1 |
| 56 | | P20 | MTCLKB, MTIOC9C, TMRI4 | | IRQ7, ADTRG0#, AN016, CVREFC0 |
| 57 | AVCC2 | | | | |
| 58 | VREF | | | | |
| 59 | AVSS2 | | | | |
| 60 | | P62 | | | AN202, IRQ6 |
| 61 | | P55 | | | AN211, IRQ3 |
| 62 | | P54 | | | AN210, IRQ2 |
| 63 | | P53 | | | AN209, IRQ1 |
| 64 | | P52 | | | AN208, IRQ0 |
| 65 | | P51 | | | AN207 |
| 66 | | P50 | | | AN206 |
| 67 | | P47 | | | AN103 |
| 68 | | P46 | | | AN102, CMPC12, CMPC13, CMPC30, CMPC31 |
| 69 | | P45 | | | AN101, CMPC02, CMPC03, CMPC20, CMPC21 |
| 70 | | P44 | | | AN100, CMPC10, CMPC11, CMPC32, CMPC33 |
| 71 | | P43 | | | AN003 |
| 72 | | P42 | | | AN002 |
| 73 | | P41 | | | AN001 |
| 74 | | P40 | | | AN000, CMPC00, CMPC01, CMPC22, CMPC23 |
| 75 | AVCC1 | | | | |
| 76 | AVCC0 | | | | |
| 77 | AVSS0 | | | | |
| 78 | AVSS1 | | | | |
| 79 | | P11 | MTIOC3A, MTCLKC, TMO3 | | IRQ1 |
| 80 | | P10 | MTIOC9B, MTCLKD, TMRI3, POE12# | CTS6#, RTS6#, SS6# | IRQ0 |

Table 1.8 List of Pins and Pin Functions (64-Pin LFQFP) (1/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCI, RSPI, RIIC) | Others |
|---------|-------------------------------------|----------|-----------------------------|----------------------------------|-------------------------------|
| 1 | | P02 | MTIOC9D | CTS1#, RTS1#, SS1# | IRQ5, ADST0 |
| 2 | | P00 | | | IRQ2, ADST1 |
| 3 | VCL | | | | |
| 4 | MD | | | | FINED |
| 5 | | P01 | POE12# | | IRQ4, ADST2 |
| 6 | RES# | | | | |
| 7 | XTAL | P37 | | | |
| 8 | VSS | | | | |
| 9 | EXTAL | P36 | | | |
| 10 | VCC | | | | |
| 11 | | PE2 | POE10# | | NMI |
| 12 | | PD7 | MTIOC9A, TMR11, TMR15 | SSLA1 | |
| 13 | | PD6 | MTIOC9C, TMO1 | CTS1#, RTS1#, SS1# | |
| 14 | | PD5 | TMR10, TMR16 | RXD1, SMISO1, SSCL1 | |
| 15 | | PD4 | TMC10, TMC16 | SCK1 | IRQ2 |
| 16 | | PD3 | TMO0 | TXD1, SMOS1, SSSA1 | |
| 17 | | PB6 | | RXD5, SMISO5, SSCL5 | IRQ5 |
| 18 | | PB5 | | TXD5, SMOS5, SSSA5 | |
| 19 | | PB4 | POE8# | CTS5#, RTS5#, SS5# | IRQ3 |
| 20 | | PB3 | MTIOC0A, CACREF | SCK6, RSPCKA | |
| 21 | | PB2 | MTIOC0B, TMR10, ADMS0 | TXD6, SMOS6, SSSA6, SDA0 | |
| 22 | | PB1 | MTIOC0C, TMC10, ADMS1 | RXD6, SMISO6, SSCL6, SCL0 | |
| 23 | VCC | | | | |
| 24 | | P96 | POE4# | | IRQ4 |
| 25 | VSS | | | | |
| 26 | | P95 | MTIOC6B | | |
| 27 | | P94 | MTIOC7A | | |
| 28 | | P93 | MTIOC7B | | |
| 29 | | P92 | MTIOC6D | | |
| 30 | | P91 | MTIOC7C | | |
| 31 | | P90 | MTIOC7D | | |
| 32 | | P76 | MTIOC4D | | |
| 33 | | P75 | MTIOC4C | | |
| 34 | | P74 | MTIOC3D | | |
| 35 | | P73 | MTIOC4B | | |
| 36 | | P72 | MTIOC4A | | |
| 37 | | P71 | MTIOC3B | | |
| 38 | | P70 | POE0# | | IRQ5 |
| 39 | VCC | | | | |
| 40 | | P31 | MTIOC0A, MTCLKC, TMR16 | SSLA1 | IRQ6 |
| 41 | VSS | | | | |
| 42 | | P30 | MTIOC0B, MTCLKD, TMC16 | SSLA0 | IRQ7, COMP3 |
| 43 | | P24 | MTIC5U, TMC12, TMO6 | RSPCKA | COMP0 |
| 44 | | P23 | MTIC5V, TMO2, CACREF | MOSIA | COMP1 |
| 45 | | P22 | MTIC5W, TMR12, TMO4 | MISOA | ADTRG2#, COMP2 |
| 46 | | P21 | MTCLKA, MTIOC9A, TMC14 | | IRQ6, ADTRG1#, AN116, CVREFC1 |
| 47 | AVCC2/REF | | | | |
| 48 | AVSS2 | | | | |
| 49 | | P54 | | | AN210, IRQ2 |
| 50 | | P53 | | | AN209, IRQ1 |
| 51 | | P52 | | | AN208, IRQ0 |
| 52 | | P51 | | | AN207 |
| 53 | | P50 | | | AN206 |

Table 1.8 List of Pins and Pin Functions (64-Pin LFQFP) (2/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCI, RSPI, RIIC) | Others |
|---------|-------------------------------------|----------|-----------------------------|----------------------------------|---------------------------------------|
| 54 | | P46 | | | AN102, CMPC12, CMPC13, CMPC30, CMPC31 |
| 55 | | P45 | | | AN101, CMPC02, CMPC03, CMPC20, CMPC21 |
| 56 | | P44 | | | AN100, CMPC10, CMPC11, CMPC32, CMPC33 |
| 57 | | P42 | | | AN002 |
| 58 | | P41 | | | AN001 |
| 59 | | P40 | | | AN000, CMPC00, CMPC01, CMPC22, CMPC23 |
| 60 | AVCC1 | | | | |
| 61 | AVCC0 | | | | |
| 62 | AVSS0 | | | | |
| 63 | AVSS1 | | | | |
| 64 | | P11 | MTIOC3A, MTCLKC, TMO3 | | IRQ1 |

2. CPU

Figure 2.1 shows register set of the CPU.

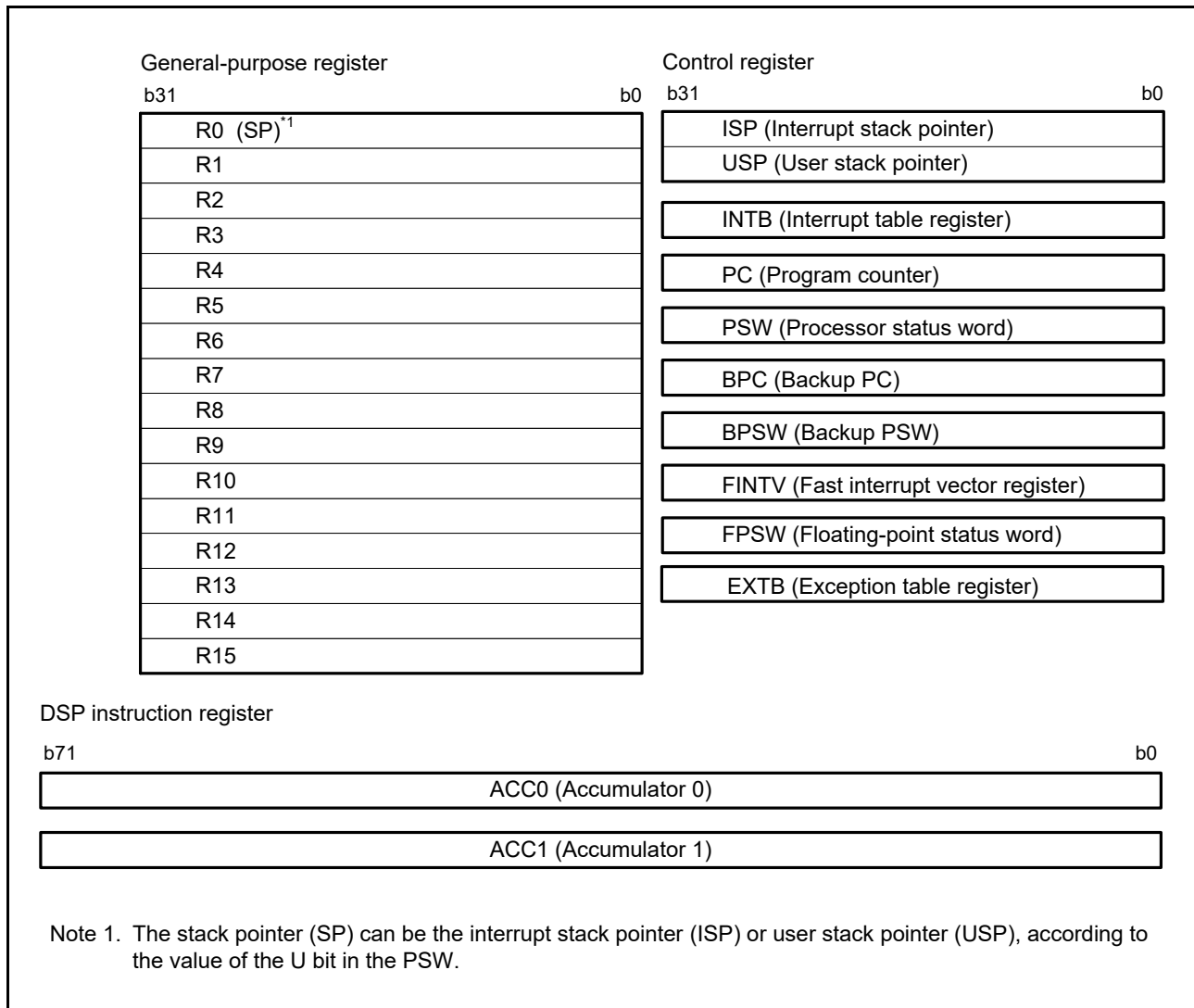


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt stack pointer (ISP) and user stack pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Exception table register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.

Set the EXTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(3) Interrupt table register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.

Set the INTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(4) Program counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor status word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast interrupt vector register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (E_j) enables the exception handling ($E_j = 1$), the exception cause can be identified by checking the corresponding C_j flag in the exception handling routine. If the exception handling is masked ($E_j = 0$), the occurrence of exception can be checked by reading the F_j flag at the end of a series of processing. Once the F_j flag has been set to 1, this value is retained until it is cleared to 0 by software ($j = X, U, Z, O, \text{ or } V$).

2.3 Accumulator

The accumulator ($ACC0$ or $ACC1$) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. $ACC0$ is also used for the multiply and multiply-and-accumulate instructions; $EMUL$, $EMULU$, $FMUL$, MUL , and $RMPA$, in which case the prior value in $ACC0$ is modified by execution of the instruction.

Use the $MVTACGU$, $MVTACHI$, and $MVTACLO$ instructions for writing to the accumulator. The $MVTACGU$, $MVTACHI$, and $MVTACLO$ instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the $MVFACGU$, $MVFACHI$, $MVFACMI$, and $MVFACLO$ instructions for reading data from the accumulator. The $MVFACGU$, $MVFACHI$, $MVFACMI$, and $MVFACLO$ instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps.

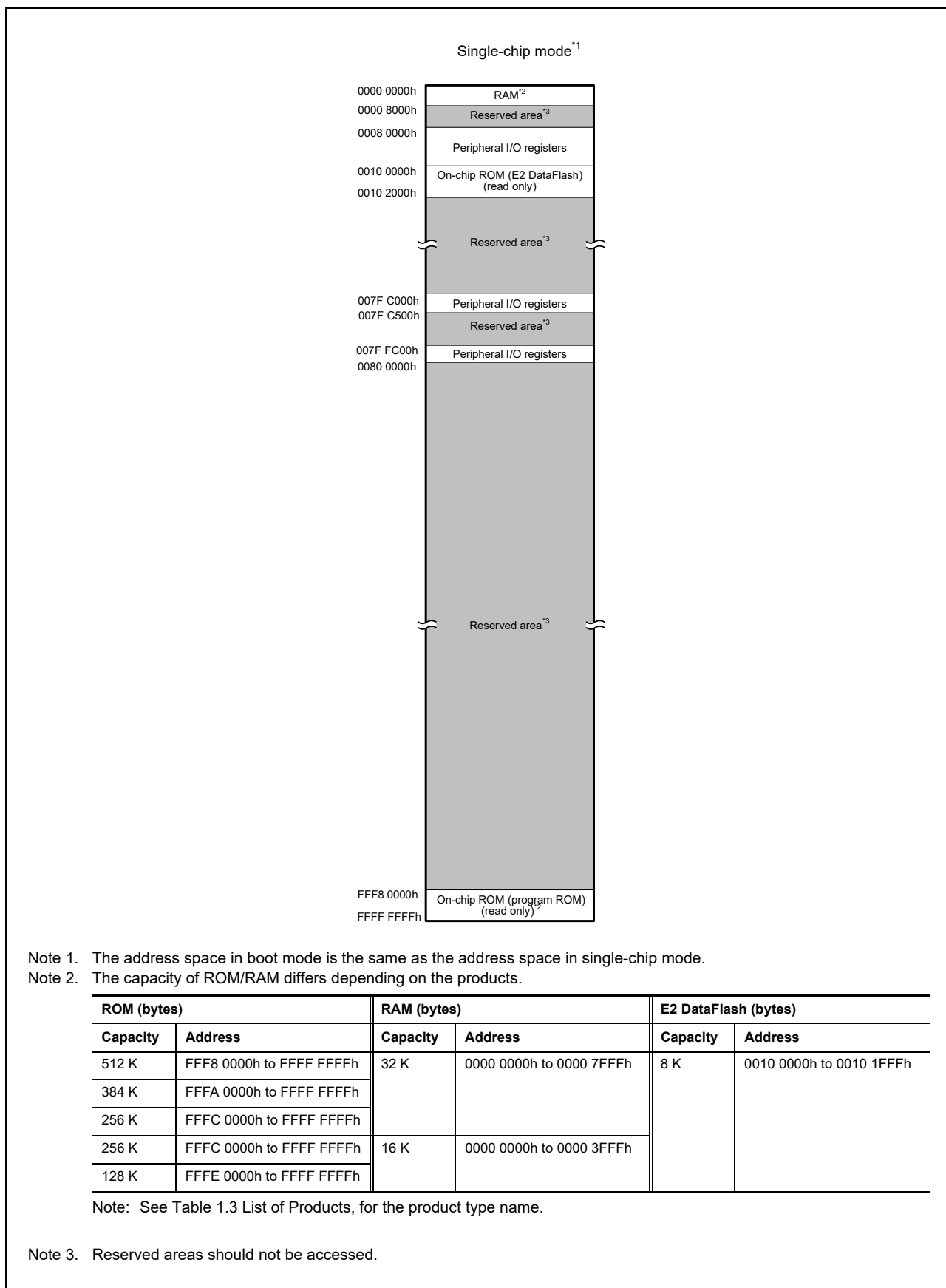


Figure 3.1 Memory Map in Each Operating Mode

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```


- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order). The number of access cycles to I/O registers is obtained by following equation.*¹

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral bus 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|--|
| | | | | | | ICLK \geq PCLK | |
| 0008 0000h | SYSTEM | Mode Monitor Register | MDMONR | 16 | 16 | 3 ICLK | |
| 0008 0008h | SYSTEM | System Control Register 1 | SYSCR1 | 16 | 16 | 3 ICLK | |
| 0008 000Ch | SYSTEM | Standby Control Register | SBYCR | 16 | 16 | 3 ICLK | |
| 0008 0010h | SYSTEM | Module Stop Control Register A | MSTPCRA | 32 | 32 | 3 ICLK | |
| 0008 0014h | SYSTEM | Module Stop Control Register B | MSTPCRB | 32 | 32 | 3 ICLK | |
| 0008 0018h | SYSTEM | Module Stop Control Register C | MSTPCRC | 32 | 32 | 3 ICLK | |
| 0008 0020h | SYSTEM | System Clock Control Register | SCKCR | 32 | 32 | 3 ICLK | |
| 0008 0026h | SYSTEM | System Clock Control Register 3 | SCKCR3 | 16 | 16 | 3 ICLK | |
| 0008 0028h | SYSTEM | PLL Control Register | PLLCR | 16 | 16 | 3 ICLK | |
| 0008 002Ah | SYSTEM | PLL Control Register 2 | PLLCR2 | 8 | 8 | 3 ICLK | |
| 0008 0031h | SYSTEM | Memory Wait Cycle Setting Register | MEMWAIT | 8 | 8 | 3 ICLK | |
| 0008 0032h | SYSTEM | Main Clock Oscillator Control Register | MOSCCR | 8 | 8 | 3 ICLK | |
| 0008 0034h | SYSTEM | Low-Speed On-Chip Oscillator Control Register | LOCOCR | 8 | 8 | 3 ICLK | |
| 0008 0035h | SYSTEM | IWDT-Dedicated On-Chip Oscillator Control Register | ILOCOCR | 8 | 8 | 3 ICLK | |
| 0008 0036h | SYSTEM | High-Speed On-Chip Oscillator Control Register | HOCOCR | 8 | 8 | 3 ICLK | |
| 0008 0037h | SYSTEM | High-Speed On-Chip Oscillator Control Register 2 | HOCOCR2 | 8 | 8 | 3 ICLK | |
| 0008 003Ch | SYSTEM | Oscillation Stabilization Flag Register | OSCOVFSR | 8 | 8 | 3 ICLK | |
| 0008 0040h | SYSTEM | Oscillation Stop Detection Control Register | OSTDCR | 8 | 8 | 3 ICLK | |
| 0008 0041h | SYSTEM | Oscillation Stop Detection Status Register | OSTDSR | 8 | 8 | 3 ICLK | |
| 0008 00A0h | SYSTEM | Operating Power Control Register | OPCCR | 8 | 8 | 3 ICLK | |
| 0008 00A2h | SYSTEM | Main Clock Oscillator Wait Control Register | MOSCWTCR | 8 | 8 | 3 ICLK | |
| 0008 00A5h | SYSTEM | High-Speed On-Chip Oscillator Wait Control Register | HOCOWTCR | 8 | 8 | 3 ICLK | |
| 0008 00C0h | SYSTEM | Reset Status Register 2 | RSTSR2 | 8 | 8 | 3 ICLK | |
| 0008 00C2h | SYSTEM | Software Reset Register | SWRR | 16 | 16 | 3 ICLK | |
| 0008 00E0h | SYSTEM | Voltage Monitoring 1 Circuit Control Register 1 | LVD1CR1 | 8 | 8 | 3 ICLK | |
| 0008 00E1h | SYSTEM | Voltage Monitoring 1 Circuit Status Register | LVD1SR | 8 | 8 | 3 ICLK | |
| 0008 00E2h | SYSTEM | Voltage Monitoring 2 Circuit Control Register 1 | LVD2CR1 | 8 | 8 | 3 ICLK | |
| 0008 00E3h | SYSTEM | Voltage Monitoring 2 Circuit Status Register | LVD2SR | 8 | 8 | 3 ICLK | |
| 0008 03FEh | SYSTEM | Protect Register | PRCR | 16 | 16 | 3 ICLK | |
| 0008 1000h | FLASH | ROM Cache Enable Register | ROMCE | 16 | 16 | 3 ICLK | |
| 0008 1004h | FLASH | ROM Cache Invalidate Register | ROMCIV | 16 | 16 | 3 ICLK | |
| 0008 1300h | BSC | Bus Error Status Clear Register | BERCLR | 8 | 8 | 2 ICLK | |
| 0008 1304h | BSC | Bus Error Monitoring Enable Register | BEREN | 8 | 8 | 2 ICLK | |
| 0008 1308h | BSC | Bus Error Status Register 1 | BERSR1 | 8 | 8 | 2 ICLK | |
| 0008 130Ah | BSC | Bus Error Status Register 2 | BERSR2 | 16 | 16 | 2 ICLK | |
| 0008 1310h | BSC | Bus Priority Control Register | BUSPRI | 16 | 16 | 2 ICLK | |
| 0008 2400h | DTC | DTC Control Register | DTCCR | 8 | 8 | 2 ICLK | |
| 0008 2404h | DTC | DTC Vector Base Register | DTCVBR | 32 | 32 | 2 ICLK | |
| 0008 2408h | DTC | DTC Address Mode Register | DTCADMOD | 8 | 8 | 2 ICLK | |
| 0008 240Ch | DTC | DTC Module Start Register | DTCST | 8 | 8 | 2 ICLK | |
| 0008 240Eh | DTC | DTC Status Register | DTCSTS | 16 | 16 | 2 ICLK | |
| 0008 6400h | MPU | Region-0 Start Page Number Register | RSPAGE0 | 32 | 32 | 1 ICLK | |
| 0008 6404h | MPU | Region-0 End Page Number Register | REPAGE0 | 32 | 32 | 1 ICLK | |
| 0008 6408h | MPU | Region-1 Start Page Number Register | RSPAGE1 | 32 | 32 | 1 ICLK | |
| 0008 640Ch | MPU | Region-1 End Page Number Register | REPAGE1 | 32 | 32 | 1 ICLK | |
| 0008 6410h | MPU | Region-2 Start Page Number Register | RSPAGE2 | 32 | 32 | 1 ICLK | |
| 0008 6414h | MPU | Region-2 End Page Number Register | REPAGE2 | 32 | 32 | 1 ICLK | |
| 0008 6418h | MPU | Region-3 Start Page Number Register | RSPAGE3 | 32 | 32 | 1 ICLK | |
| 0008 641Ch | MPU | Region-3 End Page Number Register | REPAGE3 | 32 | 32 | 1 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (2/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|------|
| | | | | | | ICLK \geq PCLK | |
| 0008 6420h | MPU | Region-4 Start Page Number Register | RSPAGE4 | 32 | 32 | 1 | ICLK |
| 0008 6424h | MPU | Region-4 End Page Number Register | REPAGE4 | 32 | 32 | 1 | ICLK |
| 0008 6428h | MPU | Region-5 Start Page Number Register | RSPAGE5 | 32 | 32 | 1 | ICLK |
| 0008 642Ch | MPU | Region-5 End Page Number Register | REPAGE5 | 32 | 32 | 1 | ICLK |
| 0008 6430h | MPU | Region-6 Start Page Number Register | RSPAGE6 | 32 | 32 | 1 | ICLK |
| 0008 6434h | MPU | Region-6 End Page Number Register | REPAGE6 | 32 | 32 | 1 | ICLK |
| 0008 6438h | MPU | Region-7 Start Page Number Register | RSPAGE7 | 32 | 32 | 1 | ICLK |
| 0008 643Ch | MPU | Region-7 End Page Number Register | REPAGE7 | 32 | 32 | 1 | ICLK |
| 0008 6500h | MPU | Memory-Protection Enable Register | MPEN | 32 | 32 | 1 | ICLK |
| 0008 6504h | MPU | Background Access Control Register | MPBAC | 32 | 32 | 1 | ICLK |
| 0008 6508h | MPU | Memory-Protection Error Status-Clearing Register | MPECLR | 32 | 32 | 1 | ICLK |
| 0008 650Ch | MPU | Memory-Protection Error Status Register | MPESTS | 32 | 32 | 1 | ICLK |
| 0008 6514h | MPU | Data Memory-Protection Error Address Register | MPDEA | 32 | 32 | 1 | ICLK |
| 0008 6520h | MPU | Region Search Address Register | MPSA | 32 | 32 | 1 | ICLK |
| 0008 6524h | MPU | Region Search Operation Register | MPOPS | 16 | 16 | 1 | ICLK |
| 0008 6526h | MPU | Region Invalidation Operation Register | MPOPI | 16 | 16 | 1 | ICLK |
| 0008 6528h | MPU | Instruction-Hit Region Register | MHITI | 32 | 32 | 1 | ICLK |
| 0008 652Ch | MPU | Data-Hit Region Register | MHITD | 32 | 32 | 1 | ICLK |
| 0008 7010h | ICU | Interrupt Request Register 016 | IR016 | 8 | 8 | 2 | ICLK |
| 0008 7017h | ICU | Interrupt Request Register 023 | IR023 | 8 | 8 | 2 | ICLK |
| 0008 701Bh | ICU | Interrupt Request Register 027 | IR027 | 8 | 8 | 2 | ICLK |
| 0008 701Ch | ICU | Interrupt Request Register 028 | IR028 | 8 | 8 | 2 | ICLK |
| 0008 701Dh | ICU | Interrupt Request Register 029 | IR029 | 8 | 8 | 2 | ICLK |
| 0008 701Eh | ICU | Interrupt Request Register 030 | IR030 | 8 | 8 | 2 | ICLK |
| 0008 701Fh | ICU | Interrupt Request Register 031 | IR031 | 8 | 8 | 2 | ICLK |
| 0008 7020h | ICU | Interrupt Request Register 032 | IR032 | 8 | 8 | 2 | ICLK |
| 0008 7021h | ICU | Interrupt Request Register 033 | IR033 | 8 | 8 | 2 | ICLK |
| 0008 7022h | ICU | Interrupt Request Register 034 | IR034 | 8 | 8 | 2 | ICLK |
| 0008 7028h | ICU | Interrupt Request Register 040*2 | IR040 | 8 | 8 | 2 | ICLK |
| 0008 7029h | ICU | Interrupt Request Register 041*2 | IR041 | 8 | 8 | 2 | ICLK |
| 0008 702Ch | ICU | Interrupt Request Register 044 | IR044 | 8 | 8 | 2 | ICLK |
| 0008 702Dh | ICU | Interrupt Request Register 045 | IR045 | 8 | 8 | 2 | ICLK |
| 0008 702Eh | ICU | Interrupt Request Register 046 | IR046 | 8 | 8 | 2 | ICLK |
| 0008 702Fh | ICU | Interrupt Request Register 047 | IR047 | 8 | 8 | 2 | ICLK |
| 0008 7030h | ICU | Interrupt Request Register 048*2 | IR048 | 8 | 8 | 2 | ICLK |
| 0008 7031h | ICU | Interrupt Request Register 049*2 | IR049 | 8 | 8 | 2 | ICLK |
| 0008 7032h | ICU | Interrupt Request Register 050*2 | IR050 | 8 | 8 | 2 | ICLK |
| 0008 7033h | ICU | Interrupt Request Register 051*2 | IR051 | 8 | 8 | 2 | ICLK |
| 0008 7034h | ICU | Interrupt Request Register 052*2 | IR052 | 8 | 8 | 2 | ICLK |
| 0008 7035h | ICU | Interrupt Request Register 053*2 | IR053 | 8 | 8 | 2 | ICLK |
| 0008 7036h | ICU | Interrupt Request Register 054*2 | IR054 | 8 | 8 | 2 | ICLK |
| 0008 7037h | ICU | Interrupt Request Register 055*2 | IR055 | 8 | 8 | 2 | ICLK |
| 0008 7038h | ICU | Interrupt Request Register 056*2 | IR056 | 8 | 8 | 2 | ICLK |
| 0008 7039h | ICU | Interrupt Request Register 057 | IR057 | 8 | 8 | 2 | ICLK |
| 0008 703Bh | ICU | Interrupt Request Register 059*2 | IR059 | 8 | 8 | 2 | ICLK |
| 0008 703Ch | ICU | Interrupt Request Register 060*2 | IR060 | 8 | 8 | 2 | ICLK |
| 0008 703Dh | ICU | Interrupt Request Register 061*2 | IR061 | 8 | 8 | 2 | ICLK |
| 0008 703Eh | ICU | Interrupt Request Register 062*2 | IR062 | 8 | 8 | 2 | ICLK |
| 0008 703Fh | ICU | Interrupt Request Register 063*2 | IR063 | 8 | 8 | 2 | ICLK |
| 0008 7040h | ICU | Interrupt Request Register 064 | IR064 | 8 | 8 | 2 | ICLK |
| 0008 7041h | ICU | Interrupt Request Register 065 | IR065 | 8 | 8 | 2 | ICLK |
| 0008 7042h | ICU | Interrupt Request Register 066 | IR066 | 8 | 8 | 2 | ICLK |

Table 4.1 List of I/O Registers (Address Order) (3/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK \geq PCLK |
| 0008 7043h | ICU | Interrupt Request Register 067 | IR067 | 8 | 8 | 2 ICLK |
| 0008 7044h | ICU | Interrupt Request Register 068 | IR068 | 8 | 8 | 2 ICLK |
| 0008 7045h | ICU | Interrupt Request Register 069 | IR069 | 8 | 8 | 2 ICLK |
| 0008 7046h | ICU | Interrupt Request Register 070 | IR070 | 8 | 8 | 2 ICLK |
| 0008 7047h | ICU | Interrupt Request Register 071 | IR071 | 8 | 8 | 2 ICLK |
| 0008 7058h | ICU | Interrupt Request Register 088 | IR088 | 8 | 8 | 2 ICLK |
| 0008 7059h | ICU | Interrupt Request Register 089 | IR089 | 8 | 8 | 2 ICLK |
| 0008 7062h | ICU | Interrupt Request Register 098*2 | IR098 | 8 | 8 | 2 ICLK |
| 0008 7063h | ICU | Interrupt Request Register 099*2 | IR099 | 8 | 8 | 2 ICLK |
| 0008 7064h | ICU | Interrupt Request Register 100*2 | IR100 | 8 | 8 | 2 ICLK |
| 0008 7065h | ICU | Interrupt Request Register 101*2 | IR101 | 8 | 8 | 2 ICLK |
| 0008 7066h | ICU | Interrupt Request Register 102 | IR102 | 8 | 8 | 2 ICLK |
| 0008 7067h | ICU | Interrupt Request Register 103 | IR103 | 8 | 8 | 2 ICLK |
| 0008 7068h | ICU | Interrupt Request Register 104 | IR104 | 8 | 8 | 2 ICLK |
| 0008 7069h | ICU | Interrupt Request Register 105 | IR105 | 8 | 8 | 2 ICLK |
| 0008 706Ah | ICU | Interrupt Request Register 106 | IR106 | 8 | 8 | 2 ICLK |
| 0008 706Bh | ICU | Interrupt Request Register 107 | IR107 | 8 | 8 | 2 ICLK |
| 0008 706Ch | ICU | Interrupt Request Register 108 | IR108 | 8 | 8 | 2 ICLK |
| 0008 706Dh | ICU | Interrupt Request Register 109 | IR109 | 8 | 8 | 2 ICLK |
| 0008 706Eh | ICU | Interrupt Request Register 110 | IR110 | 8 | 8 | 2 ICLK |
| 0008 706Fh | ICU | Interrupt Request Register 111 | IR111 | 8 | 8 | 2 ICLK |
| 0008 7070h | ICU | Interrupt Request Register 112 | IR112 | 8 | 8 | 2 ICLK |
| 0008 7071h | ICU | Interrupt Request Register 113 | IR113 | 8 | 8 | 2 ICLK |
| 0008 7072h | ICU | Interrupt Request Register 114 | IR114 | 8 | 8 | 2 ICLK |
| 0008 7073h | ICU | Interrupt Request Register 115 | IR115 | 8 | 8 | 2 ICLK |
| 0008 7074h | ICU | Interrupt Request Register 116 | IR116 | 8 | 8 | 2 ICLK |
| 0008 7075h | ICU | Interrupt Request Register 117 | IR117 | 8 | 8 | 2 ICLK |
| 0008 7076h | ICU | Interrupt Request Register 118 | IR118 | 8 | 8 | 2 ICLK |
| 0008 7077h | ICU | Interrupt Request Register 119 | IR119 | 8 | 8 | 2 ICLK |
| 0008 7078h | ICU | Interrupt Request Register 120 | IR120 | 8 | 8 | 2 ICLK |
| 0008 7079h | ICU | Interrupt Request Register 121 | IR121 | 8 | 8 | 2 ICLK |
| 0008 707Ah | ICU | Interrupt Request Register 122 | IR122 | 8 | 8 | 2 ICLK |
| 0008 707Bh | ICU | Interrupt Request Register 123 | IR123 | 8 | 8 | 2 ICLK |
| 0008 707Ch | ICU | Interrupt Request Register 124 | IR124 | 8 | 8 | 2 ICLK |
| 0008 707Dh | ICU | Interrupt Request Register 125 | IR125 | 8 | 8 | 2 ICLK |
| 0008 707Eh | ICU | Interrupt Request Register 126 | IR126 | 8 | 8 | 2 ICLK |
| 0008 707Fh | ICU | Interrupt Request Register 127 | IR127 | 8 | 8 | 2 ICLK |
| 0008 7080h | ICU | Interrupt Request Register 128 | IR128 | 8 | 8 | 2 ICLK |
| 0008 7081h | ICU | Interrupt Request Register 129 | IR129 | 8 | 8 | 2 ICLK |
| 0008 7082h | ICU | Interrupt Request Register 130 | IR130 | 8 | 8 | 2 ICLK |
| 0008 7083h | ICU | Interrupt Request Register 131 | IR131 | 8 | 8 | 2 ICLK |
| 0008 7084h | ICU | Interrupt Request Register 132 | IR132 | 8 | 8 | 2 ICLK |
| 0008 7085h | ICU | Interrupt Request Register 133 | IR133 | 8 | 8 | 2 ICLK |
| 0008 7086h | ICU | Interrupt Request Register 134 | IR134 | 8 | 8 | 2 ICLK |
| 0008 7087h | ICU | Interrupt Request Register 135 | IR135 | 8 | 8 | 2 ICLK |
| 0008 7088h | ICU | Interrupt Request Register 136 | IR136 | 8 | 8 | 2 ICLK |
| 0008 7089h | ICU | Interrupt Request Register 137 | IR137 | 8 | 8 | 2 ICLK |
| 0008 708Ah | ICU | Interrupt Request Register 138 | IR138 | 8 | 8 | 2 ICLK |
| 0008 708Bh | ICU | Interrupt Request Register 139 | IR139 | 8 | 8 | 2 ICLK |
| 0008 708Ch | ICU | Interrupt Request Register 140 | IR140 | 8 | 8 | 2 ICLK |
| 0008 708Dh | ICU | Interrupt Request Register 141 | IR141 | 8 | 8 | 2 ICLK |
| 0008 708Eh | ICU | Interrupt Request Register 142 | IR142 | 8 | 8 | 2 ICLK |

Table 4.1 List of I/O Registers (Address Order) (4/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|------|
| | | | | | | ICLK \geq PCLK | |
| 0008 708Fh | ICU | Interrupt Request Register 143 | IR143 | 8 | 8 | 2 | ICLK |
| 0008 7090h | ICU | Interrupt Request Register 144 | IR144 | 8 | 8 | 2 | ICLK |
| 0008 7091h | ICU | Interrupt Request Register 145 | IR145 | 8 | 8 | 2 | ICLK |
| 0008 7092h | ICU | Interrupt Request Register 146 | IR146 | 8 | 8 | 2 | ICLK |
| 0008 7095h | ICU | Interrupt Request Register 149 | IR149 | 8 | 8 | 2 | ICLK |
| 0008 7096h | ICU | Interrupt Request Register 150 | IR150 | 8 | 8 | 2 | ICLK |
| 0008 7097h | ICU | Interrupt Request Register 151 | IR151 | 8 | 8 | 2 | ICLK |
| 0008 7098h | ICU | Interrupt Request Register 152 | IR152 | 8 | 8 | 2 | ICLK |
| 0008 7099h | ICU | Interrupt Request Register 153 | IR153 | 8 | 8 | 2 | ICLK |
| 0008 709Fh | ICU | Interrupt Request Register 159 | IR159 | 8 | 8 | 2 | ICLK |
| 0008 70A0h | ICU | Interrupt Request Register 160 | IR160 | 8 | 8 | 2 | ICLK |
| 0008 70A1h | ICU | Interrupt Request Register 161 | IR161 | 8 | 8 | 2 | ICLK |
| 0008 70A2h | ICU | Interrupt Request Register 162 | IR162 | 8 | 8 | 2 | ICLK |
| 0008 70A3h | ICU | Interrupt Request Register 163 | IR163 | 8 | 8 | 2 | ICLK |
| 0008 70A4h | ICU | Interrupt Request Register 164 | IR164 | 8 | 8 | 2 | ICLK |
| 0008 70A5h | ICU | Interrupt Request Register 165 | IR165 | 8 | 8 | 2 | ICLK |
| 0008 70A8h | ICU | Interrupt Request Register 168 | IR168 | 8 | 8 | 2 | ICLK |
| 0008 70A9h | ICU | Interrupt Request Register 169 | IR169 | 8 | 8 | 2 | ICLK |
| 0008 70AAh | ICU | Interrupt Request Register 170 | IR170 | 8 | 8 | 2 | ICLK |
| 0008 70ABh | ICU | Interrupt Request Register 171 | IR171 | 8 | 8 | 2 | ICLK |
| 0008 70ACh | ICU | Interrupt Request Register 172 | IR172 | 8 | 8 | 2 | ICLK |
| 0008 70ADh | ICU | Interrupt Request Register 173 | IR173 | 8 | 8 | 2 | ICLK |
| 0008 70AEh | ICU | Interrupt Request Register 174 | IR174 | 8 | 8 | 2 | ICLK |
| 0008 70AFh | ICU | Interrupt Request Register 175 | IR175 | 8 | 8 | 2 | ICLK |
| 0008 70B0h | ICU | Interrupt Request Register 176 | IR176 | 8 | 8 | 2 | ICLK |
| 0008 70B1h | ICU | Interrupt Request Register 177 | IR177 | 8 | 8 | 2 | ICLK |
| 0008 70B2h | ICU | Interrupt Request Register 178 | IR178 | 8 | 8 | 2 | ICLK |
| 0008 70B3h | ICU | Interrupt Request Register 179 | IR179 | 8 | 8 | 2 | ICLK |
| 0008 70B4h | ICU | Interrupt Request Register 180 | IR180 | 8 | 8 | 2 | ICLK |
| 0008 70B5h | ICU | Interrupt Request Register 181 | IR181 | 8 | 8 | 2 | ICLK |
| 0008 70B6h | ICU | Interrupt Request Register 182 | IR182 | 8 | 8 | 2 | ICLK |
| 0008 70B7h | ICU | Interrupt Request Register 183 | IR183 | 8 | 8 | 2 | ICLK |
| 0008 70B8h | ICU | Interrupt Request Register 184 | IR184 | 8 | 8 | 2 | ICLK |
| 0008 70B9h | ICU | Interrupt Request Register 185 | IR185 | 8 | 8 | 2 | ICLK |
| 0008 70BAh | ICU | Interrupt Request Register 186 | IR186 | 8 | 8 | 2 | ICLK |
| 0008 70BBh | ICU | Interrupt Request Register 187 | IR187 | 8 | 8 | 2 | ICLK |
| 0008 70BCh | ICU | Interrupt Request Register 188 | IR188 | 8 | 8 | 2 | ICLK |
| 0008 70BDh | ICU | Interrupt Request Register 189 | IR189 | 8 | 8 | 2 | ICLK |
| 0008 70BEh | ICU | Interrupt Request Register 190 | IR190 | 8 | 8 | 2 | ICLK |
| 0008 70BFh | ICU | Interrupt Request Register 191 | IR191 | 8 | 8 | 2 | ICLK |
| 0008 70C0h | ICU | Interrupt Request Register 192 | IR192 | 8 | 8 | 2 | ICLK |
| 0008 70C1h | ICU | Interrupt Request Register 193 | IR193 | 8 | 8 | 2 | ICLK |
| 0008 70C2h | ICU | Interrupt Request Register 194 | IR194 | 8 | 8 | 2 | ICLK |
| 0008 70C3h | ICU | Interrupt Request Register 195 | IR195 | 8 | 8 | 2 | ICLK |
| 0008 70C4h | ICU | Interrupt Request Register 196 | IR196 | 8 | 8 | 2 | ICLK |
| 0008 70C5h | ICU | Interrupt Request Register 197 | IR197 | 8 | 8 | 2 | ICLK |
| 0008 70CAh | ICU | Interrupt Request Register 202*2 | IR202 | 8 | 8 | 2 | ICLK |
| 0008 70CBh | ICU | Interrupt Request Register 203*2 | IR203 | 8 | 8 | 2 | ICLK |
| 0008 70CCh | ICU | Interrupt Request Register 204*2 | IR204 | 8 | 8 | 2 | ICLK |
| 0008 70CDh | ICU | Interrupt Request Register 205*2 | IR205 | 8 | 8 | 2 | ICLK |
| 0008 70CEh | ICU | Interrupt Request Register 206*2 | IR206 | 8 | 8 | 2 | ICLK |
| 0008 70CFh | ICU | Interrupt Request Register 207*2 | IR207 | 8 | 8 | 2 | ICLK |

Table 4.1 List of I/O Registers (Address Order) (5/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|------|
| | | | | | | ICLK \geq PCLK | |
| 0008 70D0h | ICU | Interrupt Request Register 208*2 | IR208 | 8 | 8 | 2 | ICLK |
| 0008 70D1h | ICU | Interrupt Request Register 209*2 | IR209 | 8 | 8 | 2 | ICLK |
| 0008 70D2h | ICU | Interrupt Request Register 210*2 | IR210 | 8 | 8 | 2 | ICLK |
| 0008 70D3h | ICU | Interrupt Request Register 211*2 | IR211 | 8 | 8 | 2 | ICLK |
| 0008 70D4h | ICU | Interrupt Request Register 212*2 | IR212 | 8 | 8 | 2 | ICLK |
| 0008 70D5h | ICU | Interrupt Request Register 213*2 | IR213 | 8 | 8 | 2 | ICLK |
| 0008 70D6h | ICU | Interrupt Request Register 214*2 | IR214 | 8 | 8 | 2 | ICLK |
| 0008 70D7h | ICU | Interrupt Request Register 215*2 | IR215 | 8 | 8 | 2 | ICLK |
| 0008 70D8h | ICU | Interrupt Request Register 216*2 | IR216 | 8 | 8 | 2 | ICLK |
| 0008 70D9h | ICU | Interrupt Request Register 217*2 | IR217 | 8 | 8 | 2 | ICLK |
| 0008 70DAh | ICU | Interrupt Request Register 218 | IR218 | 8 | 8 | 2 | ICLK |
| 0008 70DBh | ICU | Interrupt Request Register 219 | IR219 | 8 | 8 | 2 | ICLK |
| 0008 70DCh | ICU | Interrupt Request Register 220 | IR220 | 8 | 8 | 2 | ICLK |
| 0008 70DDh | ICU | Interrupt Request Register 221 | IR221 | 8 | 8 | 2 | ICLK |
| 0008 70DEh | ICU | Interrupt Request Register 222 | IR222 | 8 | 8 | 2 | ICLK |
| 0008 70DFh | ICU | Interrupt Request Register 223 | IR223 | 8 | 8 | 2 | ICLK |
| 0008 70E0h | ICU | Interrupt Request Register 224 | IR224 | 8 | 8 | 2 | ICLK |
| 0008 70E1h | ICU | Interrupt Request Register 225 | IR225 | 8 | 8 | 2 | ICLK |
| 0008 70E2h | ICU | Interrupt Request Register 226 | IR226 | 8 | 8 | 2 | ICLK |
| 0008 70E3h | ICU | Interrupt Request Register 227 | IR227 | 8 | 8 | 2 | ICLK |
| 0008 70E4h | ICU | Interrupt Request Register 228 | IR228 | 8 | 8 | 2 | ICLK |
| 0008 70E5h | ICU | Interrupt Request Register 229 | IR229 | 8 | 8 | 2 | ICLK |
| 0008 70EEh | ICU | Interrupt Request Register 238*2 | IR238 | 8 | 8 | 2 | ICLK |
| 0008 70EFh | ICU | Interrupt Request Register 239*2 | IR239 | 8 | 8 | 2 | ICLK |
| 0008 70F0h | ICU | Interrupt Request Register 240*2 | IR240 | 8 | 8 | 2 | ICLK |
| 0008 70F1h | ICU | Interrupt Request Register 241*2 | IR241 | 8 | 8 | 2 | ICLK |
| 0008 70F2h | ICU | Interrupt Request Register 242*2 | IR242 | 8 | 8 | 2 | ICLK |
| 0008 70F3h | ICU | Interrupt Request Register 243*2 | IR243 | 8 | 8 | 2 | ICLK |
| 0008 70F4h | ICU | Interrupt Request Register 244*2 | IR244 | 8 | 8 | 2 | ICLK |
| 0008 70F6h | ICU | Interrupt Request Register 246 | IR246 | 8 | 8 | 2 | ICLK |
| 0008 70F7h | ICU | Interrupt Request Register 247 | IR247 | 8 | 8 | 2 | ICLK |
| 0008 70F8h | ICU | Interrupt Request Register 248 | IR248 | 8 | 8 | 2 | ICLK |
| 0008 70F9h | ICU | Interrupt Request Register 249 | IR249 | 8 | 8 | 2 | ICLK |
| 0008 711Bh | ICU | DTC Transfer Request Enable Register 027 | DTCER027 | 8 | 8 | 2 | ICLK |
| 0008 711Ch | ICU | DTC Transfer Request Enable Register 028 | DTCER028 | 8 | 8 | 2 | ICLK |
| 0008 711Dh | ICU | DTC Transfer Request Enable Register 029 | DTCER029 | 8 | 8 | 2 | ICLK |
| 0008 711Eh | ICU | DTC Transfer Request Enable Register 030 | DTCER030 | 8 | 8 | 2 | ICLK |
| 0008 711Fh | ICU | DTC Transfer Request Enable Register 031 | DTCER031 | 8 | 8 | 2 | ICLK |
| 0008 712Dh | ICU | DTC Transfer Request Enable Register 045 | DTCER045 | 8 | 8 | 2 | ICLK |
| 0008 712Eh | ICU | DTC Transfer Request Enable Register 046 | DTCER046 | 8 | 8 | 2 | ICLK |
| 0008 7130h | ICU | DTC Transfer Request Enable Register 048*2 | DTCER048 | 8 | 8 | 2 | ICLK |
| 0008 7131h | ICU | DTC Transfer Request Enable Register 049*2 | DTCER049 | 8 | 8 | 2 | ICLK |
| 0008 7132h | ICU | DTC Transfer Request Enable Register 050*2 | DTCER050 | 8 | 8 | 2 | ICLK |
| 0008 7133h | ICU | DTC Transfer Request Enable Register 051*2 | DTCER051 | 8 | 8 | 2 | ICLK |
| 0008 7135h | ICU | DTC Transfer Request Enable Register 053*2 | DTCER053 | 8 | 8 | 2 | ICLK |
| 0008 7136h | ICU | DTC Transfer Request Enable Register 054*2 | DTCER054 | 8 | 8 | 2 | ICLK |
| 0008 7137h | ICU | DTC Transfer Request Enable Register 055*2 | DTCER055 | 8 | 8 | 2 | ICLK |
| 0008 7138h | ICU | DTC Transfer Request Enable Register 056*2 | DTCER056 | 8 | 8 | 2 | ICLK |
| 0008 713Bh | ICU | DTC Transfer Request Enable Register 059*2 | DTCER059 | 8 | 8 | 2 | ICLK |
| 0008 7140h | ICU | DTC Transfer Request Enable Register 064 | DTCER064 | 8 | 8 | 2 | ICLK |
| 0008 7141h | ICU | DTC Transfer Request Enable Register 065 | DTCER065 | 8 | 8 | 2 | ICLK |
| 0008 7142h | ICU | DTC Transfer Request Enable Register 066 | DTCER066 | 8 | 8 | 2 | ICLK |

Table 4.1 List of I/O Registers (Address Order) (6/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|------|
| | | | | | | ICLK \geq PCLK | |
| 0008 7143h | ICU | DTC Transfer Request Enable Register 067 | DTCER067 | 8 | 8 | 2 | ICLK |
| 0008 7144h | ICU | DTC Transfer Request Enable Register 068 | DTCER068 | 8 | 8 | 2 | ICLK |
| 0008 7145h | ICU | DTC Transfer Request Enable Register 069 | DTCER069 | 8 | 8 | 2 | ICLK |
| 0008 7146h | ICU | DTC Transfer Request Enable Register 070 | DTCER070 | 8 | 8 | 2 | ICLK |
| 0008 7147h | ICU | DTC Transfer Request Enable Register 071 | DTCER071 | 8 | 8 | 2 | ICLK |
| 0008 7162h | ICU | DTC Transfer Request Enable Register 098*2 | DTCER098 | 8 | 8 | 2 | ICLK |
| 0008 7163h | ICU | DTC Transfer Request Enable Register 099*2 | DTCER099 | 8 | 8 | 2 | ICLK |
| 0008 7164h | ICU | DTC Transfer Request Enable Register 100*2 | DTCER100 | 8 | 8 | 2 | ICLK |
| 0008 7165h | ICU | DTC Transfer Request Enable Register 101*2 | DTCER101 | 8 | 8 | 2 | ICLK |
| 0008 7166h | ICU | DTC Transfer Request Enable Register 102 | DTCER102 | 8 | 8 | 2 | ICLK |
| 0008 7167h | ICU | DTC Transfer Request Enable Register 103 | DTCER103 | 8 | 8 | 2 | ICLK |
| 0008 7168h | ICU | DTC Transfer Request Enable Register 104 | DTCER104 | 8 | 8 | 2 | ICLK |
| 0008 7169h | ICU | DTC Transfer Request Enable Register 105 | DTCER105 | 8 | 8 | 2 | ICLK |
| 0008 716Ah | ICU | DTC Transfer Request Enable Register 106 | DTCER106 | 8 | 8 | 2 | ICLK |
| 0008 716Bh | ICU | DTC Transfer Request Enable Register 107 | DTCER107 | 8 | 8 | 2 | ICLK |
| 0008 716Ch | ICU | DTC Transfer Request Enable Register 108 | DTCER108 | 8 | 8 | 2 | ICLK |
| 0008 716Dh | ICU | DTC Transfer Request Enable Register 109 | DTCER109 | 8 | 8 | 2 | ICLK |
| 0008 716Eh | ICU | DTC Transfer Request Enable Register 110 | DTCER110 | 8 | 8 | 2 | ICLK |
| 0008 716Fh | ICU | DTC Transfer Request Enable Register 111 | DTCER111 | 8 | 8 | 2 | ICLK |
| 0008 7170h | ICU | DTC Transfer Request Enable Register 112 | DTCER112 | 8 | 8 | 2 | ICLK |
| 0008 7171h | ICU | DTC Transfer Request Enable Register 113 | DTCER113 | 8 | 8 | 2 | ICLK |
| 0008 7172h | ICU | DTC Transfer Request Enable Register 114 | DTCER114 | 8 | 8 | 2 | ICLK |
| 0008 7173h | ICU | DTC Transfer Request Enable Register 115 | DTCER115 | 8 | 8 | 2 | ICLK |
| 0008 7174h | ICU | DTC Transfer Request Enable Register 116 | DTCER116 | 8 | 8 | 2 | ICLK |
| 0008 7175h | ICU | DTC Transfer Request Enable Register 117 | DTCER117 | 8 | 8 | 2 | ICLK |
| 0008 7179h | ICU | DTC Transfer Request Enable Register 121 | DTCER121 | 8 | 8 | 2 | ICLK |
| 0008 717Ah | ICU | DTC Transfer Request Enable Register 122 | DTCER122 | 8 | 8 | 2 | ICLK |
| 0008 717Dh | ICU | DTC Transfer Request Enable Register 125 | DTCER125 | 8 | 8 | 2 | ICLK |
| 0008 717Eh | ICU | DTC Transfer Request Enable Register 126 | DTCER126 | 8 | 8 | 2 | ICLK |
| 0008 7181h | ICU | DTC Transfer Request Enable Register 129 | DTCER129 | 8 | 8 | 2 | ICLK |
| 0008 7182h | ICU | DTC Transfer Request Enable Register 130 | DTCER130 | 8 | 8 | 2 | ICLK |
| 0008 7183h | ICU | DTC Transfer Request Enable Register 131 | DTCER131 | 8 | 8 | 2 | ICLK |
| 0008 7184h | ICU | DTC Transfer Request Enable Register 132 | DTCER132 | 8 | 8 | 2 | ICLK |
| 0008 7186h | ICU | DTC Transfer Request Enable Register 134 | DTCER134 | 8 | 8 | 2 | ICLK |
| 0008 7187h | ICU | DTC Transfer Request Enable Register 135 | DTCER135 | 8 | 8 | 2 | ICLK |
| 0008 7188h | ICU | DTC Transfer Request Enable Register 136 | DTCER136 | 8 | 8 | 2 | ICLK |
| 0008 7189h | ICU | DTC Transfer Request Enable Register 137 | DTCER137 | 8 | 8 | 2 | ICLK |
| 0008 718Ah | ICU | DTC Transfer Request Enable Register 138 | DTCER138 | 8 | 8 | 2 | ICLK |
| 0008 718Bh | ICU | DTC Transfer Request Enable Register 139 | DTCER139 | 8 | 8 | 2 | ICLK |
| 0008 718Ch | ICU | DTC Transfer Request Enable Register 140 | DTCER140 | 8 | 8 | 2 | ICLK |
| 0008 718Dh | ICU | DTC Transfer Request Enable Register 141 | DTCER141 | 8 | 8 | 2 | ICLK |
| 0008 718Eh | ICU | DTC Transfer Request Enable Register 142 | DTCER142 | 8 | 8 | 2 | ICLK |
| 0008 718Fh | ICU | DTC Transfer Request Enable Register 143 | DTCER143 | 8 | 8 | 2 | ICLK |
| 0008 7190h | ICU | DTC Transfer Request Enable Register 144 | DTCER144 | 8 | 8 | 2 | ICLK |
| 0008 7191h | ICU | DTC Transfer Request Enable Register 145 | DTCER145 | 8 | 8 | 2 | ICLK |
| 0008 7195h | ICU | DTC Transfer Request Enable Register 149 | DTCER149 | 8 | 8 | 2 | ICLK |
| 0008 7196h | ICU | DTC Transfer Request Enable Register 150 | DTCER150 | 8 | 8 | 2 | ICLK |
| 0008 7197h | ICU | DTC Transfer Request Enable Register 151 | DTCER151 | 8 | 8 | 2 | ICLK |
| 0008 7198h | ICU | DTC Transfer Request Enable Register 152 | DTCER152 | 8 | 8 | 2 | ICLK |
| 0008 7199h | ICU | DTC Transfer Request Enable Register 153 | DTCER153 | 8 | 8 | 2 | ICLK |
| 0008 719Fh | ICU | DTC Transfer Request Enable Register 159 | DTCER159 | 8 | 8 | 2 | ICLK |
| 0008 71A0h | ICU | DTC Transfer Request Enable Register 160 | DTCER160 | 8 | 8 | 2 | ICLK |

Table 4.1 List of I/O Registers (Address Order) (7/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|------|
| | | | | | | ICLK ≥ PCLK | |
| 0008 71A1h | ICU | DTC Transfer Request Enable Register 161 | DTCER161 | 8 | 8 | 2 | ICLK |
| 0008 71A2h | ICU | DTC Transfer Request Enable Register 162 | DTCER162 | 8 | 8 | 2 | ICLK |
| 0008 71ADh | ICU | DTC Transfer Request Enable Register 173 | DTCER173 | 8 | 8 | 2 | ICLK |
| 0008 71AEh | ICU | DTC Transfer Request Enable Register 174 | DTCER174 | 8 | 8 | 2 | ICLK |
| 0008 71AFh | ICU | DTC Transfer Request Enable Register 175 | DTCER175 | 8 | 8 | 2 | ICLK |
| 0008 71B1h | ICU | DTC Transfer Request Enable Register 177 | DTCER177 | 8 | 8 | 2 | ICLK |
| 0008 71B2h | ICU | DTC Transfer Request Enable Register 178 | DTCER178 | 8 | 8 | 2 | ICLK |
| 0008 71B4h | ICU | DTC Transfer Request Enable Register 180 | DTCER180 | 8 | 8 | 2 | ICLK |
| 0008 71B5h | ICU | DTC Transfer Request Enable Register 181 | DTCER181 | 8 | 8 | 2 | ICLK |
| 0008 71B7h | ICU | DTC Transfer Request Enable Register 183 | DTCER183 | 8 | 8 | 2 | ICLK |
| 0008 71B8h | ICU | DTC Transfer Request Enable Register 184 | DTCER184 | 8 | 8 | 2 | ICLK |
| 0008 71BAh | ICU | DTC Transfer Request Enable Register 186 | DTCER186 | 8 | 8 | 2 | ICLK |
| 0008 71BBh | ICU | DTC Transfer Request Enable Register 187 | DTCER187 | 8 | 8 | 2 | ICLK |
| 0008 71BDh | ICU | DTC Transfer Request Enable Register 189 | DTCER189 | 8 | 8 | 2 | ICLK |
| 0008 71BEh | ICU | DTC Transfer Request Enable Register 190 | DTCER190 | 8 | 8 | 2 | ICLK |
| 0008 71C0h | ICU | DTC Transfer Request Enable Register 192 | DTCER192 | 8 | 8 | 2 | ICLK |
| 0008 71C1h | ICU | DTC Transfer Request Enable Register 193 | DTCER193 | 8 | 8 | 2 | ICLK |
| 0008 71C3h | ICU | DTC Transfer Request Enable Register 195 | DTCER195 | 8 | 8 | 2 | ICLK |
| 0008 71C4h | ICU | DTC Transfer Request Enable Register 196 | DTCER196 | 8 | 8 | 2 | ICLK |
| 0008 71CBh | ICU | DTC Transfer Request Enable Register 203*2 | DTCER203 | 8 | 8 | 2 | ICLK |
| 0008 71CCh | ICU | DTC Transfer Request Enable Register 204*2 | DTCER204 | 8 | 8 | 2 | ICLK |
| 0008 71CDh | ICU | DTC Transfer Request Enable Register 205*2 | DTCER205 | 8 | 8 | 2 | ICLK |
| 0008 71CEh | ICU | DTC Transfer Request Enable Register 206*2 | DTCER206 | 8 | 8 | 2 | ICLK |
| 0008 71CFh | ICU | DTC Transfer Request Enable Register 207*2 | DTCER207 | 8 | 8 | 2 | ICLK |
| 0008 71D0h | ICU | DTC Transfer Request Enable Register 208*2 | DTCER208 | 8 | 8 | 2 | ICLK |
| 0008 71D1h | ICU | DTC Transfer Request Enable Register 209*2 | DTCER209 | 8 | 8 | 2 | ICLK |
| 0008 71D2h | ICU | DTC Transfer Request Enable Register 210*2 | DTCER210 | 8 | 8 | 2 | ICLK |
| 0008 71D4h | ICU | DTC Transfer Request Enable Register 212*2 | DTCER212 | 8 | 8 | 2 | ICLK |
| 0008 71D5h | ICU | DTC Transfer Request Enable Register 213*2 | DTCER213 | 8 | 8 | 2 | ICLK |
| 0008 71D6h | ICU | DTC Transfer Request Enable Register 214*2 | DTCER214 | 8 | 8 | 2 | ICLK |
| 0008 71D7h | ICU | DTC Transfer Request Enable Register 215*2 | DTCER215 | 8 | 8 | 2 | ICLK |
| 0008 71D8h | ICU | DTC Transfer Request Enable Register 216*2 | DTCER216 | 8 | 8 | 2 | ICLK |
| 0008 71D9h | ICU | DTC Transfer Request Enable Register 217*2 | DTCER217 | 8 | 8 | 2 | ICLK |
| 0008 71DBh | ICU | DTC Transfer Request Enable Register 219 | DTCER219 | 8 | 8 | 2 | ICLK |
| 0008 71DCh | ICU | DTC Transfer Request Enable Register 220 | DTCER220 | 8 | 8 | 2 | ICLK |
| 0008 71DFh | ICU | DTC Transfer Request Enable Register 223 | DTCER223 | 8 | 8 | 2 | ICLK |
| 0008 71E0h | ICU | DTC Transfer Request Enable Register 224 | DTCER224 | 8 | 8 | 2 | ICLK |
| 0008 71E3h | ICU | DTC Transfer Request Enable Register 227 | DTCER227 | 8 | 8 | 2 | ICLK |
| 0008 71E4h | ICU | DTC Transfer Request Enable Register 228 | DTCER228 | 8 | 8 | 2 | ICLK |
| 0008 71EEh | ICU | DTC Transfer Request Enable Register 238*2 | DTCER238 | 8 | 8 | 2 | ICLK |
| 0008 71EFh | ICU | DTC Transfer Request Enable Register 239*2 | DTCER239 | 8 | 8 | 2 | ICLK |
| 0008 71F1h | ICU | DTC Transfer Request Enable Register 241*2 | DTCER241 | 8 | 8 | 2 | ICLK |
| 0008 71F2h | ICU | DTC Transfer Request Enable Register 242*2 | DTCER242 | 8 | 8 | 2 | ICLK |
| 0008 71F3h | ICU | DTC Transfer Request Enable Register 243*2 | DTCER243 | 8 | 8 | 2 | ICLK |
| 0008 71F4h | ICU | DTC Transfer Request Enable Register 244*2 | DTCER244 | 8 | 8 | 2 | ICLK |
| 0008 71F7h | ICU | DTC Transfer Request Enable Register 247 | DTCER247 | 8 | 8 | 2 | ICLK |
| 0008 71F8h | ICU | DTC Transfer Request Enable Register 248 | DTCER248 | 8 | 8 | 2 | ICLK |
| 0008 7202h | ICU | Interrupt Request Enable Register 02 | IER02 | 8 | 8 | 2 | ICLK |
| 0008 7203h | ICU | Interrupt Request Enable Register 03 | IER03 | 8 | 8 | 2 | ICLK |
| 0008 7204h | ICU | Interrupt Request Enable Register 04 | IER04 | 8 | 8 | 2 | ICLK |
| 0008 7205h | ICU | Interrupt Request Enable Register 05 | IER05 | 8 | 8 | 2 | ICLK |
| 0008 7206h | ICU | Interrupt Request Enable Register 06*2 | IER06 | 8 | 8 | 2 | ICLK |

Table 4.1 List of I/O Registers (Address Order) (8/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 0008 7207h | ICU | Interrupt Request Enable Register 07 | IER07 | 8 | 8 | 8 | 2 ICLK |
| 0008 7208h | ICU | Interrupt Request Enable Register 08 | IER08 | 8 | 8 | 8 | 2 ICLK |
| 0008 720Bh | ICU | Interrupt Request Enable Register 0B | IER0B | 8 | 8 | 8 | 2 ICLK |
| 0008 720Ch | ICU | Interrupt Request Enable Register 0C | IER0C | 8 | 8 | 8 | 2 ICLK |
| 0008 720Dh | ICU | Interrupt Request Enable Register 0D | IER0D | 8 | 8 | 8 | 2 ICLK |
| 0008 720Eh | ICU | Interrupt Request Enable Register 0E | IER0E | 8 | 8 | 8 | 2 ICLK |
| 0008 720Fh | ICU | Interrupt Request Enable Register 0F | IER0F | 8 | 8 | 8 | 2 ICLK |
| 0008 7210h | ICU | Interrupt Request Enable Register 10 | IER10 | 8 | 8 | 8 | 2 ICLK |
| 0008 7211h | ICU | Interrupt Request Enable Register 11 | IER11 | 8 | 8 | 8 | 2 ICLK |
| 0008 7212h | ICU | Interrupt Request Enable Register 12 | IER12 | 8 | 8 | 8 | 2 ICLK |
| 0008 7213h | ICU | Interrupt Request Enable Register 13 | IER13 | 8 | 8 | 8 | 2 ICLK |
| 0008 7214h | ICU | Interrupt Request Enable Register 14 | IER14 | 8 | 8 | 8 | 2 ICLK |
| 0008 7215h | ICU | Interrupt Request Enable Register 15 | IER15 | 8 | 8 | 8 | 2 ICLK |
| 0008 7216h | ICU | Interrupt Request Enable Register 16 | IER16 | 8 | 8 | 8 | 2 ICLK |
| 0008 7217h | ICU | Interrupt Request Enable Register 17 | IER17 | 8 | 8 | 8 | 2 ICLK |
| 0008 7218h | ICU | Interrupt Request Enable Register 18 | IER18 | 8 | 8 | 8 | 2 ICLK |
| 0008 7219h | ICU | Interrupt Request Enable Register 19*2 | IER19 | 8 | 8 | 8 | 2 ICLK |
| 0008 721Ah | ICU | Interrupt Request Enable Register 1A*2 | IER1A | 8 | 8 | 8 | 2 ICLK |
| 0008 721Bh | ICU | Interrupt Request Enable Register 1B | IER1B | 8 | 8 | 8 | 2 ICLK |
| 0008 721Ch | ICU | Interrupt Request Enable Register 1C | IER1C | 8 | 8 | 8 | 2 ICLK |
| 0008 721Dh | ICU | Interrupt Request Enable Register 1D*2 | IER1D | 8 | 8 | 8 | 2 ICLK |
| 0008 721Eh | ICU | Interrupt Request Enable Register 1E | IER1E | 8 | 8 | 8 | 2 ICLK |
| 0008 721Fh | ICU | Interrupt Request Enable Register 1F | IER1F | 8 | 8 | 8 | 2 ICLK |
| 0008 72E0h | ICU | Software Interrupt Generation Register | SWINTR | 8 | 8 | 8 | 2 ICLK |
| 0008 72F0h | ICU | Fast Interrupt Set Register | FIR | 16 | 16 | 16 | 2 ICLK |
| 0008 7300h | ICU | Interrupt Source Priority Register 000 | IPR000 | 8 | 8 | 8 | 2 ICLK |
| 0008 7302h | ICU | Interrupt Source Priority Register 002 | IPR002 | 8 | 8 | 8 | 2 ICLK |
| 0008 7303h | ICU | Interrupt Source Priority Register 003 | IPR003 | 8 | 8 | 8 | 2 ICLK |
| 0008 7304h | ICU | Interrupt Source Priority Register 004 | IPR004 | 8 | 8 | 8 | 2 ICLK |
| 0008 7305h | ICU | Interrupt Source Priority Register 005 | IPR005 | 8 | 8 | 8 | 2 ICLK |
| 0008 7306h | ICU | Interrupt Source Priority Register 006 | IPR006 | 8 | 8 | 8 | 2 ICLK |
| 0008 7307h | ICU | Interrupt Source Priority Register 007 | IPR007 | 8 | 8 | 8 | 2 ICLK |
| 0008 7320h | ICU | Interrupt Source Priority Register 032 | IPR032 | 8 | 8 | 8 | 2 ICLK |
| 0008 7321h | ICU | Interrupt Source Priority Register 033 | IPR033 | 8 | 8 | 8 | 2 ICLK |
| 0008 7322h | ICU | Interrupt Source Priority Register 034 | IPR034 | 8 | 8 | 8 | 2 ICLK |
| 0008 7328h | ICU | Interrupt Source Priority Register 040*2 | IPR040 | 8 | 8 | 8 | 2 ICLK |
| 0008 7329h | ICU | Interrupt Source Priority Register 041*2 | IPR041 | 8 | 8 | 8 | 2 ICLK |
| 0008 732Ch | ICU | Interrupt Source Priority Register 044 | IPR044 | 8 | 8 | 8 | 2 ICLK |
| 0008 7330h | ICU | Interrupt Source Priority Register 048*2 | IPR048 | 8 | 8 | 8 | 2 ICLK |
| 0008 7331h | ICU | Interrupt Source Priority Register 049*2 | IPR049 | 8 | 8 | 8 | 2 ICLK |
| 0008 7332h | ICU | Interrupt Source Priority Register 050*2 | IPR050 | 8 | 8 | 8 | 2 ICLK |
| 0008 7333h | ICU | Interrupt Source Priority Register 051*2 | IPR051 | 8 | 8 | 8 | 2 ICLK |
| 0008 7334h | ICU | Interrupt Source Priority Register 052*2 | IPR052 | 8 | 8 | 8 | 2 ICLK |
| 0008 7335h | ICU | Interrupt Source Priority Register 053*2 | IPR053 | 8 | 8 | 8 | 2 ICLK |
| 0008 7336h | ICU | Interrupt Source Priority Register 054*2 | IPR054 | 8 | 8 | 8 | 2 ICLK |
| 0008 7337h | ICU | Interrupt Source Priority Register 055*2 | IPR055 | 8 | 8 | 8 | 2 ICLK |
| 0008 7338h | ICU | Interrupt Source Priority Register 056*2 | IPR056 | 8 | 8 | 8 | 2 ICLK |
| 0008 7339h | ICU | Interrupt Source Priority Register 057 | IPR057 | 8 | 8 | 8 | 2 ICLK |
| 0008 733Bh | ICU | Interrupt Source Priority Register 059*2 | IPR059 | 8 | 8 | 8 | 2 ICLK |
| 0008 733Ch | ICU | Interrupt Source Priority Register 060*2 | IPR060 | 8 | 8 | 8 | 2 ICLK |
| 0008 733Dh | ICU | Interrupt Source Priority Register 061*2 | IPR061 | 8 | 8 | 8 | 2 ICLK |
| 0008 733Eh | ICU | Interrupt Source Priority Register 062*2 | IPR062 | 8 | 8 | 8 | 2 ICLK |

Table 4.1 List of I/O Registers (Address Order) (9/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|------|
| | | | | | | ICLK \geq PCLK | |
| 0008 733Fh | ICU | Interrupt Source Priority Register 063*2 | IPR063 | 8 | 8 | 2 | ICLK |
| 0008 7340h | ICU | Interrupt Source Priority Register 064 | IPR064 | 8 | 8 | 2 | ICLK |
| 0008 7341h | ICU | Interrupt Source Priority Register 065 | IPR065 | 8 | 8 | 2 | ICLK |
| 0008 7342h | ICU | Interrupt Source Priority Register 066 | IPR066 | 8 | 8 | 2 | ICLK |
| 0008 7343h | ICU | Interrupt Source Priority Register 067 | IPR067 | 8 | 8 | 2 | ICLK |
| 0008 7344h | ICU | Interrupt Source Priority Register 068 | IPR068 | 8 | 8 | 2 | ICLK |
| 0008 7345h | ICU | Interrupt Source Priority Register 069 | IPR069 | 8 | 8 | 2 | ICLK |
| 0008 7346h | ICU | Interrupt Source Priority Register 070 | IPR070 | 8 | 8 | 2 | ICLK |
| 0008 7347h | ICU | Interrupt Source Priority Register 071 | IPR071 | 8 | 8 | 2 | ICLK |
| 0008 7358h | ICU | Interrupt Source Priority Register 088 | IPR088 | 8 | 8 | 2 | ICLK |
| 0008 7359h | ICU | Interrupt Source Priority Register 089 | IPR089 | 8 | 8 | 2 | ICLK |
| 0008 7362h | ICU | Interrupt Source Priority Register 098*2 | IPR098 | 8 | 8 | 2 | ICLK |
| 0008 7363h | ICU | Interrupt Source Priority Register 099*2 | IPR099 | 8 | 8 | 2 | ICLK |
| 0008 7364h | ICU | Interrupt Source Priority Register 100*2 | IPR100 | 8 | 8 | 2 | ICLK |
| 0008 7365h | ICU | Interrupt Source Priority Register 101*2 | IPR101 | 8 | 8 | 2 | ICLK |
| 0008 7366h | ICU | Interrupt Source Priority Register 102 | IPR102 | 8 | 8 | 2 | ICLK |
| 0008 7367h | ICU | Interrupt Source Priority Register 103 | IPR103 | 8 | 8 | 2 | ICLK |
| 0008 7368h | ICU | Interrupt Source Priority Register 104 | IPR104 | 8 | 8 | 2 | ICLK |
| 0008 7369h | ICU | Interrupt Source Priority Register 105 | IPR105 | 8 | 8 | 2 | ICLK |
| 0008 736Ah | ICU | Interrupt Source Priority Register 106 | IPR106 | 8 | 8 | 2 | ICLK |
| 0008 736Bh | ICU | Interrupt Source Priority Register 107 | IPR107 | 8 | 8 | 2 | ICLK |
| 0008 736Ch | ICU | Interrupt Source Priority Register 108 | IPR108 | 8 | 8 | 2 | ICLK |
| 0008 736Dh | ICU | Interrupt Source Priority Register 109 | IPR109 | 8 | 8 | 2 | ICLK |
| 0008 736Eh | ICU | Interrupt Source Priority Register 110 | IPR110 | 8 | 8 | 2 | ICLK |
| 0008 736Fh | ICU | Interrupt Source Priority Register 111 | IPR111 | 8 | 8 | 2 | ICLK |
| 0008 7370h | ICU | Interrupt Source Priority Register 112 | IPR112 | 8 | 8 | 2 | ICLK |
| 0008 7371h | ICU | Interrupt Source Priority Register 113 | IPR113 | 8 | 8 | 2 | ICLK |
| 0008 7372h | ICU | Interrupt Source Priority Register 114 | IPR114 | 8 | 8 | 2 | ICLK |
| 0008 7376h | ICU | Interrupt Source Priority Register 118 | IPR118 | 8 | 8 | 2 | ICLK |
| 0008 7379h | ICU | Interrupt Source Priority Register 121 | IPR121 | 8 | 8 | 2 | ICLK |
| 0008 737Bh | ICU | Interrupt Source Priority Register 123 | IPR123 | 8 | 8 | 2 | ICLK |
| 0008 737Dh | ICU | Interrupt Source Priority Register 125 | IPR125 | 8 | 8 | 2 | ICLK |
| 0008 737Fh | ICU | Interrupt Source Priority Register 127 | IPR127 | 8 | 8 | 2 | ICLK |
| 0008 7381h | ICU | Interrupt Source Priority Register 129 | IPR129 | 8 | 8 | 2 | ICLK |
| 0008 7385h | ICU | Interrupt Source Priority Register 133 | IPR133 | 8 | 8 | 2 | ICLK |
| 0008 7386h | ICU | Interrupt Source Priority Register 134 | IPR134 | 8 | 8 | 2 | ICLK |
| 0008 738Ah | ICU | Interrupt Source Priority Register 138 | IPR138 | 8 | 8 | 2 | ICLK |
| 0008 738Bh | ICU | Interrupt Source Priority Register 139 | IPR139 | 8 | 8 | 2 | ICLK |
| 0008 738Eh | ICU | Interrupt Source Priority Register 142 | IPR142 | 8 | 8 | 2 | ICLK |
| 0008 7392h | ICU | Interrupt Source Priority Register 146 | IPR146 | 8 | 8 | 2 | ICLK |
| 0008 7395h | ICU | Interrupt Source Priority Register 149 | IPR149 | 8 | 8 | 2 | ICLK |
| 0008 7397h | ICU | Interrupt Source Priority Register 151 | IPR151 | 8 | 8 | 2 | ICLK |
| 0008 7399h | ICU | Interrupt Source Priority Register 153 | IPR153 | 8 | 8 | 2 | ICLK |
| 0008 739Fh | ICU | Interrupt Source Priority Register 159 | IPR159 | 8 | 8 | 2 | ICLK |
| 0008 73A3h | ICU | Interrupt Source Priority Register 163 | IPR163 | 8 | 8 | 2 | ICLK |
| 0008 73A8h | ICU | Interrupt Source Priority Register 168 | IPR168 | 8 | 8 | 2 | ICLK |
| 0008 73ADh | ICU | Interrupt Source Priority Register 173 | IPR173 | 8 | 8 | 2 | ICLK |
| 0008 73AEh | ICU | Interrupt Source Priority Register 174 | IPR174 | 8 | 8 | 2 | ICLK |
| 0008 73B1h | ICU | Interrupt Source Priority Register 177 | IPR177 | 8 | 8 | 2 | ICLK |
| 0008 73B4h | ICU | Interrupt Source Priority Register 180 | IPR180 | 8 | 8 | 2 | ICLK |
| 0008 73B7h | ICU | Interrupt Source Priority Register 183 | IPR183 | 8 | 8 | 2 | ICLK |
| 0008 73BAh | ICU | Interrupt Source Priority Register 186 | IPR186 | 8 | 8 | 2 | ICLK |

Table 4.1 List of I/O Registers (Address Order) (10/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 0008 73BDh | ICU | Interrupt Source Priority Register 189 | IPR189 | 8 | 8 | | 2 ICLK |
| 0008 73C0h | ICU | Interrupt Source Priority Register 192 | IPR192 | 8 | 8 | | 2 ICLK |
| 0008 73C3h | ICU | Interrupt Source Priority Register 195 | IPR195 | 8 | 8 | | 2 ICLK |
| 0008 73CAh | ICU | Interrupt Source Priority Register 202*2 | IPR202 | 8 | 8 | | 2 ICLK |
| 0008 73CBh | ICU | Interrupt Source Priority Register 203*2 | IPR203 | 8 | 8 | | 2 ICLK |
| 0008 73CCh | ICU | Interrupt Source Priority Register 204*2 | IPR204 | 8 | 8 | | 2 ICLK |
| 0008 73CDh | ICU | Interrupt Source Priority Register 205*2 | IPR205 | 8 | 8 | | 2 ICLK |
| 0008 73CEh | ICU | Interrupt Source Priority Register 206*2 | IPR206 | 8 | 8 | | 2 ICLK |
| 0008 73CFh | ICU | Interrupt Source Priority Register 207*2 | IPR207 | 8 | 8 | | 2 ICLK |
| 0008 73D0h | ICU | Interrupt Source Priority Register 208*2 | IPR208 | 8 | 8 | | 2 ICLK |
| 0008 73D1h | ICU | Interrupt Source Priority Register 209*2 | IPR209 | 8 | 8 | | 2 ICLK |
| 0008 73D2h | ICU | Interrupt Source Priority Register 210*2 | IPR210 | 8 | 8 | | 2 ICLK |
| 0008 73D3h | ICU | Interrupt Source Priority Register 211*2 | IPR211 | 8 | 8 | | 2 ICLK |
| 0008 73D4h | ICU | Interrupt Source Priority Register 212*2 | IPR212 | 8 | 8 | | 2 ICLK |
| 0008 73D5h | ICU | Interrupt Source Priority Register 213*2 | IPR213 | 8 | 8 | | 2 ICLK |
| 0008 73D6h | ICU | Interrupt Source Priority Register 214*2 | IPR214 | 8 | 8 | | 2 ICLK |
| 0008 73D7h | ICU | Interrupt Source Priority Register 215*2 | IPR215 | 8 | 8 | | 2 ICLK |
| 0008 73D8h | ICU | Interrupt Source Priority Register 216*2 | IPR216 | 8 | 8 | | 2 ICLK |
| 0008 73D9h | ICU | Interrupt Source Priority Register 217*2 | IPR217 | 8 | 8 | | 2 ICLK |
| 0008 73DAh | ICU | Interrupt Source Priority Register 218 | IPR218 | 8 | 8 | | 2 ICLK |
| 0008 73DEh | ICU | Interrupt Source Priority Register 222 | IPR222 | 8 | 8 | | 2 ICLK |
| 0008 73E2h | ICU | Interrupt Source Priority Register 226 | IPR226 | 8 | 8 | | 2 ICLK |
| 0008 73EEh | ICU | Interrupt Source Priority Register 238*2 | IPR238 | 8 | 8 | | 2 ICLK |
| 0008 73EFh | ICU | Interrupt Source Priority Register 239*2 | IPR239 | 8 | 8 | | 2 ICLK |
| 0008 73F0h | ICU | Interrupt Source Priority Register 240*2 | IPR240 | 8 | 8 | | 2 ICLK |
| 0008 73F1h | ICU | Interrupt Source Priority Register 241*2 | IPR241 | 8 | 8 | | 2 ICLK |
| 0008 73F2h | ICU | Interrupt Source Priority Register 242*2 | IPR242 | 8 | 8 | | 2 ICLK |
| 0008 73F3h | ICU | Interrupt Source Priority Register 243*2 | IPR243 | 8 | 8 | | 2 ICLK |
| 0008 73F4h | ICU | Interrupt Source Priority Register 244*2 | IPR244 | 8 | 8 | | 2 ICLK |
| 0008 73F6h | ICU | Interrupt Source Priority Register 246 | IPR246 | 8 | 8 | | 2 ICLK |
| 0008 73F7h | ICU | Interrupt Source Priority Register 247 | IPR247 | 8 | 8 | | 2 ICLK |
| 0008 73F8h | ICU | Interrupt Source Priority Register 248 | IPR248 | 8 | 8 | | 2 ICLK |
| 0008 73F9h | ICU | Interrupt Source Priority Register 249 | IPR249 | 8 | 8 | | 2 ICLK |
| 0008 7500h | ICU | IRQ Control Register 0 | IRQCR0 | 8 | 8 | | 2 ICLK |
| 0008 7501h | ICU | IRQ Control Register 1 | IRQCR1 | 8 | 8 | | 2 ICLK |
| 0008 7502h | ICU | IRQ Control Register 2 | IRQCR2 | 8 | 8 | | 2 ICLK |
| 0008 7503h | ICU | IRQ Control Register 3 | IRQCR3 | 8 | 8 | | 2 ICLK |
| 0008 7504h | ICU | IRQ Control Register 4 | IRQCR4 | 8 | 8 | | 2 ICLK |
| 0008 7505h | ICU | IRQ Control Register 5 | IRQCR5 | 8 | 8 | | 2 ICLK |
| 0008 7506h | ICU | IRQ Control Register 6 | IRQCR6 | 8 | 8 | | 2 ICLK |
| 0008 7507h | ICU | IRQ Control Register 7 | IRQCR7 | 8 | 8 | | 2 ICLK |
| 0008 7510h | ICU | IRQ Pin Digital Filter Enable Register 0 | IRQFLTE0 | 8 | 8 | | 2 ICLK |
| 0008 7514h | ICU | IRQ Pin Digital Filter Setting Register 0 | IRQFLTC0 | 16 | 16 | | 2 ICLK |
| 0008 7580h | ICU | Non-Maskable Interrupt Status Register | NMISR | 8 | 8 | | 2 ICLK |
| 0008 7581h | ICU | Non-Maskable Interrupt Enable Register | NMIER | 8 | 8 | | 2 ICLK |
| 0008 7582h | ICU | Non-Maskable Interrupt Status Clear Register | NMICLR | 8 | 8 | | 2 ICLK |
| 0008 7583h | ICU | NMI Pin Interrupt Control Register | NMICR | 8 | 8 | | 2 ICLK |
| 0008 7590h | ICU | NMI Pin Digital Filter Enable Register | NMIFLTE | 8 | 8 | | 2 ICLK |
| 0008 7594h | ICU | NMI Pin Digital Filter Setting Register | NMIFLTC | 8 | 8 | | 2 ICLK |
| 0008 8000h | CMT | Compare Match Timer Start Register 0 | CMSTR0 | 16 | 16 | | 2 or 3 PCLKB |
| 0008 8002h | CMT0 | Compare Match Timer Control Register | CMCR | 16 | 16 | | 2 or 3 PCLKB |
| 0008 8004h | CMT0 | Compare Match Counter | CMCNT | 16 | 16 | | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (11/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 8006h | CMT0 | Compare Match Constant Register | CMCOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8008h | CMT1 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 800Ah | CMT1 | Compare Match Counter | CMCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 800Ch | CMT1 | Compare Match Constant Register | CMCOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8010h | CMT | Compare Match Timer Start Register 1 | CMSTR1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8012h | CMT2 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8014h | CMT2 | Compare Match Counter | CMCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 8016h | CMT2 | Compare Match Constant Register | CMCOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8018h | CMT3 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 801Ah | CMT3 | Compare Match Counter | CMCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 801Ch | CMT3 | Compare Match Constant Register | CMCOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8030h | IWDT | IWDT Refresh Register | IWDTRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8032h | IWDT | IWDT Control Register | IWDTCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8034h | IWDT | IWDT Status Register | IWDTSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8036h | IWDT | IWDT Reset Control Register | IWDTRCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8038h | IWDT | IWDT Count Stop Control Register | IWDTCSTPR | 8 | 8 | 2 or 3 PCLKB |
| 0008 80C0h | DA | D/A Data Register 0 | DADR0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 80C2h | DA | D/A Data Register 1*2 | DADR1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 80C4h | DA | D/A Control Register | DACR | 8 | 8 | 2 or 3 PCLKB |
| 0008 80C5h | DA | DADRm Format Select Register | DADPR | 8 | 8 | 2 or 3 PCLKB |
| 0008 80C6h | DA | D/A A/D Synchronous Start Control Register*2 | DAADSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8200h | TMR0 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8201h | TMR1 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8202h | TMR0 | Timer Control/Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8203h | TMR1 | Timer Control/Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8204h | TMR0 | Time Constant Register A | TCORA | 8 | 8 | 2 or 3 PCLKB |
| 0008 8205h | TMR1 | Time Constant Register A | TCORA | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8206h | TMR0 | Time Constant Register B | TCORB | 8 | 8 | 2 or 3 PCLKB |
| 0008 8207h | TMR1 | Time Constant Register B | TCORB | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8208h | TMR0 | Timer Counter | TCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8209h | TMR1 | Timer Counter | TCNT | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 820Ah | TMR0 | Timer Counter Control Register | TCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 820Bh | TMR1 | Timer Counter Control Register | TCCR | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8210h | TMR2 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8211h | TMR3 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8212h | TMR2 | Timer Control/Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8213h | TMR3 | Timer Control/Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8214h | TMR2 | Time Constant Register A | TCORA | 8 | 8 | 2 or 3 PCLKB |
| 0008 8215h | TMR3 | Time Constant Register A | TCORA | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8216h | TMR2 | Time Constant Register B | TCORB | 8 | 8 | 2 or 3 PCLKB |
| 0008 8217h | TMR3 | Time Constant Register B | TCORB | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8218h | TMR2 | Timer Counter | TCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8219h | TMR3 | Timer Counter | TCNT | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 821Ah | TMR2 | Timer Counter Control Register | TCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 821Bh | TMR3 | Timer Counter Control Register | TCCR | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8220h | TMR4 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8221h | TMR5 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8222h | TMR4 | Timer Control / Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8223h | TMR5 | Timer Control / Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8224h | TMR4 | Time Constant Register A | TCORA | 8 | 8 | 2 or 3 PCLKB |
| 0008 8225h | TMR5 | Time Constant Register A | TCORA | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8226h | TMR4 | Time Constant Register B | TCORB | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (12/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 8227h | TMR5 | Time Constant Register B | TCORB | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8228h | TMR4 | Timer Counter | TCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8229h | TMR5 | Timer Counter | TCNT | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 822Ah | TMR4 | Timer Counter Control Register | TCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 822Bh | TMR5 | Timer Counter Control Register | TCCR | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8230h | TMR6 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8231h | TMR7 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8232h | TMR6 | Timer Control / Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8233h | TMR7 | Timer Control / Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8234h | TMR6 | Time Constant Register A | TCORA | 8 | 8 | 2 or 3 PCLKB |
| 0008 8235h | TMR7 | Time Constant Register A | TCORA | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8236h | TMR6 | Time Constant Register B | TCORB | 8 | 8 | 2 or 3 PCLKB |
| 0008 8237h | TMR7 | Time Constant Register B | TCORB | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8238h | TMR6 | Timer Counter | TCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8239h | TMR7 | Timer Counter | TCNT | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 823Ah | TMR6 | Timer Counter Control Register | TCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 823Bh | TMR7 | Timer Counter Control Register | TCCR | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8280h | CRC | CRC Control Register | CRCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8281h | CRC | CRC Data Input Register | CRCDIR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8282h | CRC | CRC Data Output Register | CRCDOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8300h | RIIC0 | I ² C-bus Control Register 1 | ICCR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8301h | RIIC0 | I ² C-bus Control Register 2 | ICCR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8302h | RIIC0 | I ² C-bus Mode Register 1 | ICMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8303h | RIIC0 | I ² C-bus Mode Register 2 | ICMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8304h | RIIC0 | I ² C-bus Mode Register 3 | ICMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8305h | RIIC0 | I ² C-bus Function Enable Register | ICFER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8306h | RIIC0 | I ² C-bus Status Enable Register | ICSER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8307h | RIIC0 | I ² C-bus Interrupt Enable Register | ICIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8308h | RIIC0 | I ² C-bus Status Register 1 | ICSR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8309h | RIIC0 | I ² C-bus Status Register 2 | ICSR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Ah | RIIC0 | Slave Address Register L0 | SARL0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Bh | RIIC0 | Slave Address Register U0 | SARU0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Ch | RIIC0 | Slave Address Register L1 | SARL1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Dh | RIIC0 | Slave Address Register U1 | SARU1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Eh | RIIC0 | Slave Address Register L2 | SARL2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Fh | RIIC0 | Slave Address Register U2 | SARU2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8310h | RIIC0 | I ² C-bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 8311h | RIIC0 | I ² C-bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 8312h | RIIC0 | I ² C-bus Transmit Data Register | ICDRT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8313h | RIIC0 | I ² C-bus Receive Data Register | ICDRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8380h | RSPI0 | RSPI Control Register | SPCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8381h | RSPI0 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 2 or 3 PCLKB |
| 0008 8382h | RSPI0 | RSPI Pin Control Register | SPPCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8383h | RSPI0 | RSPI Status Register | SPSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8384h | RSPI0 | RSPI Data Register | SPDR | 32 | 16, 32 | 2 or 3 PCLKB |
| 0008 8388h | RSPI0 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8389h | RSPI0 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Ah | RSPI0 | RSPI Bit Rate Register | SPBR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Bh | RSPI0 | RSPI Data Control Register | SPDCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Ch | RSPI0 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Dh | RSPI0 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Eh | RSPI0 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (13/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 838Fh | RSPI0 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8390h | RSPI0 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8392h | RSPI0 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8394h | RSPI0 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8396h | RSPI0 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8398h | RSPI0 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 2 or 3 PCLKB |
| 0008 839Ah | RSPI0 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 2 or 3 PCLKB |
| 0008 839Ch | RSPI0 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 2 or 3 PCLKB |
| 0008 839Eh | RSPI0 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9000h | S12AD | A/D Control Register | ADCSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9004h | S12AD | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9006h | S12AD | A/D Channel Select Register A1 | ADANSA1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9008h | S12AD | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 900Ah | S12AD | A/D-Converted Value Addition/Average Function Channel Select Register 1 | ADADS1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 900Ch | S12AD | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2 or 3 PCLKB |
| 0008 900Eh | S12AD | A/D Control Extended Register | ADCER | 16 | 16 | 2 or 3 PCLKB |
| 0008 9010h | S12AD | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9014h | S12AD | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9016h | S12AD | A/D Channel Select Register B1 | ADANSB1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9018h | S12AD | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 901Eh | S12AD | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2 or 3 PCLKB |
| 0008 9020h | S12AD | A/D Data Register 0 | ADDR0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9022h | S12AD | A/D Data Register 1 | ADDR1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9024h | S12AD | A/D Data Register 2 | ADDR2 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9026h | S12AD | A/D Data Register 3 | ADDR3 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9040h | S12AD | A/D Data Register 16 | ADDR16 | 16 | 16 | 2 or 3 PCLKB |
| 0008 907Ah | S12AD | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 9080h | S12AD | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9084h | S12AD | A/D Data Duplication Register A | ADDBLDR A | 16 | 16 | 2 or 3 PCLKB |
| 0008 9086h | S12AD | A/D Data Duplication Register B | ADDBLDR B | 16 | 16 | 2 or 3 PCLKB |
| 0008 90D4h | S12AD | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 90D6h | S12AD | A/D Channel Select Register C1 | ADANSC1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 90D9h | S12AD | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2 or 3 PCLKB |
| 0008 90DDh | S12AD | A/D Sampling State Register L | ADSSTR L | 8 | 8 | 2 or 3 PCLKB |
| 0008 90E0h | S12AD | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 90E1h | S12AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 90E2h | S12AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 90E3h | S12AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 91A0h | S12AD | A/D Programmable Gain Amplifier Control Register | ADPGACR | 16 | 16 | 2 or 3 PCLKB |
| 0008 91A2h | S12AD | A/D Programmable Gain Amplifier Gain Setting Register 0 | ADPGAGS0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9200h | S12AD1 | A/D Control Register | ADCSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9204h | S12AD1 | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9206h | S12AD1 | A/D Channel Select Register A1 | ADANSA1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9208h | S12AD1 | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 920Ah | S12AD1 | A/D-Converted Value Addition/Average Function Channel Select Register 1 | ADADS1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 920Ch | S12AD1 | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2 or 3 PCLKB |
| 0008 920Eh | S12AD1 | A/D Control Extended Register | ADCER | 16 | 16 | 2 or 3 PCLKB |
| 0008 9210h | S12AD1 | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (14/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 9214h | S12AD1 | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9216h | S12AD1 | A/D Channel Select Register B1 | ADANSB1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9218h | S12AD1 | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 921Eh | S12AD1 | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2 or 3 PCLKB |
| 0008 9220h | S12AD1 | A/D Data Register 0 | ADDR0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9222h | S12AD1 | A/D Data Register 1 | ADDR1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9224h | S12AD1 | A/D Data Register 2 | ADDR2 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9226h | S12AD1 | A/D Data Register 3 | ADDR3 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9240h | S12AD1 | A/D Data Register 16 | ADDR16 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9266h | S12AD1 | A/D Sample-and-hold Circuit Control Register | ADSHCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 927Ah | S12AD1 | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 9280h | S12AD1 | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9284h | S12AD1 | A/D Data Duplication Register A | ADDBLDRA | 16 | 16 | 2 or 3 PCLKB |
| 0008 9286h | S12AD1 | A/D Data Duplication Register B | ADDBLDRB | 16 | 16 | 2 or 3 PCLKB |
| 0008 92D4h | S12AD1 | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 92D6h | S12AD1 | A/D Channel Select Register C1 | ADANSC1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 92D9h | S12AD1 | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2 or 3 PCLKB |
| 0008 92DDh | S12AD1 | A/D Sampling State Register L | ADSSTRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 92E0h | S12AD1 | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 92E1h | S12AD1 | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 92E2h | S12AD1 | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 92E3h | S12AD1 | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 93A0h | S12AD1 | A/D Programmable Gain Amplifier Control Register | ADPGACR | 16 | 16 | 2 or 3 PCLKB |
| 0008 93A2h | S12AD1 | A/D Programmable Gain Amplifier Gain Setting Register 0 | ADPGAGS0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9400h | S12AD2 | A/D Control Register | ADCSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9404h | S12AD2 | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9408h | S12AD2 | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 940Ch | S12AD2 | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2 or 3 PCLKB |
| 0008 940Eh | S12AD2 | A/D Control Extended Register | ADCER | 16 | 16 | 2 or 3 PCLKB |
| 0008 9410h | S12AD2 | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9412h | S12AD2 | A/D Conversion Extended Input Control Register | ADEXICR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9414h | S12AD2 | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9418h | S12AD2 | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 941Ch | S12AD2 | A/D Internal Reference Voltage Data Register | ADOCDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 941Eh | S12AD2 | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2 or 3 PCLKB |
| 0008 9420h | S12AD2 | A/D Data Register 0 | ADDR0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9422h | S12AD2 | A/D Data Register 1 | ADDR1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9424h | S12AD2 | A/D Data Register 2 | ADDR2 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9426h | S12AD2 | A/D Data Register 3 | ADDR3 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9428h | S12AD2 | A/D Data Register 4 | ADDR4 | 16 | 16 | 2 or 3 PCLKB |
| 0008 942Ah | S12AD2 | A/D Data Register 5 | ADDR5 | 16 | 16 | 2 or 3 PCLKB |
| 0008 942Ch | S12AD2 | A/D Data Register 6 | ADDR6 | 16 | 16 | 2 or 3 PCLKB |
| 0008 942Eh | S12AD2 | A/D Data Register 7 | ADDR7 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9430h | S12AD2 | A/D Data Register 8 | ADDR8 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9432h | S12AD2 | A/D Data Register 9 | ADDR9 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9434h | S12AD2 | A/D Data Register 10 | ADDR10 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9436h | S12AD2 | A/D Data Register 11 | ADDR11 | 16 | 16 | 2 or 3 PCLKB |
| 0008 947Ah | S12AD2 | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 9480h | S12AD2 | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9484h | S12AD2 | A/D Data Duplication Register A | ADDBLDRA | 16 | 16 | 2 or 3 PCLKB |
| 0008 9486h | S12AD2 | A/D Data Duplication Register B | ADDBLDRB | 16 | 16 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (15/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|-------------------------------------|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 94D4h | S12AD2 | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 94D9h | S12AD2 | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2 or 3 PCLKB |
| 0008 94DFh | S12AD2 | A/D Sampling State Register 0 | ADSSTRO | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E0h | S12AD2 | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E1h | S12AD2 | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E2h | S12AD2 | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E3h | S12AD2 | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E4h | S12AD2 | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E5h | S12AD2 | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E6h | S12AD2 | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E7h | S12AD2 | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E8h | S12AD2 | A/D Sampling State Register 8 | ADSSTR8 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94E9h | S12AD2 | A/D Sampling State Register 9 | ADSSTR9 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94EAh | S12AD2 | A/D Sampling State Register 10 | ADSSTR10 | 8 | 8 | 2 or 3 PCLKB |
| 0008 94EBh | S12AD2 | A/D Sampling State Register 11 | ADSSTR11 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A026h | SMCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A028h | SCI1 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A029h | SCI1 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Ah | SCI1 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Bh | SCI1 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Ch | SCI1 | I ² C Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Dh | SCI1 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Eh | SCI1 | Transmit Data Register HL | TDRHL | 16 | 16 | 4 or 5 PCLKB |
| 0008 A02Eh | SCI1 | Transmit Data Register H | TDRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Fh | SCI1 | Transmit Data Register L | TDRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 A030h | SCI1 | Receive Data Register HL | RDRHL | 16 | 16 | 4 or 5 PCLKB |
| 0008 A030h | SCI1 | Receive Data Register H | RDRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 A031h | SCI1 | Receive Data Register L | RDRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 A032h | SCI1 | Modulation Duty Register | MDDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A0h | SCI5 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A1h | SCI5 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A2h | SCI5 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A3h | SCI5 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A4h | SCI5 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A5h | SCI5 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A6h | SMCI5 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A7h | SCI5 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A8h | SCI5 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A9h | SCI5 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0AAh | SCI5 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ABh | SCI5 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ACh | SCI5 | I ² C Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ADh | SCI5 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0AEh | SCI5 | Transmit Data Register HL | TDRHL | 16 | 16 | 4 or 5 PCLKB |
| 0008 A0AEh | SCI5 | Transmit Data Register H | TDRH | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (16/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 A0AFh | SCI5 | Transmit Data Register L | TDRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0B0h | SCI5 | Receive Data Register HL | RDRHL | 16 | 16 | 4 or 5 PCLKB |
| 0008 A0B0h | SCI5 | Receive Data Register H | RDRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0B1h | SCI5 | Receive Data Register L | RDRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0B2h | SCI5 | Modulation Duty Register | MDDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C0h | SCI6 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C1h | SCI6 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C2h | SCI6 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C3h | SCI6 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C4h | SCI6 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C5h | SCI6 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C6h | SMCI6 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C7h | SCI6 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C8h | SCI6 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0C9h | SCI6 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0CAh | SCI6 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0CBh | SCI6 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0CCh | SCI6 | I ² C Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0CDh | SCI6 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0CEh | SCI6 | Transmit Data Register HL | TDRHL | 16 | 16 | 4 or 5 PCLKB |
| 0008 A0CEh | SCI6 | Transmit Data Register H | TDRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0CFh | SCI6 | Transmit Data Register L | TDRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0D0h | SCI6 | Receive Data Register HL | RDRHL | 16 | 16 | 4 or 5 PCLKB |
| 0008 A0D0h | SCI6 | Receive Data Register H | RDRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0D1h | SCI6 | Receive Data Register L | RDRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0D2h | SCI6 | Modulation Duty Register | MDDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B000h | CAC | CAC Control Register 0 | CACR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B001h | CAC | CAC Control Register 1 | CACR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B002h | CAC | CAC Control Register 2 | CACR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B003h | CAC | CAC Interrupt Request Enable Register | CAICR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B004h | CAC | CAC Status Register | CASTR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B006h | CAC | CAC Upper-Limit Value Setting Register | CAULVR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B008h | CAC | CAC Lower-Limit Value Setting Register | CALLVR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B00Ah | CAC | CAC Counter Buffer Register | CACNTBR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B080h | DOC | DOC Control Register | DOCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B082h | DOC | DOC Data Input Register | DODIR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B084h | DOC | DOC Data Setting Register | DODSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 C000h | PORT0 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C001h | PORT1 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C002h | PORT2 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C003h | PORT3 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C004h | PORT4 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C005h | PORT5 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C006h | PORT6 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C007h | PORT7 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C008h | PORT8 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C009h | PORT9 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Ah | PORTA | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Bh | PORTB | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Dh | PORTD | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Eh | PORTE | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C020h | PORT0 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (17/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|-------------------------------|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 C021h | PORT1 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C022h | PORT2 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C023h | PORT3 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C024h | PORT4 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C025h | PORT5 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C026h | PORT6 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C027h | PORT7 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C028h | PORT8 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C029h | PORT9 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Ah | PORTA | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Bh | PORTB | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Dh | PORTD | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Eh | PORTE | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C040h | PORT0 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C041h | PORT1 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C042h | PORT2 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C043h | PORT3 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C044h | PORT4 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C045h | PORT5 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C046h | PORT6 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C047h | PORT7 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C048h | PORT8 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C049h | PORT9 | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C04Ah | PORTA | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C04Bh | PORTB | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C04Dh | PORTD | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C04Eh | PORTE | Port Input Data Register | PIDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C060h | PORT0 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C061h | PORT1 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C062h | PORT2 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C063h | PORT3 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C067h | PORT7 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C068h | PORT8 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C069h | PORT9 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Ah | PORTA | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Bh | PORTB | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Dh | PORTD | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Eh | PORTE | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C080h | PORT0 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C082h | PORT1 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C084h | PORT2 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C085h | PORT2 | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C086h | PORT3 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C08Eh | PORT7 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C08Fh | PORT7 | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C090h | PORT8 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C092h | PORT9 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C093h | PORT9 | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C094h | PORTA | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C095h | PORTA | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C096h | PORTB | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C097h | PORTB | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (18/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 C09Ah | PORTD | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C09Bh | PORTD | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C09Ch | PORTE | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C09Dh | PORTE | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C0C0h | PORT0 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C1h | PORT1 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C2h | PORT2 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C3h | PORT3 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C4h | PORT4 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C5h | PORT5 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C6h | PORT6 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C7h | PORT7 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C8h | PORT8 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C9h | PORT9 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CAh | PORTA | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CBh | PORTB | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CDh | PORTD | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CEh | PORTE | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0E0h | PORT0 | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0E1h | PORT1 | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0E2h | PORT2 | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0E3h | PORT3 | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0E7h | PORT7 | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0E8h | PORT8 | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0E9h | PORT9 | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0EAh | PORTA | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0EBh | PORTB | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0EDh | PORTD | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0EEh | PORTE | Drive Capacity Control Register | DSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C140h | MPC | P00 Pin Function Control Register | P00PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C141h | MPC | P01 Pin Function Control Register | P01PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C142h | MPC | P02 Pin Function Control Register | P02PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C148h | MPC | P10 Pin Function Control Register | P10PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C149h | MPC | P11 Pin Function Control Register | P11PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C150h | MPC | P20 Pin Function Control Register | P20PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C151h | MPC | P21 Pin Function Control Register | P21PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C152h | MPC | P22 Pin Function Control Register | P22PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C153h | MPC | P23 Pin Function Control Register | P23PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C154h | MPC | P24 Pin Function Control Register | P24PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C158h | MPC | P30 Pin Function Control Register | P30PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C159h | MPC | P31 Pin Function Control Register | P31PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C15Ah | MPC | P32 Pin Function Control Register | P32PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C15Bh | MPC | P33 Pin Function Control Register | P33PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C160h | MPC | P40 Pin Function Control Register | P40PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C161h | MPC | P41 Pin Function Control Register | P41PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C162h | MPC | P42 Pin Function Control Register | P42PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C163h | MPC | P43 Pin Function Control Register | P43PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C164h | MPC | P44 Pin Function Control Register | P44PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C165h | MPC | P45 Pin Function Control Register | P45PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C166h | MPC | P46 Pin Function Control Register | P46PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C167h | MPC | P47 Pin Function Control Register | P47PFS | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (19/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 0008 C168h | MPC | P50 Pin Function Control Register | P50PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C169h | MPC | P51 Pin Function Control Register | P51PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C16Ah | MPC | P52 Pin Function Control Register | P52PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C16Bh | MPC | P53 Pin Function Control Register | P53PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C16Ch | MPC | P54 Pin Function Control Register | P54PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C16Dh | MPC | P55 Pin Function Control Register | P55PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C170h | MPC | P60 Pin Function Control Register | P60PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C171h | MPC | P61 Pin Function Control Register | P61PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C172h | MPC | P62 Pin Function Control Register | P62PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C173h | MPC | P63 Pin Function Control Register | P63PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C174h | MPC | P64 Pin Function Control Register | P64PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C175h | MPC | P65 Pin Function Control Register | P65PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C178h | MPC | P70 Pin Function Control Register | P70PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C179h | MPC | P71 Pin Function Control Register | P71PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C17Ah | MPC | P72 Pin Function Control Register | P72PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C17Bh | MPC | P73 Pin Function Control Register | P73PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C17Ch | MPC | P74 Pin Function Control Register | P74PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C17Dh | MPC | P75 Pin Function Control Register | P75PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C17Eh | MPC | P76 Pin Function Control Register | P76PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C180h | MPC | P80 Pin Function Control Register | P80PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C181h | MPC | P81 Pin Function Control Register | P81PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C182h | MPC | P82 Pin Function Control Register | P82PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C188h | MPC | P90 Pin Function Control Register | P90PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C189h | MPC | P91 Pin Function Control Register | P91PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C18Ah | MPC | P92 Pin Function Control Register | P92PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C18Bh | MPC | P93 Pin Function Control Register | P93PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C18Ch | MPC | P94 Pin Function Control Register | P94PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C18Dh | MPC | P95 Pin Function Control Register | P95PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C18Eh | MPC | P96 Pin Function Control Register | P96PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C190h | MPC | PA0 Pin Function Control Register | PA0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C191h | MPC | PA1 Pin Function Control Register | PA1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C192h | MPC | PA2 Pin Function Control Register | PA2PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C193h | MPC | PA3 Pin Function Control Register | PA3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C194h | MPC | PA4 Pin Function Control Register | PA4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C195h | MPC | PA5 Pin Function Control Register | PA5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C198h | MPC | PB0 Pin Function Control Register | PB0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C199h | MPC | PB1 Pin Function Control Register | PB1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Ah | MPC | PB2 Pin Function Control Register | PB2PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Bh | MPC | PB3 Pin Function Control Register | PB3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Ch | MPC | PB4 Pin Function Control Register | PB4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Dh | MPC | PB5 Pin Function Control Register | PB5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Eh | MPC | PB6 Pin Function Control Register | PB6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Fh | MPC | PB7 Pin Function Control Register | PB7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A8h | MPC | PD0 Pin Function Control Register | PD0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A9h | MPC | PD1 Pin Function Control Register | PD1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1AAh | MPC | PD2 Pin Function Control Register | PD2PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1ABh | MPC | PD3 Pin Function Control Register | PD3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1ACh | MPC | PD4 Pin Function Control Register | PD4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1ADh | MPC | PD5 Pin Function Control Register | PD5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1AEh | MPC | PD6 Pin Function Control Register | PD6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1AFh | MPC | PD7 Pin Function Control Register | PD7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B0h | MPC | PE0 Pin Function Control Register | PE0PFS | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (20/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------|
| | | | | | | ICLK ≥ PCLK | |
| 0008 C1B1h | MPC | PE1 Pin Function Control Register | PE1PFS | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C1B2h | MPC | PE2 Pin Function Control Register | PE2PFS | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C1B3h | MPC | PE3 Pin Function Control Register | PE3PFS | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C1B4h | MPC | PE4 Pin Function Control Register | PE4PFS | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C1B5h | MPC | PE5 Pin Function Control Register | PE5PFS | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C290h | SYSTEM | Reset Status Register 0 | RSTSR0 | 8 | 8 | 4 or 5 | PCLKB |
| 0008 C291h | SYSTEM | Reset Status Register 1 | RSTSR1 | 8 | 8 | 4 or 5 | PCLKB |
| 0008 C293h | SYSTEM | Main Clock Oscillator Forced Oscillation Control Register | MOFCR | 8 | 8 | 4 or 5 | PCLKB |
| 0008 C297h | SYSTEM | Voltage Monitoring Circuit Control Register | LVCMPCR | 8 | 8 | 4 or 5 | PCLKB |
| 0008 C298h | SYSTEM | Voltage Detection Level Select Register | LVDLVL | 8 | 8 | 4 or 5 | PCLKB |
| 0008 C29Ah | SYSTEM | Voltage Monitoring 1 Circuit Control Register 0 | LVD1CR0 | 8 | 8 | 4 or 5 | PCLKB |
| 0008 C29Bh | SYSTEM | Voltage Monitoring 2 Circuit Control Register 0 | LVD2CR0 | 8 | 8 | 4 or 5 | PCLKB |
| 0008 C4C0h | POE | Input Level Control/Status Register 1 | ICSR1 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4C2h | POE | Output Level Control/Status Register 1 | OCSR1 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4C4h | POE | Input Level Control/Status Register 2 | ICSR2 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4C6h | POE | Output Level Control/Status Register 2 | OCSR2 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4C8h | POE | Input Level Control/Status Register 3 | ICSR3 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4CAh | POE | Software Port Output Enable Register | SPOER | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C4CBh | POE | Port Output Enable Control Register 1 | POECR1 | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C4CCh | POE | Port Output Enable Control Register 2 | POECR2 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4CEh | POE | Port Output Enable Control Register 3*2 | POECR3 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4D0h | POE | Port Output Enable Control Register 4 | POECR4 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4D2h | POE | Port Output Enable Control Register 5 | POECR5 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4D4h | POE | Port Output Enable Control Register 6*2 | POECR6 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4D6h | POE | Input Level Control/Status Register 4 | ICSR4 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4D8h | POE | Input Level Control/Status Register 5 | ICSR5 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4DAh | POE | Active Level Setting Register 1 | ALR1 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4DCh | POE | Input Level Control/Status Register 6 | ICSR6 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4DEh | POE | Active Level Setting Register 2 | ALR2 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4E0h | POE | Input Level Control/Status Register 7 | ICSR7 | 16 | 8, 16 | 2 or 3 | PCLKB |
| 0008 C4E2h | POE | Port Output Enable Control Register 7 | POECR7 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4E4h | POE | Port Output Enable Control Register 8 | POECR8 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4E6h | POE | Port Output Enable Comparator Output Detection Flag Register | POECMPFR | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4E8h | POE | Port Output Enable Comparator Request Select Register | POECMPSEL | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4F0h | POE | Port Mode Mask Control Register 0*2 | PMMCR0 | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C4F2h | POE | Port Mode Mask Control Register 1*2 | PMMCR1 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4F4h | POE | Port Mode Mask Control Register 2*2 | PMMCR2 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4F6h | POE | Port Mode Mask Control Register 3*2 | PMMCR3 | 16 | 16 | 2 or 3 | PCLKB |
| 0008 C4F8h | POE | Port Output Enable Comparator Request Extended Selection Register 0*2 | POECMPX0 | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C4F9h | POE | Port Output Enable Comparator Request Extended Selection Register 1*2 | POECMPX1 | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C4FAh | POE | Port Output Enable Comparator Request Extended Selection Register 2*2 | POECMPX2 | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C4FCh | POE | Port Output Enable Comparator Request Extended Selection Register 4*2 | POECMPX4 | 8 | 8 | 2 or 3 | PCLKB |
| 0008 C4FDh | POE | Port Output Enable Comparator Request Extended Selection Register 5*2 | POECMPX5 | 8 | 8 | 2 or 3 | PCLKB |
| 000A 0C80h | CMPC0 | Comparator Control Register 0 | CMPCTL | 8 | 8 | 1 or 2 | PCLKB |
| 000A 0C84h | CMPC0 | Comparator Input Select Register 0 | CMPSEL0 | 8 | 8 | 1 or 2 | PCLKB |
| 000A 0C88h | CMPC0 | Comparator Reference Voltage Select Register 0 | CMPSEL1 | 8 | 8 | 1 or 2 | PCLKB |
| 000A 0C8Ch | CMPC0 | Comparator Output Monitor Register 0 | CMPMON | 8 | 8 | 1 or 2 | PCLKB |
| 000A 0C90h | CMPC0 | Comparator External Output Enable Register 0 | CMPIOC | 8 | 8 | 1 or 2 | PCLKB |

Table 4.1 List of I/O Registers (Address Order) (21/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|-------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 000A 0CA0h | CMPC1 | Comparator Control Register 1 | CMPCTL | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CA4h | CMPC1 | Comparator Input Select Register 1 | CMPSEL0 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CA8h | CMPC1 | Comparator Reference Voltage Select Register 1 | CMPSEL1 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CACH | CMPC1 | Comparator Output Monitor Register 1 | CMPMON | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CB0h | CMPC1 | Comparator External Output Enable Register 1 | CMPIOC | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CC0h | CMPC2 | Comparator Control Register 2 | CMPCTL | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CC4h | CMPC2 | Comparator Input Select Register 2 | CMPSEL0 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CC8h | CMPC2 | Comparator Reference Voltage Select Register 2 | CMPSEL1 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CCCCh | CMPC2 | Comparator Output Monitor Register 2 | CMPMON | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CD0h | CMPC2 | Comparator External Output Enable Register 2 | CMPIOC | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CE0h | CMPC3 | Comparator Control Register 3 | CMPCTL | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CE4h | CMPC3 | Comparator Input Select Register 3 | CMPSEL0 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CE8h | CMPC3 | Comparator Reference Voltage Select Register 3 | CMPSEL1 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CECh | CMPC3 | Comparator Output Monitor Register 3 | CMPMON | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CF0h | CMPC3 | Comparator External Output Enable Register 3 | CMPIOC | 8 | 8 | 1 or 2 PCLKB |
| 000A 8300h | RSCAN0 | Bit Configuration Register L*2 | CFGL | 16 | 16 | 2 or 3 PCLKB |
| 000A 8302h | RSCAN0 | Bit Configuration Register H*2 | CFGH | 16 | 16 | 2 or 3 PCLKB |
| 000A 8304h | RSCAN0 | Control Register L*2 | CTRL | 16 | 16 | 2 or 3 PCLKB |
| 000A 8306h | RSCAN0 | Control Register H*2 | CTRH | 16 | 16 | 2 or 3 PCLKB |
| 000A 8308h | RSCAN0 | Status Register L*2 | STSL | 16 | 16 | 2 or 3 PCLKB |
| 000A 830Ah | RSCAN0 | Status Register H*2 | STSH | 16 | 16 | 2 or 3 PCLKB |
| 000A 830Ch | RSCAN0 | Error Flag Register L*2 | ERFLL | 16 | 16 | 2 or 3 PCLKB |
| 000A 830Eh | RSCAN0 | Error Flag Register H*2 | ERFLH | 16 | 16 | 2 or 3 PCLKB |
| 000A 8322h | RSCAN | Global Configuration Register L*2 | GCFGL | 16 | 16 | 2 or 3 PCLKB |
| 000A 8324h | RSCAN | Global Configuration Register H*2 | GCFGH | 16 | 16 | 2 or 3 PCLKB |
| 000A 8326h | RSCAN | Global Control Register L*2 | GCTRL | 16 | 16 | 2 or 3 PCLKB |
| 000A 8328h | RSCAN | Global Control Register H*2 | GCTRH | 16 | 16 | 2 or 3 PCLKB |
| 000A 832Ah | RSCAN | Global Status Register*2 | GSTS | 16 | 16 | 2 or 3 PCLKB |
| 000A 832Ch | RSCAN | Global Error Flag Register*2 | GERFLL | 8 | 8 | 1 or 2 PCLKB |
| 000A 832Eh | RSCAN | Timestamp Register*2 | GTSC | 16 | 16 | 2 or 3 PCLKB |
| 000A 8330h | RSCAN | Receive Rule Number Configuration Register*2 | GAFLCFG | 16 | 16 | 2 or 3 PCLKB |
| 000A 8332h | RSCAN | Receive Buffer Number Configuration Register*2 | RMNB | 16 | 16 | 2 or 3 PCLKB |
| 000A 8334h | RSCAN | Receive Buffer Receive Complete Flag Register*2 | RMND0 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8338h | RSCAN | Receive FIFO Control Register 0*2 | RFCC0 | 16 | 16 | 2 or 3 PCLKB |
| 000A 833Ah | RSCAN | Receive FIFO Control Register 1*2 | RFCC1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8340h | RSCAN | Receive FIFO Status Register 0*2 | RFSTS0 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8342h | RSCAN | Receive FIFO Status Register 1*2 | RFSTS1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8348h | RSCAN | Receive FIFO Pointer Control Register 0*2 | RFPCTR0 | 16 | 16 | 2 or 3 PCLKB |
| 000A 834Ah | RSCAN | Receive FIFO Pointer Control Register 1*2 | RFPCTR1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8350h | RSCAN0 | Transmit/Receive FIFO Control Register 0L*2 | CFCCLO | 16 | 16 | 2 or 3 PCLKB |
| 000A 8352h | RSCAN0 | Transmit/Receive FIFO Control Register 0H*2 | CFCCHO | 16 | 16 | 2 or 3 PCLKB |
| 000A 8358h | RSCAN0 | Transmit/Receive FIFO Status Register 0*2 | CFSTS0 | 16 | 16 | 2 or 3 PCLKB |
| 000A 835Ch | RSCAN0 | Transmit/Receive FIFO Pointer Control Register 0*2 | CFPCTR0 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8360h | RSCAN | Receive FIFO Message Lost Status Register*2 | RFMSTS | 8 | 8 | 1 or 2 PCLKB |
| 000A 8361h | RSCAN0 | Transmit/Receive FIFO Message Lost Status Register*2 | CFMSTS | 8 | 8 | 1 or 2 PCLKB |
| 000A 8362h | RSCAN | Receive FIFO Interrupt Status Register*2 | RFISTS | 8 | 8 | 1 or 2 PCLKB |
| 000A 8363h | RSCAN | Transmit/Receive FIFO Receive Interrupt Status Register*2 | CFISTS | 8 | 8 | 1 or 2 PCLKB |
| 000A 8364h | RSCAN0 | Transmit Buffer Control Register 0*2 | TMC0 | 8 | 8 | 1 or 2 PCLKB |
| 000A 8365h | RSCAN0 | Transmit Buffer Control Register 1*2 | TMC1 | 8 | 8 | 1 or 2 PCLKB |
| 000A 8366h | RSCAN0 | Transmit Buffer Control Register 2*2 | TMC2 | 8 | 8 | 1 or 2 PCLKB |
| 000A 8367h | RSCAN0 | Transmit Buffer Control Register 3*2 | TMC3 | 8 | 8 | 1 or 2 PCLKB |
| 000A 836Ch | RSCAN0 | Transmit Buffer Status Register 0*2 | TMSTS0 | 8 | 8 | 1 or 2 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (22/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 000A 836Dh | RSCAN0 | Transmit Buffer Status Register 1*2 | TMSTS1 | 8 | 8 | | 1 or 2 PCLKB |
| 000A 836Eh | RSCAN0 | Transmit Buffer Status Register 2*2 | TMSTS2 | 8 | 8 | | 1 or 2 PCLKB |
| 000A 836Fh | RSCAN0 | Transmit Buffer Status Register 3*2 | TMSTS3 | 8 | 8 | | 1 or 2 PCLKB |
| 000A 8374h | RSCAN0 | Transmit Buffer Transmit Request Status Register*2 | TMTRSTS | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8376h | RSCAN0 | Transmit Buffer Transmit Complete Status Register*2 | TMTCSTS | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8378h | RSCAN0 | Transmit Buffer Transmit Abort Status Register*2 | TMTASTS | 16 | 16 | | 2 or 3 PCLKB |
| 000A 837Ah | RSCAN0 | Transmit Buffer Interrupt Enable Register*2 | TMIEC | 16 | 16 | | 2 or 3 PCLKB |
| 000A 837Ch | RSCAN0 | Transmit History Buffer Control Register*2 | THLCC0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8380h | RSCAN0 | Transmit History Buffer Status Register*2 | THLSTS0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8384h | RSCAN0 | Transmit History Buffer Pointer Control Register*2 | THLPCTR0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8388h | RSCAN | Global Transmit Interrupt Status Register*2 | GTINTSTS | 16 | 16 | | 2 or 3 PCLKB |
| 000A 838Ah | RSCAN | Global RAM Window Control Register*2 | GRWCR | 16 | 16 | | 2 or 3 PCLKB |
| 000A 838Ch | RSCAN | Global Test Configuration Register*2 | GTSTCFG | 16 | 16 | | 2 or 3 PCLKB |
| 000A 838Eh | RSCAN | Global Test Control Register*2 | GTSTCTRL | 8 | 8 | | 1 or 2 PCLKB |
| 000A 8394h | RSCAN | Global Test Protection Unlock Register*2 | GLOCKK | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A0h | RSCAN | Receive Rule Entry Register 0AL*2 | GAFLIDL0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A0h | RSCAN | Receive Buffer Register 0AL*2 | RMIDL0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A2h | RSCAN | Receive Rule Entry Register 0AH*2 | GAFLIDH0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A2h | RSCAN | Receive Buffer Register 0AH*2 | RMIDH0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A4h | RSCAN | Receive Rule Entry Register 0BL*2 | GAFLML0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A4h | RSCAN | Receive Buffer Register 0BL*2 | RMTS0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A6h | RSCAN | Receive Rule Entry Register 0BH*2 | GAFLMH0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A6h | RSCAN | Receive Buffer Register 0BH*2 | RMPTR0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A8h | RSCAN | Receive Rule Entry Register 0CL*2 | GAFLPL0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83A8h | RSCAN | Receive Buffer Register 0CL*2 | RMDF00 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83AAh | RSCAN | Receive Rule Entry Register 0CH*2 | GAFLPH0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83AAh | RSCAN | Receive Buffer Register 0CH*2 | RMDF10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83ACh | RSCAN | Receive Rule Entry Register 1AL*2 | GAFLIDL1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83ACh | RSCAN | Receive Buffer Register 0DL*2 | RMDF20 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83AEh | RSCAN | Receive Rule Entry Register 1AH*2 | GAFLIDH1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83AEh | RSCAN | Receive Buffer Register 0DH*2 | RMDF30 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B0h | RSCAN | Receive Rule Entry Register 1BL*2 | GAFLML1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B0h | RSCAN | Receive Buffer Register 1AL*2 | RMIDL1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B2h | RSCAN | Receive Rule Entry Register 1BH*2 | GAFLMH1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B2h | RSCAN | Receive Buffer Register 1AH*2 | RMIDH1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B4h | RSCAN | Receive Rule Entry Register 1CL*2 | GAFLPL1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B4h | RSCAN | Receive Buffer Register 1BL*2 | RMTS1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B6h | RSCAN | Receive Rule Entry Register 1CH*2 | GAFLPH1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B6h | RSCAN | Receive Buffer Register 1BH*2 | RMPTR1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B8h | RSCAN | Receive Rule Entry Register 2AL*2 | GAFLIDL2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83B8h | RSCAN | Receive Buffer Register 1CL*2 | RMDF01 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83BAh | RSCAN | Receive Rule Entry Register 2AH*2 | GAFLIDH2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83BAh | RSCAN | Receive Buffer Register 1CH*2 | RMDF11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83BCh | RSCAN | Receive Rule Entry Register 2BL*2 | GAFLML2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83BCh | RSCAN | Receive Buffer Register 1DL*2 | RMDF21 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83BEh | RSCAN | Receive Rule Entry Register 2BH*2 | GAFLMH2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83BEh | RSCAN | Receive Buffer Register 1DH*2 | RMDF31 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C0h | RSCAN | Receive Rule Entry Register 2CL*2 | GAFLPL2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C0h | RSCAN | Receive Buffer Register 2AL*2 | RMIDL2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C2h | RSCAN | Receive Rule Entry Register 2CH*2 | GAFLPH2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C2h | RSCAN | Receive Buffer Register 2AH*2 | RMIDH2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C4h | RSCAN | Receive Rule Entry Register 3AL*2 | GAFLIDL3 | 16 | 16 | | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (23/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 000A 83C4h | RSCAN | Receive Buffer Register 2BL*2 | RMTS2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C6h | RSCAN | Receive Rule Entry Register 3AH*2 | GAFLIDH3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C6h | RSCAN | Receive Buffer Register 2BH*2 | RMPTR2 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C8h | RSCAN | Receive Rule Entry Register 3BL*2 | GAFLML3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83C8h | RSCAN | Receive Buffer Register 2CL*2 | RMDF02 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83CAh | RSCAN | Receive Rule Entry Register 3BH*2 | GAFLMH3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83CAh | RSCAN | Receive Buffer Register 2CH*2 | RMDF12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83CCh | RSCAN | Receive Rule Entry Register 3CL*2 | GAFLPL3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83CCh | RSCAN | Receive Buffer Register 2DL*2 | RMDF22 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83CEh | RSCAN | Receive Rule Entry Register 3CH*2 | GAFLPH3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83CEh | RSCAN | Receive Buffer Register 2DH*2 | RMDF32 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D0h | RSCAN | Receive Rule Entry Register 4AL*2 | GAFLIDL4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D0h | RSCAN | Receive Buffer Register 3AL*2 | RMIDL3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D2h | RSCAN | Receive Rule Entry Register 4AH*2 | GAFLIDH4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D2h | RSCAN | Receive Buffer Register 3AH*2 | RMIDH3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D4h | RSCAN | Receive Rule Entry Register 4BL*2 | GAFLML4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D4h | RSCAN | Receive Buffer Register 3BL*2 | RMTS3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D6h | RSCAN | Receive Rule Entry Register 4BH*2 | GAFLMH4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D6h | RSCAN | Receive Buffer Register 3BH*2 | RMPTR3 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D8h | RSCAN | Receive Rule Entry Register 4CL*2 | GAFLPL4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83D8h | RSCAN | Receive Buffer Register 3CL*2 | RMDF03 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83DAh | RSCAN | Receive Rule Entry Register 4CH*2 | GAFLPH4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83DAh | RSCAN | Receive Buffer Register 3CH*2 | RMDF13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83DCh | RSCAN | Receive Rule Entry Register 5AL*2 | GAFLIDL5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83DCh | RSCAN | Receive Buffer Register 3DL*2 | RMDF23 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83DEh | RSCAN | Receive Rule Entry Register 5AH*2 | GAFLIDH5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83DEh | RSCAN | Receive Buffer Register 3DH*2 | RMDF33 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E0h | RSCAN | Receive Rule Entry Register 5BL*2 | GAFLML5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E0h | RSCAN | Receive Buffer Register 4AL*2 | RMIDL4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E2h | RSCAN | Receive Rule Entry Register 5BH*2 | GAFLMH5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E2h | RSCAN | Receive Buffer Register 4AH*2 | RMIDH4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E4h | RSCAN | Receive Rule Entry Register 5CL*2 | GAFLPL5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E4h | RSCAN | Receive Buffer Register 4BL*2 | RMTS4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E6h | RSCAN | Receive Rule Entry Register 5CH*2 | GAFLPH5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E6h | RSCAN | Receive Buffer Register 4BH*2 | RMPTR4 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E8h | RSCAN | Receive Rule Entry Register 6AL*2 | GAFLIDL6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83E8h | RSCAN | Receive Buffer Register 4CL*2 | RMDF04 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83EAh | RSCAN | Receive Rule Entry Register 6AH*2 | GAFLIDH6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83EAh | RSCAN | Receive Buffer Register 4CH*2 | RMDF14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83ECh | RSCAN | Receive Rule Entry Register 6BL*2 | GAFLML6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83ECh | RSCAN | Receive Buffer Register 4DL*2 | RMDF24 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83EEh | RSCAN | Receive Rule Entry Register 6BH*2 | GAFLMH6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83EEh | RSCAN | Receive Buffer Register 4DH*2 | RMDF34 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F0h | RSCAN | Receive Rule Entry Register 6CL*2 | GAFLPL6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F0h | RSCAN | Receive Buffer Register 5AL*2 | RMIDL5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F2h | RSCAN | Receive Rule Entry Register 6CH*2 | GAFLPH6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F2h | RSCAN | Receive Buffer Register 5AH*2 | RMIDH5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F4h | RSCAN | Receive Rule Entry Register 7AL*2 | GAFLIDL7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F4h | RSCAN | Receive Buffer Register 5BL*2 | RMTS5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F6h | RSCAN | Receive Rule Entry Register 7AH*2 | GAFLIDH7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F6h | RSCAN | Receive Buffer Register 5BH*2 | RMPTR5 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83F8h | RSCAN | Receive Rule Entry Register 7BL*2 | GAFLML7 | 16 | 16 | | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (24/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 000A 83F8h | RSCAN | Receive Buffer Register 5CL* ² | RMDF05 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83FAh | RSCAN | Receive Rule Entry Register 7BH* ² | GAFLMH7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83FAh | RSCAN | Receive Buffer Register 5CH* ² | RMDF15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83FCh | RSCAN | Receive Rule Entry Register 7CL* ² | GAFLPL7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83FCh | RSCAN | Receive Buffer Register 5DL* ² | RMDF25 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83FEh | RSCAN | Receive Rule Entry Register 7CH* ² | GAFLPH7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 83FEh | RSCAN | Receive Buffer Register 5DH* ² | RMDF35 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8400h | RSCAN | Receive Rule Entry Register 8AL* ² | GAFLIDL8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8400h | RSCAN | Receive Buffer Register 6AL* ² | RMIDL6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8402h | RSCAN | Receive Rule Entry Register 8AH* ² | GAFLIDH8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8402h | RSCAN | Receive Buffer Register 6AH* ² | RMIDH6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8404h | RSCAN | Receive Rule Entry Register 8BL* ² | GAFLML8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8404h | RSCAN | Receive Buffer Register 6BL* ² | RMTS6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8406h | RSCAN | Receive Rule Entry Register 8BH* ² | GAFLMH8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8406h | RSCAN | Receive Buffer Register 6BH* ² | RMPTR6 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8408h | RSCAN | Receive Rule Entry Register 8CL* ² | GAFLPL8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8408h | RSCAN | Receive Buffer Register 6CL* ² | RMDF06 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 840Ah | RSCAN | Receive Rule Entry Register 8CH* ² | GAFLPH8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 840Ah | RSCAN | Receive Buffer Register 6CH* ² | RMDF16 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 840Ch | RSCAN | Receive Rule Entry Register 9AL* ² | GAFLIDL9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 840Ch | RSCAN | Receive Buffer Register 6DL* ² | RMDF26 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 840Eh | RSCAN | Receive Rule Entry Register 9AH* ² | GAFLIDH9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 840Eh | RSCAN | Receive Buffer Register 6DH* ² | RMDF36 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8410h | RSCAN | Receive Rule Entry Register 9BL* ² | GAFLML9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8410h | RSCAN | Receive Buffer Register 7AL* ² | RMIDL7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8412h | RSCAN | Receive Rule Entry Register 9BH* ² | GAFLMH9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8412h | RSCAN | Receive Buffer Register 7AH* ² | RMIDH7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8414h | RSCAN | Receive Rule Entry Register 9CL* ² | GAFLPL9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8414h | RSCAN | Receive Buffer Register 7BL* ² | RMTS7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8416h | RSCAN | Receive Rule Entry Register 9CH* ² | GAFLPH9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8416h | RSCAN | Receive Buffer Register 7BH* ² | RMPTR7 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8418h | RSCAN | Receive Rule Entry Register 10AL* ² | GAFLIDL10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8418h | RSCAN | Receive Buffer Register 7CL* ² | RMDF07 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 841Ah | RSCAN | Receive Rule Entry Register 10AH* ² | GAFLIDH10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 841Ah | RSCAN | Receive Buffer Register 7CH* ² | RMDF17 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 841Ch | RSCAN | Receive Rule Entry Register 10BL* ² | GAFLML10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 841Ch | RSCAN | Receive Buffer Register 7DL* ² | RMDF27 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 841Eh | RSCAN | Receive Rule Entry Register 10BH* ² | GAFLMH10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 841Eh | RSCAN | Receive Buffer Register 7DH* ² | RMDF37 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8420h | RSCAN | Receive Rule Entry Register 10CL* ² | GAFLPL10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8420h | RSCAN | Receive Buffer Register 8AL* ² | RMIDL8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8422h | RSCAN | Receive Rule Entry Register 10CH* ² | GAFLPH10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8422h | RSCAN | Receive Buffer Register 8AH* ² | RMIDH8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8424h | RSCAN | Receive Rule Entry Register 11AL* ² | GAFLIDL11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8424h | RSCAN | Receive Buffer Register 8BL* ² | RMTS8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8426h | RSCAN | Receive Rule Entry Register 11AH* ² | GAFLIDH11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8426h | RSCAN | Receive Buffer Register 8BH* ² | RMPTR8 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8428h | RSCAN | Receive Rule Entry Register 11BL* ² | GAFLML11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8428h | RSCAN | Receive Buffer Register 8CL* ² | RMDF08 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 842Ah | RSCAN | Receive Rule Entry Register 11BH* ² | GAFLMH11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 842Ah | RSCAN | Receive Buffer Register 8CH* ² | RMDF18 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 842Ch | RSCAN | Receive Rule Entry Register 11CL* ² | GAFLPL11 | 16 | 16 | | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (25/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 000A 842Ch | RSCAN | Receive Buffer Register 8DL* ² | RMDF28 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 842Eh | RSCAN | Receive Rule Entry Register 11CH* ² | GAFLPH11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 842Eh | RSCAN | Receive Buffer Register 8DH* ² | RMDF38 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8430h | RSCAN | Receive Rule Entry Register 12AL* ² | GAFLIDL12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8430h | RSCAN | Receive Buffer Register 9AL* ² | RMIDL9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8432h | RSCAN | Receive Rule Entry Register 12AH* ² | GAFLIDH12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8432h | RSCAN | Receive Buffer Register 9AH* ² | RMIDH9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8434h | RSCAN | Receive Rule Entry Register 12BL* ² | GAFLML12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8434h | RSCAN | Receive Buffer Register 9BL* ² | RMTS9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8436h | RSCAN | Receive Rule Entry Register 12BH* ² | GAFLMH12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8436h | RSCAN | Receive Buffer Register 9BH* ² | RMPTR9 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8438h | RSCAN | Receive Rule Entry Register 12CL* ² | GAFLPL12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8438h | RSCAN | Receive Buffer Register 9CL* ² | RMDF09 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 843Ah | RSCAN | Receive Rule Entry Register 12CH* ² | GAFLPH12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 843Ah | RSCAN | Receive Buffer Register 9CH* ² | RMDF19 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 843Ch | RSCAN | Receive Rule Entry Register 13AL* ² | GAFLIDL13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 843Ch | RSCAN | Receive Buffer Register 9DL* ² | RMDF29 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 843Eh | RSCAN | Receive Rule Entry Register 13AH* ² | GAFLIDH13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 843Eh | RSCAN | Receive Buffer Register 9DH* ² | RMDF39 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8440h | RSCAN | Receive Rule Entry Register 13BL* ² | GAFLML13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8440h | RSCAN | Receive Buffer Register 10AL* ² | RMIDL10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8442h | RSCAN | Receive Rule Entry Register 13BH* ² | GAFLMH13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8442h | RSCAN | Receive Buffer Register 10AH* ² | RMIDH10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8444h | RSCAN | Receive Rule Entry Register 13CL* ² | GAFLPL13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8444h | RSCAN | Receive Buffer Register 10BL* ² | RMTS10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8446h | RSCAN | Receive Rule Entry Register 13CH* ² | GAFLPH13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8446h | RSCAN | Receive Buffer Register 10BH* ² | RMPTR10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8448h | RSCAN | Receive Rule Entry Register 14AL* ² | GAFLIDL14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8448h | RSCAN | Receive Buffer Register 10CL* ² | RMDF010 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 844Ah | RSCAN | Receive Rule Entry Register 14AH* ² | GAFLIDH14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 844Ah | RSCAN | Receive Buffer Register 10CH* ² | RMDF110 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 844Ch | RSCAN | Receive Rule Entry Register 14BL* ² | GAFLML14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 844Ch | RSCAN | Receive Buffer Register 10DL* ² | RMDF210 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 844Eh | RSCAN | Receive Rule Entry Register 14BH* ² | GAFLMH14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 844Eh | RSCAN | Receive Buffer Register 10DH* ² | RMDF310 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8450h | RSCAN | Receive Rule Entry Register 14CL* ² | GAFLPL14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8450h | RSCAN | Receive Buffer Register 11AL* ² | RMIDL11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8452h | RSCAN | Receive Rule Entry Register 14CH* ² | GAFLPH14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8452h | RSCAN | Receive Buffer Register 11AH* ² | RMIDH11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8454h | RSCAN | Receive Rule Entry Register 15AL* ² | GAFLIDL15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8454h | RSCAN | Receive Buffer Register 11BL* ² | RMTS11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8456h | RSCAN | Receive Rule Entry Register 15AH* ² | GAFLIDH15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8456h | RSCAN | Receive Buffer Register 11BH* ² | RMPTR11 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8458h | RSCAN | Receive Rule Entry Register 15BL* ² | GAFLML15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8458h | RSCAN | Receive Buffer Register 11CL* ² | RMDF011 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 845Ah | RSCAN | Receive Rule Entry Register 15BH* ² | GAFLMH15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 845Ah | RSCAN | Receive Buffer Register 11CH* ² | RMDF111 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 845Ch | RSCAN | Receive Rule Entry Register 15CL* ² | GAFLPL15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 845Ch | RSCAN | Receive Buffer Register 11DL* ² | RMDF211 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 845Eh | RSCAN | Receive Rule Entry Register 15CH* ² | GAFLPH15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 845Eh | RSCAN | Receive Buffer Register 11DH* ² | RMDF311 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8460h | RSCAN | Receive Buffer Register 12AL* ² | RMIDL12 | 16 | 16 | | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (26/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|--------------------------------|---------------|------------------------------------|------------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 000A 8462h | RSCAN | Receive Buffer Register 12AH*2 | RMIDH12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8464h | RSCAN | Receive Buffer Register 12BL*2 | RMTS12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8466h | RSCAN | Receive Buffer Register 12BH*2 | RMPTR12 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8468h | RSCAN | Receive Buffer Register 12CL*2 | RMDF012 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 846Ah | RSCAN | Receive Buffer Register 12CH*2 | RMDF112 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 846Ch | RSCAN | Receive Buffer Register 12DL*2 | RMDF212 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 846Eh | RSCAN | Receive Buffer Register 12DH*2 | RMDF312 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8470h | RSCAN | Receive Buffer Register 13AL*2 | RMIDL13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8472h | RSCAN | Receive Buffer Register 13AH*2 | RMIDH13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8474h | RSCAN | Receive Buffer Register 13BL*2 | RMTS13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8476h | RSCAN | Receive Buffer Register 13BH*2 | RMPTR13 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8478h | RSCAN | Receive Buffer Register 13CL*2 | RMDF013 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 847Ah | RSCAN | Receive Buffer Register 13CH*2 | RMDF113 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 847Ch | RSCAN | Receive Buffer Register 13DL*2 | RMDF213 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 847Eh | RSCAN | Receive Buffer Register 13DH*2 | RMDF313 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8480h | RSCAN | Receive Buffer Register 14AL*2 | RMIDL14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8482h | RSCAN | Receive Buffer Register 14AH*2 | RMIDH14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8484h | RSCAN | Receive Buffer Register 14BL*2 | RMTS14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8486h | RSCAN | Receive Buffer Register 14BH*2 | RMPTR14 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8488h | RSCAN | Receive Buffer Register 14CL*2 | RMDF014 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 848Ah | RSCAN | Receive Buffer Register 14CH*2 | RMDF114 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 848Ch | RSCAN | Receive Buffer Register 14DL*2 | RMDF214 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 848Eh | RSCAN | Receive Buffer Register 14DH*2 | RMDF314 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8490h | RSCAN | Receive Buffer Register 15AL*2 | RMIDL15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8492h | RSCAN | Receive Buffer Register 15AH*2 | RMIDH15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8494h | RSCAN | Receive Buffer Register 15BL*2 | RMTS15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8496h | RSCAN | Receive Buffer Register 15BH*2 | RMPTR15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8498h | RSCAN | Receive Buffer Register 15CL*2 | RMDF015 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 849Ah | RSCAN | Receive Buffer Register 15CH*2 | RMDF115 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 849Ch | RSCAN | Receive Buffer Register 15DL*2 | RMDF215 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 849Eh | RSCAN | Receive Buffer Register 15DH*2 | RMDF315 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8580h to 000A 859Fh | RSCAN | RAM Test Register 0 to 15*2 | RPGACC0 to 15 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A0h | RSCAN | Receive FIFO Access Register 0AL*2 | RFIDL0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A0h | RSCAN | RAM Test Register 16*2 | RPGACC16 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A2h | RSCAN | Receive FIFO Access Register 0AH*2 | RFIDH0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A2h | RSCAN | RAM Test Register 17*2 | RPGACC17 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A4h | RSCAN | Receive FIFO Access Register 0BL*2 | RFTS0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A4h | RSCAN | RAM Test Register 18*2 | RPGACC18 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A6h | RSCAN | Receive FIFO Access Register 0BH*2 | RFPTR0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A6h | RSCAN | RAM Test Register 19*2 | RPGACC19 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A8h | RSCAN | Receive FIFO Access Register 0CL*2 | RFDF00 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85A8h | RSCAN | RAM Test Register 20*2 | RPGACC20 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85AAh | RSCAN | Receive FIFO Access Register 0CH*2 | RFDF10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85AAh | RSCAN | RAM Test Register 21*2 | RPGACC21 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85ACh | RSCAN | Receive FIFO Access Register 0DL*2 | RFDF20 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85ACh | RSCAN | RAM Test Register 22*2 | RPGACC22 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85AEh | RSCAN | Receive FIFO Access Register 0DH*2 | RFDF30 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85AEh | RSCAN | RAM Test Register 23*2 | RPGACC23 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B0h | RSCAN | Receive FIFO Access Register 1AL*2 | RFIDL1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B0h | RSCAN | RAM Test Register 24*2 | RPGACC24 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B2h | RSCAN | Receive FIFO Access Register 1AH*2 | RFIDH1 | 16 | 16 | | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (27/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|--------------------------|---------------|---|-----------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 000A 85B2h | RSCAN | RAM Test Register 25*2 | RPGACC25 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B4h | RSCAN | Receive FIFO Access Register 1BL*2 | RFTS1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B4h | RSCAN | RAM Test Register 26*2 | RPGACC26 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B6h | RSCAN | Receive FIFO Access Register 1BH*2 | RFPTR1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B6h | RSCAN | RAM Test Register 27*2 | RPGACC27 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B8h | RSCAN | Receive FIFO Access Register 1CL*2 | RDF01 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85B8h | RSCAN | RAM Test Register 28*2 | RPGACC28 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85BAh | RSCAN | Receive FIFO Access Register 1CH*2 | RDF01 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85BAh | RSCAN | RAM Test Register 29*2 | RPGACC29 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85BCh | RSCAN | Receive FIFO Access Register 1DL*2 | RDF01 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85BCh | RSCAN | RAM Test Register 30*2 | RPGACC30 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85BEh | RSCAN | Receive FIFO Access Register 1DH*2 | RDF01 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85BEh | RSCAN | RAM Test Register 31*2 | RPGACC31 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85C0h to 000A 85DEh | RSCAN | RAM Test Register 32 to 47*2 | RPGACC32 to 47 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E0h | RSCAN0 | Transmit/Receive FIFO Access Register 0AL*2 | CFIDL0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E0h | RSCAN | RAM Test Register 48*2 | RPGACC48 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E2h | RSCAN0 | Transmit/Receive FIFO Access Register 0AH*2 | CFIDH0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E2h | RSCAN | RAM Test Register 49*2 | RPGACC49 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E4h | RSCAN0 | Transmit/Receive FIFO Access Register 0BL*2 | CFTS0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E4h | RSCAN | RAM Test Register 50*2 | RPGACC50 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E6h | RSCAN0 | Transmit/Receive FIFO Access Register 0BH*2 | CFPTR0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E6h | RSCAN | RAM Test Register 51*2 | RPGACC51 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E8h | RSCAN0 | Transmit/Receive FIFO Access Register 0CL*2 | CFDF00 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85E8h | RSCAN | RAM Test Register 52*2 | RPGACC52 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85EAh | RSCAN0 | Transmit/Receive FIFO Access Register 0CH*2 | CFDF10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85EAh | RSCAN | RAM Test Register 53*2 | RPGACC53 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85ECh | RSCAN0 | Transmit/Receive FIFO Access Register 0DL*2 | CFDF20 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85ECh | RSCAN | RAM Test Register 54*2 | RPGACC54 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85EEh | RSCAN0 | Transmit/Receive FIFO Access Register 0DH*2 | CFDF30 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85EEh | RSCAN | RAM Test Register 55*2 | RPGACC55 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 85F0h to 000A 85FEh | RSCAN | RAM Test Register 56 to 63*2 | RPGACC56 to 63 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8600h | RSCAN0 | Transmit Buffer Register 0AL*2 | TMIDL0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8600h | RSCAN | RAM Test Register 64*2 | RPGACC64 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8602h | RSCAN0 | Transmit Buffer Register 0AH*2 | TMIDH0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8602h | RSCAN | RAM Test Register 65*2 | RPGACC65 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8604h | RSCAN | RAM Test Register 66*2 | RPGACC66 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8606h | RSCAN0 | Transmit Buffer Register 0BH*2 | TMPTR0 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8606h | RSCAN | RAM Test Register 67*2 | RPGACC67 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8608h | RSCAN0 | Transmit Buffer Register 0CL*2 | TMDF00 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8608h | RSCAN | RAM Test Register 68*2 | RPGACC68 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 860Ah | RSCAN0 | Transmit Buffer Register 0CH*2 | TMDF10 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 860Ah | RSCAN | RAM Test Register 69*2 | RPGACC69 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 860Ch | RSCAN0 | Transmit Buffer Register 0DL*2 | TMDF20 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 860Ch | RSCAN | RAM Test Register 70*2 | RPGACC70 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 860Eh | RSCAN0 | Transmit Buffer Register 0DH*2 | TMDF30 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 860Eh | RSCAN | RAM Test Register 71*2 | RPGACC71 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8610h | RSCAN0 | Transmit Buffer Register 1AL*2 | TMIDL1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8610h | RSCAN | RAM Test Register 72*2 | RPGACC72 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8612h | RSCAN0 | Transmit Buffer Register 1AH*2 | TMIDH1 | 16 | 16 | | 2 or 3 PCLKB |
| 000A 8612h | RSCAN | RAM Test Register 73*2 | RPGACC73 | 16 | 16 | | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (28/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|--------------------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 000A 8614h | RSCAN | RAM Test Register 74*2 | RPGACC74 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8616h | RSCAN0 | Transmit Buffer Register 1BH*2 | TMPTTR1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8616h | RSCAN | RAM Test Register 75*2 | RPGACC75 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8618h | RSCAN0 | Transmit Buffer Register 1CL*2 | TMDf01 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8618h | RSCAN | RAM Test Register 76*2 | RPGACC76 | 16 | 16 | 2 or 3 PCLKB |
| 000A 861Ah | RSCAN0 | Transmit Buffer Register 1CH*2 | TMDf11 | 16 | 16 | 2 or 3 PCLKB |
| 000A 861Ah | RSCAN | RAM Test Register 77*2 | RPGACC77 | 16 | 16 | 2 or 3 PCLKB |
| 000A 861Ch | RSCAN0 | Transmit Buffer Register 1DL*2 | TMDf21 | 16 | 16 | 2 or 3 PCLKB |
| 000A 861Ch | RSCAN | RAM Test Register 78*2 | RPGACC78 | 16 | 16 | 2 or 3 PCLKB |
| 000A 861Eh | RSCAN0 | Transmit Buffer Register 1DH*2 | TMDf31 | 16 | 16 | 2 or 3 PCLKB |
| 000A 861Eh | RSCAN | RAM Test Register 79*2 | RPGACC79 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8620h | RSCAN0 | Transmit Buffer Register 2AL*2 | TMIDL2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8620h | RSCAN | RAM Test Register 80*2 | RPGACC80 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8622h | RSCAN0 | Transmit Buffer Register 2AH*2 | TMIDH2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8622h | RSCAN | RAM Test Register 81*2 | RPGACC81 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8624h | RSCAN | RAM Test Register 82*2 | RPGACC82 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8626h | RSCAN0 | Transmit Buffer Register 2BH*2 | TMPTTR2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8626h | RSCAN | RAM Test Register 83*2 | RPGACC83 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8628h | RSCAN0 | Transmit Buffer Register 2CL*2 | TMDf02 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8628h | RSCAN | RAM Test Register 84*2 | RPGACC84 | 16 | 16 | 2 or 3 PCLKB |
| 000A 862Ah | RSCAN0 | Transmit Buffer Register 2CH*2 | TMDf12 | 16 | 16 | 2 or 3 PCLKB |
| 000A 862Ah | RSCAN | RAM Test Register 85*2 | RPGACC85 | 16 | 16 | 2 or 3 PCLKB |
| 000A 862Ch | RSCAN0 | Transmit Buffer Register 2DL*2 | TMDf22 | 16 | 16 | 2 or 3 PCLKB |
| 000A 862Ch | RSCAN | RAM Test Register 86*2 | RPGACC86 | 16 | 16 | 2 or 3 PCLKB |
| 000A 862Eh | RSCAN0 | Transmit Buffer Register 2DH*2 | TMDf32 | 16 | 16 | 2 or 3 PCLKB |
| 000A 862Eh | RSCAN | RAM Test Register 87*2 | RPGACC87 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8630h | RSCAN0 | Transmit Buffer Register 3AL*2 | TMIDL3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8630h | RSCAN | RAM Test Register 88*2 | RPGACC88 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8632h | RSCAN0 | Transmit Buffer Register 3AH*2 | TMIDH3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8632h | RSCAN | RAM Test Register 89*2 | RPGACC89 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8634h | RSCAN | RAM Test Register 90*2 | RPGACC90 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8636h | RSCAN0 | Transmit Buffer Register 3BH*2 | TMPTTR3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8636h | RSCAN | RAM Test Register 91*2 | RPGACC91 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8638h | RSCAN0 | Transmit Buffer Register 3CL*2 | TMDf03 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8638h | RSCAN | RAM Test Register 92*2 | RPGACC92 | 16 | 16 | 2 or 3 PCLKB |
| 000A 863Ah | RSCAN0 | Transmit Buffer Register 3CH*2 | TMDf13 | 16 | 16 | 2 or 3 PCLKB |
| 000A 863Ah | RSCAN | RAM Test Register 93*2 | RPGACC93 | 16 | 16 | 2 or 3 PCLKB |
| 000A 863Ch | RSCAN0 | Transmit Buffer Register 3DL*2 | TMDf23 | 16 | 16 | 2 or 3 PCLKB |
| 000A 863Ch | RSCAN | RAM Test Register 94*2 | RPGACC94 | 16 | 16 | 2 or 3 PCLKB |
| 000A 863Eh | RSCAN0 | Transmit Buffer Register 3DH*2 | TMDf33 | 16 | 16 | 2 or 3 PCLKB |
| 000A 863Eh | RSCAN | RAM Test Register 95*2 | RPGACC95 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8640h to 000A 867Eh | RSCAN | RAM Test Register 96 to 127*2 | RPGACC96 to 127 | 16 | 16 | 2 or 3 PCLKB |
| 000A 8680h | RSCAN0 | Transmit History Buffer Access Register*2 | THLACC0 | 16 | 16 | 2 or 3 PCLKB |
| 000C 1200h | MTU3 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1201h | MTU4 | Timer Control Register | TCR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1202h | MTU3 | Timer Mode Register 1 | TMDR1 | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1203h | MTU4 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1204h | MTU3 | Timer I/O Control Register H | TIORH | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1205h | MTU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1206h | MTU4 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1207h | MTU4 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |

Table 4.1 List of I/O Registers (Address Order) (29/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 000C 1208h | MTU3 | Timer Interrupt Enable Register | TIER | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1209h | MTU4 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 or 5 PCLKA |
| 000C 120Ah | MTU | Timer Output Master Enable Register A | TOERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 120Dh | MTU | Timer Gate Control Register | TGCRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 120Eh | MTU | Timer Output Control Register 1A | TOCR1A | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 120Fh | MTU | Timer Output Control Register 2A | TOCR2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1210h | MTU3 | Timer Counter | TCNT | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1212h | MTU4 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1214h | MTU | Timer Period Data Register A | TCDRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1216h | MTU | Timer Dead Time Data Register A | TDDRA | 16 | 16 | 4 or 5 PCLKA |
| 000C 1218h | MTU3 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 121Ah | MTU3 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 121Ch | MTU4 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 121Eh | MTU4 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1220h | MTU | Timer Subcounters A | TCNTSA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1222h | MTU | Timer Period Buffer Register A | TCBRA | 16 | 16 | 4 or 5 PCLKA |
| 000C 1224h | MTU3 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1226h | MTU3 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 1228h | MTU4 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 122Ah | MTU4 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 122Ch | MTU3 | Timer Status Register | TSR | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 122Dh | MTU4 | Timer Status Register | TSR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1230h | MTU | Timer Interrupt Skipping Set Register 1A | TITCR1A | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1231h | MTU | Timer Interrupt Skipping Counters 1A | TITCNT1A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1232h | MTU | Timer Buffer Transfer Set Register A | TBTERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1234h | MTU | Timer Dead Time Enable Register A | TDERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1236h | MTU | Timer Output Level Buffer Register A | TOLBRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1238h | MTU3 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1239h | MTU4 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 or 5 PCLKA |
| 000C 123Ah | MTU | Timer Interrupt Skipping Mode Register A | TITMRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 123Bh | MTU | Timer Interrupt Skipping Set Register 2A | TITCR2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 123Ch | MTU | Timer Interrupt Skipping Counters 2A | TITCNT2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1240h | MTU4 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4 or 5 PCLKA |
| 000C 1244h | MTU4 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1246h | MTU4 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1248h | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 124Ah | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 124Ch | MTU3 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 124Dh | MTU4 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1260h | MTU | Timer Waveform Control Register A | TWCRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1270h | MTU | Timer Mode Register 2A | TMDR2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1272h | MTU3 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1274h | MTU4 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1276h | MTU4 | Timer General Register F | TGRF | 16 | 16 | 4 or 5 PCLKA |
| 000C 1280h | MTU | Timer Start Register A | TSTRA | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1281h | MTU | Timer Synchronous Register A | TSYRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1282h | MTU | Timer Counter Synchronous Start Register | TCSYSTR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1284h | MTU | Timer Read/Write Enable Register A | TRWERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1290h | MTU0 | Noise Filter Control Register 0 | NFCR0 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1291h | MTU1 | Noise Filter Control Register 1 | NFCR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1292h | MTU2 | Noise Filter Control Register 2 | NFCR2 | 8 | 8 | 4 or 5 PCLKA |

Table 4.1 List of I/O Registers (Address Order) (30/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 000C 1293h | MTU3 | Noise Filter Control Register 3 | NFCR3 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1294h | MTU4 | Noise Filter Control Register 4 | NFCR4 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1296h | MTU9 | Noise Filter Control Register 9 | NFCR9 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1299h | MTU0 | Noise Filter Control Register C | NFCRC | 8 | 8 | 4 or 5 PCLKA |
| 000C 1300h | MTU0 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1301h | MTU0 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1302h | MTU0 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1303h | MTU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1304h | MTU0 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1306h | MTU0 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1308h | MTU0 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 130Ah | MTU0 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 130Ch | MTU0 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 130Eh | MTU0 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 1320h | MTU0 | Timer General Register E | TGRE | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 4 or 5 PCLKA |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 or 5 PCLKA |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 4 or 5 PCLKA |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 4 or 5 PCLKA |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 4 or 5 PCLKA |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1405h | MTU2 | Timer Status Register | TSR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1406h | MTU2 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1408h | MTU2 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 140Ah | MTU2 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 140Ch | MTU2 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1580h | MTU9 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1581h | MTU9 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1582h | MTU9 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1583h | MTU9 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1584h | MTU9 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1586h | MTU9 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1588h | MTU9 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 158Ah | MTU9 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 158Ch | MTU9 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 158Eh | MTU9 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |

Table 4.1 List of I/O Registers (Address Order) (31/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 000C 15A0h | MTU9 | Timer General Register E | TGRE | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 15A2h | MTU9 | Timer General Register F | TGRF | 16 | 16 | 4 or 5 PCLKA |
| 000C 15A4h | MTU9 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 15A6h | MTU9 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 or 5 PCLKA |
| 000C 15A8h | MTU9 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A00h | MTU6 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1A01h | MTU7 | Timer Control Register | TCR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A02h | MTU6 | Timer Mode Register 1 | TMDR1 | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A03h | MTU7 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A04h | MTU6 | Timer I/O Control Register H | TIORH | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1A05h | MTU6 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A06h | MTU7 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A07h | MTU7 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A08h | MTU6 | Timer Interrupt Enable Register | TIER | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A09h | MTU7 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A0Ah | MTU | Timer Output Master Enable Register B | TOERB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A0Dh | MTU | Timer Gate Control Register | TGCRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A0Eh | MTU | Timer Output Control Register 1B | TOCR1B | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A0Fh | MTU | Timer Output Control Register 2B | TOCR2B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A10h | MTU6 | Timer Counter | TCNT | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A12h | MTU7 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A14h | MTU | Timer Period Data Register B | TCDRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A16h | MTU | Timer Dead Time Data Register B | TDDRb | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A18h | MTU6 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A1Ah | MTU6 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A1Ch | MTU7 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A1Eh | MTU7 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A20h | MTU | Timer Subcounters B | TCNTSB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A22h | MTU | Timer Period Buffer Register B | TCBRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A24h | MTU6 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A26h | MTU6 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A28h | MTU7 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A2Ah | MTU7 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A2Ch | MTU6 | Timer Status Register | TSR | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A2Dh | MTU7 | Timer Status Register | TSR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A30h | MTU | Timer Interrupt Skipping Set Register 1B | TITCR1B | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A31h | MTU | Timer Interrupt Skipping Counters 1B | TITCNT1B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A32h | MTU | Timer Buffer Transfer Set Register B | TBTERB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A34h | MTU | Timer Dead Time Enable Register B | TDERB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A36h | MTU | Timer Output Level Buffer Register B | TOLBRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A38h | MTU6 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A39h | MTU7 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A3Ah | MTU | Timer Interrupt Skipping Mode Register B | TITMRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A3Bh | MTU | Timer Interrupt Skipping Set Register 2B | TITCR2B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A3Ch | MTU | Timer Interrupt Skipping Counters 2B | TITCNT2B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A40h | MTU7 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A44h | MTU7 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A46h | MTU7 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A48h | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A4Ah | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A4Ch | MTU6 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |

Table 4.1 List of I/O Registers (Address Order) (32/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 000C 1A4Dh | MTU7 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A50h | MTU6 | Timer Synchronous Clear Register | TSYCR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A60h | MTU | Timer Waveform Control Register B | TWCRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A70h | MTU | Timer Mode Register 2B | TMDR2B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A72h | MTU6 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A74h | MTU7 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A76h | MTU7 | Timer General Register F | TGRF | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A80h | MTU | Timer Start Register B | TSTRB | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A81h | MTU | Timer Synchronous Register B | TSYRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A84h | MTU | Timer Read/Write Enable Register B | TRWERB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A93h | MTU6 | Noise Filter Control Register 6 | NFCR6 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A94h | MTU7 | Noise Filter Control Register 7 | NFCR7 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A95h | MTU5 | Noise Filter Control Register 5 | NFCR5 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C80h | MTU5 | Timer Counter U | TCNTU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1C82h | MTU5 | Timer General Register U | TGRU | 16 | 16 | 4 or 5 PCLKA |
| 000C 1C84h | MTU5 | Timer Control Register U | TCRU | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C85h | MTU5 | Timer Control Register 2U | TCR2U | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C86h | MTU5 | Timer I/O Control Register U | TIORU | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C90h | MTU5 | Timer Counter V | TCNTV | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1C92h | MTU5 | Timer General Register V | TGRV | 16 | 16 | 4 or 5 PCLKA |
| 000C 1C94h | MTU5 | Timer Control Register V | TCRV | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C95h | MTU5 | Timer Control Register 2V | TCR2V | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C96h | MTU5 | Timer I/O Control Register V | TIORV | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CA0h | MTU5 | Timer Counter W | TCNTW | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1CA2h | MTU5 | Timer General Register W | TGRW | 16 | 16 | 4 or 5 PCLKA |
| 000C 1CA4h | MTU5 | Timer Control Register W | TCRW | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CA5h | MTU5 | Timer Control Register 2W | TCR2W | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CA6h | MTU5 | Timer I/O Control Register W | TIORW | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CB2h | MTU5 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CB4h | MTU5 | Timer Start Register | TSTR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CB6h | MTU5 | Timer Compare Match Clear Register | TCNTCMPCLR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1D30h | MTU | A/D Conversion Start Request Select Register 0 | TADSTRGR0 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1D32h | MTU | A/D Conversion Start Request Select Register 1 | TADSTRGR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 2000h | GPT | General PWM Timer Software Start Register*2 | GTSTR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2002h | GPT | Noise Filter Control Register*2 | NFCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2004h | GPT | General PWM Timer Hardware Source Start/Stop Control Register 0*2 | GTHSCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2006h | GPT | General PWM Timer Hardware Source Clear Control Register*2 | GTHCCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2008h | GPT | General PWM Timer Hardware Start Source Select Register*2 | GTHSSR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 200Ah | GPT | General PWM Timer Hardware Stop/Clear Source Select Register*2 | GTHPSR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 200Ch | GPT | General PWM Timer Write-Protection Register*2 | GTWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 200Eh | GPT | General PWM Timer Sync Register*2 | GTSYNC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2010h | GPT | General PWM Timer External Trigger Input Interrupt Register*2 | GTETINT | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2014h | GPT | General PWM Timer Buffer Operation Disable Register*2 | GTBDR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2018h | GPT | General PWM Timer Start Write-Protection Register*2 | GTSWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 201Ch | GPT | General PWM Timer Clearing Write-Protection Register*2 | GTCWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2020h | GPT | General PWM Timer Common Register Write-Protection Register*2 | GTCMNWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2024h | GPT | General PWM Timer Mode Register*2 | GTMDR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2028h | GPT | General PWM Timer External Clock Noise Filter Control Register*2 | GTECNFCR | 32 | 8, 16, 32 | 4 or 5 PCLKA |

Table 4.1 List of I/O Registers (Address Order) (33/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 000C 202Ch | GPT | General PWM Timer A/D Conversion Start Request Signal Monitor Register*2 | GTADSMR | 32 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2100h | GPT0 | General PWM Timer I/O Control Register*2 | GTIOR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2102h | GPT0 | General PWM Timer Interrupt Output Setting Register*2 | GTINTAD | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2104h | GPT0 | General PWM Timer Control Register*2 | GTCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2106h | GPT0 | General PWM Timer Buffer Enable Register*2 | GTBER | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2108h | GPT0 | General PWM Timer Count Direction Register*2 | GTUDC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 210Ah | GPT0 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2 | GTITC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 210Ch | GPT0 | General PWM Timer Status Register*2 | GTST | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 210Eh | GPT0 | General PWM Timer Counter*2 | GTCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 2110h | GPT0 | General PWM Timer Compare Capture Register A*2 | GTCCRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2112h | GPT0 | General PWM Timer Compare Capture Register B*2 | GTCCRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2114h | GPT0 | General PWM Timer Compare Capture Register C*2 | GTCCRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2116h | GPT0 | General PWM Timer Compare Capture Register D*2 | GTCCRD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2118h | GPT0 | General PWM Timer Compare Capture Register E*2 | GTCCRE | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 211Ah | GPT0 | General PWM Timer Compare Capture Register F*2 | GTCCRF | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 211Ch | GPT0 | General PWM Timer Period Setting Register*2 | GTPR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 211Eh | GPT0 | General PWM Timer Period Setting Buffer Register*2 | GTPBR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2120h | GPT0 | General PWM Timer Period Setting Double Buffer Register*2 | GTPDBR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2124h | GPT0 | A/D Converter Start Request Timing Register A*2 | GTADTRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2126h | GPT0 | A/D Converter Start Request Timing Buffer Register A*2 | GTADTBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2128h | GPT0 | A/D Converter Start Request Timing Double Buffer Register A*2 | GTADTDBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 212Ch | GPT0 | A/D Converter Start Request Timing Register B*2 | GTADTRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 212Eh | GPT0 | A/D Converter Start Request Timing Buffer Register B*2 | GTADTBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2130h | GPT0 | A/D Converter Start Request Timing Double Buffer Register B*2 | GTADTDBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2134h | GPT0 | General PWM Timer Output Negate Control Register*2 | GTONCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2136h | GPT0 | General PWM Timer Dead Time Control Register*2 | GTDTCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2138h | GPT0 | General PWM Timer Dead Time Value Register U*2 | GTDVU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 213Ah | GPT0 | General PWM Timer Dead Time Value Register D*2 | GTDVD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 213Ch | GPT0 | General PWM Timer Dead Time Buffer Register U*2 | GTDBU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 213Eh | GPT0 | General PWM Timer Dead Time Buffer Register D*2 | GTDBD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2140h | GPT0 | General PWM Timer Output Protection Function Status Register*2 | GTSOS | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2142h | GPT0 | General PWM Timer Output Protection Function Temporary Release Register*2 | GTSOTR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2180h | GPT1 | General PWM Timer I/O Control Register*2 | GTIOR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2182h | GPT1 | General PWM Timer Interrupt Output Setting Register*2 | GTINTAD | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2184h | GPT1 | General PWM Timer Control Register*2 | GTCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2186h | GPT1 | General PWM Timer Buffer Enable Register*2 | GTBER | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2188h | GPT1 | General PWM Timer Count Direction Register*2 | GTUDC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 218Ah | GPT1 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2 | GTITC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 218Ch | GPT1 | General PWM Timer Status Register*2 | GTST | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 218Eh | GPT1 | General PWM Timer Counter*2 | GTCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 2190h | GPT1 | General PWM Timer Compare Capture Register A*2 | GTCCRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2192h | GPT1 | General PWM Timer Compare Capture Register B*2 | GTCCRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2194h | GPT1 | General PWM Timer Compare Capture Register C*2 | GTCCRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2196h | GPT1 | General PWM Timer Compare Capture Register D*2 | GTCCRD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2198h | GPT1 | General PWM Timer Compare Capture Register E*2 | GTCCRE | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 219Ah | GPT1 | General PWM Timer Compare Capture Register F*2 | GTCCRF | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 219Ch | GPT1 | General PWM Timer Period Setting Register*2 | GTPR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 219Eh | GPT1 | General PWM Timer Period Setting Buffer Register*2 | GTPBR | 16 | 16, 32 | 4 or 5 PCLKA |

Table 4.1 List of I/O Registers (Address Order) (34/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------|
| | | | | | | ICLK ≥ PCLK | |
| 000C 21A0h | GPT1 | General PWM Timer Period Setting Double Buffer Register*2 | GTPDBR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21A4h | GPT1 | A/D Converter Start Request Timing Register A*2 | GTADTRA | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21A6h | GPT1 | A/D Converter Start Request Timing Buffer Register A*2 | GTADTBRA | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21A8h | GPT1 | A/D Converter Start Request Timing Double Buffer Register A*2 | GTADTDBRA | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21ACh | GPT1 | A/D Converter Start Request Timing Register B*2 | GTADTRB | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21AEh | GPT1 | A/D Converter Start Request Timing Buffer Register B*2 | GTADTBRB | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21B0h | GPT1 | A/D Converter Start Request Timing Double Buffer Register B*2 | GTADTDBRB | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21B4h | GPT1 | General PWM Timer Output Negate Control Register*2 | GTONCR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21B6h | GPT1 | General PWM Timer Dead Time Control Register*2 | GTDTCR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21B8h | GPT1 | General PWM Timer Dead Time Value Register U*2 | GTDVU | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21BAh | GPT1 | General PWM Timer Dead Time Value Register D*2 | GTDVD | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21BCh | GPT1 | General PWM Timer Dead Time Buffer Register U*2 | GTDBU | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21BEh | GPT1 | General PWM Timer Dead Time Buffer Register D*2 | GTDBD | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21C0h | GPT1 | General PWM Timer Output Protection Function Status Register*2 | GTSOS | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 21C2h | GPT1 | General PWM Timer Output Protection Function Temporary Release Register*2 | GTSOTR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2200h | GPT2 | General PWM Timer I/O Control Register*2 | GTIOR | 16 | 8, 16, 32 | 4 or 5 | PCLKA |
| 000C 2202h | GPT2 | General PWM Timer Interrupt Output Setting Register*2 | GTINTAD | 16 | 8, 16, 32 | 4 or 5 | PCLKA |
| 000C 2204h | GPT2 | General PWM Timer Control Register*2 | GTCR | 16 | 8, 16, 32 | 4 or 5 | PCLKA |
| 000C 2206h | GPT2 | General PWM Timer Buffer Enable Register*2 | GTBER | 16 | 8, 16, 32 | 4 or 5 | PCLKA |
| 000C 2208h | GPT2 | General PWM Timer Count Direction Register*2 | GTUDC | 16 | 8, 16, 32 | 4 or 5 | PCLKA |
| 000C 220Ah | GPT2 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2 | GTITC | 16 | 8, 16, 32 | 4 or 5 | PCLKA |
| 000C 220Ch | GPT2 | General PWM Timer Status Register*2 | GTST | 16 | 8, 16, 32 | 4 or 5 | PCLKA |
| 000C 220Eh | GPT2 | General PWM Timer Counter*2 | GTCNT | 16 | 16 | 4 or 5 | PCLKA |
| 000C 2210h | GPT2 | General PWM Timer Compare Capture Register A*2 | GTCCRA | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2212h | GPT2 | General PWM Timer Compare Capture Register B*2 | GTCCRB | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2214h | GPT2 | General PWM Timer Compare Capture Register C*2 | GTCCRC | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2216h | GPT2 | General PWM Timer Compare Capture Register D*2 | GTCCRD | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2218h | GPT2 | General PWM Timer Compare Capture Register E*2 | GTCCRE | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 221Ah | GPT2 | General PWM Timer Compare Capture Register F*2 | GTCCRF | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 221Ch | GPT2 | General PWM Timer Period Setting Register*2 | GTPR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 221Eh | GPT2 | General PWM Timer Period Setting Buffer Register*2 | GTPBR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2220h | GPT2 | General PWM Timer Period Setting Double Buffer Register*2 | GTPDBR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2224h | GPT2 | A/D Converter Start Request Timing Register A*2 | GTADTRA | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2226h | GPT2 | A/D Converter Start Request Timing Buffer Register A*2 | GTADTBRA | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2228h | GPT2 | A/D Converter Start Request Timing Double Buffer Register A*2 | GTADTDBRA | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 222Ch | GPT2 | A/D Converter Start Request Timing Register B*2 | GTADTRB | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 222Eh | GPT2 | A/D Converter Start Request Timing Buffer Register B*2 | GTADTBRB | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2230h | GPT2 | A/D Converter Start Request Timing Double Buffer Register B*2 | GTADTDBRB | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2234h | GPT2 | General PWM Timer Output Negate Control Register*2 | GTONCR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2236h | GPT2 | General PWM Timer Dead Time Control Register*2 | GTDTCR | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2238h | GPT2 | General PWM Timer Dead Time Value Register U*2 | GTDVU | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 223Ah | GPT2 | General PWM Timer Dead Time Value Register D*2 | GTDVD | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 223Ch | GPT2 | General PWM Timer Dead Time Buffer Register U*2 | GTDBU | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 223Eh | GPT2 | General PWM Timer Dead Time Buffer Register D*2 | GTDBD | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2240h | GPT2 | General PWM Timer Output Protection Function Status Register*2 | GTSOS | 16 | 16, 32 | 4 or 5 | PCLKA |
| 000C 2242h | GPT2 | General PWM Timer Output Protection Function Temporary Release Register*2 | GTSOTR | 16 | 16, 32 | 4 or 5 | PCLKA |

Table 4.1 List of I/O Registers (Address Order) (35/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|--------------|
| | | | | | | Access Size | ICLK ≥ PCLK |
| 000C 2280h | GPT3 | General PWM Timer I/O Control Register* ² | GTIOR | 16 | 8, 16, 32 | | 4 or 5 PCLKA |
| 000C 2282h | GPT3 | General PWM Timer Interrupt Output Setting Register* ² | GTINTAD | 16 | 8, 16, 32 | | 4 or 5 PCLKA |
| 000C 2284h | GPT3 | General PWM Timer Control Register* ² | GTCCR | 16 | 8, 16, 32 | | 4 or 5 PCLKA |
| 000C 2286h | GPT3 | General PWM Timer Buffer Enable Register* ² | GTBER | 16 | 8, 16, 32 | | 4 or 5 PCLKA |
| 000C 2288h | GPT3 | General PWM Timer Count Direction Register* ² | GTUDC | 16 | 8, 16, 32 | | 4 or 5 PCLKA |
| 000C 228Ah | GPT3 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register* ² | GTITC | 16 | 8, 16, 32 | | 4 or 5 PCLKA |
| 000C 228Ch | GPT3 | General PWM Timer Status Register* ² | GTST | 16 | 8, 16, 32 | | 4 or 5 PCLKA |
| 000C 228Eh | GPT3 | General PWM Timer Counter* ² | GT CNT | 16 | 16 | | 4 or 5 PCLKA |
| 000C 2290h | GPT3 | General PWM Timer Compare Capture Register A* ² | GTCCRA | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 2292h | GPT3 | General PWM Timer Compare Capture Register B* ² | GTCCRB | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 2294h | GPT3 | General PWM Timer Compare Capture Register C* ² | GTCCRC | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 2296h | GPT3 | General PWM Timer Compare Capture Register D* ² | GTCCRD | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 2298h | GPT3 | General PWM Timer Compare Capture Register E* ² | GTCCRE | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 229Ah | GPT3 | General PWM Timer Compare Capture Register F* ² | GTCCRF | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 229Ch | GPT3 | General PWM Timer Period Setting Register* ² | GTPR | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 229Eh | GPT3 | General PWM Timer Period Setting Buffer Register* ² | GTPBR | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22A0h | GPT3 | General PWM Timer Period Setting Double Buffer Register* ² | GTPDBR | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22A4h | GPT3 | A/D Converter Start Request Timing Register A* ² | GTADTRA | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22A6h | GPT3 | A/D Converter Start Request Timing Buffer Register A* ² | GTADTBRA | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22A8h | GPT3 | A/D Converter Start Request Timing Double Buffer Register A* ² | GTADTDBRA | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22ACh | GPT3 | A/D Converter Start Request Timing Register B* ² | GTADTRB | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22AEh | GPT3 | A/D Converter Start Request Timing Buffer Register B* ² | GTADTB RB | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22B0h | GPT3 | A/D Converter Start Request Timing Double Buffer Register B* ² | GTADTDBRB | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22B4h | GPT3 | General PWM Timer Output Negate Control Register* ² | GT ONCR | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22B6h | GPT3 | General PWM Timer Dead Time Control Register* ² | GTDT CR | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22B8h | GPT3 | General PWM Timer Dead Time Value Register U* ² | GT DVU | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22BAh | GPT3 | General PWM Timer Dead Time Value Register D* ² | GT DVD | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22BCh | GPT3 | General PWM Timer Dead Time Buffer Register U* ² | GT DBU | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22BEh | GPT3 | General PWM Timer Dead Time Buffer Register D* ² | GT DBD | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22C0h | GPT3 | General PWM Timer Output Protection Function Status Register* ² | GTSOS | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 22C2h | GPT3 | General PWM Timer Output Protection Function Temporary Release Register* ² | GTSOTR | 16 | 16, 32 | | 4 or 5 PCLKA |
| 000C 2300h | GPT01 | General PWM Timer Longword Counter* ² | GT CNTLW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2304h | GPT01 | General PWM Timer Longword Compare Capture Register A* ² | GTCCRALW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2308h | GPT01 | General PWM Timer Longword Compare Capture Register B* ² | GTCCRBLW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 230Ch | GPT01 | General PWM Timer Longword Compare Capture Register C* ² | GTCCRCLW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2310h | GPT01 | General PWM Timer Longword Compare Capture Register D* ² | GTCCRD LW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2314h | GPT01 | General PWM Timer Longword Compare Capture Register E* ² | GTCCRELW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2318h | GPT01 | General PWM Timer Longword Compare Capture Register F* ² | GTCCRFLW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 231Ch | GPT01 | General PWM Timer Longword Period Setting Register* ² | GTPRLW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2320h | GPT01 | General PWM Timer Longword Period Setting Buffer Register* ² | GTPBRLW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2324h | GPT01 | General PWM Timer Longword Period Setting Double Buffer Register* ² | GTPDBRLW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 2328h | GPT01 | Longword A/D Converter Start Request Timing Register A* ² | GTADTRALW | 32 | 32 | | 4 or 5 PCLKA |
| 000C 232Ch | GPT01 | Longword A/D Converter Start Request Timing Buffer Register A* ² | GTADTBALW | 32 | 32 | | 4 or 5 PCLKA |

Table 4.1 List of I/O Registers (Address Order) (36/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------|
| | | | | | | ICLK ≥ PCLK | |
| 000C 2330h | GPT01 | Longword A/D Converter Start Request Timing Double Buffer Register A*2 | GTADTDBRALW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2334h | GPT01 | Longword A/D Converter Start Request Timing Register B*2 | GTADTRBLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2338h | GPT01 | Longword A/D Converter Start Request Timing Buffer Register B*2 | GTADTBRBLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 233Ch | GPT01 | Longword A/D Converter Start Request Timing Double Buffer Register B*2 | GTADTDBRBLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2340h | GPT01 | General PWM Timer Longword Dead Time Value Register U*2 | GTDVULW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2344h | GPT01 | General PWM Timer Longword Dead Time Value Register D*2 | GTDVDLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2348h | GPT01 | General PWM Timer Longword Dead Time Buffer Register U*2 | GTDBULW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 234Ch | GPT01 | General PWM Timer Longword Dead Time Buffer Register D*2 | GTDBDLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2380h | GPT23 | General PWM Timer Longword Counter*2 | GTCTLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2384h | GPT23 | General PWM Timer Longword Compare Capture Register A*2 | GTCCRALW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2388h | GPT23 | General PWM Timer Longword Compare Capture Register B*2 | GTCCRBLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 238Ch | GPT23 | General PWM Timer Longword Compare Capture Register C*2 | GTCCRCLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2390h | GPT23 | General PWM Timer Longword Compare Capture Register D*2 | GTCCRDW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2394h | GPT23 | General PWM Timer Longword Compare Capture Register E*2 | GTCCRELW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 2398h | GPT23 | General PWM Timer Longword Compare Capture Register F*2 | GTCCRFLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 239Ch | GPT23 | General PWM Timer Longword Period Setting Register*2 | GTPRLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23A0h | GPT23 | General PWM Timer Longword Period Setting Buffer Register*2 | GTPBRLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23A4h | GPT23 | General PWM Timer Longword Period Setting Double Buffer Register*2 | GTPDBRLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23A8h | GPT23 | Longword A/D Converter Start Request Timing Register A*2 | GTADTRALW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23ACh | GPT23 | Longword A/D Converter Start Request Timing Buffer Register A*2 | GTADTBALW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23B0h | GPT23 | Longword A/D Converter Start Request Timing Double Buffer Register A*2 | GTADTDBRALW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23B4h | GPT23 | Longword A/D Converter Start Request Timing Register B*2 | GTADTRBLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23B8h | GPT23 | Longword A/D Converter Start Request Timing Buffer Register B*2 | GTADTBRBLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23BCh | GPT23 | Longword A/D Converter Start Request Timing Double Buffer Register B*2 | GTADTDBRBLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23C0h | GPT23 | General PWM Timer Longword Dead Time Value Register U*2 | GTDVULW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23C4h | GPT23 | General PWM Timer Longword Dead Time Value Register D*2 | GTDVDLW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23C8h | GPT23 | General PWM Timer Longword Dead Time Buffer Register U*2 | GTDBULW | 32 | 32 | 4 or 5 | PCLKA |
| 000C 23CCh | GPT23 | General PWM Timer Longword Dead Time Buffer Register D*2 | GTDBDLW | 32 | 32 | 4 or 5 | PCLKA |
| 007F C090h | FLASH | E2 DataFlash Control Register | DFLCTL | 8 | 8 | 2 or 3 | FCLK |
| 007F C100h | FLASH | Flash P/E Mode Control Register | FPMCR | 8 | 8 | 2 or 3 | FCLK |
| 007F C104h | FLASH | Flash Area Select Register | FASR | 8 | 8 | 2 or 3 | FCLK |
| 007F C108h | FLASH | Flash Processing Start Address Register L | FSARL | 16 | 16 | 2 or 3 | FCLK |
| 007F C110h | FLASH | Flash Processing Start Address Register H | FSARH | 16 | 16 | 2 or 3 | FCLK |
| 007F C114h | FLASH | Flash Control Register | FCR | 8 | 8 | 2 or 3 | FCLK |
| 007F C118h | FLASH | Flash Processing End Address Register L | FEARL | 16 | 16 | 2 or 3 | FCLK |
| 007F C120h | FLASH | Flash Processing End Address Register H | FEARH | 16 | 16 | 2 or 3 | FCLK |
| 007F C124h | FLASH | Flash Reset Register | FRESETR | 8 | 8 | 2 or 3 | FCLK |
| 007F C12Ch | FLASH | Flash Status Register 1 | FSTATR1 | 8 | 8 | 2 or 3 | FCLK |
| 007F C130h | FLASH | Flash Write Buffer 0 Register | FWB0 | 16 | 16 | 2 or 3 | FCLK |
| 007F C138h | FLASH | Flash Write Buffer 1 Register | FWB1 | 16 | 16 | 2 or 3 | FCLK |
| 007F C140h | FLASH | Flash Write Buffer 2 Register | FWB2 | 16 | 16 | 2 or 3 | FCLK |

Table 4.1 List of I/O Registers (Address Order) (37/37)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|------------|----------------|--|-----------------|----------------|-------------|-------------------------|
| | | | | | | ICLK ≥ PCLK |
| 007F C144h | FLASH | Flash Write Buffer 3 Register | FWB3 | 16 | 16 | 2 or 3 FCLK |
| 007F C180h | FLASH | Protection Unlock Register | FPR | 8 | 8 | 2 or 3 FCLK |
| 007F C184h | FLASH | Protection Unlock Status Register | FPSR | 8 | 8 | 2 or 3 FCLK |
| 007F C1C0h | FLASH | Flash Start-Up Setting Monitor Register | FSCMR | 16 | 16 | 2 or 3 FCLK |
| 007F C1C8h | FLASH | Flash Access Window Start Address Monitor Register | FAWSMR | 16 | 16 | 2 or 3 FCLK |
| 007F C1D0h | FLASH | Flash Access Window End Address Monitor Register | FAWEMR | 16 | 16 | 2 or 3 FCLK |
| 007F C1D8h | FLASH | Flash Initial Setting Register | FISR | 8 | 8 | 2 or 3 FCLK |
| 007F C1DCh | FLASH | Flash Extra Area Control Register | FEXCR | 8 | 8 | 2 or 3 FCLK |
| 007F C1E0h | FLASH | Flash Error Address Monitor Register L | FEAML | 16 | 16 | 2 or 3 FCLK |
| 007F C1E8h | FLASH | Flash Error Address Monitor Register H | FEAMH | 16 | 16 | 2 or 3 FCLK |
| 007F C1F0h | FLASH | Flash Status Register 0 | FSTATR0 | 8 | 8 | 2 or 3 FCLK |
| 007F C350h | FLASHCON ST | Unique ID Register 0 | UIDR0 | 32 | 32 | 2 or 3 FCLK |
| 007F C354h | FLASHCON ST | Unique ID Register 1 | UIDR1 | 32 | 32 | 2 or 3 FCLK |
| 007F C358h | FLASHCON ST | Unique ID Register 2 | UIDR2 | 32 | 32 | 2 or 3 FCLK |
| 007F C35Ch | FLASHCON ST | Unique ID Register 3 | UIDR3 | 32 | 32 | 2 or 3 FCLK |
| 007F FFB2h | FLASH | Flash P/E Mode Entry Register | FENTRYR | 16 | 16 | 2 or 3 FCLK |

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0, TMR2, TMR4, or TMR6 register. Table 23.5 lists register allocation for 16-bit access in the User's Manual: Hardware.

Note 2. This register is not available for chip version A.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

| Item | Symbol | Value | Unit |
|-----------------------------|---------------------------|--|--------------------|
| Power supply voltage | VCC | -0.3 to +6.5 | V |
| Input voltage | V _{in} | Port 4, port 5, port 6 | -0.3 to VREF + 0.3 |
| | | Except for port 4, port 5, port 6 and ports for 5 V tolerant*1 | -0.3 to VCC + 0.3 |
| | | Ports for 5 V tolerant*1 | -0.3 to +6.5 |
| Analog power supply voltage | AVCC0, AVCC1, AVCC2, VREF | -0.3 to +6.5 | V |
| Analog input voltage | V _{AN} | When AN000 to AN003, AN100 to AN103, AN200 to AN211 used | -0.3 to VREF + 0.3 |
| | | When AN016, AN116, CVREFC0, CVREFC1 used | -0.3 to VCC + 0.3 |
| Operating temperature | T _{opr} | -40 to +85 | °C |
| Storage temperature | T _{stg} | -55 to +125 | °C |

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the AVCC2 and AVSS2 pins, between the VREF and AVSS2 pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 4.7 μF capacitor. The capacitor must be placed close to the pin.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Even if -0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports B1 and B2 are 5 V tolerant.

Table 5.2 Recommended Operating Voltage Conditions

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|------------------------------|---------------------------------|------------|------|------|------|------|
| Power supply voltages | VCC*1, *2 | | 2.7 | — | 5.5 | V |
| | VSS | | — | 0 | — | |
| Analog power supply voltages | AVCC0, AVCC1, AVCC2, VREF*1, *2 | | VCC | — | 5.5 | V |
| | AVSS0, AVSS1, AVSS2 | | — | 0 | — | |

Note 1. AVCC0/AVCC1/AVCC2/VREF and VCC can be set individually within the operating range.

Note 2. When powering on the VCC and AVCC0/AVCC1/AVCC2/VREF pins, power them on at the same time or the VCC pin first and then the AVCC0/AVCC1/AVCC2/VREF pin.

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|-----------------|------------|------------|-------------|------|-----------------|
| Schmitt trigger input voltage | RIIC input pin (except for SMBus, 5 V tolerant) | V _{IH} | VCC × 0.7 | — | 5.8 | V | |
| | Ports B1, B2 (5 V tolerant) | | VCC × 0.8 | — | 5.8 | | |
| | Ports 00 to 02, ports 10, 11, ports 20 to 24, ports 30 to 33, 36, 37, ports 70 to 76, ports 80 to 82, ports 90 to 96, ports A0 to A5, port B0, ports B3 to B7, ports D0 to D7, ports E0 to E5, RES# | | VCC × 0.8 | — | VCC + 0.3 | | |
| | Ports 40 to 47, ports 50 to 55, ports 60 to 65 | VREF × 0.8 | — | VREF + 0.3 | | | |
| | RIIC input pin (except for SMBus) | V _{IL} | -0.3 | — | VCC × 0.3 | | |
| | Ports 40 to 47, ports 50 to 55, ports 60 to 65 | | -0.3 | — | VREF × 0.2 | | |
| | Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65 | | -0.3 | — | VCC × 0.2 | | |
| | RIIC input pin (except for SMBus) | ΔV _T | VCC × 0.05 | — | — | | |
| | Ports 40 to 47, ports 50 to 55, ports 60 to 65 | | VREF × 0.1 | — | — | | |
| | Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65 | | VCC × 0.1 | — | — | | |
| Input level voltage (except for Schmitt trigger input pins) | MD | V _{IH} | VCC × 0.9 | — | VCC + 0.3 | V | |
| | EXTAL (external clock input) | | VCC × 0.8 | — | VCC + 0.3 | | |
| | RIIC input pin (SMBus) | 2.1 | — | VCC + 0.3 | VCC ≤ 5.2 V | | |
| | MD | V _{IL} | -0.3 | — | VCC × 0.1 | | |
| | EXTAL (external clock input) | | -0.3 | — | VCC × 0.2 | | |
| | RIIC input pin (SMBus) | | -0.3 | — | 0.8 | | |

Table 5.4 DC Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | | |
|---|--|-----------|------|------|------|--|-----|---------------------|
| Input leakage current | RES#, MD, port E2 | I_{in} | — | — | 1.0 | μ A, $V_{in} = 0$ V, VCC | | |
| Three-state leakage current (off-state) | Port 4, port 5, port 6 | I_{TSI} | — | — | 1.0 | μ A, $V_{in} = 0$ V, VREF | | |
| | Ports except for 5-V tolerant ports and port 4, port 5, port 6 | | | | | | 0.2 | $V_{in} = 0$ V, VCC |
| | Ports for 5 V tolerant | | | | | | 1.0 | |
| Input capacitance | All input pins | C_{in} | — | 4 | 15 | pF, $V_{in} = 0$ mV, $f = 1$ MHz, $T_a = 25^\circ$ C | | |
| Input pull-up resistor | All ports (except for port E2) | R_U | 10 | 20 | 50 | k Ω , $V_{in} = 0$ V | | |

Table 5.5 DC Characteristics (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = -40 to +85°C

| Item | Symbol | Chip Version A | | Chip Version B | | Unit | Test Conditions | | | |
|-------------------|----------|--------------------------------|----------------------------------|----------------------------------|-----------------|------|-----------------|------|---|----|
| | | Typ. *7 | Max. | Typ. *7 | Max. | | | | | |
| Supply current *1 | I_{CC} | High-speed operating mode | Normal operating mode | No peripheral operation*2 | ICLK = 80 MHz | 26.0 | — | 26.0 | — | mA |
| | | | | | ICLK = 64 MHz | 20.7 | — | 20.7 | — | |
| | | | | | ICLK = 32 MHz | 11.8 | — | 11.8 | — | |
| | | | | | ICLK = 16 MHz | 7.0 | — | 7.0 | — | |
| | | | | | ICLK = 8 MHz | 4.7 | — | 4.7 | — | |
| | | | | All peripheral operation: Normal | ICLK = 80 MHz*3 | 35.0 | — | 40.5 | — | |
| | | | | | ICLK = 64 MHz*4 | 28.5 | — | 32.5 | — | |
| | | | | | ICLK = 32 MHz*5 | 18.5 | — | 20.9 | — | |
| | | | | | ICLK = 16 MHz*5 | 10.5 | — | 11.7 | — | |
| | | | | | ICLK = 8 MHz*5 | 6.4 | — | 7.0 | — | |
| | | All peripheral operation: Max. | ICLK = 80 MHz*3 | — | 70.0 | — | 80.0 | | | |
| | | | ICLK = 64 MHz*4 | — | 60.0 | — | 70.0 | | | |
| | | | ICLK = 32 MHz*5 | — | 40.0 | — | 45.0 | | | |
| | | Sleep mode | No peripheral operation*2 | ICLK = 80 MHz | 7.2 | — | 7.2 | — | | |
| | | | | ICLK = 64 MHz | 6.1 | — | 6.1 | — | | |
| | | | | ICLK = 32 MHz | 4.4 | — | 4.4 | — | | |
| | | | | ICLK = 16 MHz | 3.4 | — | 3.4 | — | | |
| | | | | ICLK = 8 MHz | 2.9 | — | 2.9 | — | | |
| | | | All peripheral operation: Normal | ICLK = 80 MHz*3 | 22.4 | — | 26.9 | — | | |
| | | | | ICLK = 64 MHz*4 | 18.4 | — | 21.9 | — | | |
| ICLK = 32 MHz*5 | 13.5 | | | — | 15.5 | — | | | | |
| ICLK = 16 MHz*5 | 8.0 | | | — | 9.0 | — | | | | |
| ICLK = 8 MHz*5 | 5.2 | | | — | 5.7 | — | | | | |

| Item | | | | | Symbol | Chip Version A | | Chip Version B | | Unit | Test Conditions |
|----------------------------------|---------------------------------|------------------------------------|------------------------------------|------------------|-----------------|----------------|------|----------------|------|------|-----------------|
| | | | | | | Typ. *7 | Max. | Typ. *7 | Max. | | |
| Supply current *1 | High-speed operating mode | Deep sleep mode | No peripheral operation*2 | ICLK = 80 MHz | I _{CC} | 3.4 | — | 3.4 | — | mA | |
| | | | | ICLK = 64 MHz | | 2.9 | — | 2.9 | — | | |
| | | | | ICLK = 32 MHz | | 2.5 | — | 2.5 | — | | |
| | | | | ICLK = 16 MHz | | 2.3 | — | 2.3 | — | | |
| | | | | ICLK = 8 MHz | | 2.2 | — | 2.2 | — | | |
| | | All peripheral operation: Normal | ICLK = 80 MHz*3 | 17.7 | | — | 22.2 | — | | | |
| | | | ICLK = 64 MHz*4 | 14.4 | | — | 17.9 | — | | | |
| | | | ICLK = 32 MHz*5 | 10.9 | | — | 12.9 | — | | | |
| | | | ICLK = 16 MHz*5 | 6.6 | | — | 7.6 | — | | | |
| | | | ICLK = 8 MHz*5 | 4.3 | | — | 4.8 | — | | | |
| | Increase during BGO operation*6 | | | | 2.5 | — | 2.5 | — | | | |
| | Middle-speed operating modes | Normal operating mode | No peripheral operation*8 | ICLK = 12 MHz*10 | I _{CC} | 5.3 | — | 5.3 | — | | |
| | | | | ICLK = 8 MHz | | 4.5 | — | 4.5 | — | | |
| | | | | ICLK = 1 MHz | | 2.5 | — | 2.5 | — | | |
| | | | All peripheral operation: Normal*9 | ICLK = 12 MHz*10 | | 7.8 | — | 8.7 | — | | |
| ICLK = 8 MHz | | | | 6.3 | | — | 6.9 | — | | | |
| ICLK = 1 MHz | | | | 2.7 | | — | 2.7 | — | | | |
| All peripheral operation: Max.*9 | | | ICLK = 12 MHz*10 | | | — | 17.0 | — | 18.0 | | |
| | | | | | | | | | | | |
| Sleep mode | | | No peripheral operation*8 | ICLK = 12 MHz*10 | | 2.6 | — | 2.6 | — | | |
| | | | | ICLK = 8 MHz | | 2.7 | — | 2.7 | — | | |
| | | ICLK = 1 MHz | | 2.2 | | — | 2.2 | — | | | |
| | | All peripheral operation: Normal*9 | ICLK = 12 MHz*10 | 6.0 | | — | 6.7 | — | | | |
| | | | ICLK = 8 MHz | 5.1 | | — | 5.6 | — | | | |
| | | | ICLK = 1 MHz | 2.5 | | — | 2.5 | — | | | |
| Deep sleep mode | | No peripheral operation*8 | ICLK = 12 MHz*10 | 1.8 | | — | 1.8 | — | | | |
| | | | ICLK = 8 MHz | 2.1 | | — | 2.1 | — | | | |
| | | | ICLK = 1 MHz | 2.1 | | — | 2.1 | — | | | |
| | | All peripheral operation: Normal*9 | ICLK = 12 MHz*10 | 5.0 | | — | 5.7 | — | | | |
| | | | ICLK = 8 MHz | 4.3 | | — | 4.8 | — | | | |
| | | | ICLK = 1 MHz | 2.3 | | — | 2.3 | — | | | |
| Increase during BGO operation*6 | | | | 2.5 | | — | 2.5 | — | | | |

- Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
- Note 2. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
- Note 3. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. FCLK is set to divided by 4. PCLKA is set to divided by 1. PCLKB and PCLKD are set to divided by 2.
- Note 4. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. PCLKA is set to divided by 1. FCLK, PCLKB, and PCLKD are set to divided by 2.
- Note 5. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
- Note 6. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.
- Note 7. Values when VCC = 5 V.
- Note 8. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
- Note 9. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
- Note 10. When the frequency of PLL is 48 MHz.

Table 5.6 DC Characteristics (4)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = VREF = VCC$ to 5.5 V , $VSS = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | | | Symbol | Chip Version A | | Chip Version B | | Unit | Test Conditions |
|------------------|-------------------------|--------------------------|----------|----------------|-------|----------------|-------|---------------|-----------------|
| | | | | Typ.*3 | Max. | Typ.*3 | Max. | | |
| Supply current*1 | Software standby mode*2 | $T_a = 25^\circ\text{C}$ | I_{CC} | 1.0 | 55.0 | 1.5 | 15.0 | μA | |
| | | $T_a = 55^\circ\text{C}$ | | 1.5 | 60.0 | 3.0 | 38.0 | | |
| | | $T_a = 85^\circ\text{C}$ | | 5.5 | 260.0 | 13.0 | 135.0 | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. The IWDT and LVD are stopped.

Note 3. $V_{CC} = 5\text{ V}$.

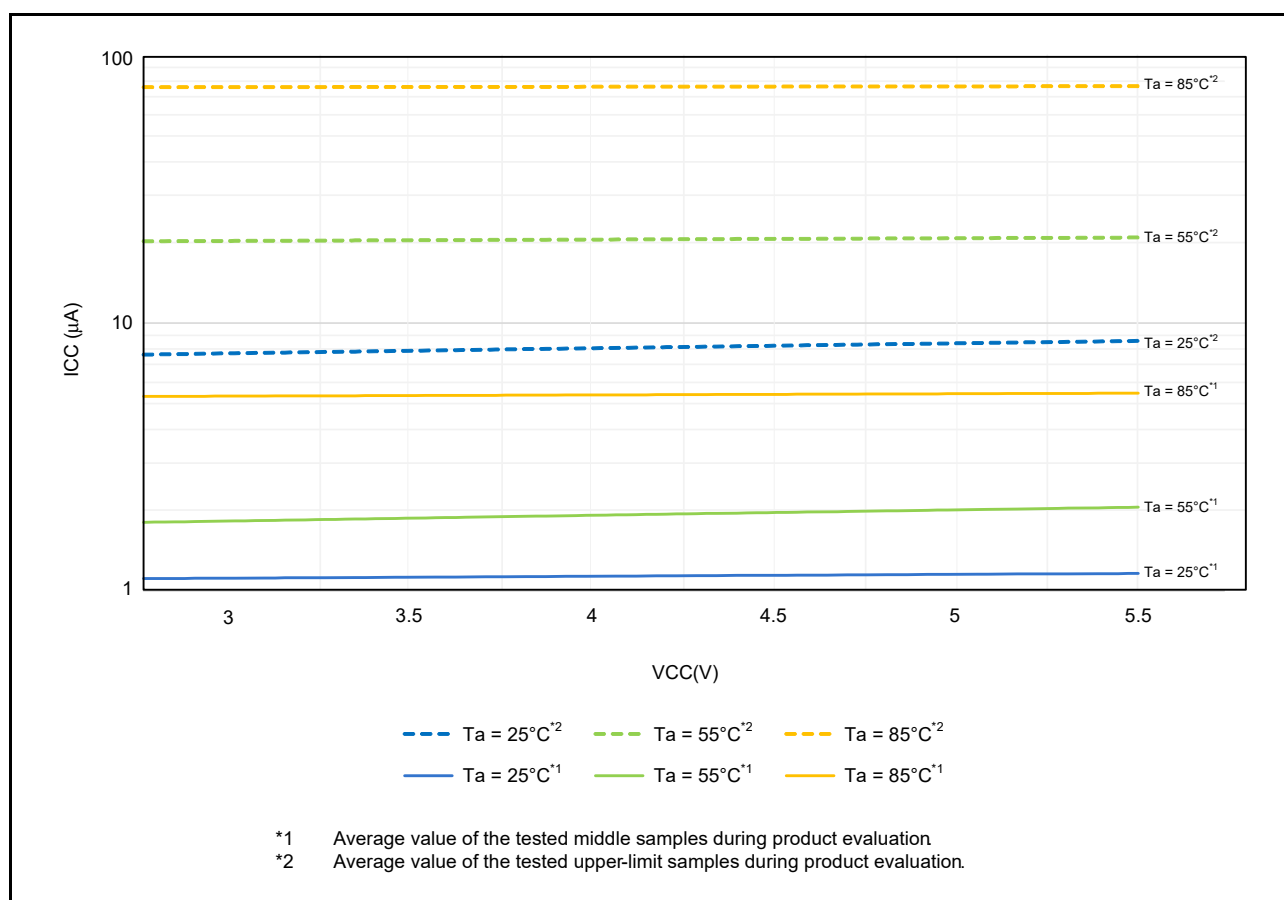


Figure 5.1 Voltage Dependency in Software Standby Mode (Chip Version A) (Reference Data)

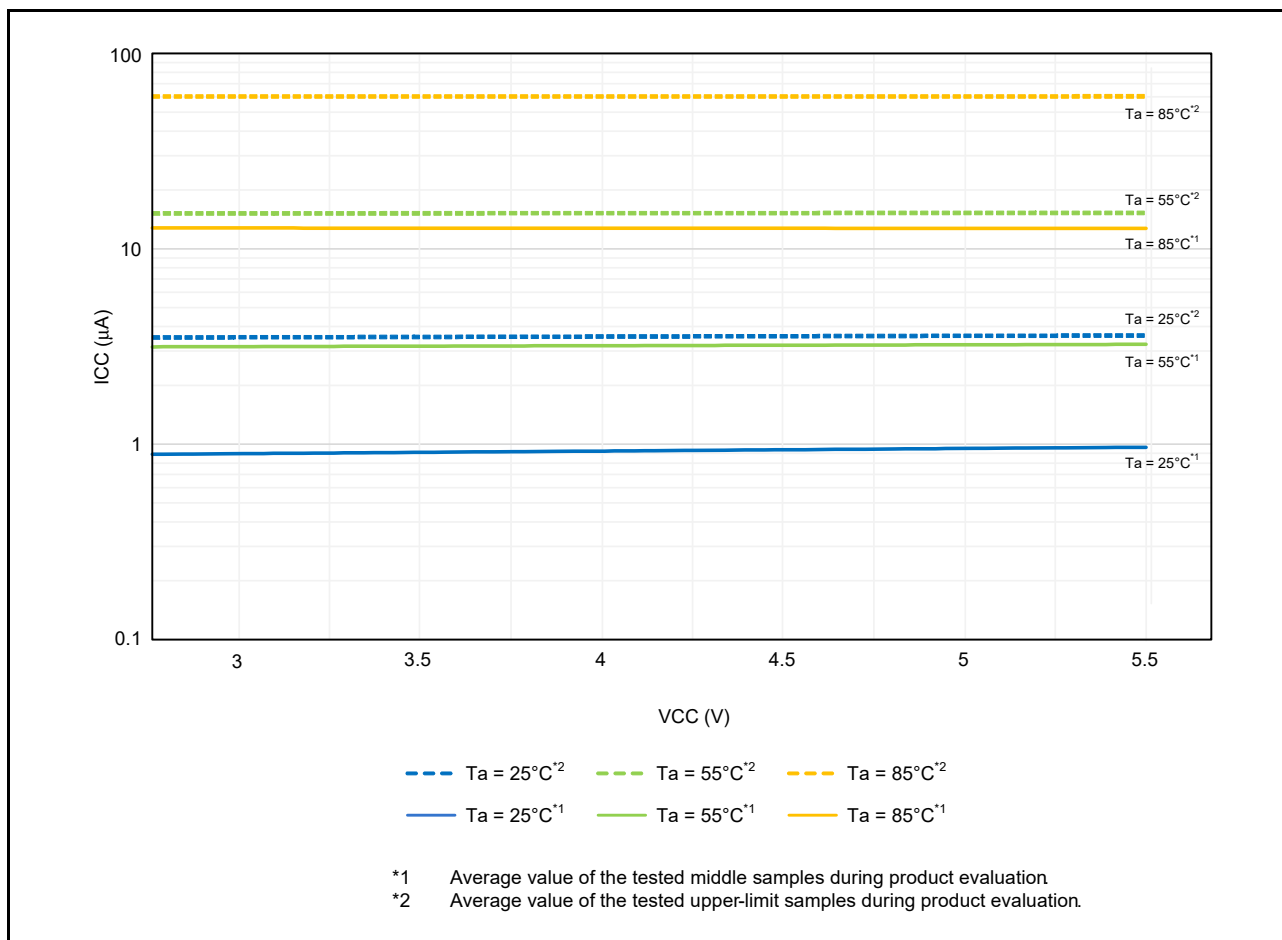


Figure 5.2 Voltage Dependency in Software Standby Mode (Chip Version B) (Reference Data)

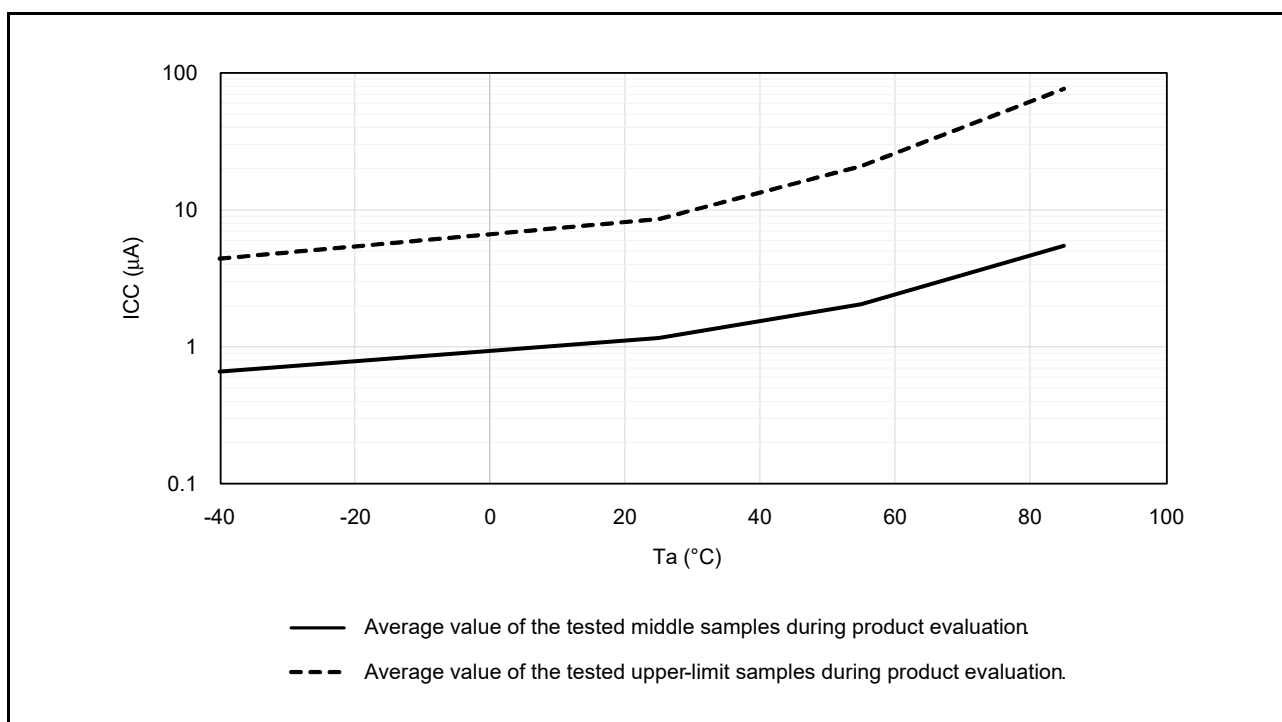


Figure 5.3 Temperature Dependency in Software Standby Mode (Chip Version A) (Reference Data)

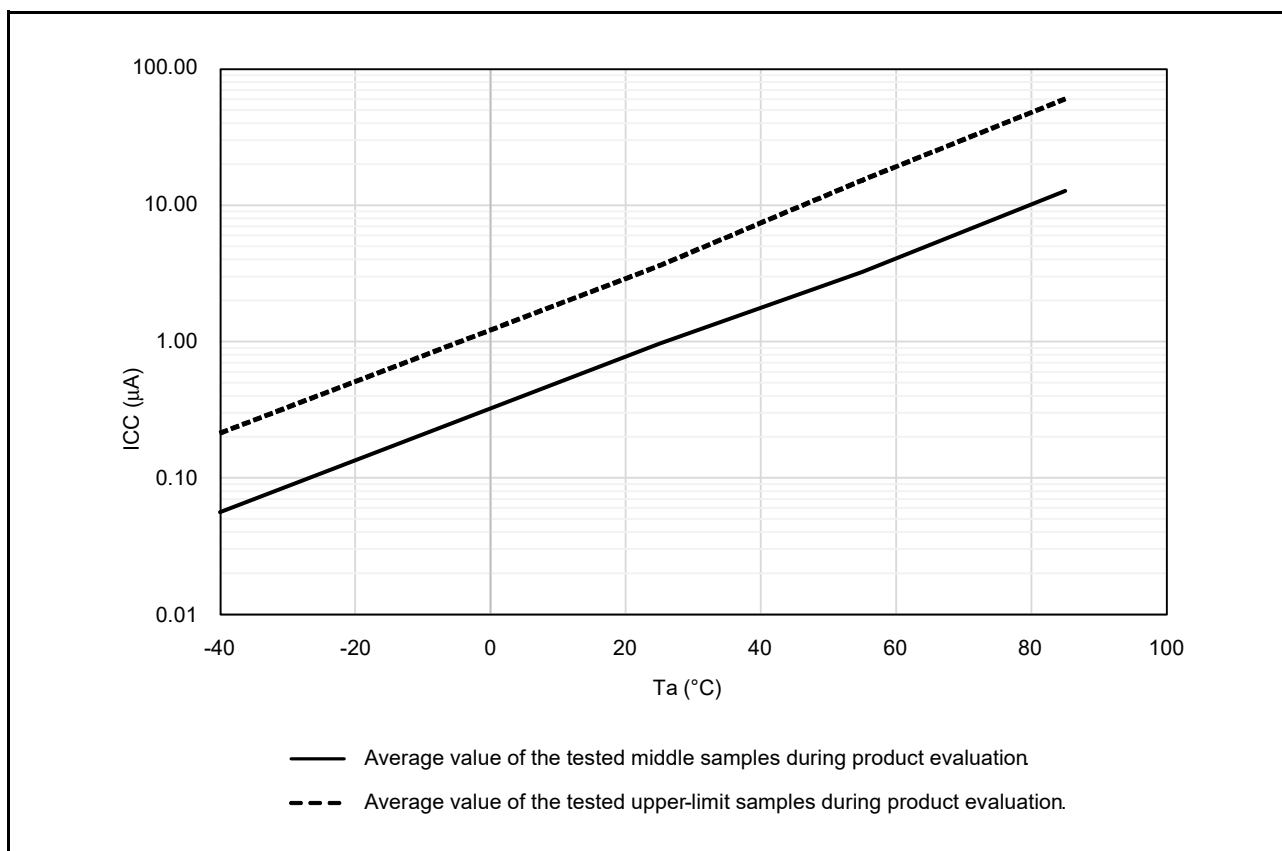


Figure 5.4 Temperature Dependency in Software Standby Mode (Chip Version B) (Reference Data)

Table 5.7 DC Characteristics (5)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | Symbol | Typ. | Max. | Unit | Test Conditions |
|---------------------------------------|--------|------|------|------|-----------------|
| Permissible total consumption power*1 | P_d | — | 570 | mW | |

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.8 DC Characteristics (6)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| | Item | | Symbol | Min. | Typ.*2 | Max. | Unit | Test Conditions | |
|----------------------------------|---|---|------------|------|--------|------|---------------|-----------------|---------------|
| Analog power supply current | A/D unit 0 | During A/D conversion (programmable gain amplifier in use) | I_{AVCC} | — | 1.5 | 2.5 | mA | | |
| | | During A/D conversion (programmable gain amplifier not in use) | | — | 1.0 | 1.8 | | | |
| | A/D unit 1 | During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier in use) | | — | 4.6 | 6.9 | | | |
| | | During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier not in use) | | — | 3.1 | 4.8 | | | |
| | | During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier in use) | | — | 2.5 | 3.9 | | | |
| | | During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier not in use) | | — | 1.0 | 1.8 | | | |
| | A/D unit 2 | | | — | 1.0 | 1.8 | | | |
| | During D/A conversion (per channel)*1 | | | — | 0.7 | 1.0 | | | |
| | Waiting for A/D or D/A conversion (all units) | | | — | — | 2.2 | | | μA |
| | Waiting for A/D conversion (all units) | | | — | — | 1.2 | | | μA |
| Comparator C operating current*3 | Comparator enabled | | I_{CMP} | — | 40.0 | 60.0 | μA | | |

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.

Note 2. When $V_{CC} = AVCC0 = AVCC1 = AVCC2 = V_{REF} = 5\text{ V}$.

Note 3. Current consumed only by the comparator C module.

Table 5.9 DC Characteristics (7)

Conditions: $V_{CC} = 0\text{ V to }AVCC0$, $AVCC0 = AVCC1 = AVCC2 = V_{REF} = 0\text{ V to }5.5\text{ V}$, $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| | Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------------|---|---------|------|------|------|------|-----------------|
| Power-on VCC rising gradient | At normal startup | $SrVCC$ | 0.02 | — | 20 | ms/V | |
| | Voltage monitoring 0 reset enabled at startup*1, *2 | | 0.02 | — | — | | |

Note 1. When $OFS1.LVDAS = 0$.

Note 2. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by $OFS1$ are not read in boot mode.

Table 5.10 DC Characteristics (8)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = VREF = VCC$ to 5.5 V , $VSS = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

The ripple voltage must meet the allowable ripple frequency $f_r(V_{CC})$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds $V_{CC} \pm 10\%$, the allowable voltage change rising/falling gradient dt/dV_{CC} must be met.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|---------------|------|------|------|------|---|
| Allowable ripple frequency | $f_r(V_{CC})$ | — | — | 10 | kHz | Figure 5.5 $V_r(V_{CC}) \leq V_{CC} \times 0.2$ |
| | | — | — | 1 | MHz | Figure 5.5 $V_r(V_{CC}) \leq V_{CC} \times 0.08$ |
| | | — | — | 10 | MHz | Figure 5.5 $V_r(V_{CC}) \leq V_{CC} \times 0.06$ |
| Allowable voltage change rising/falling gradient | dt/dV_{CC} | 1.0 | — | — | ms/V | When VCC change exceeds $V_{CC} \pm 10\%$ |

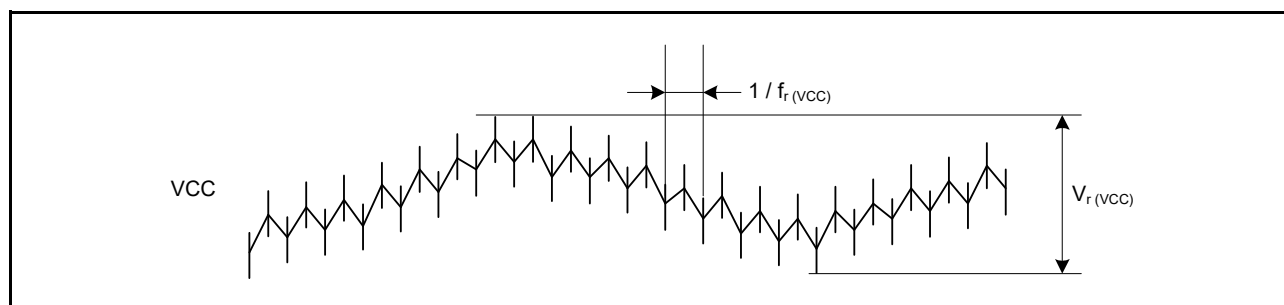


Figure 5.5 Ripple Waveform

Table 5.11 DC Characteristics (9)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = VREF = VCC$ to 5.5 V , $VSS = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|-----------|------|------|------|---------------|-----------------|
| Permissible error of VCL pin external capacitance | C_{VCL} | 3.3 | 4.7 | 6.1 | μF | |

Note: The recommended capacitance is $4.7\ \mu\text{F}$. Variations in connected capacitors should be within the above range.

Table 5.12 Permissible Output Currents

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | | Symbol | Max. | Unit | |
|---------------------------------|--|-----------------|------------------------|------|-----|
| Permissible output low current | Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3 | I_{OL} | 10.0 | mA | |
| | RIIC pins | | 6.0 | | |
| | Ports other than above | | Normal output mode | | 4.0 |
| | | | High-drive output mode | | 8.0 |
| Permissible output low current | Total of all output pins | ΣI_{OL} | 110.0 | | |
| | Total of ports 40 to 47, ports 50 to 55, ports 60 to 65 | | 50.0 | | |
| | Total of port 02, port E5, ports 10 and 11, ports 80 to 82 | | 50.0 | | |
| | Total of ports B4 to B7, ports D0 to D7, ports E0 and E1 | | 55.0 | | |
| | Total of ports 71 to 76 | | 30.0 | | |
| | Total of ports 90 to 95 | | 30.0 | | |
| Permissible output high current | Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3 | I_{OH} | -5.0 | | |
| | Ports other than above | | Normal output mode | -4.0 | |
| | | | High-drive output mode | -8.0 | |
| Permissible output high current | Total of all output pins | ΣI_{OH} | -35.0 | | |
| | Total of ports 40 to 47, ports 50 to 55, ports 60 to 65 | | -25.0 | | |

Note: Do not exceed the permissible total supply current.

Table 5.13 Output Values of Voltage

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | | Symbol | Min. | Max. | Unit | Test Conditions | |
|-------------|---|----------|------------------------|----------------|------|--------------------------|--------------------------|
| Output low | Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3 | V_{OL} | — | 0.8 | V | $I_{OL} = 10.0\text{mA}$ | |
| | RIIC pins | | Standard mode | — | | 0.4 | $I_{OL} = 3.0\text{mA}$ |
| | | | Fast mode | — | | 0.6 | $I_{OL} = 6.0\text{mA}$ |
| | Ports other than above | | Normal output mode | — | | 0.8 | $I_{OL} = 1.0\text{mA}$ |
| | | | High-drive output mode | — | | 0.8 | $I_{OL} = 2.0\text{mA}$ |
| Output high | Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3 | V_{OH} | $V_{CC} - 0.8$ | — | V | $I_{OH} = -5.0\text{mA}$ | |
| | Ports 40 to 47, ports 50 to 55, ports 60 to 65 | | $V_{REF} - 0.8$ | — | | $I_{OH} = -2.0\text{mA}$ | |
| | Ports other than above | | Normal output mode | $V_{CC} - 0.8$ | | — | $I_{OH} = -2.0\text{mA}$ |
| | | | High-drive output mode | $V_{CC} - 0.8$ | | — | $I_{OH} = -4.0\text{mA}$ |

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.6 to Figure 5.9 show the characteristics when normal output is selected by the drive capacity control register.

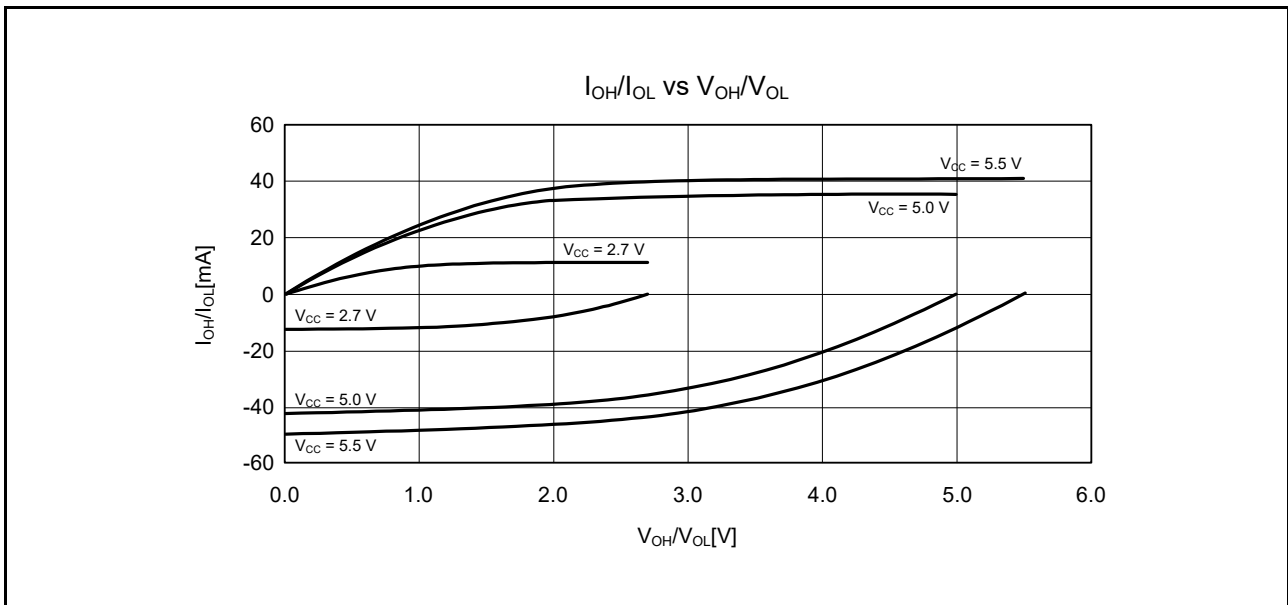


Figure 5.6 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^\circ\text{C}$ When Normal Output is Selected (Reference Data)

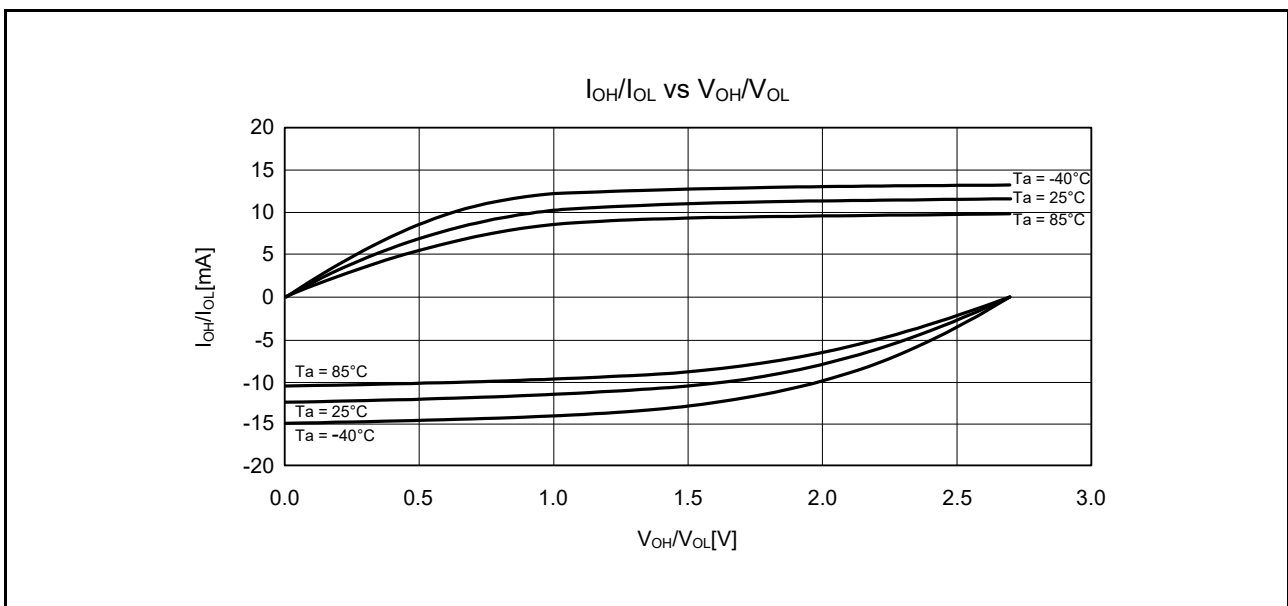


Figure 5.7 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 2.7\text{V}$ when Normal Output is Selected (Reference Data)

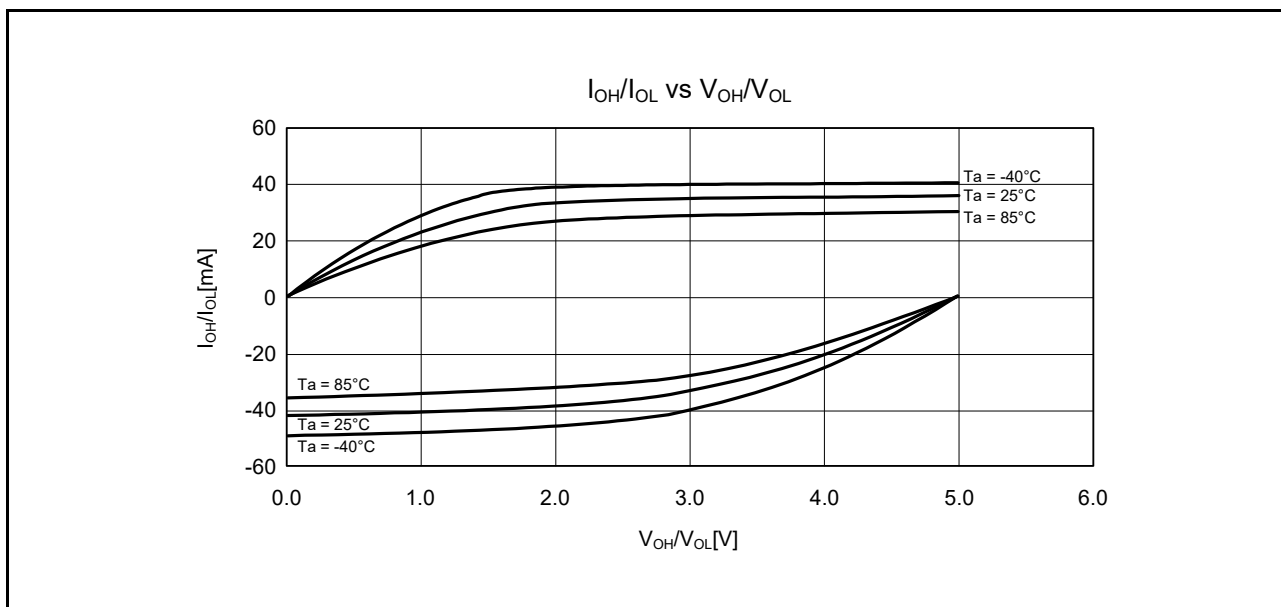


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.0$ V when Normal Output is Selected (Reference Data)

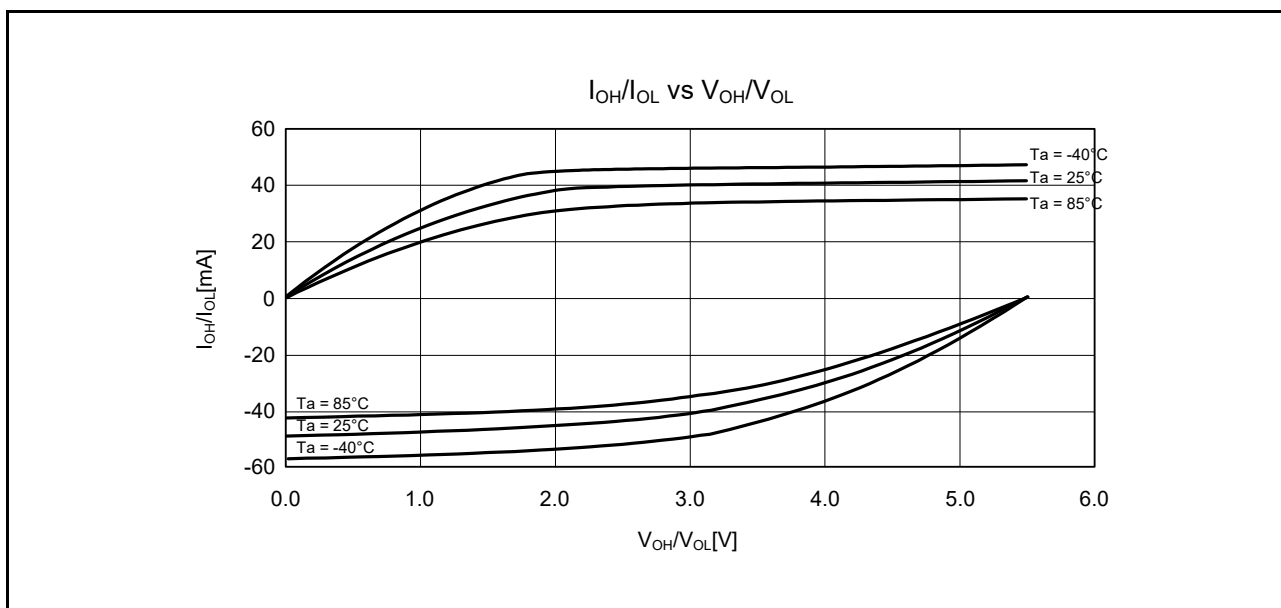


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.5$ V when Normal Output is Selected (Reference Data)

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.10 to Figure 5.13 show the characteristics when high-drive output is selected by the drive capacity control register.

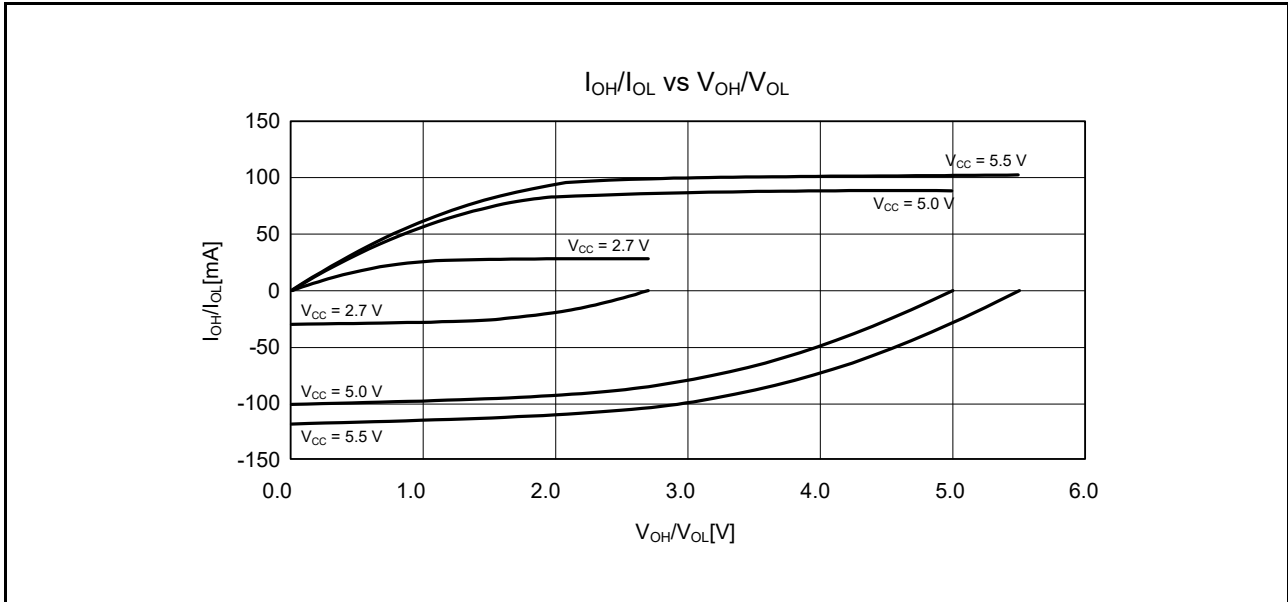


Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^\circ\text{C}$ When Normal Output is Selected (Reference Data)

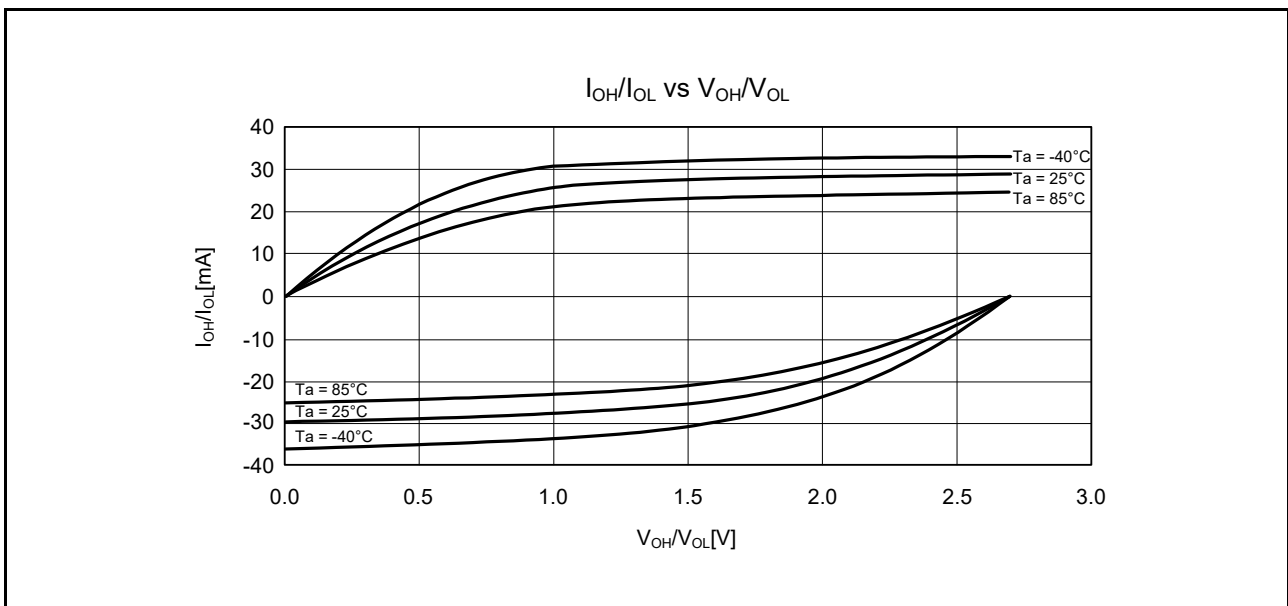


Figure 5.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 2.7\text{ V}$ when Normal Output is Selected (Reference Data)

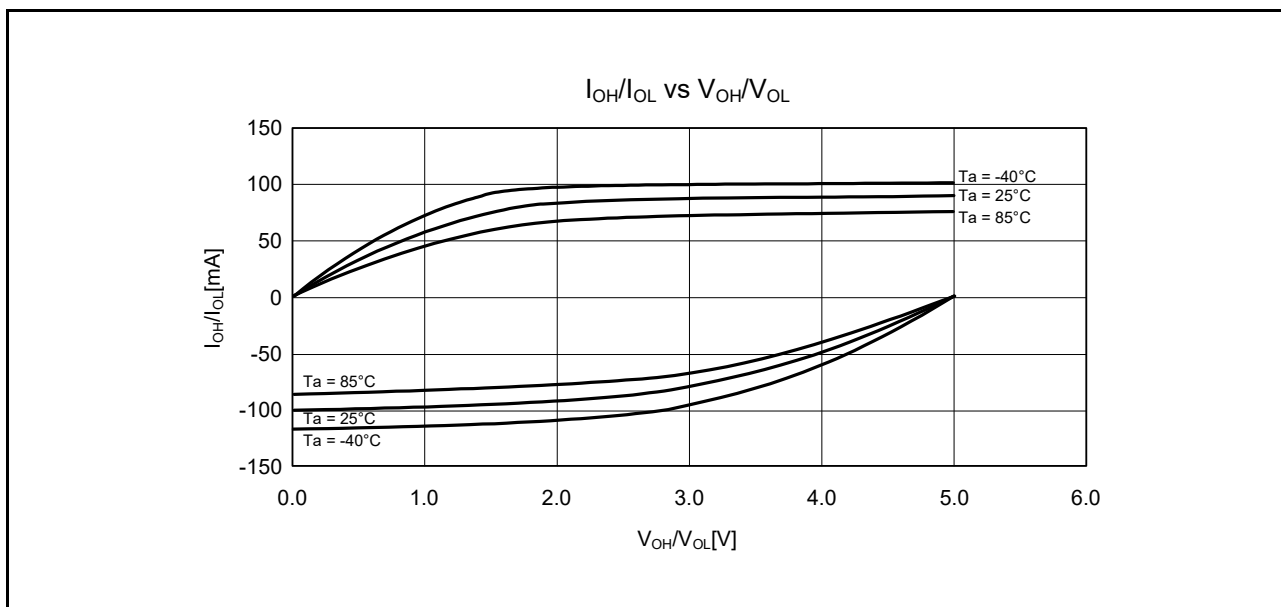


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.0$ V when Normal Output is Selected (Reference Data)

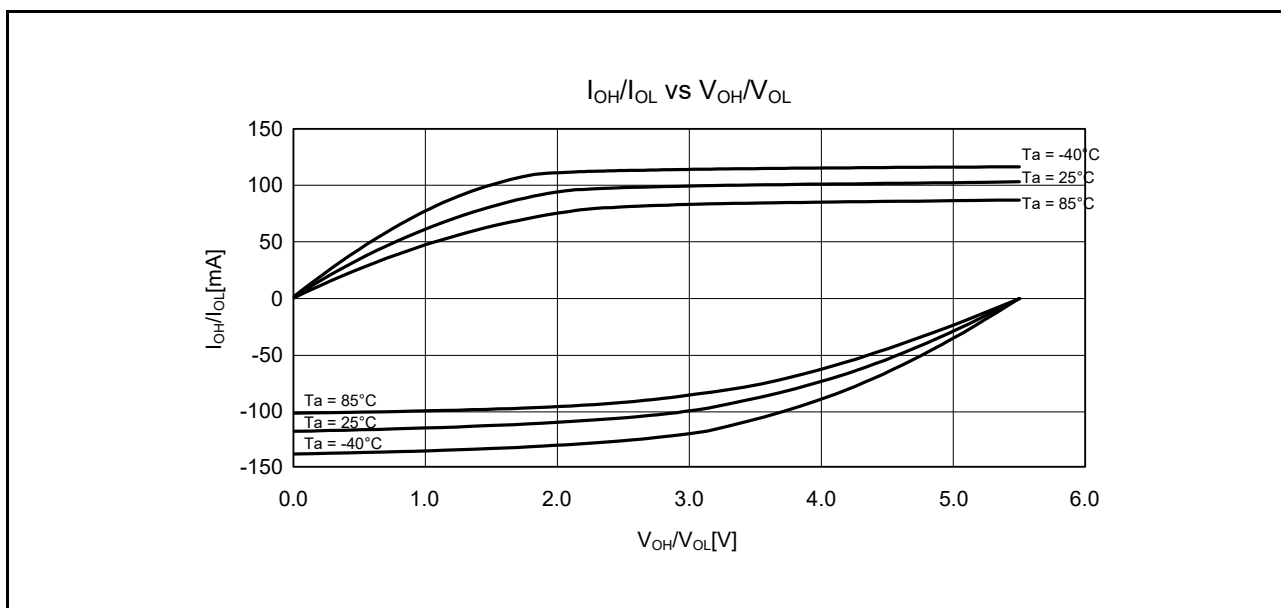


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.5$ V when Normal Output is Selected (Reference Data)

5.2.3 Standard I/O Pin Output Characteristics (3)

Figure 5.14 to Figure 5.17 show the output characteristics of the large current ports.

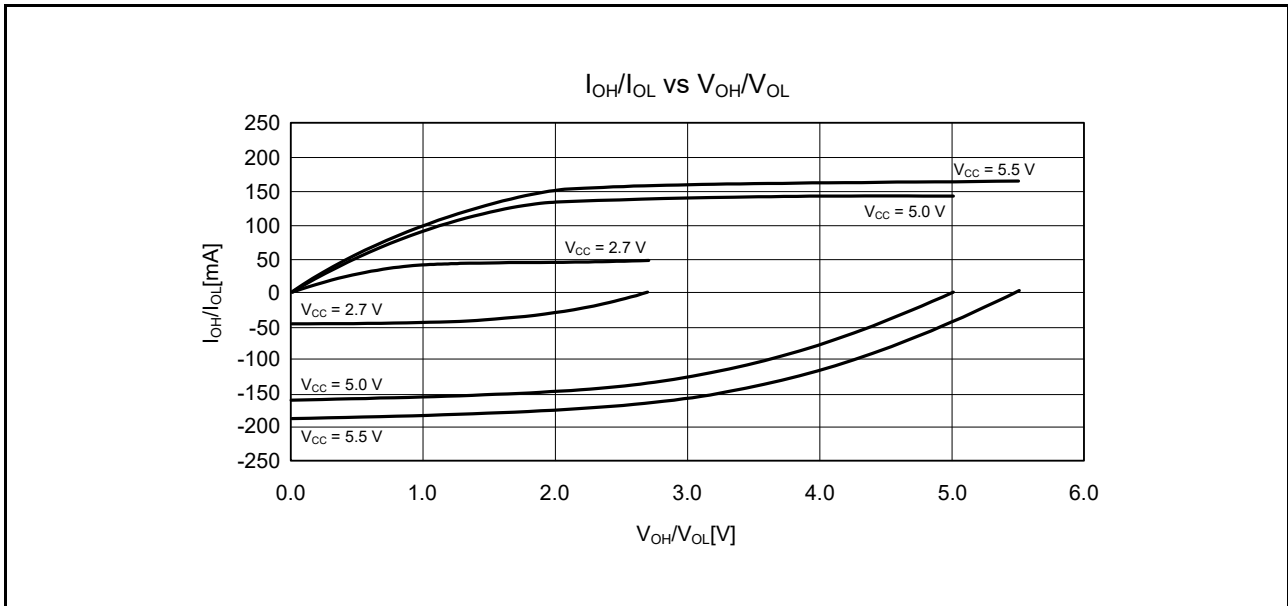


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of Large Current Ports at $T_a = 25^\circ\text{C}$ (Reference Data)

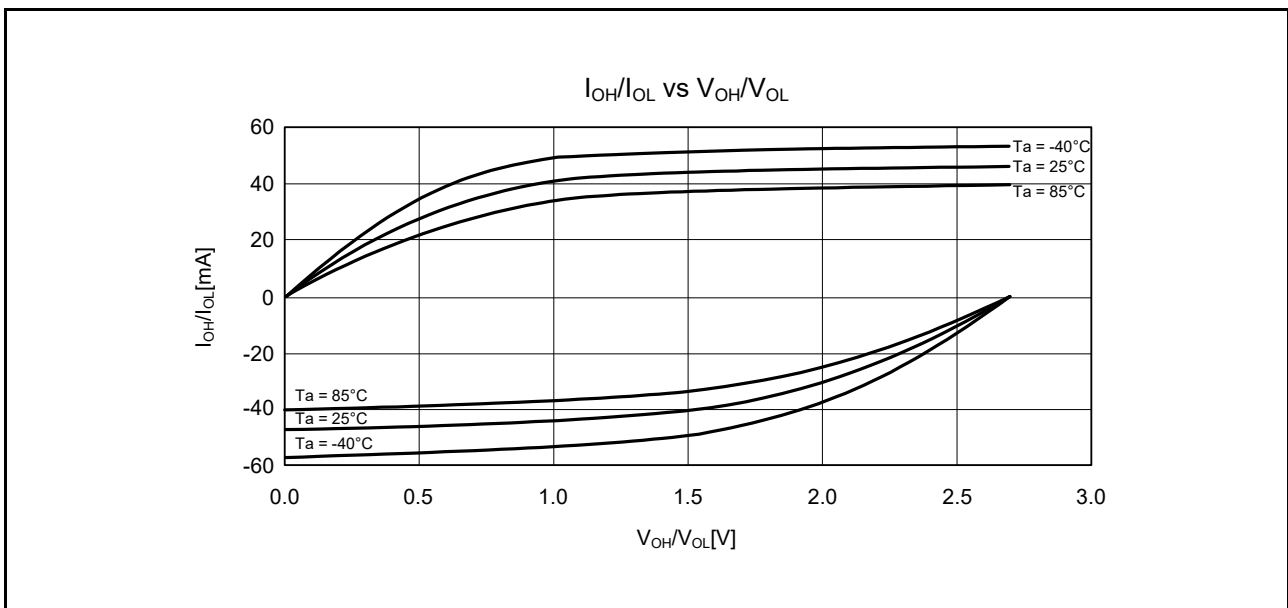


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at $V_{CC} = 2.7\text{ V}$ (Reference Data)

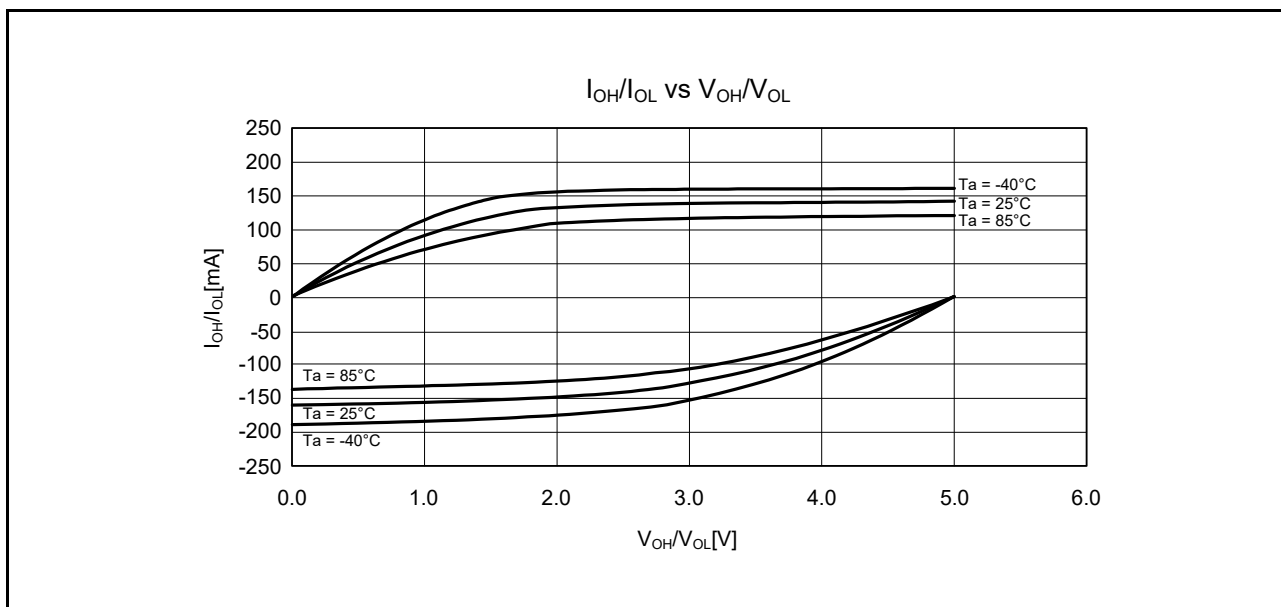


Figure 5.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at $V_{CC} = 5.0$ V (Reference Data)

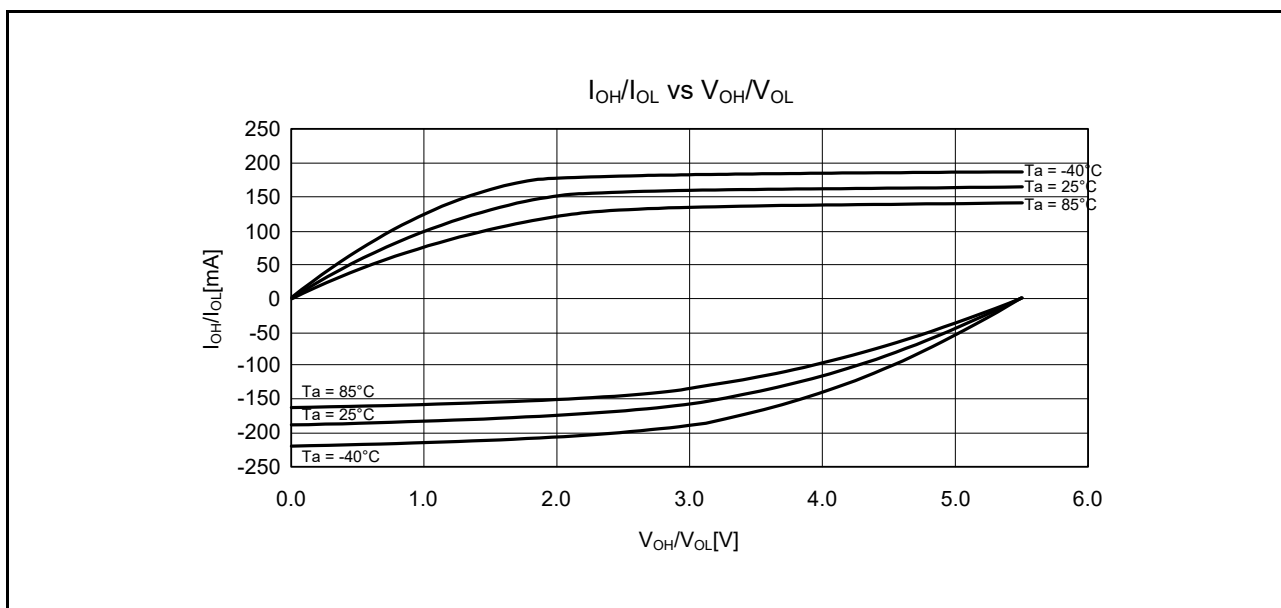


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at $V_{CC} = 5.5$ V (Reference Data)

5.2.4 RIIC Pin Output Characteristics

Figure 5.18 to Figure 5.21 show the output characteristics of the RIIC pin.

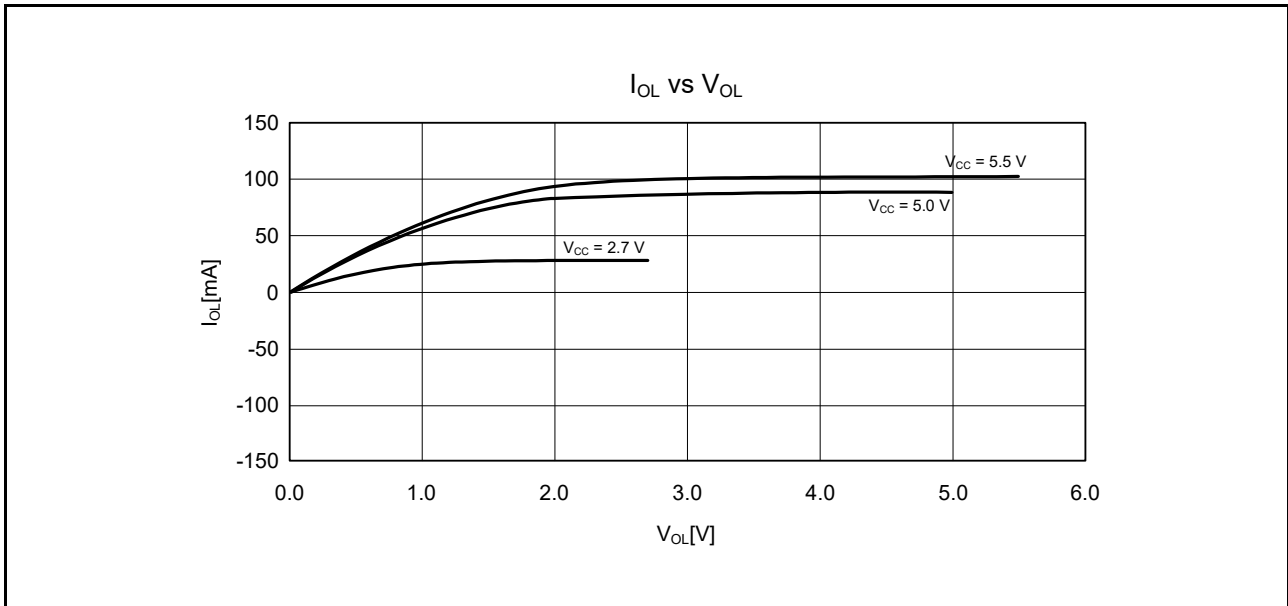


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

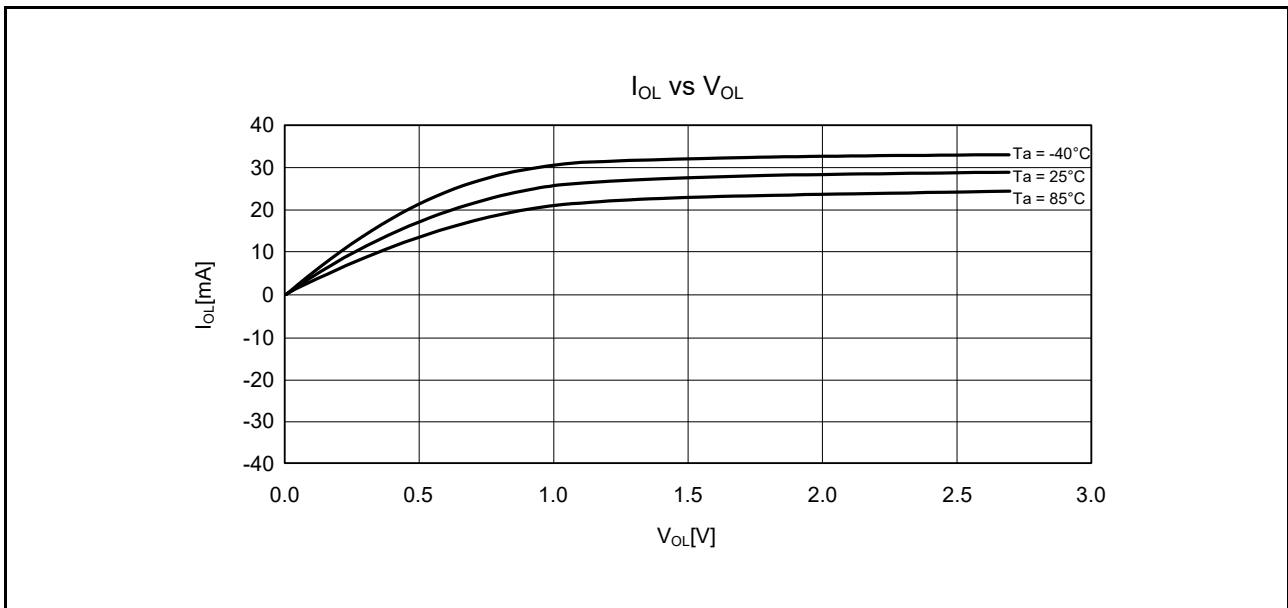


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at V_{CC} = 2.7 V (Reference Data)

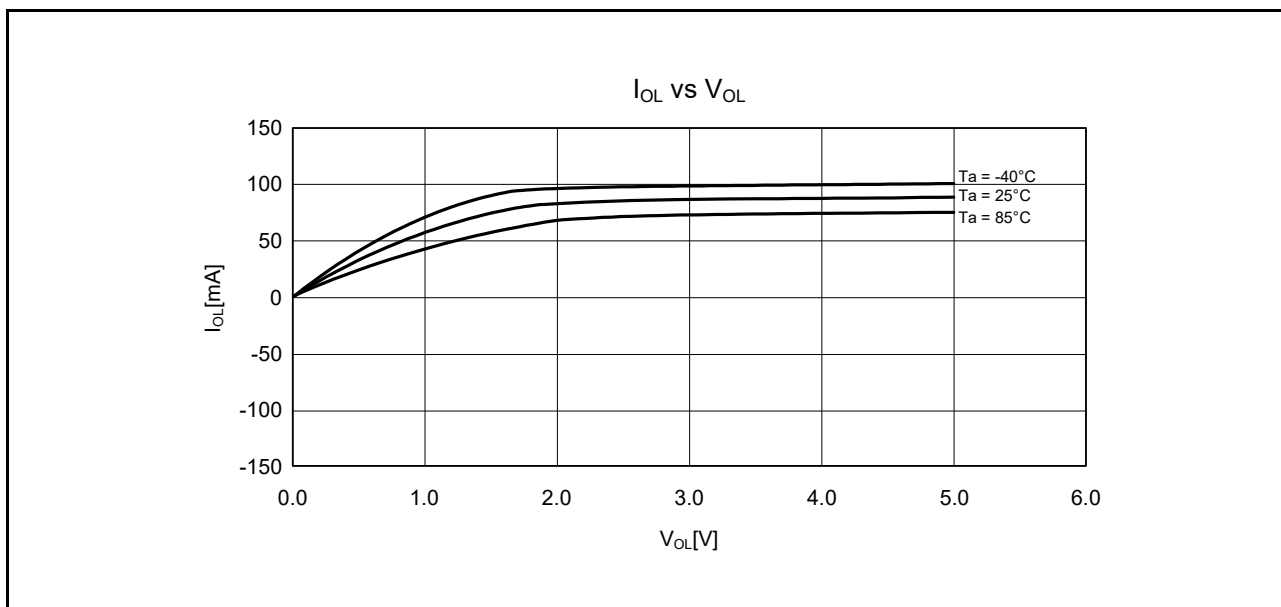


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 5.0$ V (Reference Data)

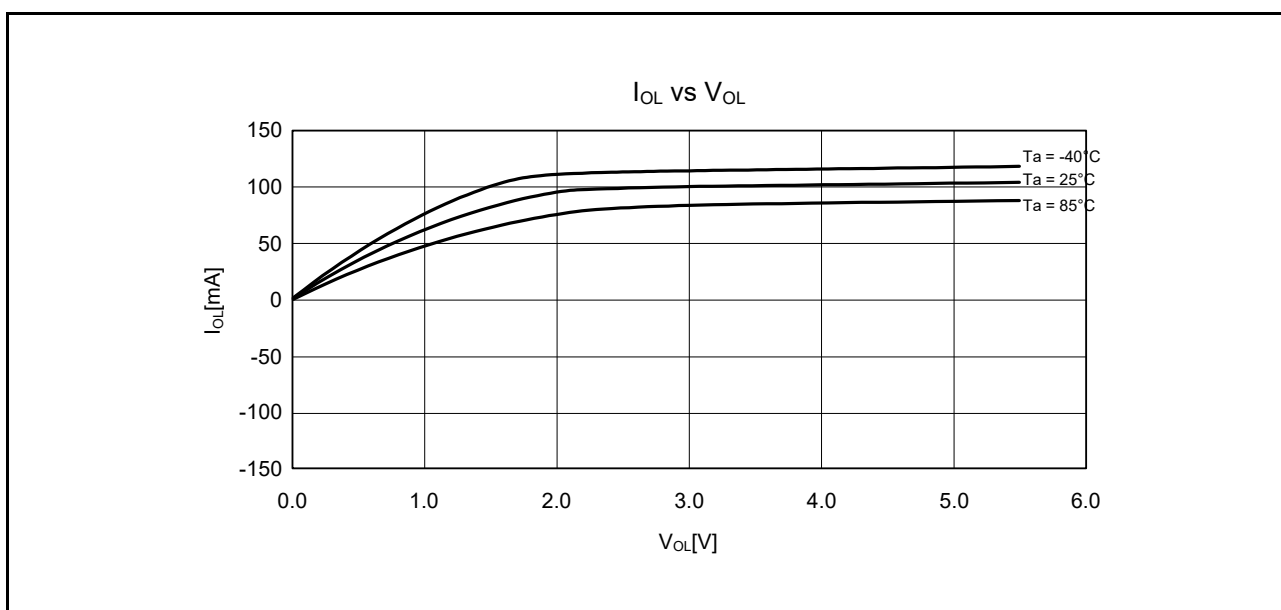


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 5.5$ V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.14 Operating Frequency Value (High-Speed Operating Mode)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = VREF = VCC\text{ to }5.5\text{ V}$, $VSS = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | | Symbol | min. | typ. | max. | Unit |
|---------------------|---------------------------------|------------|------|------|------|------|
| Operating frequency | System clock (ICLK) | f_{\max} | — | — | 80 | MHz |
| | FlashIF clock (FCLK)*1, *2 | | — | — | 32 | |
| | Peripheral module clock (PCLKA) | | — | — | 80 | |
| | Peripheral module clock (PCLKB) | | — | — | 40 | |
| | Peripheral module clock (PCLKD) | | — | — | 40 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK should be $\pm 3.5\%$.

Table 5.15 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = VREF = VCC\text{ to }5.5\text{ V}$, $VSS = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | | Symbol | min. | typ. | max. | Unit |
|---------------------|---------------------------------|------------|------|------|------|------|
| Operating frequency | System clock (ICLK) | f_{\max} | — | — | 12 | MHz |
| | FlashIF clock (FCLK)*1, *2 | | — | — | 12 | |
| | Peripheral module clock (PCLKA) | | — | — | 12 | |
| | Peripheral module clock (PCLKB) | | — | — | 12 | |
| | Peripheral module clock (PCLKD) | | — | — | 12 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK should be $\pm 3.5\%$.

Table 5.16 Clock Timing

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

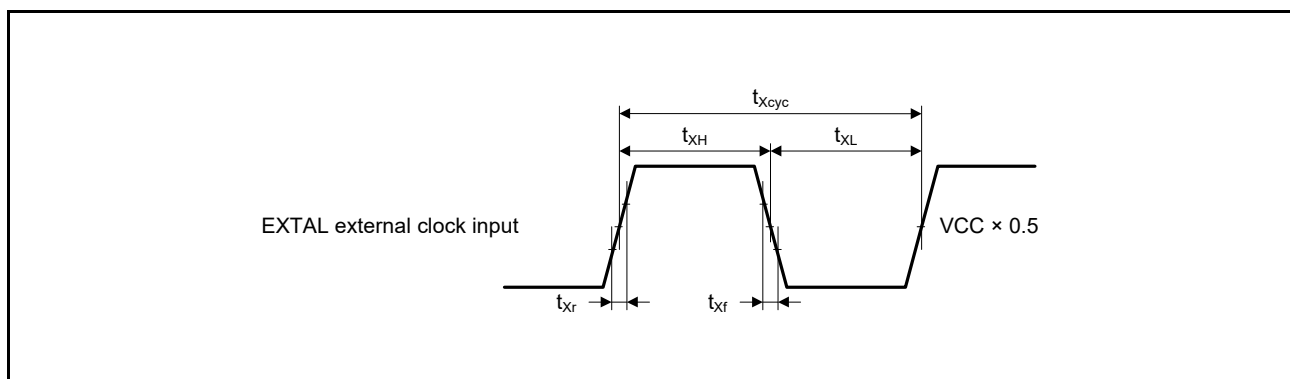
| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|-----------------------|-------|------|-------|---------------|---|
| EXTAL external clock input cycle time | t_{Xcyc} | 50 | — | — | ns | Figure 5.22 |
| EXTAL external clock input high pulse width | t_{XH} | 20 | — | — | ns | |
| EXTAL external clock input low pulse width | t_{XL} | 20 | — | — | ns | |
| EXTAL external clock rise time | t_{Xr} | — | — | 5 | ns | |
| EXTAL external clock fall time | t_{Xf} | — | — | 5 | ns | |
| EXTAL external clock input wait time*1 | t_{XWT} | 0.5 | — | — | μs | Figure 5.23 |
| Main clock oscillator oscillation frequency | f_{MAIN} | 1 | — | 20 | MHz | |
| Main clock oscillation stabilization time (crystal)*2 | $t_{MAINOSC}$ | — | 3 | — | ms | Figure 5.23 |
| Main clock oscillation stabilization time (ceramic resonator)*2 | $t_{MAINOSC}$ | — | 50 | — | μs | |
| LOCO clock oscillation frequency | f_{LOCO} | 3.44 | 4.0 | 4.56 | MHz | Figure 5.24 |
| LOCO clock oscillation stabilization time | t_{LOCO} | — | — | 0.5 | μs | |
| HOCO clock oscillation frequency | f_{HOCO} (32MHz) | 31.52 | 32 | 32.48 | MHz | $T_a = -40\text{ to }-20^\circ\text{C}$ |
| | | 31.68 | 32 | 32.32 | MHz | $T_a = -20\text{ to }+75^\circ\text{C}$ |
| | | 31.52 | 32 | 32.48 | MHz | $T_a = +75\text{ to }+85^\circ\text{C}$ |
| | f_{HOCO} (64MHz) | 63.04 | 64 | 64.96 | MHz | $T_a = -40\text{ to }-20^\circ\text{C}$ |
| | | 63.36 | 64 | 64.64 | MHz | $T_a = -20\text{ to }+75^\circ\text{C}$ |
| | | 63.04 | 64 | 64.96 | MHz | $T_a = +75\text{ to }+85^\circ\text{C}$ |
| HOCO clock oscillation stabilization time | t_{HOCO} (32MHz) | — | — | 37.1 | μs | Figure 5.26 |
| | t_{HOCO} (64MHz) | — | — | 80.6 | μs | Figure 5.26 |
| IWDT-dedicated clock oscillation frequency | f_{ILOCO} | 12.75 | 15 | 17.25 | kHz | Figure 5.27 |
| IWDT-dedicated clock oscillation stabilization time | t_{ILOCO} | — | — | 50 | μs | |
| PLL circuit oscillation frequency | f_{PLL} | 40 | — | 80 | MHz | Figure 5.28 |
| PLL clock oscillation stabilization time | t_{PLL} | — | — | 50 | μs | |
| PLL free-running oscillation frequency | f_{PLLFR} | — | 8 | — | MHz | |

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.

When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.

After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that it has become 1, and then start using the main clock.

**Figure 5.22 EXTAL External Clock Input Timing**

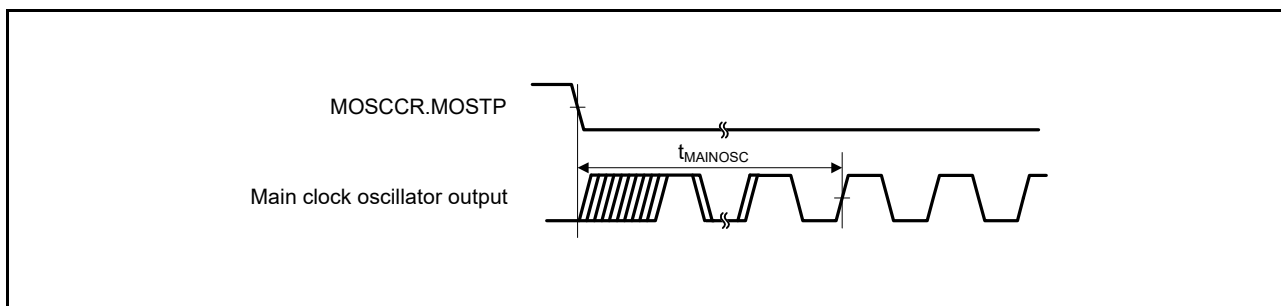


Figure 5.23 Main Clock Oscillation Start Timing

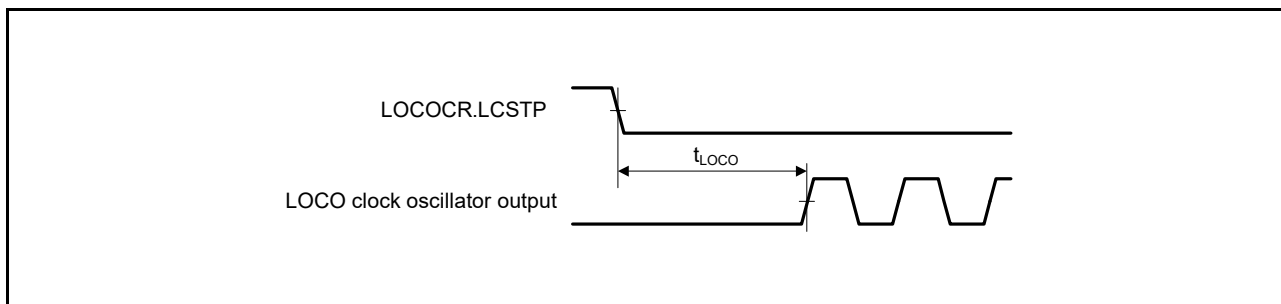


Figure 5.24 LOCO Clock Oscillation Start Timing

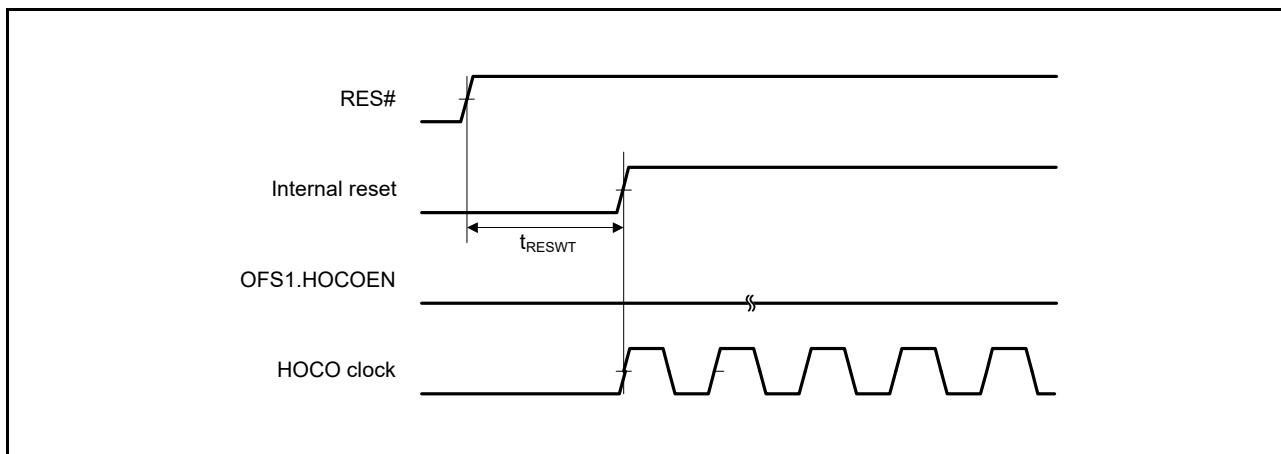


Figure 5.25 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

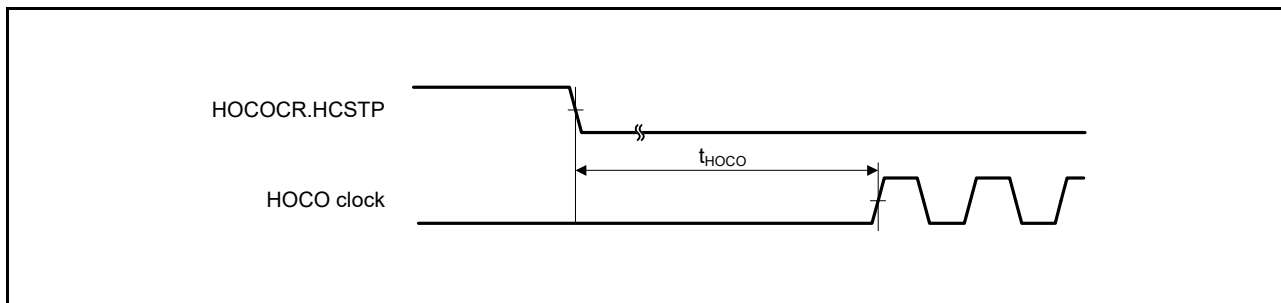


Figure 5.26 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOEN.HCSTP Bit)

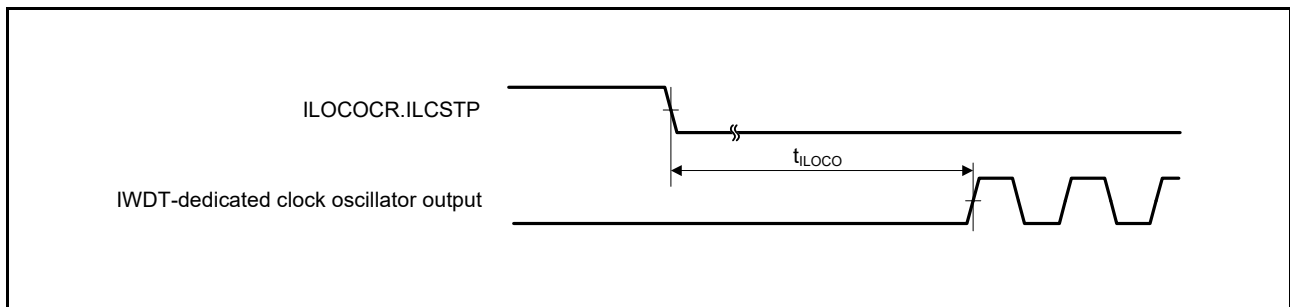


Figure 5.27 IWDt-Dedicated Clock Oscillation Start Timing

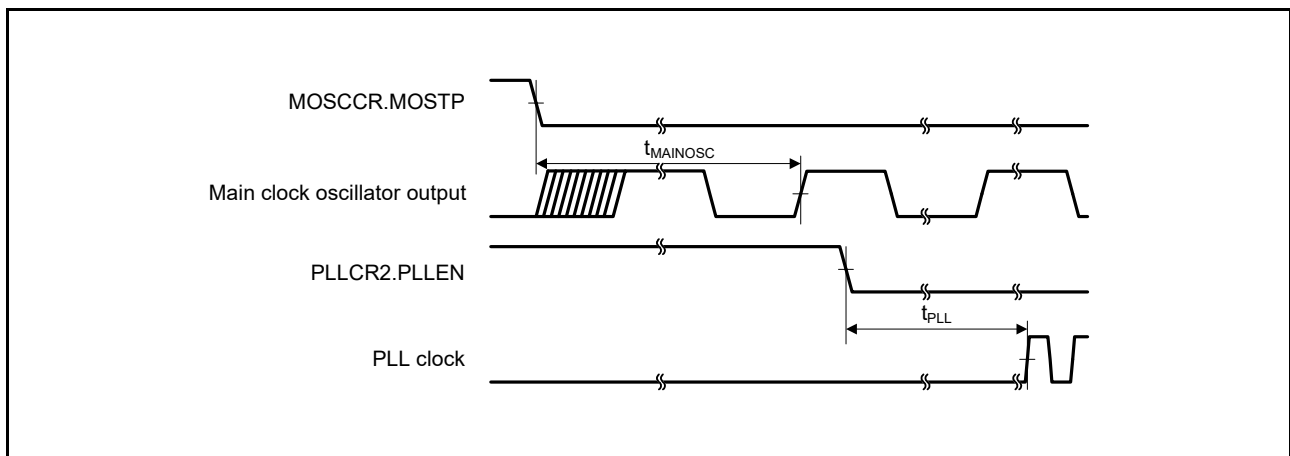


Figure 5.28 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

5.3.2 Reset Timing

Table 5.17 Reset Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|------------------|---------------------|------|------|------|------------------|-----------------|
| RES# pulse width | At power-on | t _{RESWP} | 3 | — | — | ms | Figure 5.29 |
| | Other than above | t _{RESW} | 30 | — | — | μs | Figure 5.30 |
| Wait time after RES# cancellation (at power-on) | | t _{RESWT} | — | 27.5 | — | ms | Figure 5.29 |
| Wait time after RES# cancellation (during powered-on state) | | t _{RESWT} | — | 114 | — | μs | Figure 5.30 |
| Independent watchdog timer reset period | | t _{RESWIW} | — | 1 | — | IWDT clock cycle | Figure 5.31 |
| Software reset period | | t _{RESWSW} | — | 1 | — | ICLK cycle | |
| Wait time after independent watchdog timer reset cancellation*1 | | t _{RESW2} | — | 300 | — | μs | |
| Wait time after software reset cancellation | | t _{RESW2} | — | 168 | — | μs | |

Note 1. When IWDTCR.CKS[3:0] = 0000b.

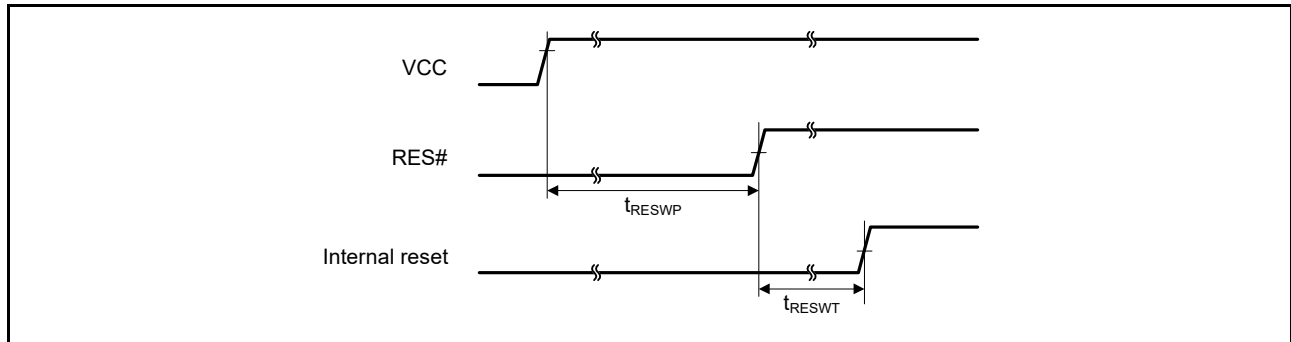


Figure 5.29 Reset Input Timing at Power-On

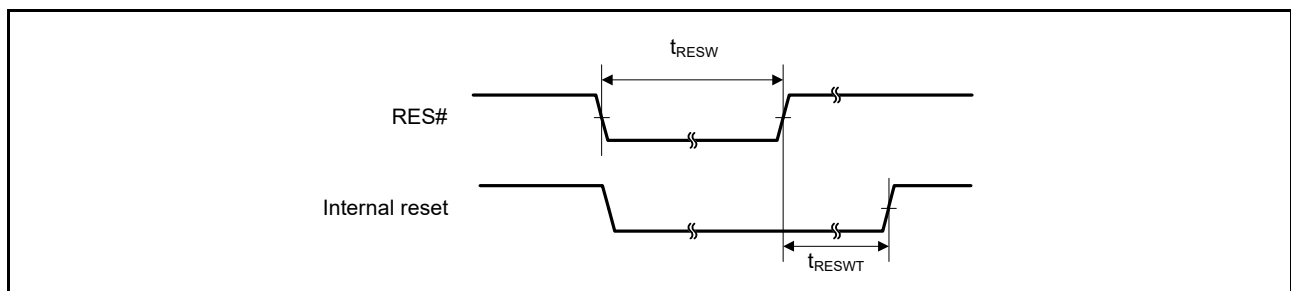


Figure 5.30 Reset Input Timing (1)

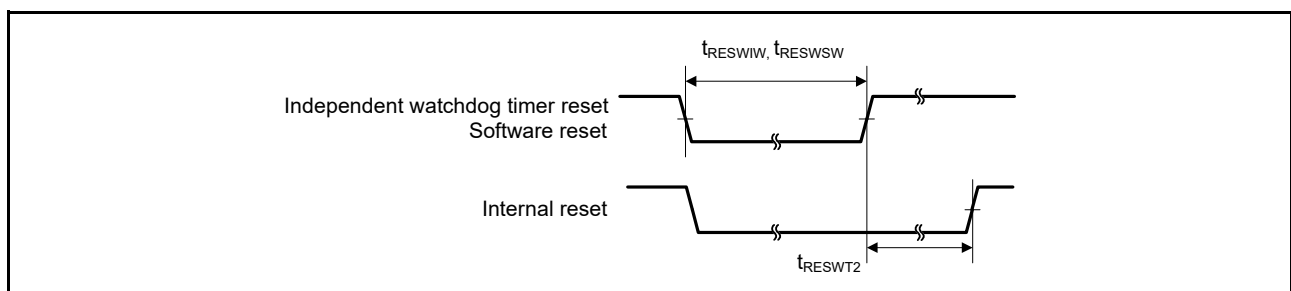


Figure 5.31 Reset Input Timing (2)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | | |
|--|---|---|---|--------------------|------|------|-----------------|----|-------------|
| Recovery time from software standby mode*1 | High-speed mode | Crystal connected to main clock oscillator | Main clock oscillator operating*2 | t _{SBYMC} | — | 2 | 3 | ms | Figure 5.32 |
| | | | Main clock oscillator and PLL circuit operating*3 | t _{SBYPC} | — | 2 | 3 | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating*4 | t _{SBYEX} | — | 35 | 50 | μs | | |
| | | Main clock oscillator and PLL circuit operating*5 | t _{SBYPE} | — | 70 | 95 | μs | | |
| | HOCO clock operation | HOCO clock oscillator operation 1*6 | t _{SBYHO} | — | 40 | 55 | μs | | |
| | | | | — | 75 | 90 | μs | | |
| | | HOCO clock oscillator, PLL circuit operation*8 | t _{SBYPH} | — | 110 | 130 | μs | | |
| | LOCO clock oscillator operating*9 | t _{SBYLO} | — | 40 | 55 | μs | | | |

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of crystal is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 80 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 4. When the frequency of the external clock is 20 MHz.

When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 80 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK and PCLKA are set to 64 MHz, and the frequencies of PCLKB, PCLKD, and FCLK are set to 32 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK and PCLKA are set to 80 MHz, the frequencies of PCLKB and PCLKD are set to 40 MHz, and the frequency of FCLK is set to 20MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | | |
|--|---|---|---|-------------|------|---------------|-----------------|----|-------------|
| Recovery time from software standby mode*1 | Middle-speed mode | Crystal connected to main clock oscillator | Main clock oscillator operating*2 | t_{SBYMC} | — | 2 | 3 | ms | Figure 5.32 |
| | | | Main clock oscillator and PLL circuit operating*3 | t_{SBYPC} | — | 2 | 3 | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating*4 | t_{SBYEX} | — | 3 | 4 | μs | | |
| | | Main clock oscillator and PLL circuit operating*5 | t_{SBYPE} | — | 65 | 85 | μs | | |
| | HOCO clock oscillator operating | HOCO clock oscillator operating 1*6 | t_{SBYHO} | — | 40 | 50 | μs | | |
| | | HOCO clock oscillator operating 2*7 | | — | 75 | 85 | μs | | |
| | | HOCO clock oscillator and PLL circuit operating*8 | t_{SBYPH} | — | 110 | 125 | μs | | |
| | LOCO clock oscillator operating*9 | t_{SBYLO} | — | 5 | 7 | μs | | | |

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 48 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 4. When the frequency of the external clock is 12 MHz.

When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 48 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 10 MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

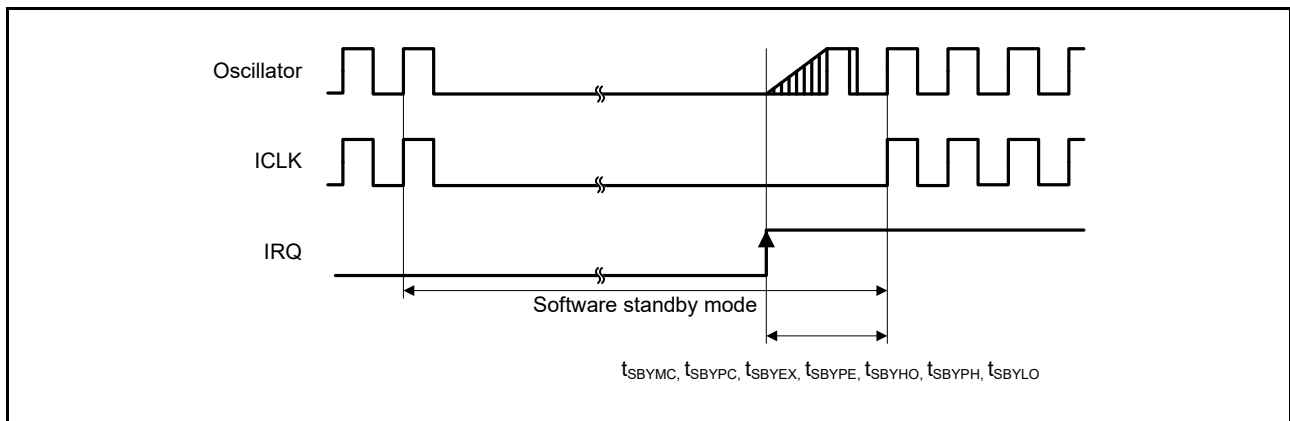


Figure 5.32 Software Standby Mode Recovery Timing

Table 5.20 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------------------------------|---------------------|------|------|------|------|-----------------|
| Recovery time from deep sleep mode*1 | High-speed mode*2 | — | 2 | 3.5 | μs | Figure 5.33 |
| | Middle-speed mode*3 | — | 3 | 4 | μs | |

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 32 MHz.

Note 3. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 12 MHz.

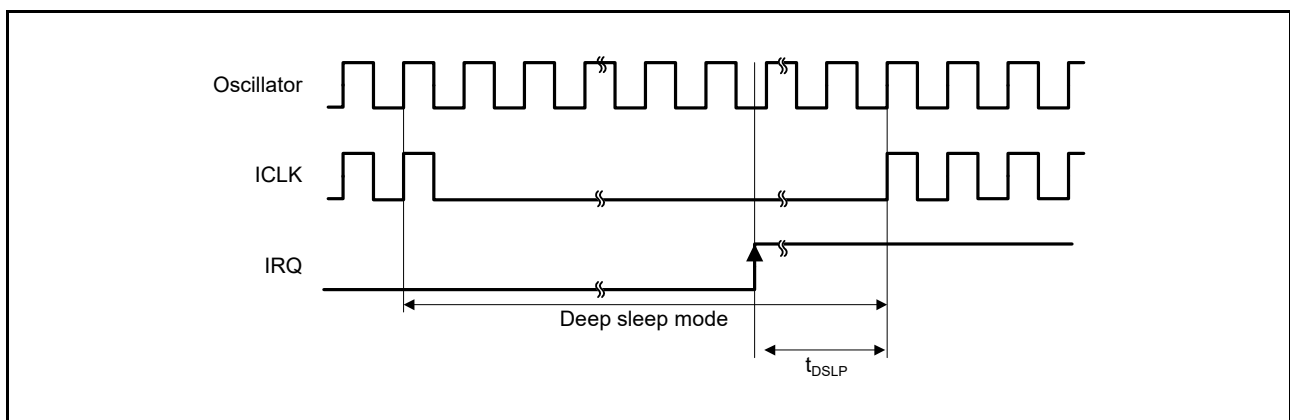


Figure 5.33 Deep Sleep Mode Recovery Timing

Table 5.21 Operating Mode Transition Time

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = -40 to +85°C

| Mode before Transition | Mode after Transition | ICLK Frequency | Transition Time | | | Unit |
|------------------------------|------------------------------|----------------|-----------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| High-speed operating mode | Middle-speed operating modes | 8 MHz | — | 10 | — | μs |
| Middle-speed operating modes | High-speed operating mode | 8 MHz | — | 37.5 | — | μs |

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK are not divided.

5.3.4 Control Signal Timing

Table 5.22 Control Signal Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|-----------------|-------------------|--|------|------|------|---|---------------------------------|
| NMI pulse width | t _{NMIW} | 200 | — | — | ns | NMI digital filter disabled (NMIFLTE.NFLTEN = 0) | t _{Pcyc} × 2 ≤ 200 ns |
| | | t _{Pcyc} × 2* ¹ | — | — | | | t _{Pcyc} × 2 > 200 ns |
| | | 200 | — | — | | NMI digital filter enabled (NMIFLTE.NFLTEN = 1) | t _{NMICK} × 3 ≤ 200 ns |
| | | t _{NMICK} × 3.5* ² | — | — | | | t _{NMICK} × 3 > 200 ns |
| IRQ pulse width | t _{IRQW} | 200 | — | — | ns | IRQ digital filter disabled (IRQFLTE0.FLTENi = 0) | t _{Pcyc} × 2 ≤ 200 ns |
| | | t _{Pcyc} × 2* ¹ | — | — | | | t _{Pcyc} × 2 > 200 ns |
| | | 200 | — | — | | IRQ digital filter enabled (IRQFLTE0.FLTENi = 1) | t _{IRQCK} × 3 ≤ 200 ns |
| | | t _{IRQCK} × 3.5* ³ | — | — | | | t _{IRQCK} × 3 > 200 ns |

Note: 200 ns minimum in software standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

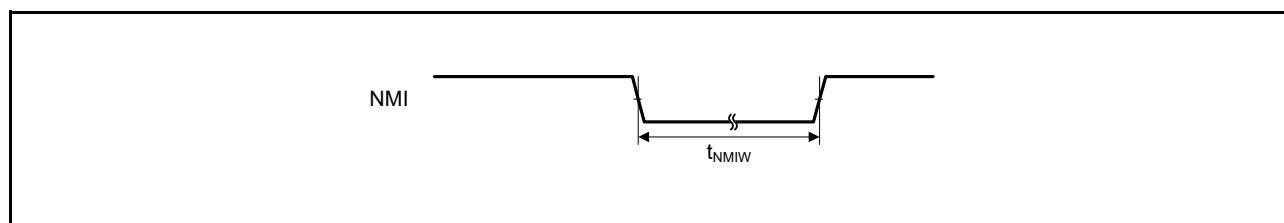


Figure 5.34 NMI Interrupt Input Timing

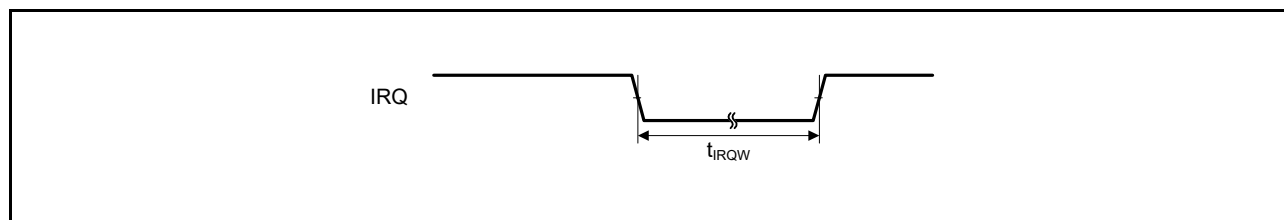


Figure 5.35 IRQ Interrupt Input Timing

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.23 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit *1 | Test Conditions | |
|----------------------------------|------------------------------------|--|--|--|----------------------|--------------------|--------------------|-------------|
| I/O ports | Input data pulse width | | t _{PRW} | 1.5 | — | t _{Pcyc} | Figure 5.36 | |
| MTU3 | Input capture input pulse width | Single-edge setting | t _{TICW} | 3 | — | t _{PAcyc} | Figure 5.37 | |
| | | Both-edge setting | | 5 | — | | | |
| | Timer clock pulse width | Single-edge setting | t _{TCKWH} , t _{TCKWL} | 3 | — | t _{PAcyc} | Figure 5.38 | |
| Both-edge setting | | 5 | | — | | | | |
| Phase counting mode | | 5 | | — | | | | |
| POE3 | POE# input pulse width | | t _{POEW} | 1.5 | — | t _{Pcyc} | Figure 5.39 | |
| GPT | Input capture input pulse width | Single-edge setting | t _{GTICW} | 1.5 | — | t _{PAcyc} | Figure 5.40 | |
| | | Both-edge setting | | 2.5 | — | | | |
| | External trigger input pulse width | Single-edge setting | t _{GTETW} | 1.5 | — | t _{PAcyc} | Figure 5.41 | |
| | | Both-edge setting | | 2.5 | — | | | |
| Timer clock pulse width | | | t _{GTCKWH} | 1.5 | — | t _{PAcyc} | Figure 5.42 | |
| | | | t _{GTCKWL} | | | | | |
| TMR | Timer clock pulse width | Single-edge setting | t _{TMCWH} , t _{TMCWL} | 1.5 | — | t _{Pcyc} | Figure 5.43 | |
| | | Both-edge setting | | 2.5 | — | | | |
| SCI | Input clock cycle | Asynchronous | t _{Scyc} | 4 | — | t _{Pcyc} | Figure 5.44 | |
| | | Clock synchronous | | 6 | — | | | |
| | Input clock pulse width | | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} | |
| | Input clock rise time | | | t _{SCKr} | — | 20 | ns | |
| | Input clock fall time | | | t _{SCKf} | — | 20 | ns | |
| | Output clock cycle | Asynchronous | t _{Scyc} | t _{Scyc} | 16 | — | t _{Pcyc} | Figure 5.45 |
| | | Clock synchronous | | | 4 | — | | |
| | Output clock pulse width | | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} | |
| | Output clock rise time | | | t _{SCKr} | — | 20 | ns | |
| | Output clock fall time | | | t _{SCKf} | — | 20 | ns | |
| | Transmit data delay time (master) | Clock synchronous | | t _{TXD} | — | 40 | ns | |
| | | Transmit data delay time (slave) | Clock synchronous | | VCC = 4.0 V or above | — | 40 | ns |
| | VCC = 2.7 V or above | | | — | 65 | ns | | |
| Receive data setup time (master) | Clock synchronous | Clock synchronous | t _{RXS} | VCC = 4.0 V or above | 40 | — | ns | |
| | | | | VCC = 2.7 V or above | 65 | — | ns | |
| Receive data setup time (slave) | Clock synchronous | | | 40 | — | ns | | |
| Receive data hold time | Clock synchronous | | t _{RXH} | 40 | — | ns | | |
| A/D converter | Trigger input pulse width | | t _{TRGW} | 1.5 | — | t _{Pcyc} | Figure 5.46 | |
| CAC | CACREF input pulse width | t _{Pcyc} ≤ t _{cac} ^{*2} | t _{CACREF} | 4.5 t _{cac} + 3 t _{Pcyc} | — | ns | | |
| | | t _{Pcyc} > t _{cac} ^{*2} | | 5 t _{cac} + 6.5 t _{Pcyc} | | | | |

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

Note 2. t_{cac}: CAC count clock source cycle

Table 5.24 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C, C = 30pF

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|------------------------------------|-------------------|---|--|---|--|-------------------|----------------------------|
| RSPI | RSPCK clock cycle | Master | t _{SPcyc} | 2 | 4096 | t _{Pcyc} | Figure 5.47 |
| | | Slave | | 6 | — | | |
| RSPCK clock high pulse width | Master | VCC = 4.0 V or above | t _{SPCKWH} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$ | — | ns | |
| | | VCC = 2.7 V or above | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$ | — | | |
| | Slave | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$ | | — | | | |
| RSPCK clock low pulse width | Master | VCC = 4.0 V or above | t _{SPCKWL} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$ | — | ns | |
| | | VCC = 2.7 V or above | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$ | — | | |
| | Slave | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$ | | — | | | |
| RSPCK clock rise/fall time | Output | VCC = 4.0 V or above | t _{SPCKr} t _{SPCKf} | — | 6 | ns | |
| | | VCC = 2.7 V or above | | — | 10 | | |
| | Input | — | | 0.1 | μs/V | | |
| Data input setup time | Master | VCC = 4.0 V or above | t _{SU} | 10 | — | ns | Figure 5.48 to Figure 5.51 |
| | | VCC = 2.7 V or above | | 26 | — | | |
| | Slave | 20 | | — | | | |
| Data input hold time | Master | RSPCK set to a division ratio other than PCLKB divided by 2 | t _H | t _{Pcyc} | — | ns | |
| | | RSPCK set to PCLKB divided by 2 | | t _{HF} | 0 | | |
| | Slave | t _H | 0 | — | | | |
| SSL setup time | Master | | t _{LEAD} | -30 + N*2 × t _{SPcyc} | — | ns | |
| | Slave | | | 6 | — | t _{Pcyc} | |
| SSL hold time | Master | | t _{LAG} | -30 + N*3 × t _{SPcyc} | — | ns | |
| | Slave | | | 6 | — | t _{Pcyc} | |
| Data output delay time | Master | VCC = 4.0 V or above | t _{OD} | — | 10 | ns | |
| | | VCC = 2.7 V or above | | — | 14 | | |
| | Slave | — | | 65 | | | |
| Data output hold time | Master | | t _{OH} | 0 | — | ns | |
| | Slave | | | 0 | — | | |
| Successive transmission delay time | Master | | t _{TD} | t _{SPcyc} + 2 × t _{Pcyc} | 8 × t _{SPcyc} + 2 × t _{Pcyc} | ns | |
| | Slave | | | 6 × t _{Pcyc} | — | | |
| MOSI and MISO rise/fall time | Output | | t _{Dr} , t _{Df} | — | 10 | ns | |
| | Input | | | — | 1 | μs | |
| SSL rise/fall time | Output | | t _{SSLr} t _{SSLf} | — | 10 | ns | |
| | Input | | | — | 1 | μs | |
| Slave access time | | | t _{SA} | — | 6 | t _{Pcyc} | Figure 5.50, |
| Slave output release time | | | t _{REL} | — | 5 | t _{Pcyc} | Figure 5.51 |

Note 1. t_{Pcyc}: PCLK cycle

Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)

Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C, C = 30pF

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | |
|---------------------------|---------------------------------------|---|----------------------|-------------------|--------------------------|-----------------|--------------------------|
| Simple SPI | SCK clock cycle output (master) | t _{SPcyc} | 4 | 65536 | t _{Pcyc} | Figure 5.47 | |
| | SCK clock cycle input (slave) | | 6 | — | t _{Pcyc} | | |
| | SCK clock high pulse width | t _{SPCKWH} | 0.4 | 0.6 | t _{SPcyc} | | |
| | SCK clock low pulse width | t _{SPCKWL} | 0.4 | 0.6 | t _{SPcyc} | | |
| | SCK clock rise/fall time | t _{SPCKr} , t _{SPCKf} | — | 20 | ns | | |
| | Data input setup time (master) | VCC = 4.0 V or above | t _{SU} | 40 | — | ns | Figure 5.48, Figure 5.49 |
| | | VCC = 2.7 V or above | | 65 | — | | |
| | Data input setup time (slave) | 40 | | — | | | |
| | Data input hold time | t _H | 40 | — | ns | | |
| | SS input setup time | t _{LEAD} | 3 | — | t _{SPcyc} | | |
| | SS input hold time | t _{LAG} | 3 | — | t _{SPcyc} | | |
| | Data output delay time (master) | t _{OD} | — | 40 | ns | | |
| | Data output delay time (slave) | | VCC = 4.0 V or above | — | | 40 | |
| | | | VCC = 2.7 V or above | — | | 65 | |
| | Data output hold time | Master | t _{OH} | -10 | — | ns | |
| Slave | | -10 | | — | | | |
| Data rise/fall time | t _{Dr} , t _{Df} | — | 20 | ns | | | |
| SS input rise/fall time | t _{SSLr} , t _{SSLf} | — | 20 | ns | | | |
| Slave access time | t _{SA} | — | 6 | t _{Pcyc} | Figure 5.50, Figure 5.51 | | |
| Slave output release time | t _{REL} | — | 6 | t _{Pcyc} | | | |

Note 1. t_{Pcyc}: PCLK cycle

Table 5.26 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | Symbol | Min. *1, *2 | Max. | Unit | Test Conditions | |
|--------------------------------|-------------------------------------|-------------------|-------------------------------------|-----------------------------|-----------------|-------------|
| RIIC (Standard mode, SMBus) | SCL cycle time | t _{SCL} | 6 (12) × t _{IICcyc} + 1300 | — | ns | Figure 5.52 |
| | SCL high pulse width | t _{SCLH} | 3 (6) × t _{IICcyc} + 300 | — | ns | |
| | SCL low pulse width | t _{SCLL} | 3 (6) × t _{IICcyc} + 300 | — | ns | |
| | SCL, SDA rise time | t _{Sr} | — | 1000 | ns | |
| | SCL, SDA fall time | t _{Sf} | — | 300 | ns | |
| | SCL, SDA spike pulse removal time | t _{SP} | 0 | 1 (4) × t _{IICcyc} | ns | |
| | SDA bus free time | t _{BUF} | 3 (6) × t _{IICcyc} + 300 | — | ns | |
| | START condition hold time | t _{STAH} | t _{IICcyc} + 300 | — | ns | |
| | Repeated START condition setup time | t _{STAS} | 1000 | — | ns | |
| | STOP condition setup time | t _{STOS} | 1000 | — | ns | |
| | Data setup time | t _{SDAS} | t _{IICcyc} + 50 | — | ns | |
| | Data hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |
| RIIC (Fast mode) | SCL cycle time | t _{SCL} | 6 (12) × t _{IICcyc} + 600 | — | ns | Figure 5.52 |
| | SCL high pulse width | t _{SCLH} | 3 (6) × t _{IICcyc} + 300 | — | ns | |
| | SCL low pulse width | t _{SCLL} | 3 (6) × t _{IICcyc} + 300 | — | ns | |
| | SCL, SDA rise time | t _{Sr} | — | 300 | ns | |
| | SCL, SDA fall time | t _{Sf} | — | 300 | ns | |
| | SCL, SDA spike pulse removal time | t _{SP} | 0 | 1 (4) × t _{IICcyc} | ns | |
| | SDA bus free time | t _{BUF} | 3 (6) × t _{IICcyc} + 300 | — | ns | |
| | START condition hold time | t _{STAH} | t _{IICcyc} + 300 | — | ns | |
| | Repeated START condition setup time | t _{STAS} | 300 | — | ns | |
| | STOP condition setup time | t _{STOS} | 300 | — | ns | |
| | Data setup time | t _{SDAS} | t _{IICcyc} + 50 | — | ns | |
| | Data hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |

Note 1. t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 2. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Table 5.27 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = -40 to +85°C

| Item | | Symbol | Min.*2 | Max. | Unit | Test Conditions |
|--|------------------------------|-------------------|--------|--------------------------|------|-----------------|
| Simple I ² C (Standard mode) | SDA rise time | t _{Sr} | — | 1000 | ns | Figure 5.52 |
| | SDA fall time | t _{Sf} | — | 300 | ns | |
| | SDA spike pulse removal time | t _{SP} | 0 | 4 × t _{pcyc} *1 | ns | |
| | Data setup time | t _{SDAS} | 250 | — | ns | |
| | Data hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |
| Simple I ² C (Fast mode) | SDA rise time | t _{Sr} | — | 300 | ns | Figure 5.52 |
| | SDA fall time | t _{Sf} | — | 300 | ns | |
| | SDA spike pulse removal time | t _{SP} | 0 | 4 × t _{pcyc} *1 | ns | |
| | Data setup time | t _{SDAS} | 100 | — | ns | |
| | Data hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |

Note 1. t_{pcyc}: PCLKB cycle

Note 2. C_b is the total capacitance of the bus lines.

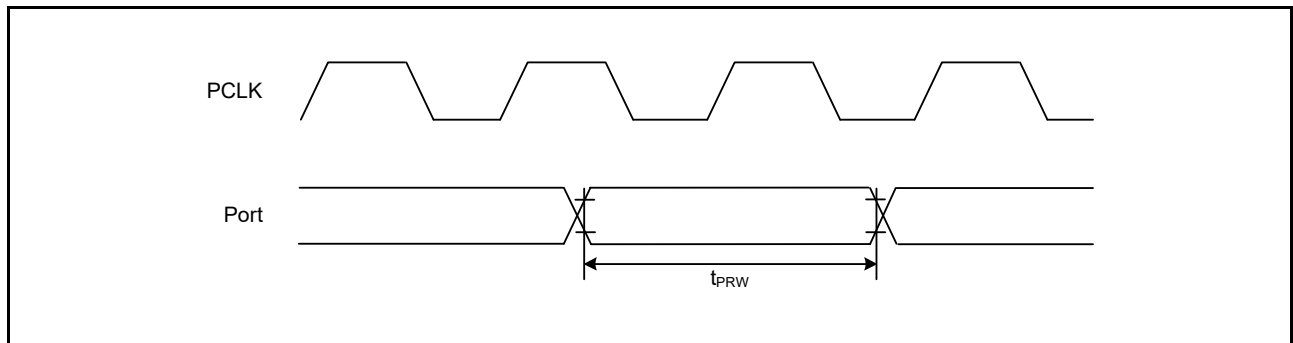


Figure 5.36 I/O Port Input Timing

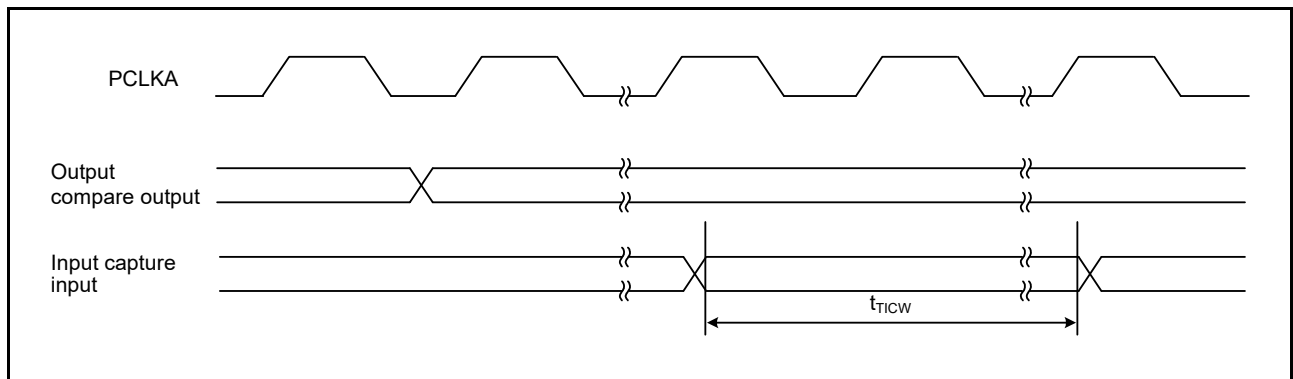


Figure 5.37 MTU3 Input/Output Timing

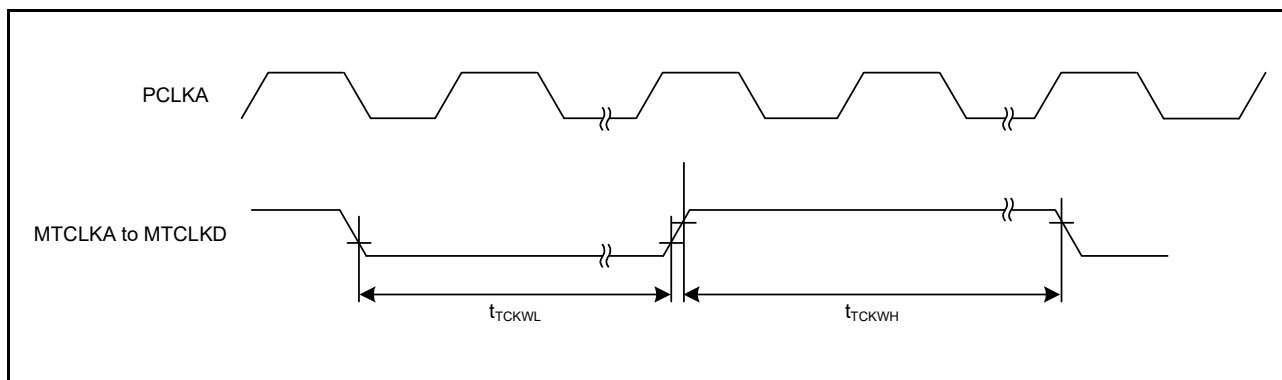


Figure 5.38 MTU3 Clock Input Timing

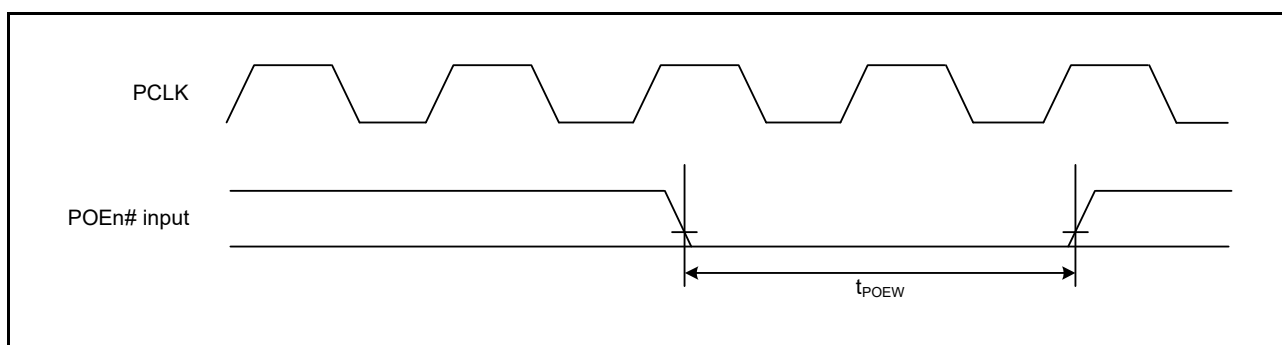


Figure 5.39 POE# Input Timing

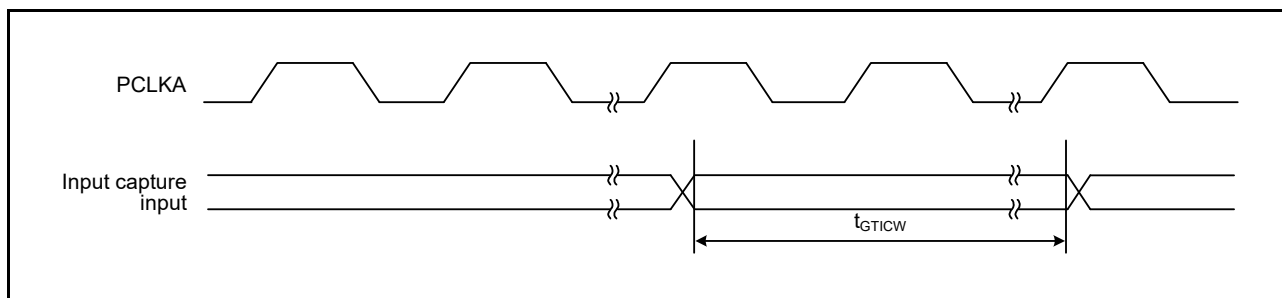


Figure 5.40 Input Timing of GPT Input Capture

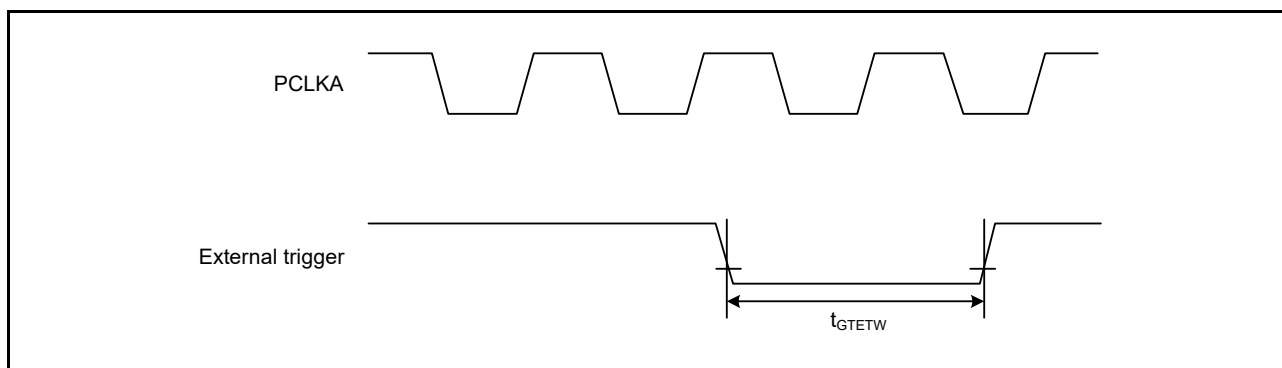


Figure 5.41 Timing of the GPT External Trigger Input

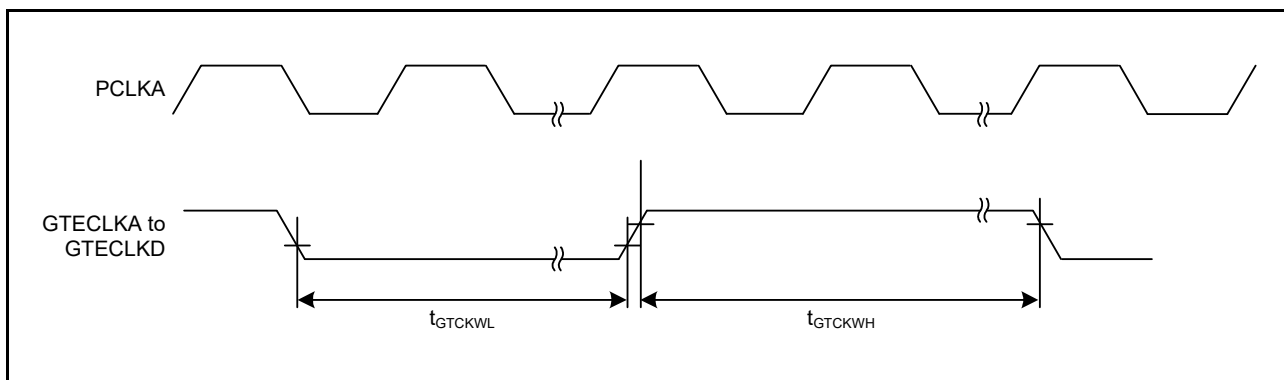


Figure 5.42 GPT Clock Input Timing

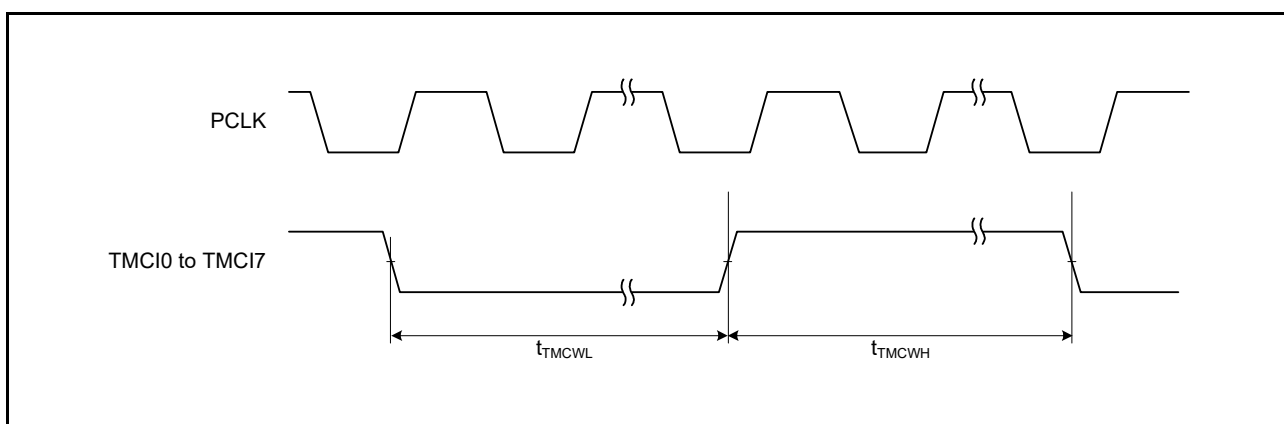


Figure 5.43 TMR Clock Input Timing

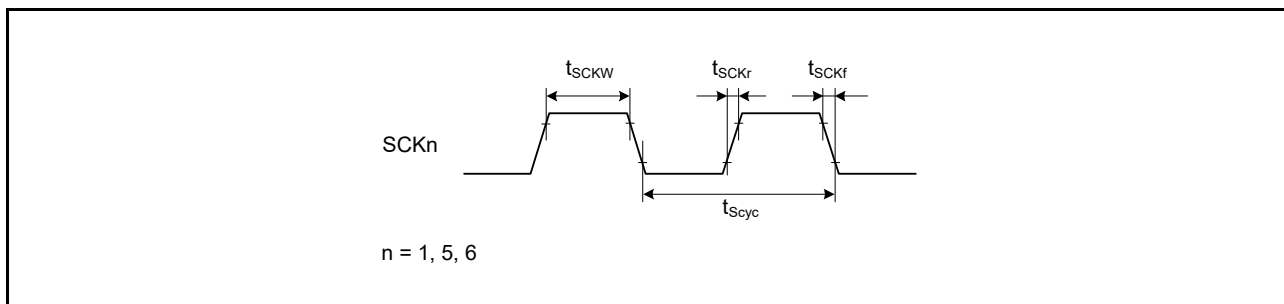


Figure 5.44 SCK Clock Input Timing

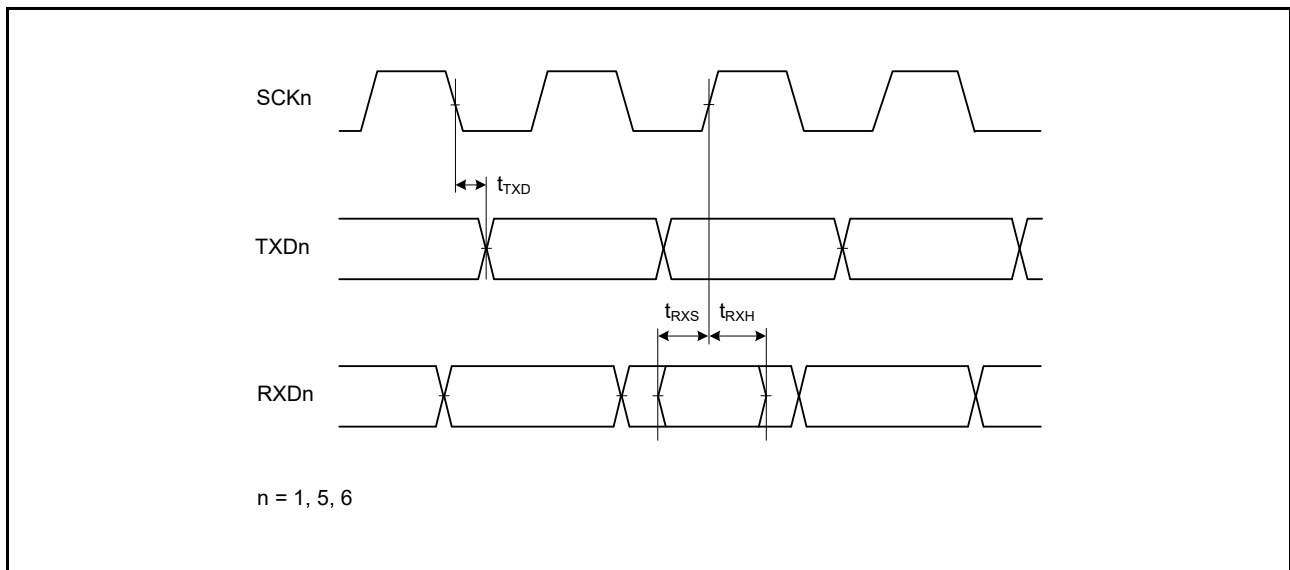


Figure 5.45 SCI Input/Output Timing: Clock Synchronous Mode

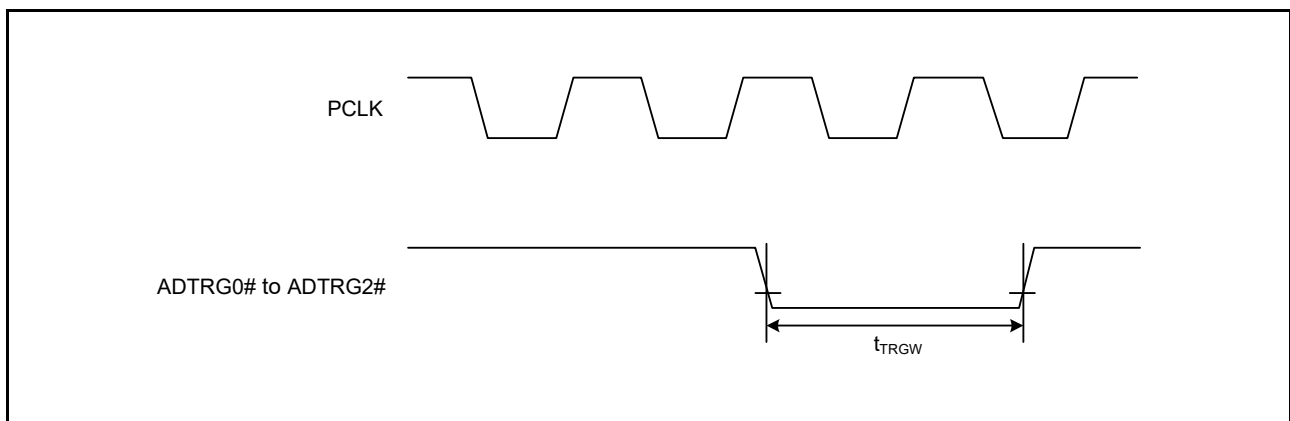


Figure 5.46 A/D Converter External Trigger Input Timing

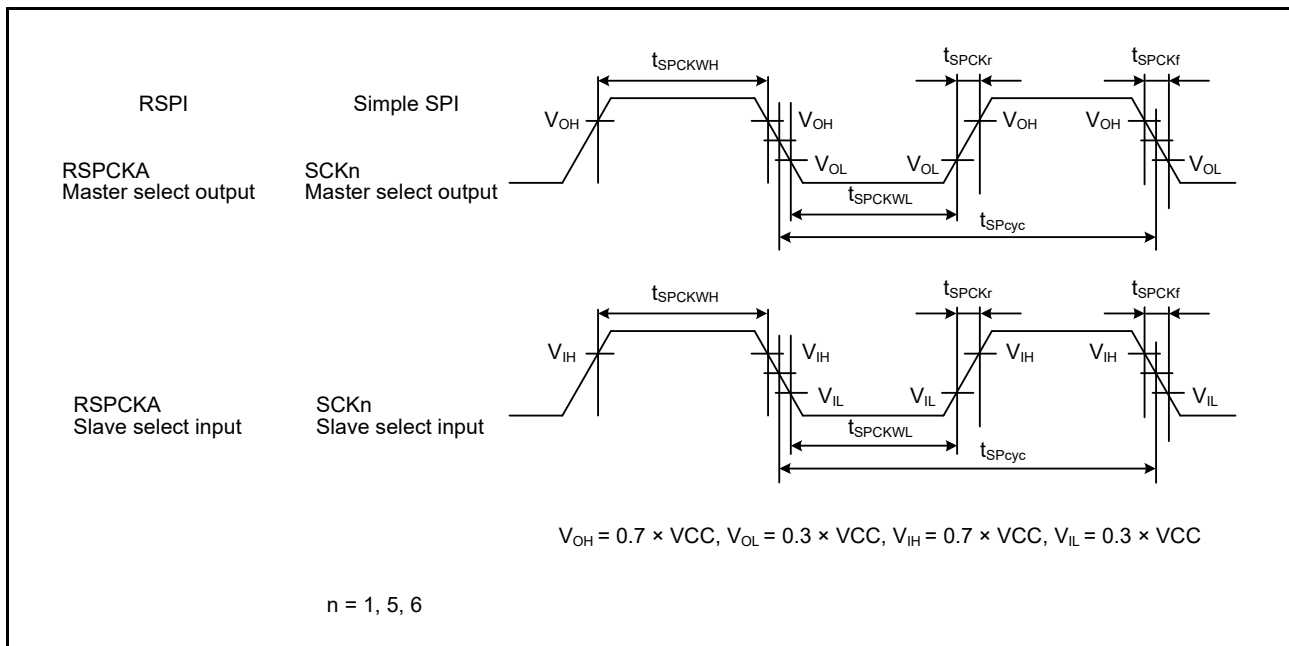


Figure 5.47 RSPI Clock Timing and Simple SPI Clock Timing

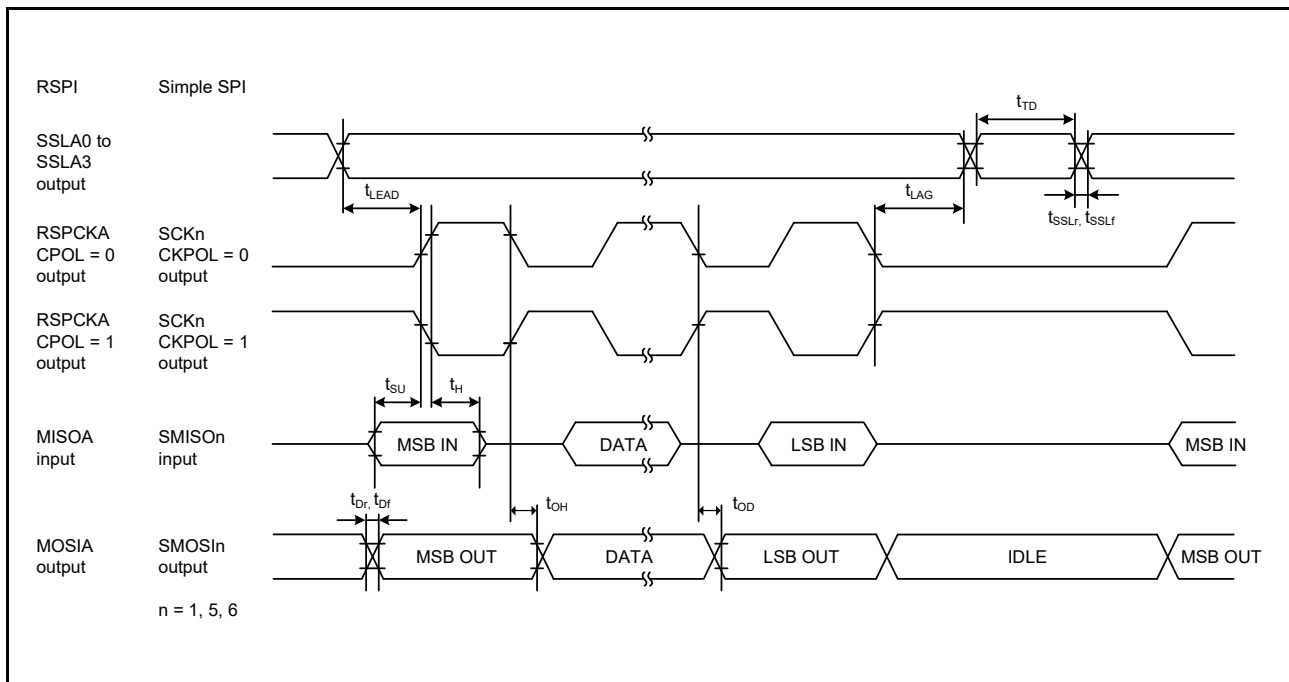


Figure 5.48 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

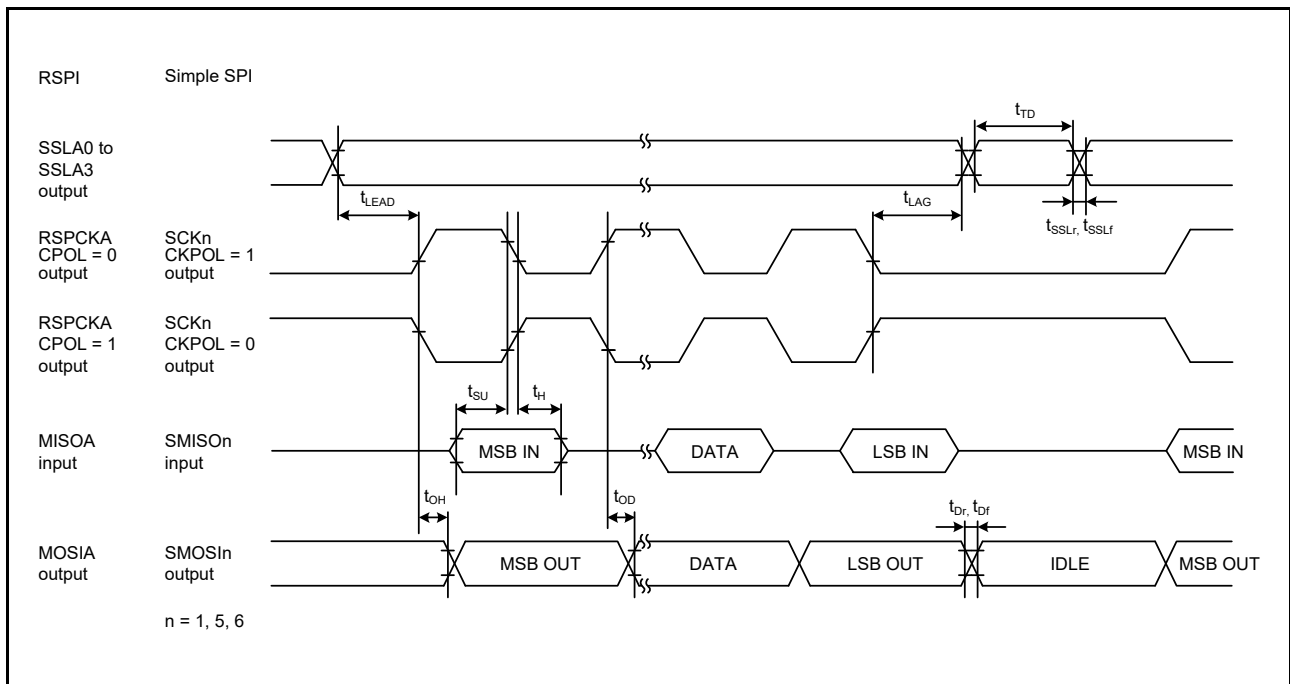


Figure 5.49 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

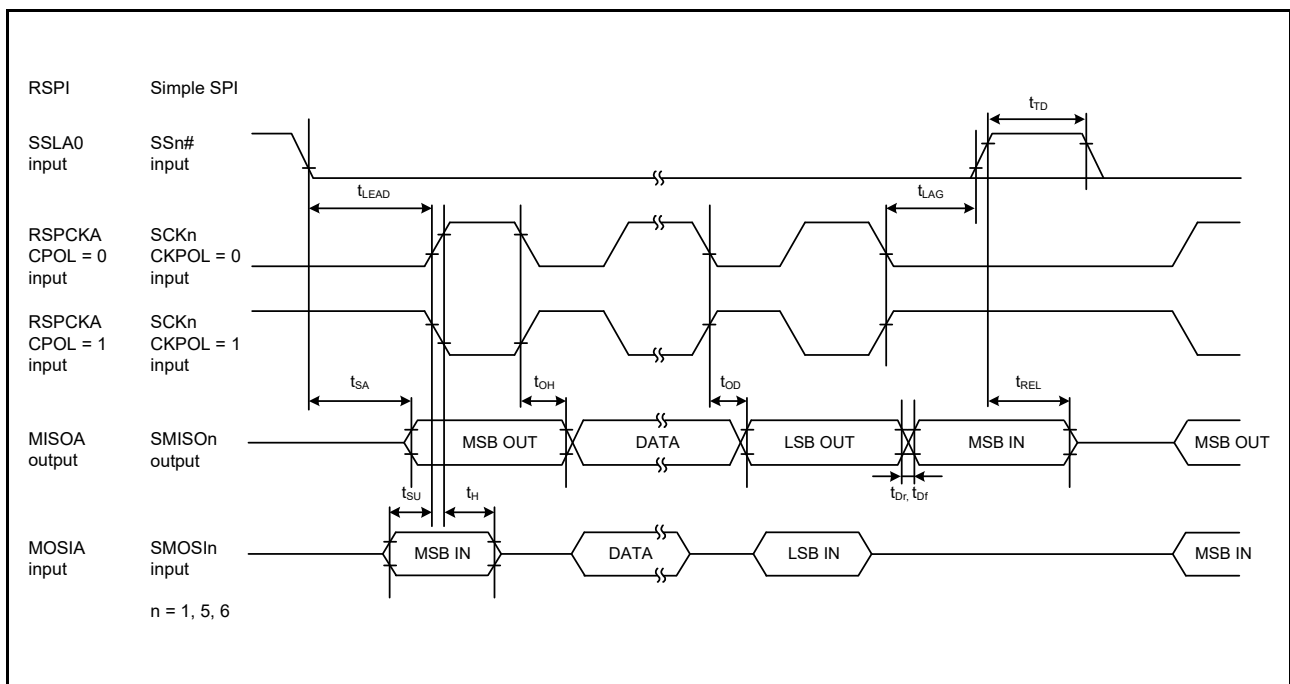


Figure 5.50 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

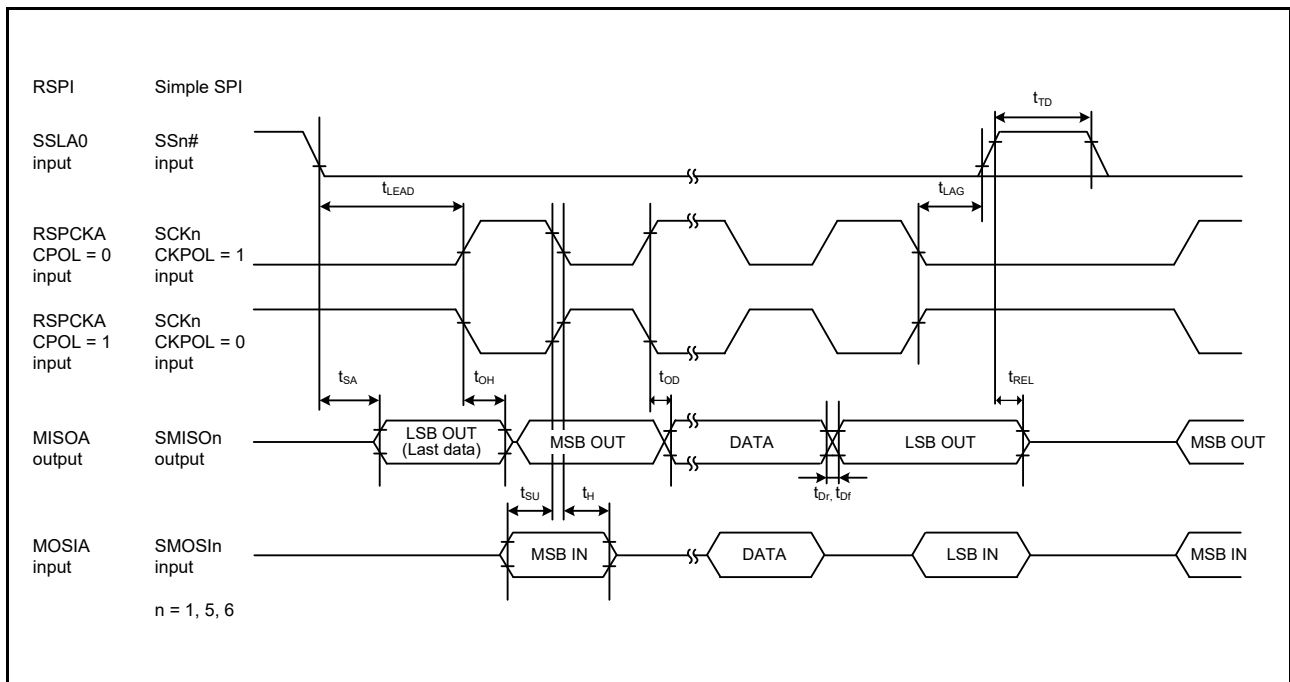


Figure 5.51 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

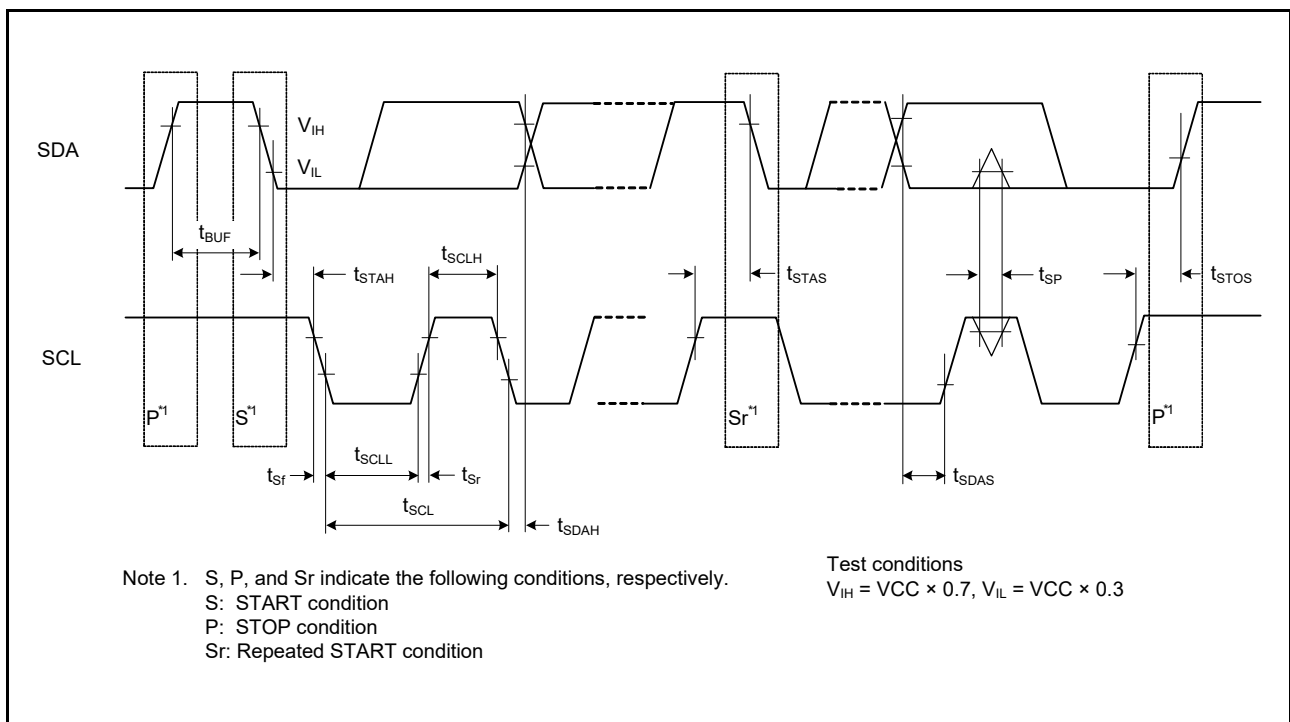


Figure 5.52 IIC Bus Interface Input/Output Timing and Simple I2C Bus Interface Input/Output Timing

5.4 A/D Conversion Characteristics

Table 5.28 A/D Conversion Characteristics (1)

Conditions: VCC = 4.5 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|------|------|------|------|---|
| Frequency | | 1 | — | 40 | MHz | |
| Resolution | | — | — | 12 | Bit | |
| Conversion time*1 (Operation at PCLKD = 40 MHz) | Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use | 1.00 | — | — | μs | High-precision channel ADSSTRn.SST[7:0] bits = 08h |
| | | 1.25 | — | — | μs | Normal-precision channel ADSSTRn.SST[7:0] bits = 12h |
| | Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit in use | 1.65 | — | — | μs | High-precision channel ADSSTRn.SST[7:0] bits = 08h ADSHCR.SSTSH[7:0] bits = 0Dh AN100 to 102 = 0.25 V to AVCC1 – 0.25 V |
| Analog input capacitance | | — | — | 12 | pF | |
| Offset error | | — | ±2.0 | ±6.5 | LSB | |
| Full-scale error | | — | ±2.0 | ±6.5 | LSB | |
| Quantization error | | — | ±0.5 | — | LSB | |
| Absolute accuracy | Sample-and-hold circuit in use | — | ±2.5 | ±8.0 | LSB | AN100 to 102 = 0.25V to AVCC1 – 0.25 |
| | Sample-and-hold circuit not in use | — | ±3.0 | ±8.0 | LSB | |
| DNL differential nonlinearity error | | — | ±0.5 | ±1.5 | LSB | |
| INL integral nonlinearity error | | — | ±1.5 | ±4.0 | LSB | |

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.29 A/D Conversion Characteristics (2)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|------|------|------|------|--|
| Frequency | | 1 | — | 40 | MHz | |
| Resolution | | — | — | 12 | Bit | |
| Conversion time*1 (Operation at PCLKD = 40 MHz) | Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use | 1.15 | — | — | μs | High-precision channel ADSSTRn.SST[7:0] bits = 0Eh |
| | | 1.30 | — | — | μs | Normal-precision channel ADSSTRn.SST[7:0] bits = 14h |
| | Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit in use | 1.90 | — | — | μs | High-precision channel ADSSTRn.SST[7:0] bits = 0Eh ADSHCR.SSTSH[7:0] bits = 11h AN100 to 102 = 0.25 V to $AV_{CC1} - 0.25\text{ V}$ |
| Analog input capacitance | | — | — | 12 | pF | |
| Offset error | | — | ±2.0 | ±6.5 | LSB | |
| Full-scale error | | — | ±2.0 | ±6.5 | LSB | |
| Quantization error | | — | ±0.5 | — | LSB | |
| Absolute accuracy | | — | ±3.0 | ±8.0 | LSB | |
| DNL differential nonlinearity error | | — | ±0.5 | ±1.5 | LSB | |
| INL integral nonlinearity error | | — | ±1.5 | ±4.0 | LSB | |

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.30 A/D Converter Channel Classification

| Classification | Channel | Conditions | Remarks |
|--|--|--|---------|
| High-precision channel | AN000 to AN003, AN100 to AN103, AN200 to AN211 | $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = 2.7$ to 5.5 V | |
| Normal-precision channel | AN016, AN116 | $V_{CC} = AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = 2.7$ to 5.5 V | |
| Internal reference voltage input channel | Internal reference voltage | $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = 2.7$ to 5.5 V | |

Table 5.31 A/D Internal Reference Voltage Characteristics

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|--|------|------|------|------|-----------------|
| Internal reference voltage input channel*1 | 1.35 | 1.43 | 1.50 | V | |

Note 1. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

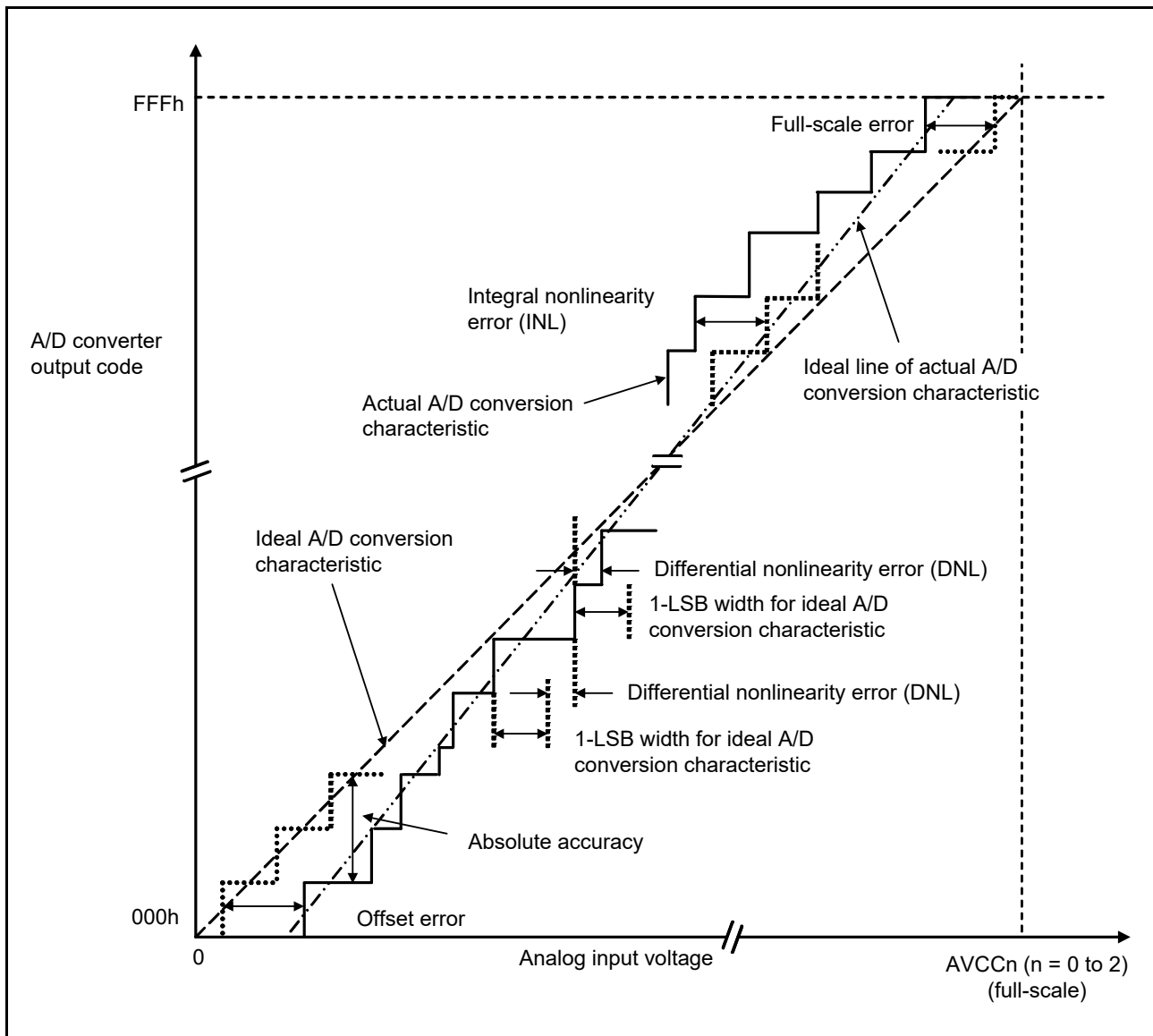


Figure 5.53 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (AVCCn (n = 0 to 2)) is 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ± 5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.5 Programmable Gain Amplifier Characteristics

Table 5.32 Programmable Gain Amplifier Characteristics

Conditions: $V_{CC} = 2.7\text{ V to AVCC0, AVCC1 = AVCC2 = VREF} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------------------------|--------------------|---------------------------------|-----------|---------------------------------|------------------|-------------------------|
| Input offset voltage | V_{poff} | — | — | 8 | mV | |
| Input voltage range | V_{pin} | $V_{\text{pout}}(\text{min})/G$ | — | $V_{\text{pout}}(\text{max})/G$ | V | |
| Output voltage range | V_{pout} | $0.1 \times AVCC$ | — | $0.9 \times AVCC$ | V | |
| Gain | G | 2.000 | — | 4.444 | | |
| Gain error | G_{err} | — | ± 1.0 | ± 2.0 | % | G = 2.000, 2.500, 3.077 |
| | | — | ± 1.5 | ± 3.0 | % | G = 3.636, 4.000, 4.444 |
| Slew rate | SR | 10 | — | — | V/ μs | |
| Operation stabilization wait time | t_{start} | — | — | 5.0 | μs | |

5.6 Comparator Characteristics

Table 5.33 Comparator Characteristics

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|-------------|------|------|------|---------------|---------------------------------|
| Offset voltage | V_{cioff} | — | — | 40 | mV | |
| Reference input voltage range | V_{cref} | 0 | — | VREF | V | |
| Response time | t_{cr} | — | — | 200 | ns | VOD = 100 mV CMPCTL.CDFS = 0 |
| | t_{cf} | — | — | 200 | ns | |
| Stabilization wait time for input selection | t_{cwait} | 300 | — | — | ns | |
| Operation stabilization wait time | t_{cmp} | | — | 1 | μs | |

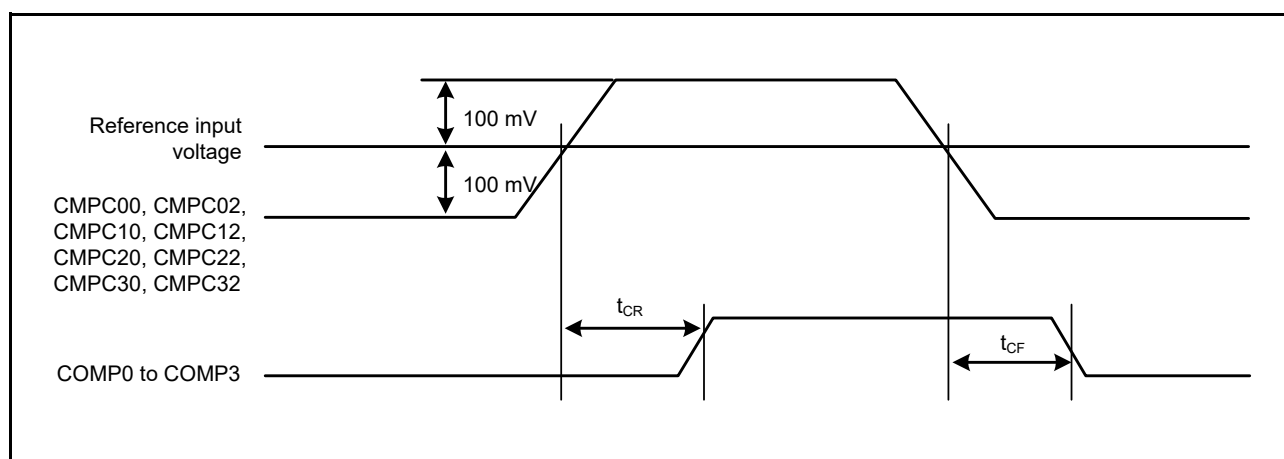


Figure 5.54 Comparator Response Time

5.7 D/A Conversion Characteristics

Table 5.34 Characteristics of D/A Conversion (Chip Version A)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------|-------------|------|------|-----------|---------------|-----------------|
| Resolution | — | — | — | 8 | Bit | |
| Conversion time | t_{DCONV} | — | — | 3.0 | μs | |
| Absolute accuracy | — | — | — | ± 3.0 | LSB | |

Table 5.35 Characteristics of D/A Conversion (Chip Version B)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = V_{CC}$ to 5.5 V , $V_{SS} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------|-------------|------|------|-----------|------------------|-----------------|
| Resolution | — | — | — | 8 | Bit | |
| Conversion time | t_{DCONV} | — | — | 3.0 | μs | |
| Absolute accuracy | — | — | — | ± 3.0 | LSB | |
| Output load resistance | — | 4 | — | — | $\text{M}\Omega$ | |
| Output load capacity | — | — | — | 35 | pF | |
| Output resistance | — | — | 9.0 | — | $\text{k}\Omega$ | |

Note: When using ports 23 and 24 as DA0 and DA1 outputs, make sure that $V_{CC} \geq \text{DA output voltage}$.

5.8 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.36 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = 0 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------------|--|---------------------|------|------|------|------|------------------------------------|
| Voltage detection level | Power-on reset (POR) | V _{POR} | 1.35 | 1.50 | 1.65 | V | Figure 5.55, Figure 5.56 |
| | Voltage detection circuit (LVD0)* ¹ | V _{det0_0} | 3.67 | 3.84 | 3.97 | V | |
| | | V _{det0_1} | 2.70 | 2.82 | 3.00 | | |
| | | V _{det0_2} | 2.37 | 2.51 | 2.67 | | |
| | Voltage detection circuit (LVD1)* ² | V _{det1_0} | 4.12 | 4.29 | 4.42 | V | Figure 5.58 At falling edge VCC |
| | | V _{det1_1} | 3.98 | 4.14 | 4.28 | | |
| | | V _{det1_2} | 3.86 | 4.02 | 4.16 | | |
| | | V _{det1_3} | 3.68 | 3.84 | 3.98 | | |
| | | V _{det1_4} | 2.99 | 3.10 | 3.29 | | |
| | | V _{det1_5} | 2.89 | 3.00 | 3.19 | | |
| | | V _{det1_6} | 2.79 | 2.90 | 3.09 | | |
| | | V _{det1_7} | 2.68 | 2.79 | 2.98 | | |
| | | V _{det1_8} | 2.57 | 2.68 | 2.87 | | |
| | Voltage detection circuit (LVD2)* ³ | V _{det2_0} | 4.08 | 4.29 | 4.48 | V | Figure 5.59 At falling edge VCC |
| | | V _{det2_1} | 3.95 | 4.14 | 4.35 | | |
| | | V _{det2_2} | 3.82 | 4.02 | 4.22 | | |
| V _{det2_3} | | 3.62 | 3.84 | 4.02 | | | |

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det0_n} denotes the value of the LVDS0[1:0] bits.

Note 2. n in the symbol V_{det1_n} denotes the value of the LVDLVL.R.LVD1LVL[3:0] bits.

Note 3. n in the symbol V_{det2_n} denotes the value of the LVDLVL.R.LVD2LVL[3:0] bits.

Table 5.37 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = 0 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|-------------------|---------------------|------|------|------|------|---|
| Wait time after power-on reset cancellation | At normal startup | t _{POR} | — | 28.4 | — | ms | Figure 5.56 |
| Wait time after voltage monitoring 0 reset cancellation | | t _{LVD0} | — | 568 | — | μs | Figure 5.57 |
| Wait time after voltage monitoring 1 reset cancellation | | t _{LVD1} | — | 100 | — | μs | Figure 5.58 |
| Wait time after voltage monitoring 2 reset cancellation | | t _{LVD2} | — | 100 | — | μs | Figure 5.59 |
| Response delay time | | t _{det} | — | — | 350 | μs | Figure 5.55 |
| Minimum VCC down time* ¹ | | t _{VOFF} | 350 | — | — | μs | Figure 5.55, VCC = 1.0 V or above |
| Power-on reset enable time | | t _{W(POR)} | 1 | — | — | ms | Figure 5.56, VCC = below 1.0 V |
| LVD operation stabilization time (after LVD is enabled) | | T _{d(E-A)} | — | — | 300 | μs | Figure 5.58, Figure 5.59 |
| Hysteresis width (LVD0, LVD1 and LVD2) | | V _{L VH} | — | 70 | — | mV | Vdet1_0 to 4 selected |
| | | | — | 60 | — | | Vdet0_0 to 2 selected Vdet1_5 to 8 selected LVD2 selected |

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

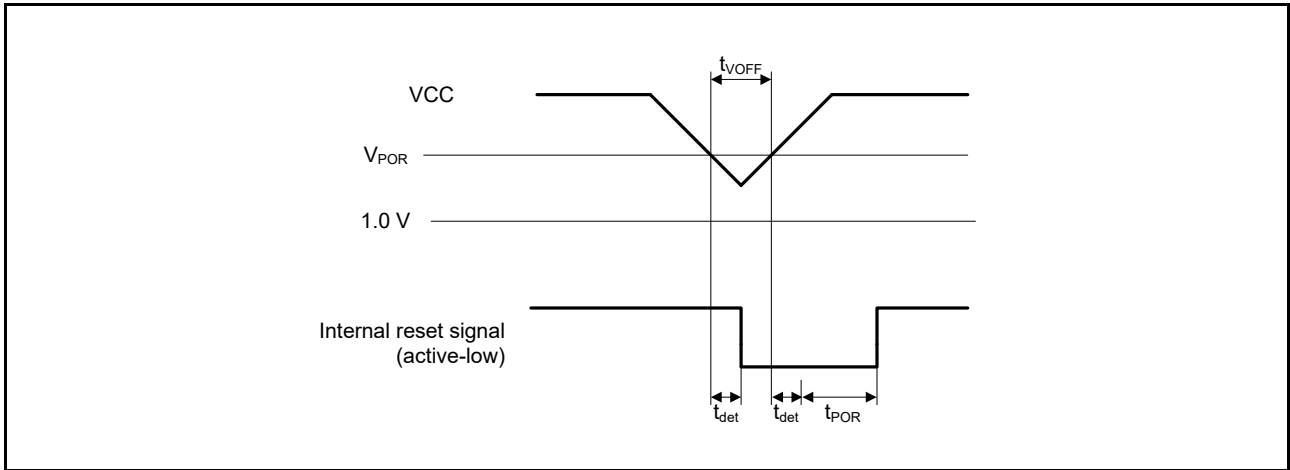


Figure 5.55 Voltage Detection Reset Timing

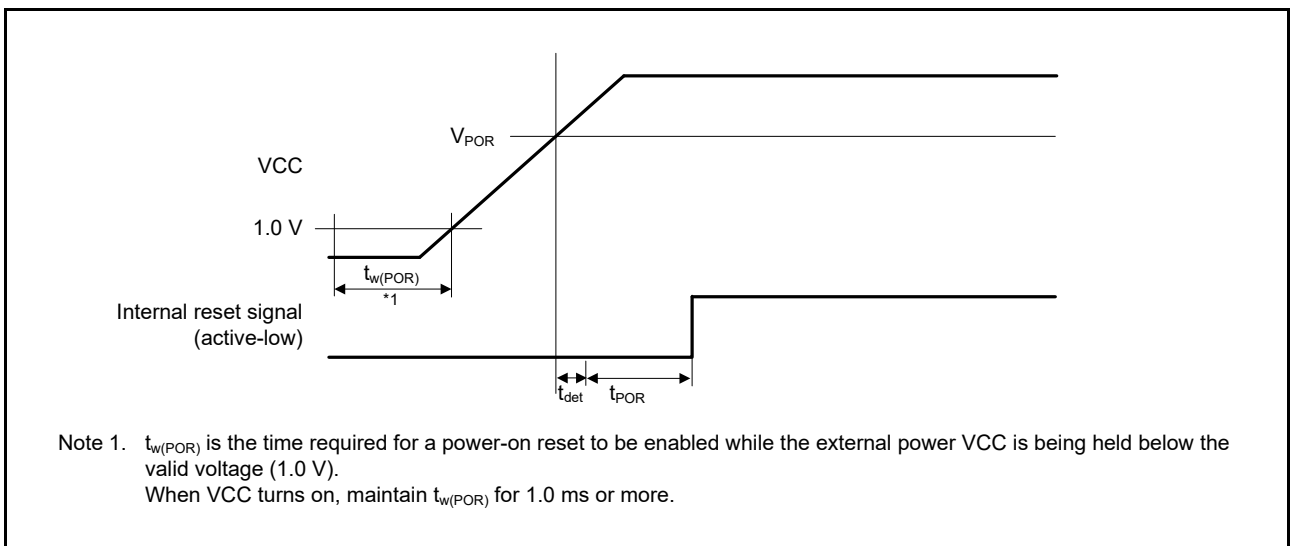


Figure 5.56 Power-On Reset Timing

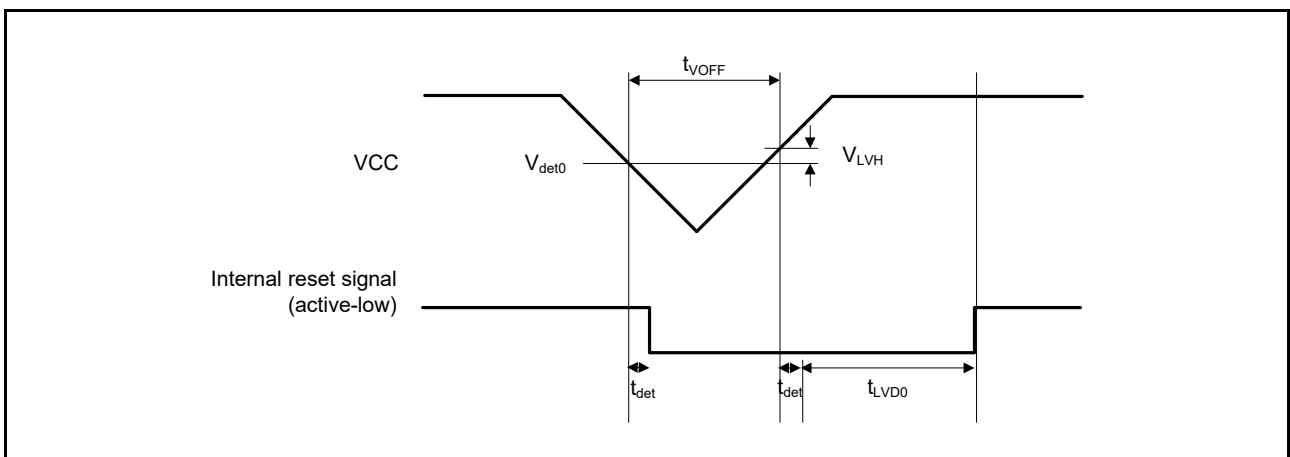


Figure 5.57 Voltage Detection Circuit Timing (Vdet0)

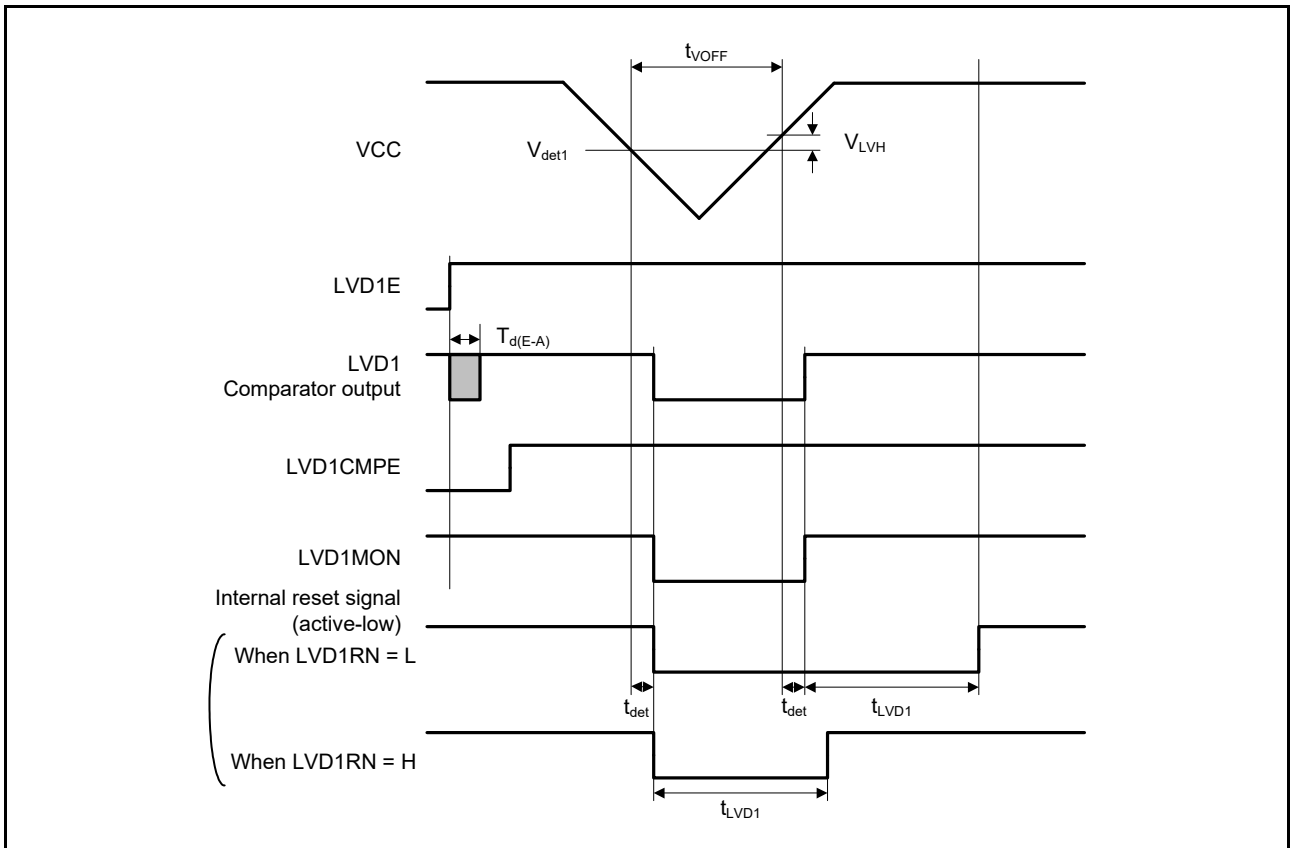


Figure 5.58 Voltage Detection Circuit Timing (V_{det1})

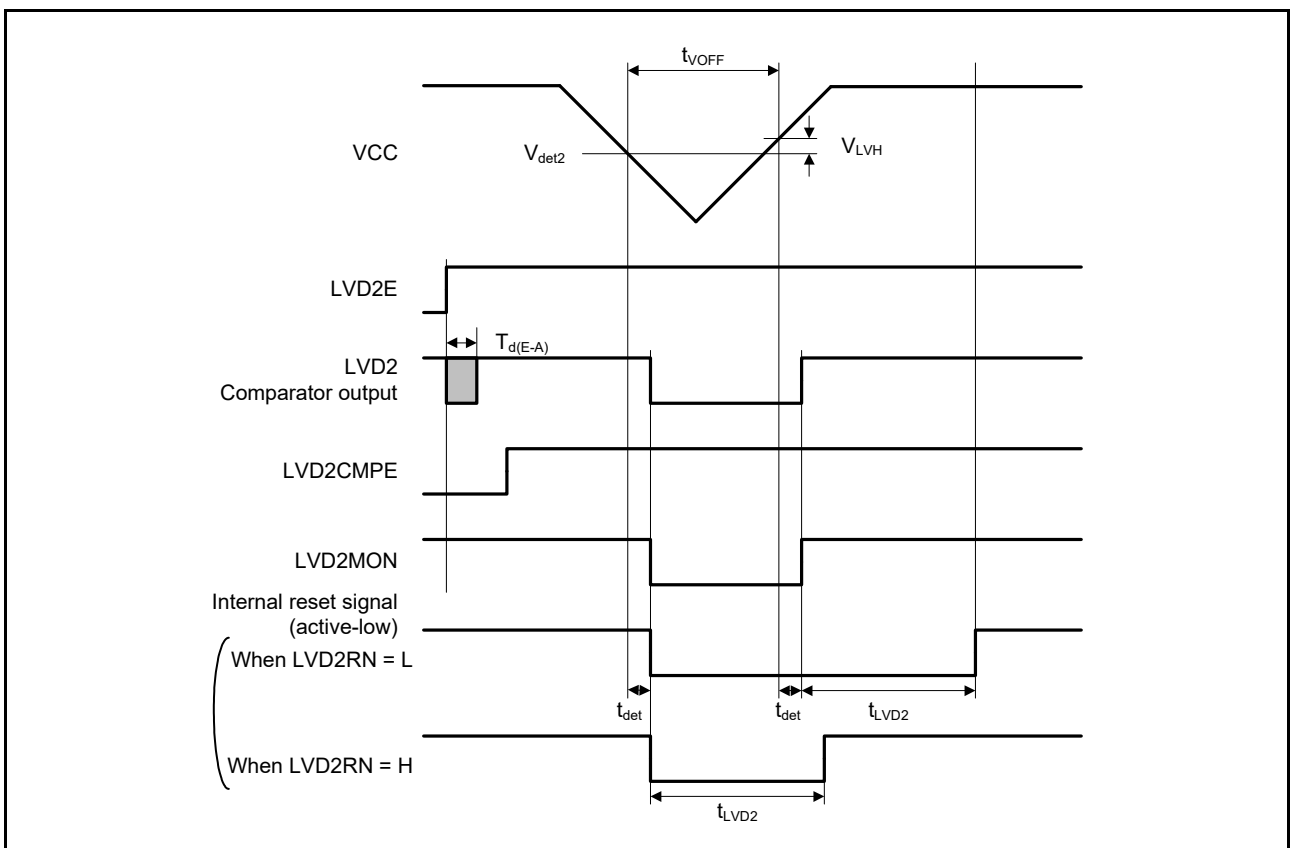


Figure 5.59 Voltage Detection Circuit Timing (V_{det2})

5.9 Oscillation Stop Detection Timing

Table 5.38 Oscillation Stop Detection Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------|----------|------|------|------|------|-----------------|
| Detection time | t_{dr} | — | — | 1 | ms | Figure 5.60 |

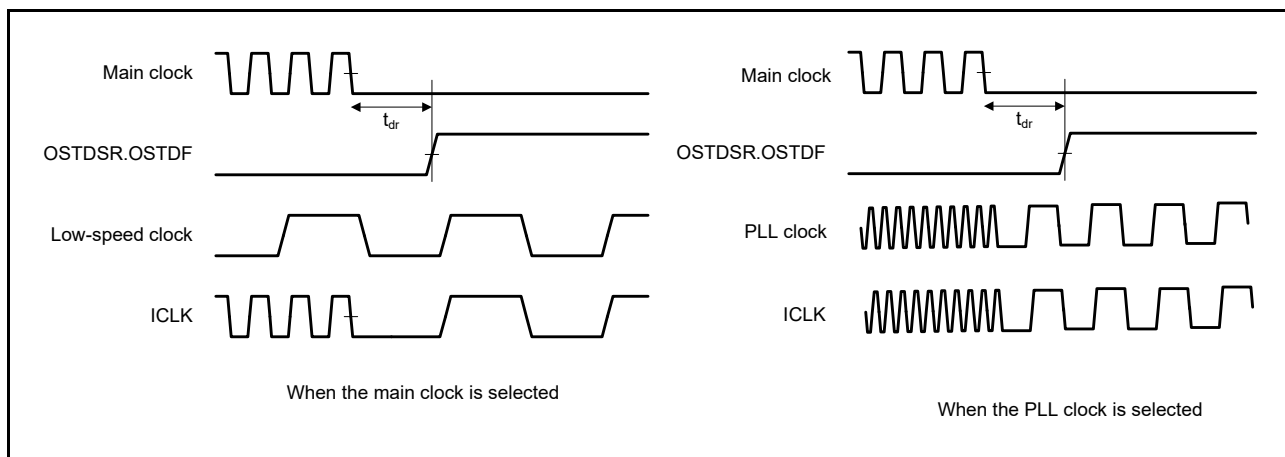


Figure 5.60 Oscillation Stop Detection Timing

5.10 ROM (Flash Memory for Code Storage) Characteristics

Table 5.39 ROM (Flash Memory for Code Storage) Characteristics (1)

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-------------------------------|--|----------|------|------|-------|---------------------------|
| Reprogramming/erasure cycle*1 | N_{PEC} | 1000 | — | — | Times | |
| Data hold time | After 1000 times of N_{PEC} t_{DRP} | 20*2, *3 | — | — | Year | $T_a = +85^\circ\text{C}$ |

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.40 ROM (Flash Memory for Code Storage) Characteristics (2): High-Speed Operating Mode

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = V_{REF} = V_{CC}$ to 5.5 V, $V_{SS} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$

Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^\circ\text{C}$

| Item | Symbol | FCLK = 1 MHz | | | FCLK = 32 MHz | | | Unit | |
|--------------------------------------|--|--------------|------|-------|---------------|------|------|--------|---------------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time | 8-byte | t_{P8} | — | 112.0 | 967.0 | — | 52.3 | 490.5 | μs |
| Erasure time | 2-Kbyte | t_{E2K} | — | 8.7 | 278.1 | — | 5.5 | 214.6 | ms |
| | 256-Kbyte (when block erase command used) | t_{E256K} | — | 469.1 | 9813.6 | — | 41.2 | 1049.2 | ms |
| | 256-Kbyte (when all- block erase command used) | t_{EA256K} | — | 463.9 | 9609.0 | — | 36.0 | 839.5 | ms |
| | 512-Kbyte (when block erase command used) | t_{E512K} | — | 927.8 | 19218.0 | — | 72.0 | 1678.9 | ms |
| | 512-Kbyte (when all- block erase command used) | t_{EA512K} | — | 922.7 | 19013.4 | — | 66.7 | 1469.2 | ms |
| Blank check time | 8-byte | t_{BC8} | — | — | 55.0 | — | — | 16.1 | μs |
| | 2-Kbyte | t_{BC2K} | — | — | 1840.0 | — | — | 135.7 | μs |
| Erasure operation forcible stop time | | t_{SED} | — | — | 18.0 | — | — | 10.7 | μs |
| Start-up area switching setting time | | t_{SAS} | — | 12.3 | 566.5 | — | 6.2 | 433.5 | ms |
| Access window time | | t_{AWS} | — | 12.3 | 566.5 | — | 6.2 | 433.5 | ms |
| ROM mode transition wait time 1 | | t_{DIS} | 2.0 | — | — | 2.0 | — | — | μs |
| ROM mode transition wait time 2 | | t_{MS} | 5.0 | — | — | 5.0 | — | — | μs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be $\pm 3.5\%$.

Table 5.41 ROM (Flash Memory for Code Storage) Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

| Item | Symbol | FCLK = 1 MHz | | | FCLK = 8 MHz | | | Unit | |
|--------------------------------------|--|---------------------|------|-------|--------------|------|-------|--------|----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time | 8-byte | t _{P8} | — | 152.0 | 1367.0 | — | 97.9 | 936.0 | μs |
| Erasure time | 2-Kbyte | t _{E2K} | — | 8.8 | 279.7 | — | 5.9 | 220.8 | ms |
| | 256-Kbyte (when block erase command used) | t _{E256K} | — | 469.2 | 9816.9 | — | 100.5 | 2260.1 | ms |
| | 256-Kbyte (when all- block erase command used) | t _{EA256K} | — | 464.0 | 9610.7 | — | 95.3 | 2053.7 | ms |
| | 512-Kbyte (when block erase command used) | t _{E512K} | — | 928.0 | 19221.2 | — | 190.6 | 4107.3 | ms |
| | 512-Kbyte (when all- block erase command used) | t _{EA512K} | — | 922.7 | 19015.0 | — | 185.4 | 3901.0 | ms |
| Blank check time | 8-byte | t _{BC8} | — | — | 85.0 | — | — | 50.9 | μs |
| | 2-Kbyte | t _{BC2K} | — | — | 1870.0 | — | — | 401.5 | μs |
| Erasure operation forcible stop time | | t _{SED} | — | — | 28.0 | — | — | 21.3 | μs |
| Start-up area switching setting time | | t _{SAS} | — | 13.0 | 573.3 | — | 7.7 | 450.1 | ms |
| Access window time | | t _{AWS} | — | 13.0 | 573.3 | — | 7.7 | 450.1 | ms |
| ROM mode transition wait time 1 | | t _{DIS} | 2.0 | — | — | 2.0 | — | — | μs |
| ROM mode transition wait time 2 | | t _{MS} | 3.0 | — | — | 3.0 | — | — | μs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.

5.11 E2 DataFlash Characteristics

Table 5.42 E2 DataFlash Characteristics (1)

| Item | | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-------------------------------|--|-------------------|----------|---------|------|-------|------------------------|
| Reprogramming/erasure cycle*1 | | N _{DPEC} | 100000 | 1000000 | — | Times | |
| Data hold time | After 10000 times of N _{DPEC} | t _{DDRP} | 20*2, *3 | — | — | Year | T _a = +85°C |
| | After 100000 times of N _{DPEC} | | | | | Year | |
| | After 1000000 times of N _{DPEC} | | — | 1*2, *3 | — | Year | T _a = +25°C |

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.43 E2 DataFlash Characteristics (2): High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

| Item | Symbol | FCLK = 1 MHz | | | FCLK = 32 MHz | | | Unit | |
|-------------------------------------|--------------------|--------------------|------|-------|---------------|------|------|-------|----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time | 1-byte | t _{Dp1} | — | 95.0 | 797.0 | — | 40.8 | 375.5 | μs |
| Erasure time | 1-Kbyte | t _{DE1K} | — | 19.5 | 498.5 | — | 6.2 | 229.4 | ms |
| | 8-Kbyte | t _{DE8K} | — | 119.8 | 2555.7 | — | 12.9 | 367.2 | ms |
| Blank check time | 1-byte | t _{DBC1} | — | — | 55.0 | — | — | 16.1 | μs |
| | 1-Kbyte | t _{DBC1K} | — | — | 7216.0 | — | — | 495.7 | μs |
| Erase operation forcible stop time | t _{DSED} | — | — | 16.0 | — | — | 10.7 | μs | |
| Data flash-module stop release time | t _{DSTOP} | 5.0 | — | — | 5.0 | — | — | μs | |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.

Table 5.44 E2 DataFlash Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

| Item | Symbol | FCLK = 1 MHz | | | FCLK = 8 MHz | | | Unit | |
|-------------------------------------|--------------------|--------------------|------|-------|--------------|------|------|--------|----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time | 1-byte | t _{Dp1} | — | 135.0 | 1197.0 | — | 86.5 | 822.5 | μs |
| Erasure time | 1-Kbyte | t _{DE1K} | — | 19.6 | 500.1 | — | 8.0 | 264.1 | ms |
| | 8-Kbyte | t _{DE8K} | — | 119.9 | 2557.4 | — | 27.7 | 668.2 | ms |
| Blank check time | 1-byte | t _{DBC1} | — | — | 85.0 | — | — | 50.9 | μs |
| | 1-Kbyte | t _{DBC1K} | — | — | 7246.0 | — | — | 1457.5 | μs |
| Erase operation forcible stop time | t _{DSED} | — | — | 28.0 | — | — | 21.3 | μs | |
| Data flash-module stop release time | t _{DSTOP} | 0.72 | — | — | 0.72 | — | — | μs | |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.

5.12 Usage Notes

5.12.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7- μF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 5.61 to Figure 5.63 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 μF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 31, 12-Bit A/D Converter (S12ADF) in the User's Manual: Hardware.

For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.

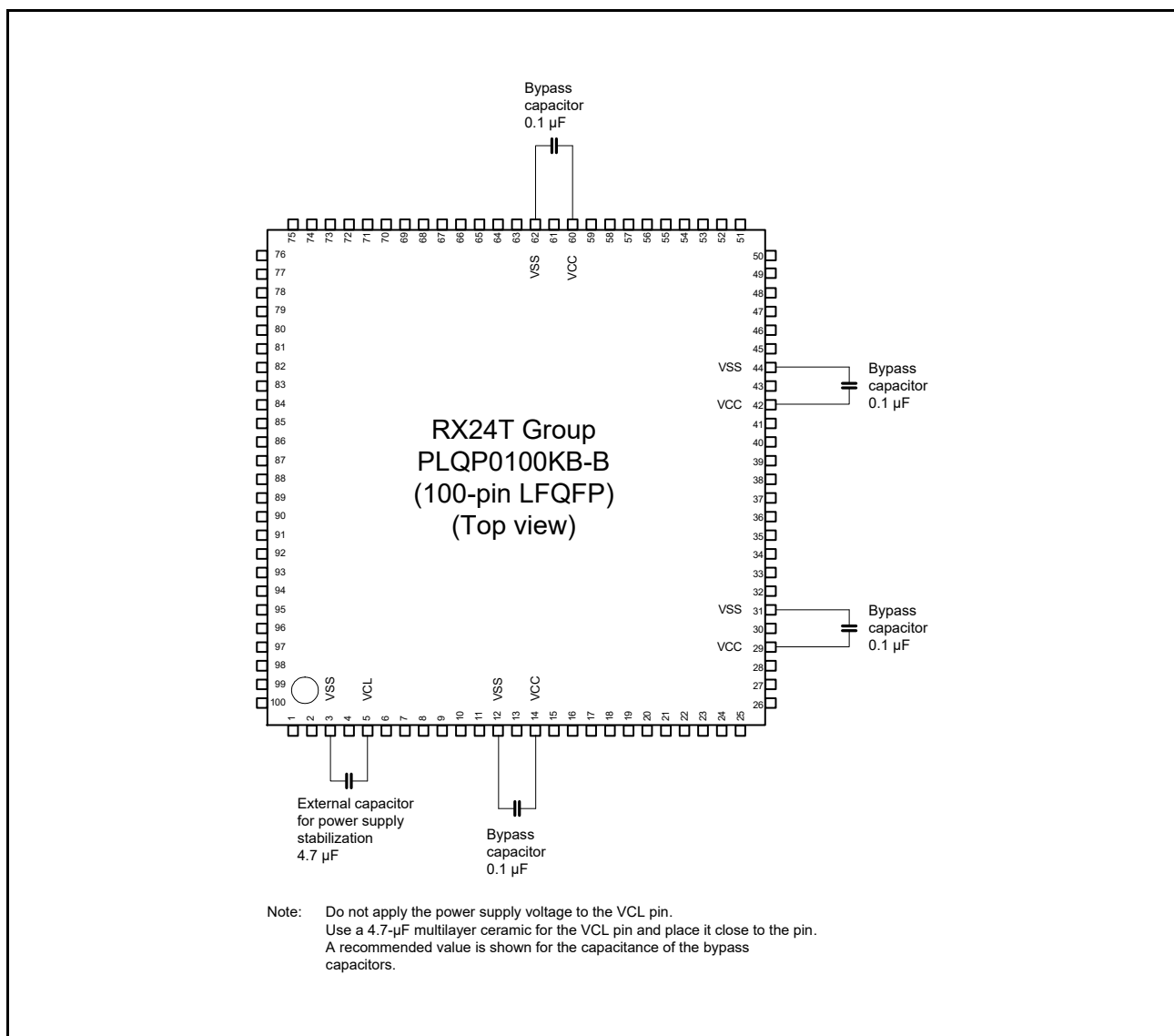


Figure 5.61 Connecting Capacitors (100 Pins)

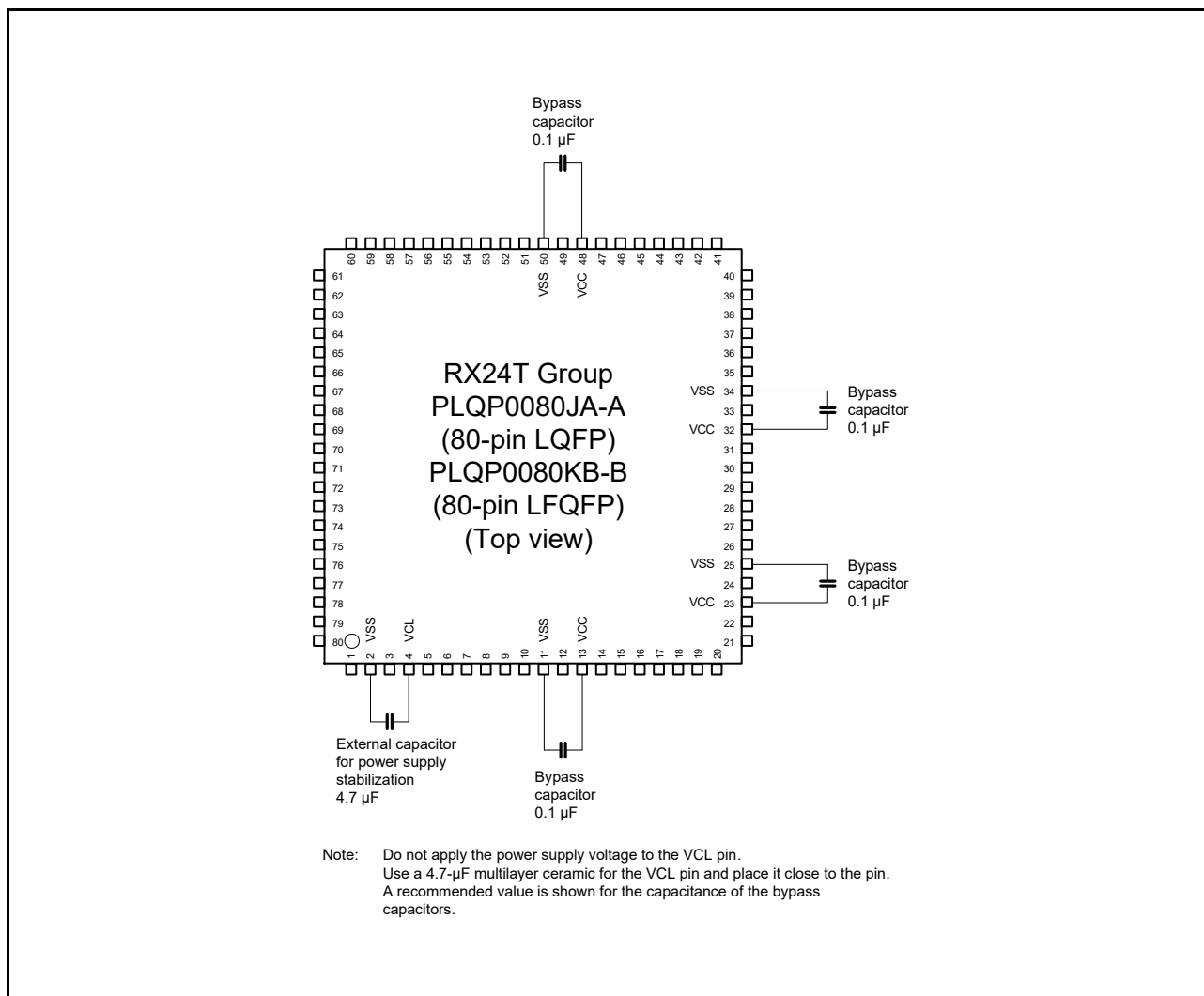


Figure 5.62 Connecting Capacitors (80 Pins)

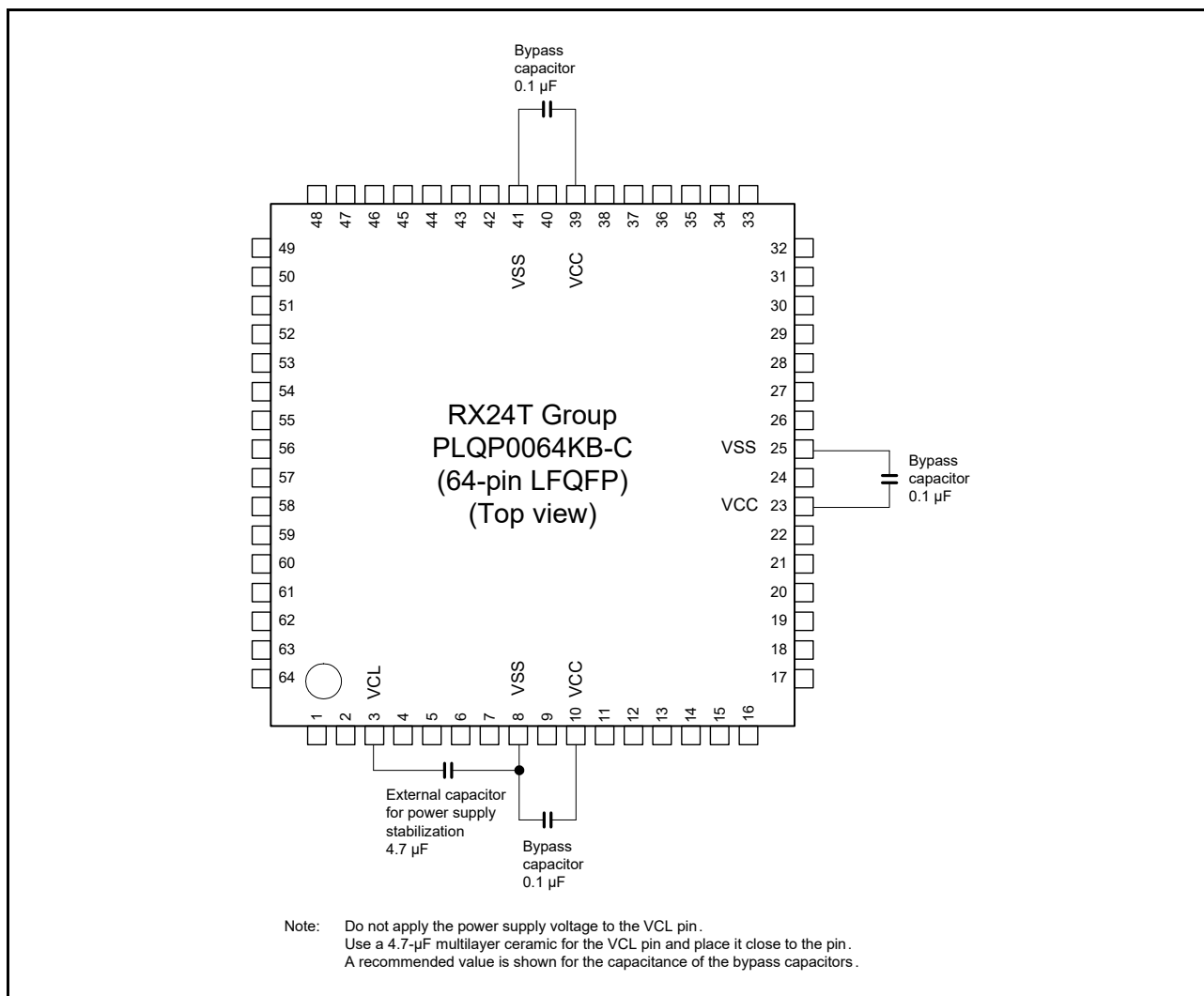


Figure 5.63 Connecting Capacitors (64 Pins)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

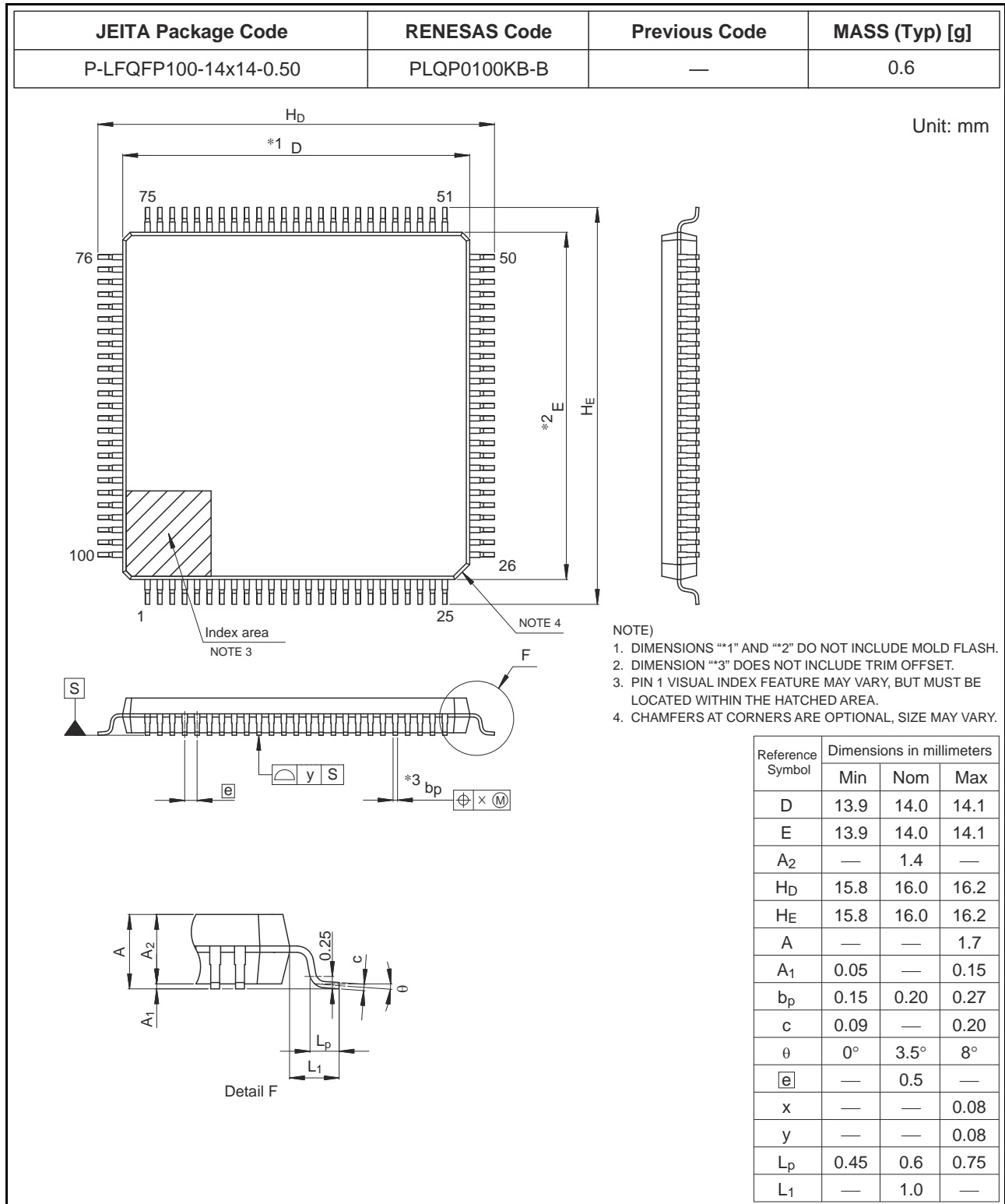


Figure A 100-Pin LFQFP (PLQP0100KB-B)

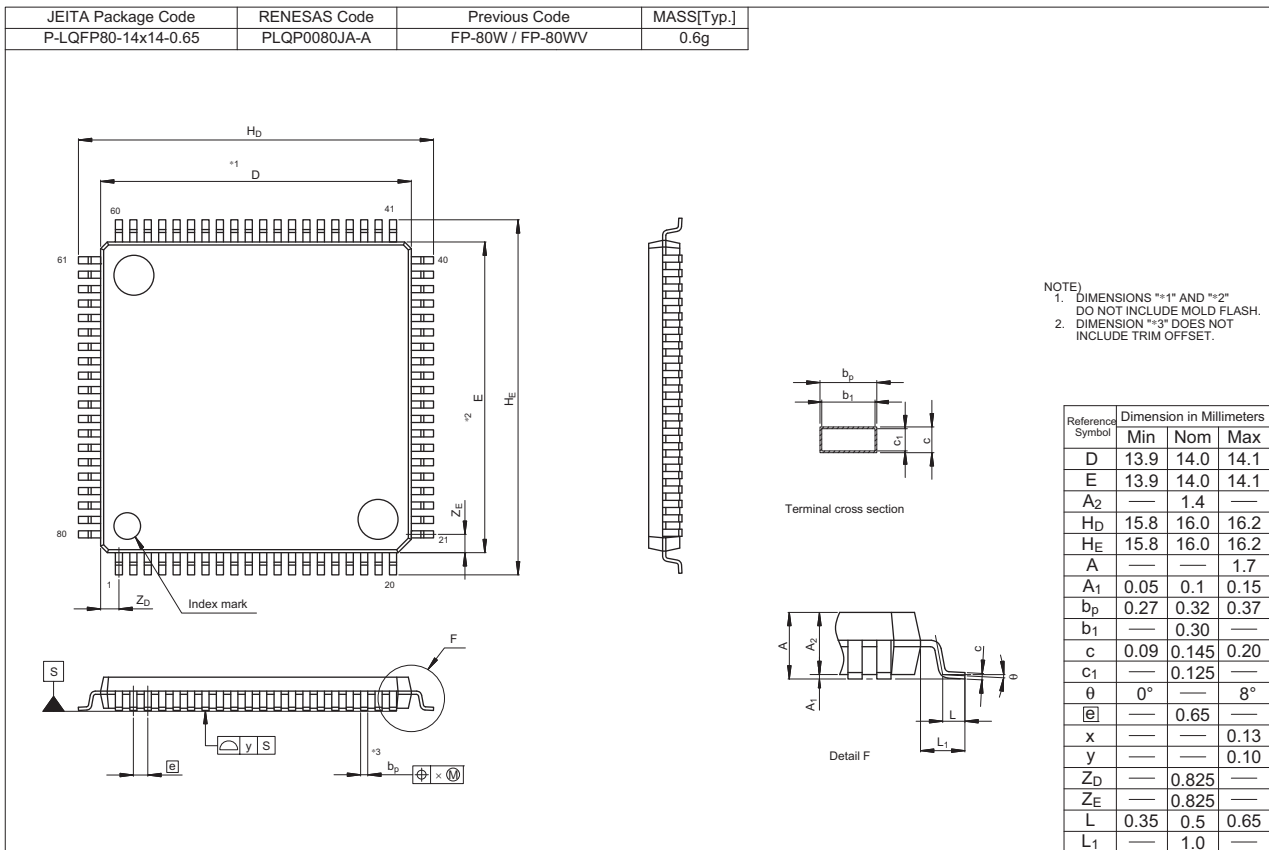


Figure B 80-Pin LQFP (PLQP0080JA-A)

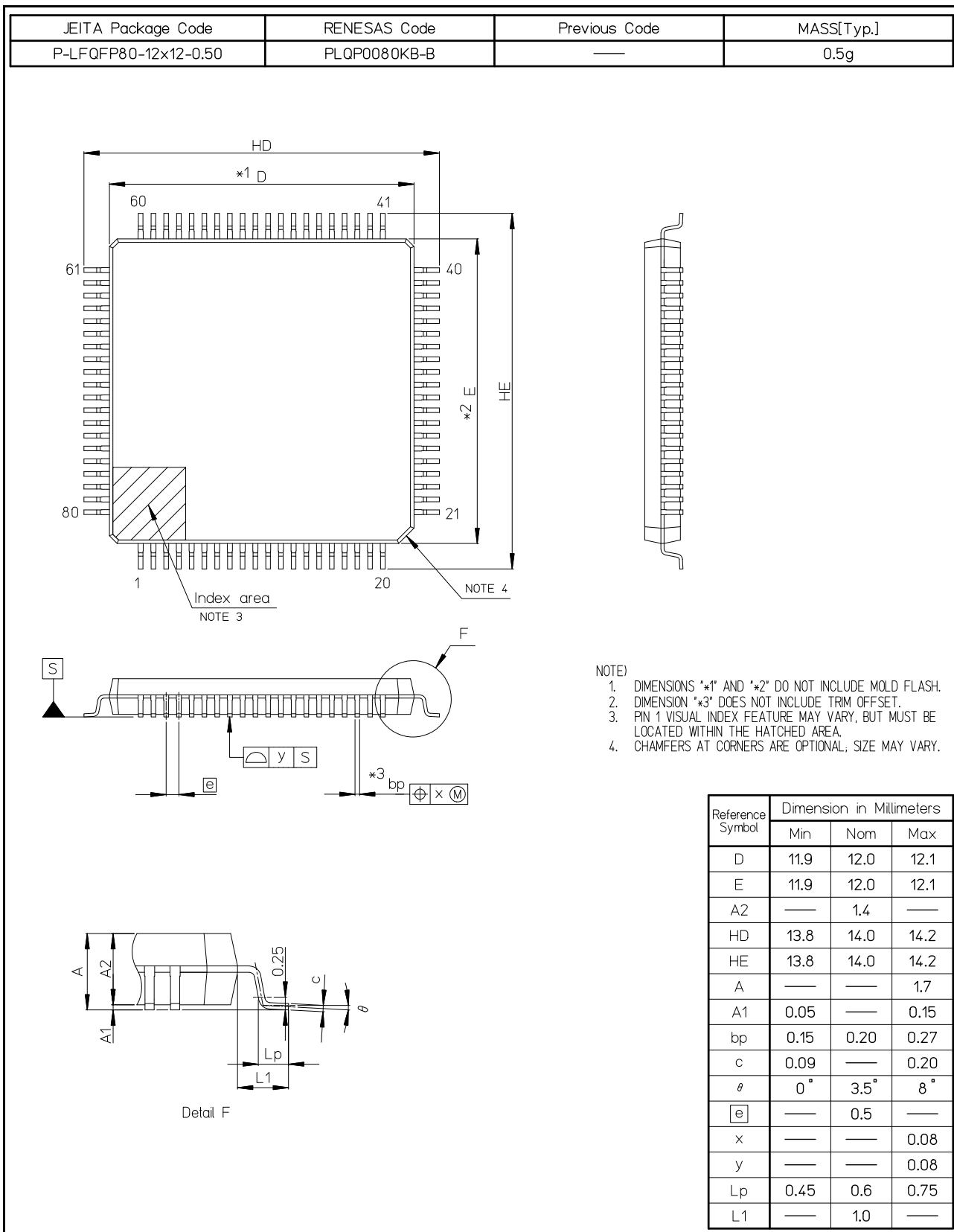


Figure C 80-Pin LFQFP (PLQP0080KB-B)

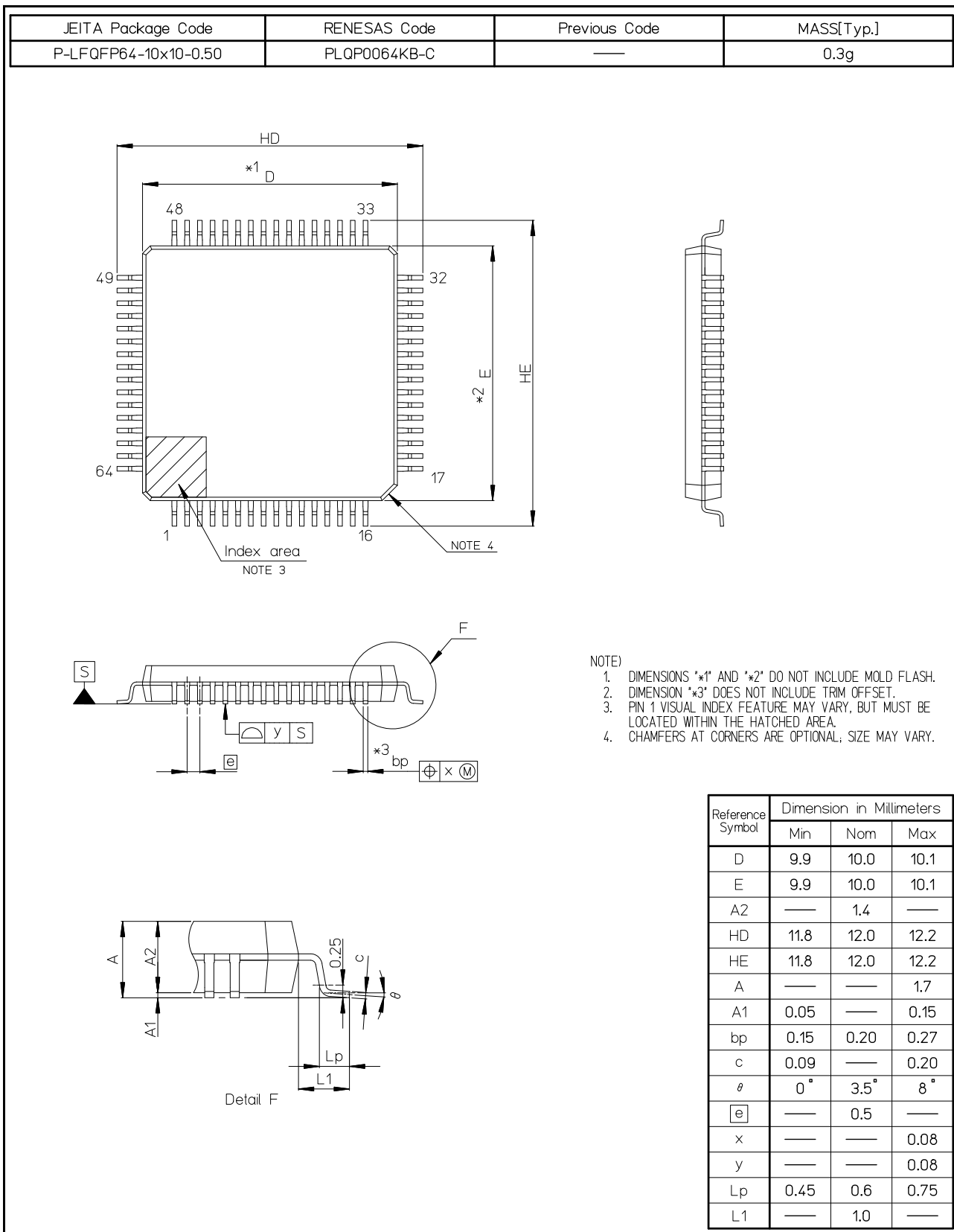


Figure D 64-Pin LFQFP (PLQP0064KB-C)

| | |
|------------------|-----------------------|
| REVISION HISTORY | RX24T Group Datasheet |
|------------------|-----------------------|

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|------|---|--------------------------------|--|----------------|
| | | Page | Summary | |
| 1.00 | Nov 30, 2015 | — | First edition, issued | |
| 2.00 | Apr 14, 2017 | All | Chip version B, added The name of the previous product, changed to chip version A according to the above The specification of the HOCO, added The 64-pin package, added The specification of the voltage detection 0 level select bit, changed | TN-RX*-A171A/E |
| | | 5. Electrical Characteristics | | |
| | | — | The characteristics of HOCO-/GPT-/RSCAN-related and chip version B, added | |
| | | 72 | Table 5.3 DC Characteristics (1): ports 36 and 37, added | |
| | | 78 | Table 5.8 DC Characteristics (6), changed | |
| | | 100 | Table 5.25 Timing of On-Chip Peripheral Modules (3), changed | TN-RX*-A170A/E |
| | | 115 | Table 5.34 Characteristics of D/A Conversion (Chip Version A), changed | TN-RX*-A170A/E |
| | | 125 | Figure 5.63 Connecting Capacitors (64 Pins), added | |
| | | Appendix 1. Package Dimensions | | |
| | | 126 | Figure A 100-Pin LFQFP (PLQP0100KB-B), package part number, changed | |
| | | 128 | Figure C 80-Pin LFQFP (PLQP0080KB-B), package part number, changed | |
| 129 | Figure D 64-Pin LFQFP (PLQP0064KB-C), added | | | |

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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[R5F524TAADFN#31](#) [R5F524TBADFP#31](#) [R5F524T8ADFP#31](#) [R5F524T8ADFN#31](#) [R5F524T8ADFF#31](#)
[R5F524TCADFP#31](#) [R5F524T8ADFM#31](#) [R5F524T8ADFF#51](#) [R5F524T8ADFK#31](#) [R5F524T8ADFK#51](#)
[R5F524T8ADFM#51](#) [R5F524T8ADFN#51](#) [R5F524T8ADFP#51](#) [R5F524TBADFP#51](#) [R5F524TCADFP#51](#)
[R5F524TEADFP#51](#) [R5F524TAADFF#51](#) [R5F524TAADFK#31](#) [R5F524TAADFK#51](#) [R5F524TAADFM#51](#)
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[R5F524TAADFM#11](#) [R5F524TAADFN#11](#) [R5F524TAADFP#11](#) [R5F524TBADFP#11](#) [R5F524TCADFP#11](#)

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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