# **74LVC00A**

# Quad 2-input NAND gate Rev. 7 — 25 April 2012

**Product data sheet** 

#### 1. **General description**

The 74LVC00A provides four 2-input NAND gates.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

#### **Features and benefits** 2.

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

#### **Ordering information** 3.

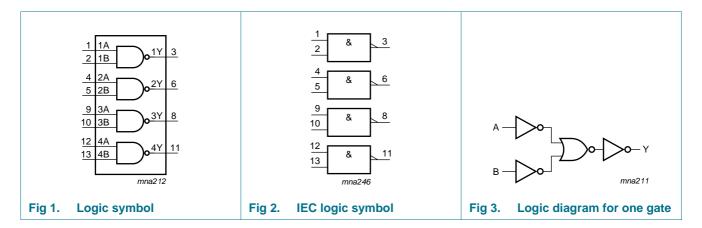
Table 1. **Ordering information** 

Type number	Package	Package										
	Temperature range	Name	Description	Version								
74LVC00AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1								
74LVC00ADB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1								
74LVC00APW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1								
74LVC00ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5\times3\times0.85$ mm	SOT762-1								



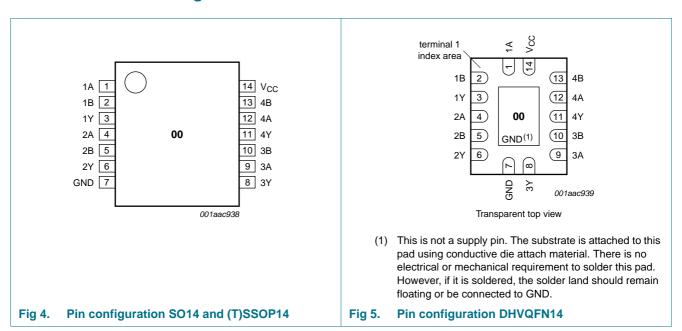
**Quad 2-input NAND gate** 

## 4. Functional diagram



## 5. Pinning information

## 5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8,11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

74LVC00

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## 6. Functional description

Table 3. Function selection[1]

Input		Output
nA	nB	nY
L	X	Н
X	L	Н
Н	Н	L

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
$V_{I}$	input voltage		<u>[1]</u> –0.5	+6.5	V
I <sub>OK</sub>	output clamping current	$V_O > V_{CC}$ or $V_O < 0 V$	-	±50	mA
V <sub>O</sub>	output voltage	output in HIGH or LOW-state	<b>2</b> -0.5	$V_{CC} + 0.5$	V
I <sub>O</sub>	output current	$V_O = 0 V to V_{CC}$	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[3]	500	mW
$T_{stg}$	storage temperature		-65	+150	°C

<sup>[1]</sup> The minimum input voltage ratings may be exceeded if the input current ratings are observed.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	$V_{CC}$	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and	$V_{CC}$ = 1.65 V to 2.7 V	0	-	20	ns/V
	fall rate	$V_{CC}$ = 2.7 V to 3.6 V	0	-	10	ns/V

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<sup>[2]</sup> The output voltage ratings may be exceeded if the output current ratings are observed.

<sup>[3]</sup> For SO14 packages: above 70 °C derate linearly with 8 mW/K. For (T)SSOP14 packages: above 60 °C derate linearly with 5.5 mW/K. For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	35 °C	–40 °C to	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	$0.65 \times V_{CC}$	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
	input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$						
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
II	input leakage current	$V_{CC} = 3.6 \text{ V}; V_{I} = 5.5 \text{ V or GND}$	-	±0.1	±5	-	±20	μΑ
I <sub>CC</sub>	supply current	$V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A	-	0.1	10	-	40	μΑ
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$	-	5	500	-	5000	μΑ
C <sub>I</sub>	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_I = \text{GND to } V_{CC}$	-	4.0	-	-	-	pF

<sup>[1]</sup> All typical values are measured at  $V_{CC}$  = 3.3 V (unless stated otherwise) and  $T_{amb}$  = 25 °C.

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions	Conditions			5 °C	-40 °C to	o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Figure 6	[2]						
		$V_{CC} = 1.2 \text{ V}$		-	12	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.3	3.8	8.4	0.3	9.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.0	2.2	4.8	1.0	5.7	ns
		$V_{CC} = 2.7 \text{ V}$		1.0	2.3	5.1	1.0	5.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.5	2.0	4.3	0.5	5.1	ns
t <sub>sk(o)</sub>	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[3]	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation	per gate; $V_I = GND$ to $V_{CC}$	<u>[4]</u>						
	capacitance	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		-	5.6	-	-	-	рF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-	8.9	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	11.8	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb} = 25$  °C and  $V_{CC} = 1.2$  V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

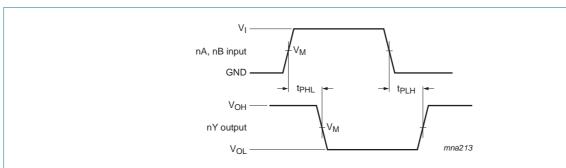
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

## 11. Waveforms



 $V_M = 1.5 \text{ V at } V_{CC} \ge 2.7 \text{ V}.$ 

 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7$  V.

 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 6. The input (nA, nB) to output (nY) propagation delays

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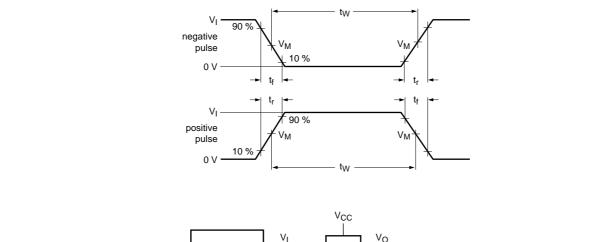
<sup>[2]</sup>  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

<sup>[3]</sup> Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

<sup>[4]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

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**Quad 2-input NAND gate** 



PULSE GENERATOR DUT VO DUT CL RL 001aaf615

Test data is given in Table 8. Definitions for test circuit:

R<sub>L</sub> = Load resistance

C<sub>L</sub> = Load capacitance including jig and probe capacitance

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator

Fig 7. Load circuitry for measuring switching times

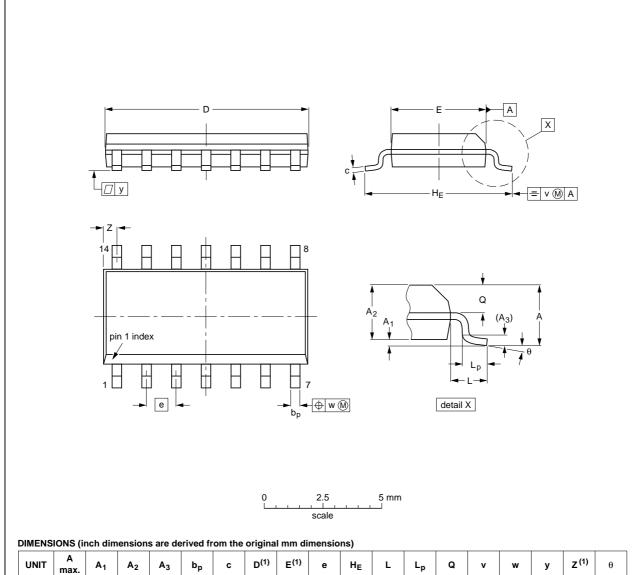
Table 8. Test data

Supply voltage	Input		Load	Load			
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>			
1.2 V	$V_{CC}$	≤ 2 ns	30 pF	1 kΩ			
1.65 V to 1.95 V	$V_{CC}$	≤ 2 ns	30 pF	1 kΩ			
2.3 V to 2.7 V	$V_{CC}$	≤ 2 ns	30 pF	500 Ω			
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω			
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω			

## 12. Package outline

#### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	1	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	1	0.01	0.01	0.004	0.028 0.012	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

	REFER	ENCES	EUROPEAN	ISSUE DATE
IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
076E06	MS-012			<del>99-12-27</del> 03-02-19
_	-	IEC JEDEC	IEC JEDEC JEITA	IEC JEDEC JEITA PROJECTION

Fig 8. Package outline SOT108-1 (SO14)

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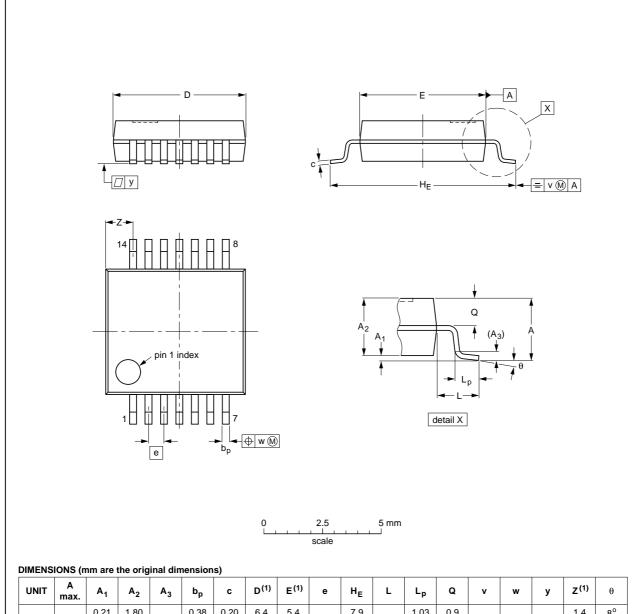
**Product data sheet** 

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	Lp	ď	٧	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES		EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT337-1		MO-150				<del>99-12-27</del> 03-02-19
				1	1	

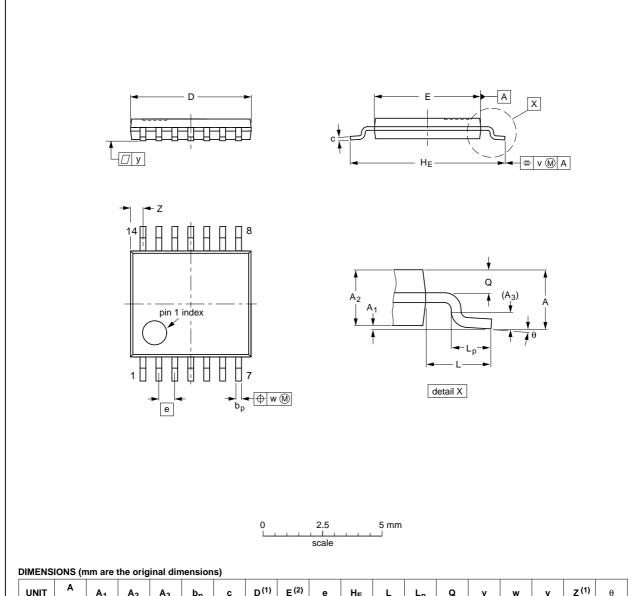
Package outline SOT337-1 (SSOP14) Fig 9.

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(2)</sup>	е	HE	L	Lp	ø	٧	8	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

	REFERENCES				
JEDEC	JEITA		PROJECTION	ISSUE DATE	
MO-153				<del>99-12-27</del> 03-02-18	
_				JEDEC JEHA	

Fig 10. Package outline SOT402-1 (TSSOP14)

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

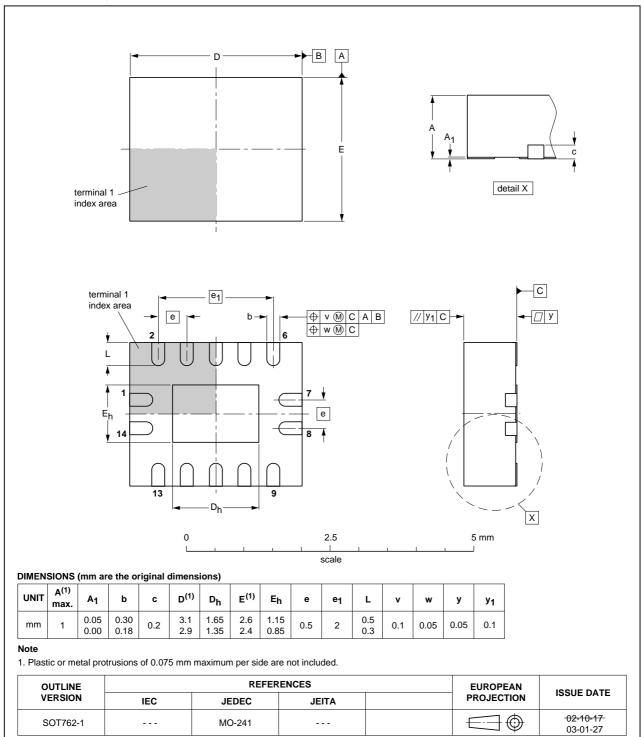


Fig 11. Package outline SOT762-1 (DHVQFN14)

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## 13. Abbreviations

#### Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

## Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC00A v.7	20120425	Product data sheet	-	74LVC00A v.6
Modifications:	• <u>Table 2</u> : Errata	in pin description corrected	l.	
74LVC00A v.6	20120106	Product data sheet	-	74LVC00A v.5
Modifications:	<ul> <li>The format of to of NXP Semicon</li> </ul>		designed to comply wit	h the new identity guidelines
	<ul> <li>Legal texts have</li> </ul>	ve been adapted to the new	company name where	e appropriate.
	• Table 4, Table	5, Table 6, Table 7 and Tabl	e 8: values added for l	lower voltage ranges.
74LVC00A v.5	20030904	Product specification	-	74LVC00A v.4
74LVC00A v.4	20030507	Product specification	-	74LVC00A v.3
74LVC00A v.3	20020305	Product specification	-	74LVC00A v.2
74LVC00A v.2	19980428	Product specification	-	74LVC00A v.1
74LVC00A v.1	19970811	Product specification	-	-

## 15. Legal information

#### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions"
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#### **Quad 2-input NAND gate**

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