

DF2B6USL

1. General

The DF2B6USL is a bidirectional TVS diode with low capacitance designed to protect IC devices from ESD and other transients voltage.

By using original process, low dynamic resistance is incarnated, the clamp voltage can be suppressed to a low level. And ultra-compact package is ideal for high-density mounting.

2. Applications

Mobile Equipment

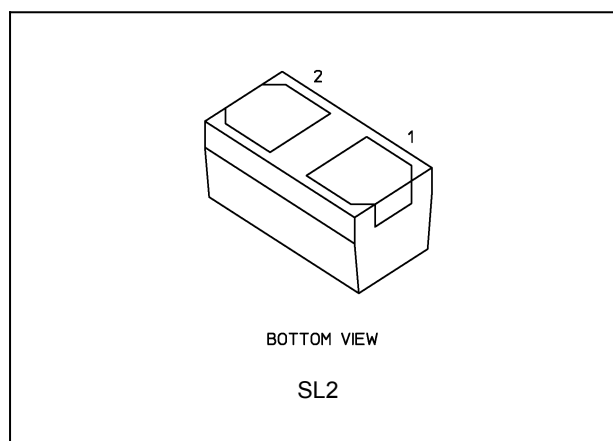
- Smartphones
- Tablets
- Notebook PCs
- USB 2.0

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

3. Features

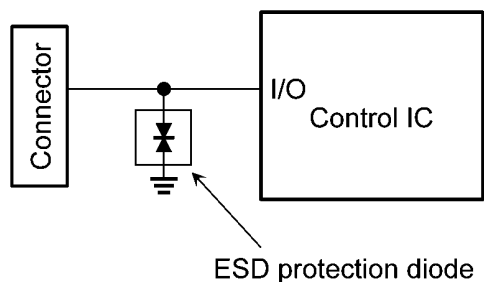
- (1) Suitable for use with a 5 V signal line. ($V_{RWM} \leq 5.5$ V)
- (2) Protects devices with its high ESD performance.
($V_{ESD} = \pm 10$ kV (Contact / Air) @IEC61000-4-2)
- (3) Low dynamic resistance protects semiconductor devices from static electricity and noise.
($R_{DYN} = 0.25$ Ω (typ.))
- (4) Snapback characteristics realizing low clamping voltage protects semiconductor devices.
($V_C = 7.7$ V@ $I_{PP} = 1.5$ A (typ.))
- (5) Compact package is suitable for use in high density board layouts such as in mobile devices.
(0.62 mm \times 0.32 mm size (Nickname: SL2))

4. Packaging



Start of commercial production
2016-09

5. Example of Circuit Diagram



6. Quick Reference Data

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)		—	—	5.5	V
Total capacitance	C_t		$V_R = 0\text{ V}, f = 1\text{ MHz}$	—	1.5	3.0	pF
Dynamic resistance	R_{DYN}	(Note 2)		—	0.25	—	Ω
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V_{ESD}	(Note 3)		—	—	10	kV

Note 1: Recommended operating condition.

Note 2: TLP parameters: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 8\text{ A}$ and $I_{PP2} = 16\text{ A}$.

Note 3: Criterion: No damage to devices.

6.1. ESD Clamp Waveform (Note)

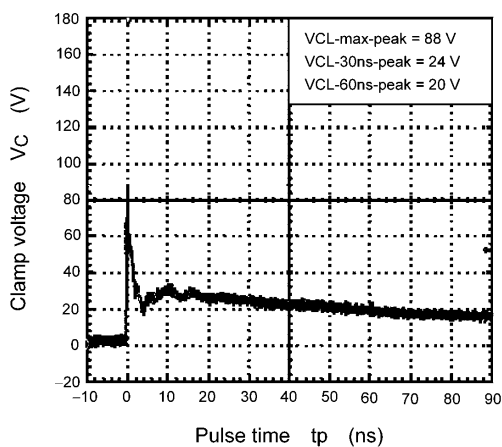


Fig. 6.1.1 +8 kV

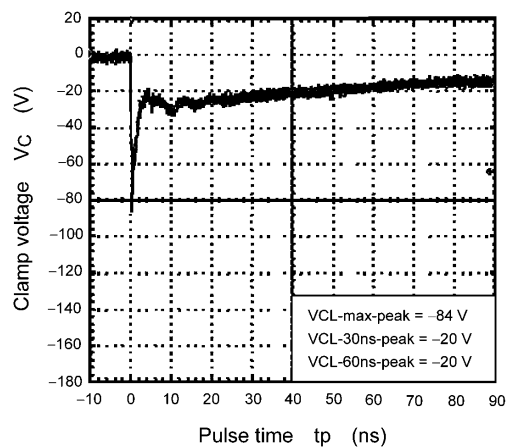


Fig. 6.1.2 -8 kV

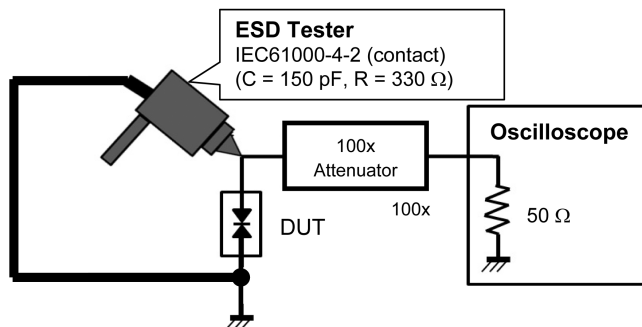
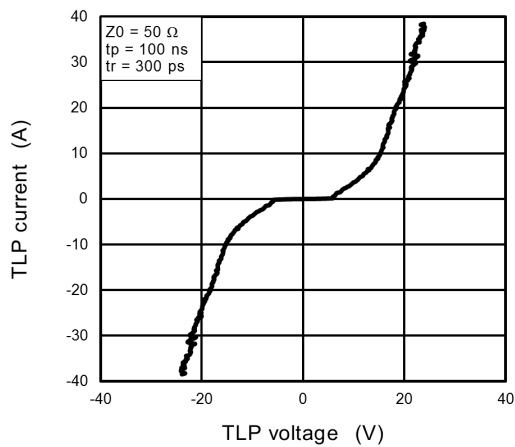


Fig. 6.1.3 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

6.2. TLP Characteristics (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

6.3. Clamp Voltage - Peak Pulse Current (V_C - I_{PP}) (Note)

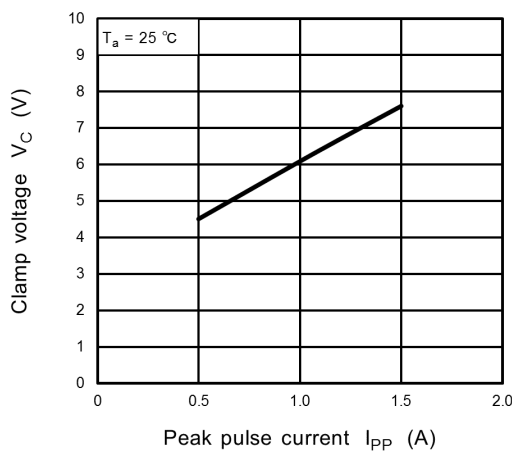


Fig. 6.3.1 V_C - I_{PP}

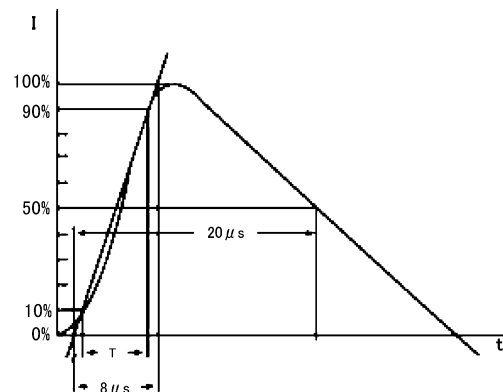


Fig. 6.3.2 Based on IEC61000-4-5 8/20 μ s pulse.

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V_{ESD}	(Note 1)	± 10	kV
Electrostatic discharge voltage (IEC61000-4-2) (Air)			± 10	
Peak pulse power ($t_p = 8/20\text{ }\mu\text{s}$)	P_{PK}		30	W
Peak pulse current ($t_p = 8/20\text{ }\mu\text{s}$)	I_{PP}	(Note 2)	1.5	A
Junction temperature	T_j		150	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.

Note 2: According to IEC61000-4-5.

8. Electrical Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

V_{RWM} : Working peak reverse voltage
 V_{BR} : Reverse breakdown voltage
 I_{BR} : Reverse breakdown current
 I_R : Reverse current
 V_C : Clamp voltage
 I_{PP} : Peak pulse current
 R_{DYN} : Dynamic resistance

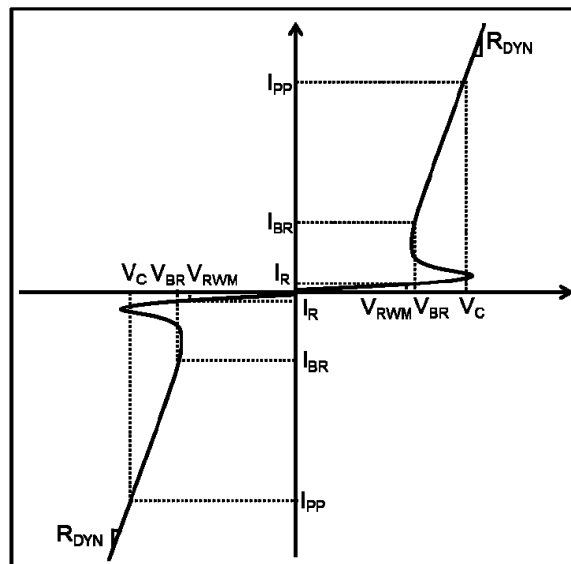


Fig. 8.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)	—	—	—	5.5	V
Total capacitance	C_t		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$	—	1.5	3.0	pF
Dynamic resistance	R_{DYN}	(Note 2)	—	—	0.25	—	Ω
Reverse breakdown voltage	V_{BR}		$I_{BR} = 1\text{ mA}$	5.7	—	8	V
Reverse current	I_R		$V_{RWM} = 5.5\text{ V}$	—	—	100	nA
Clamp voltage	V_C	(Note 3)	$I_{PP} = 1\text{ A}$	—	6	—	V
			$I_{PP} = 1.5\text{ A}$	—	7.7	20	
		(Note 2)	$I_{TLP} = 16\text{ A}$	—	18	—	V
			$I_{TLP} = 30\text{ A}$	—	21.5	—	

Note 1: Recommended operating condition.

Note 2: TLP parameters: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 8\text{ A}$ and $I_{PP2} = 16\text{ A}$.

Note 3: Based on IEC61000-4-5 8/20 μs pulse.

9. Characteristics Curves (Note)

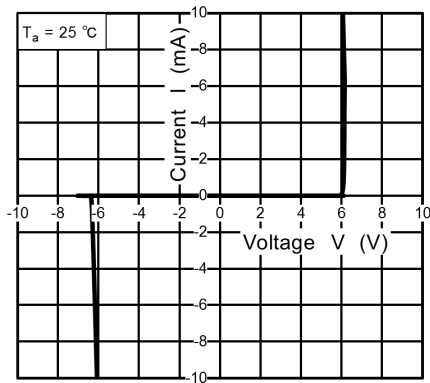


Fig. 9.1 I - V

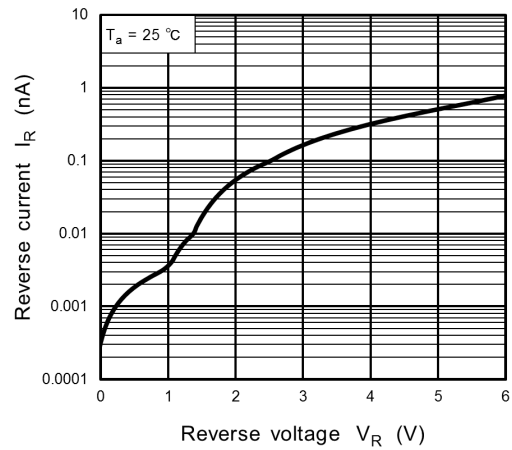


Fig. 9.2 $I_R - V_R$

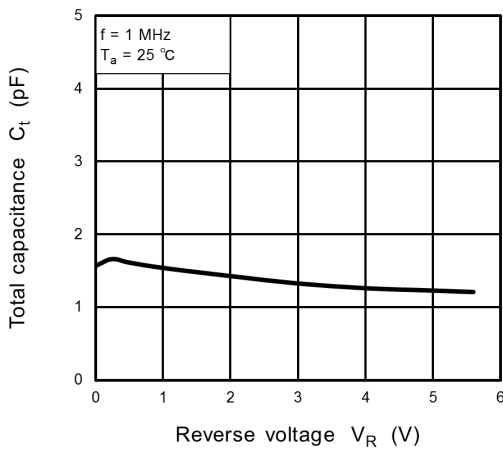


Fig. 9.3 $C_t - V_R$

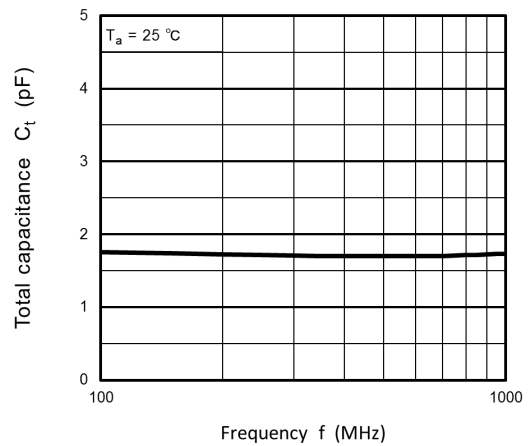


Fig. 9.4 $C_t - f$

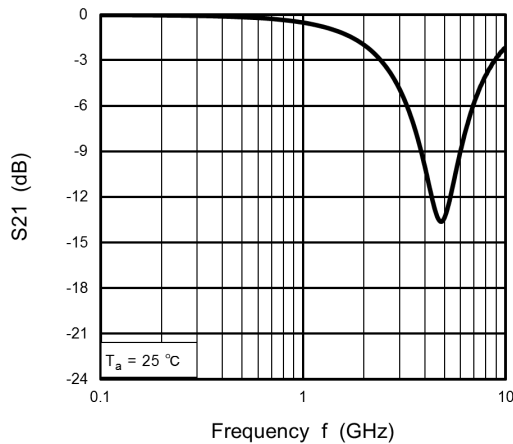
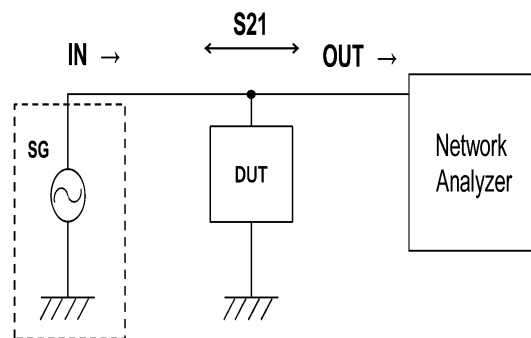
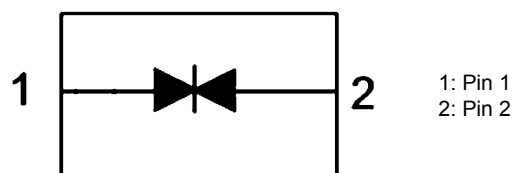


Fig. 9.5 $S_{21} - f$



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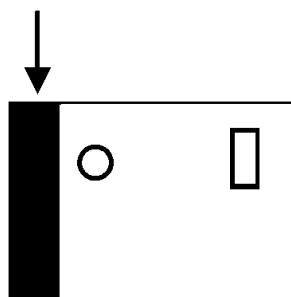
10. Internal Circuit (Note)



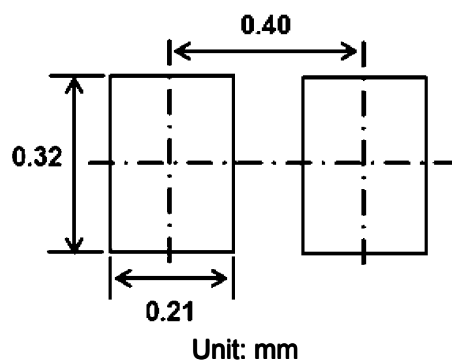
Note: Connect Pin 2 to GND when using Pin 1 for I/O.
Connect Pin 1 to GND when using Pin 2 for I/O.

11. Marking (Top view)

Pin 1 mark

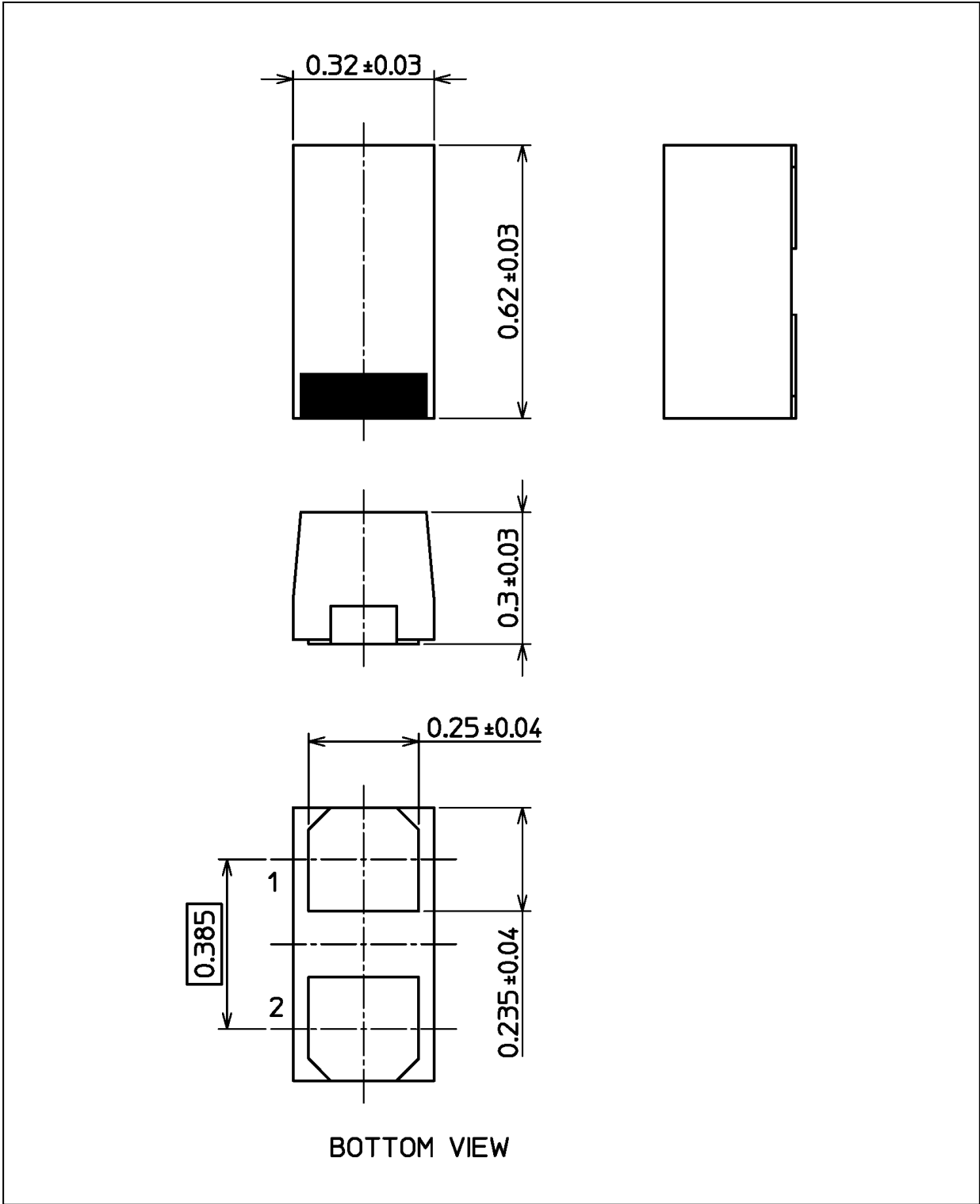


12. Land Pattern Dimensions (for reference only)



Package Dimensions

Unit: mm



Weight: 0.2 mg (typ.)

Package Name(s)
Nickname: SL2

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