

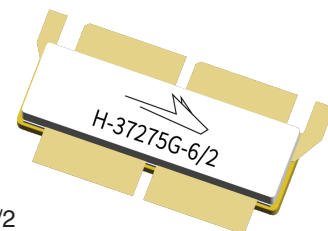
# PXAD184218FV

## Thermally-Enhanced High Power RF LDMOS FET

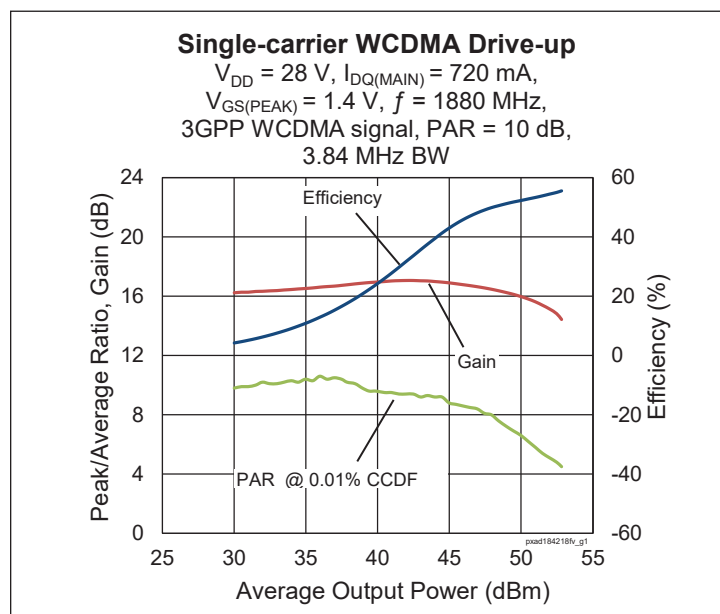
420 W, 28 V, 1805 – 1880 MHz

### Description

The PXAD184218FV is a 420-watt ( $P_{3dB}$ ) LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 1805 to 1880 MHz frequency band. Features include dual-path design, input and output matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PXAD184218FV  
Package H-37275G-6/2



### Features

- Broadband internal input and output matching
- Asymmetrical Doherty design
  - Main :  $P_{1dB} = 130\text{ W Typ}$
  - Peak :  $P_{1dB} = 290\text{ W Typ}$
- Typical Pulsed CW performance, 1842.5 MHz, 28 V, Doherty configuration
  - Output power at  $P_{3dB} = 420\text{ W}$
  - Efficiency = 62%
  - Gain = 14 dB
- Capable of handling 10:1 VSWR @ 28 V, 110 W (WCDMA) output power
- Integrated ESD protection
- Human Body Model class 2 (per ANSI/ESDA/ JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

### RF Characteristics

#### Two-carrier WCDMA Specifications (tested in Wolfspeed Doherty production test fixture)

$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 720\text{ mA}$ ,  $V_{GS(PEAK)} = 1.4\text{ V}$ ,  $P_{OUT} = 60\text{ W avg}$ ,  $f = 1880\text{ MHz}$ , 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	$G_{ps}$	15	16	—	dB
Drain Efficiency	$\eta_D$	49	51.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-28	-25.0	dBc
Output PAR@0.01% CCDF	OPAR	6.8	7.7	—	dBc

All published data at  $T_{CASE} = 25^\circ\text{C}$  unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

**DC Characteristics** (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	1	$\mu\text{A}$
	$V_{DS} = 63\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	10	$\mu\text{A}$
Gate Leakage Current	$V_{GS} = 10\text{ V}, V_{DS} = 0\text{ V}$	$I_{GSS}$	—	—	1	$\mu\text{A}$
On-State Resistance (Main)	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.03	—	$\Omega$
	(Peak) $V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.02	—	$\Omega$
Operating Gate Voltage (Main)	$V_{DS} = 28\text{ V}, I_{DQ} = 720\text{ mA}$	$V_{GS}$	2.3	2.6	2.9	V
	(Peak) $V_{DS} = 28\text{ V}, I_{DQ} = 0\text{ mA}$	$V_{GS}$	—	1.5	—	V

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	V
Gate-Source Voltage	$V_{GS}$	-6 to +10	V
Junction Temperature	$T_J$	225	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-65 to +150	$^{\circ}\text{C}$

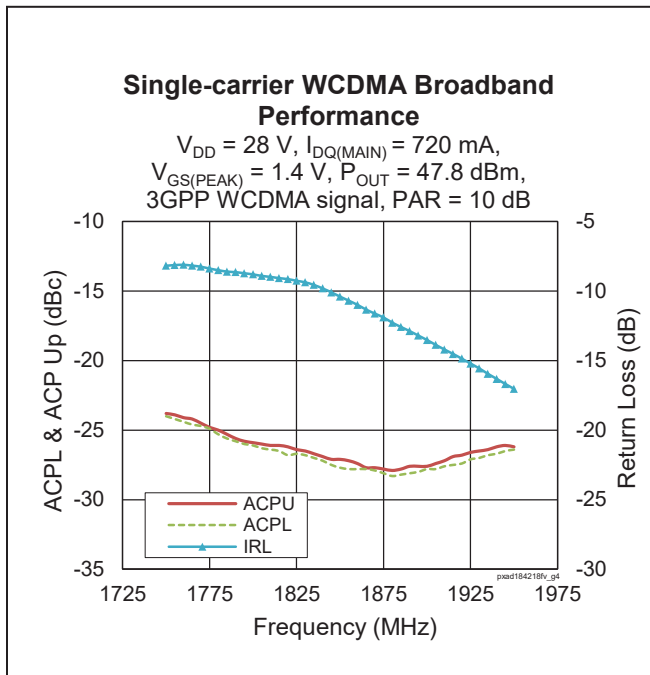
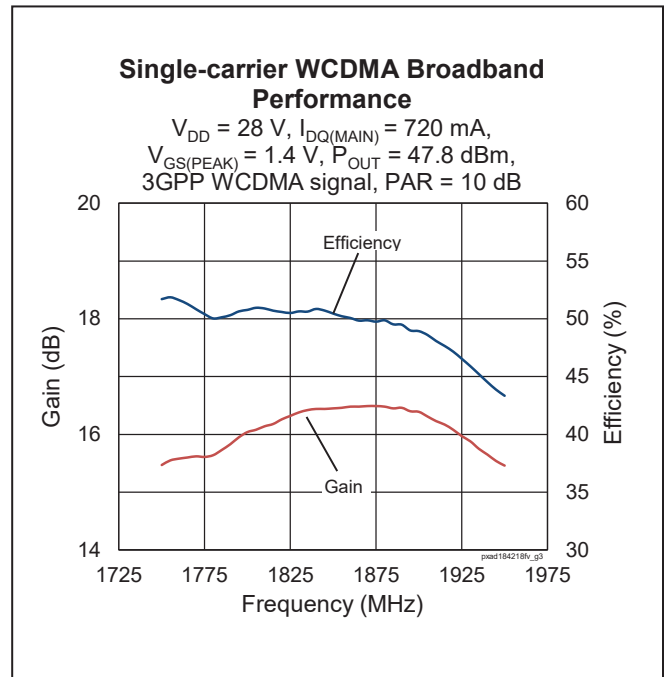
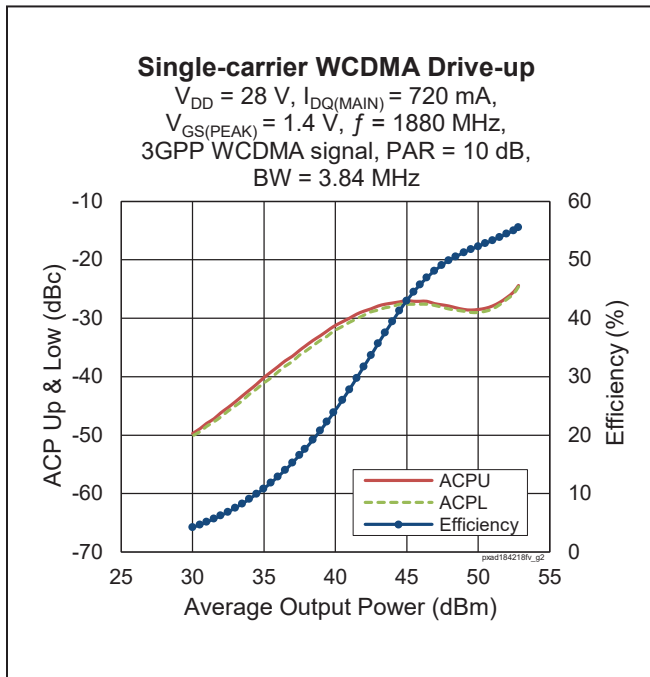
**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal Resistance (Main, $T_{CASE} = 70^{\circ}\text{C}$ , 60 W CW)	$R_{\theta JC}$	0.514	$^{\circ}\text{C}/\text{W}$
(Peak, $T_{CASE} = 70^{\circ}\text{C}$ , 280 W CW)	$R_{\theta JC}$	0.297	$^{\circ}\text{C}/\text{W}$

**Ordering Information**

Type and Version	Order Code	Package Description	Shipping
PXAD184218FV V1 R0	PXAD184218FV-V1-R0	H-37275G-6/2, earless flange	Tape & Reel, 50 pcs
PXAD184218FV V1 R2	PXAD184218FV-V1-R2	H-37275G-6/2, earless flange	Tape & Reel, 250 pcs

**Typical RF Performance** (data taken in production test fixture)





## Load Pull Performance

**Main Side Load Pull Performance** – Pulsed CW signal: 10  $\mu$ s, 10% duty cycle,  $V_{DD} = 28$  V,  $I_{DQ} = 960$  mA, class AB

		P <sub>1dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>1dB</sub> [dBm]	P <sub>1dB</sub> [W]	$\eta^D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>1dB</sub> [dBm]	P <sub>1dB</sub> [W]	$\eta^D$ [%]
1805	2.3 - j6.3	1.6 - j3.3	20.9	52.40	173	58.7	3.5 - j3.1	23.1	50.60	116	66.6
1842.5	3.2 - j7.4	1.4 - j3.5	20.2	52.45	176	56.2	2.7 - j2.7	22.4	51.30	134	67.7
1880	5.1 - j8.9	1.4 - j3.5	20.7	52.50	180	57.4	2.7 - j 3.1	22.8	51.40	138	67.5

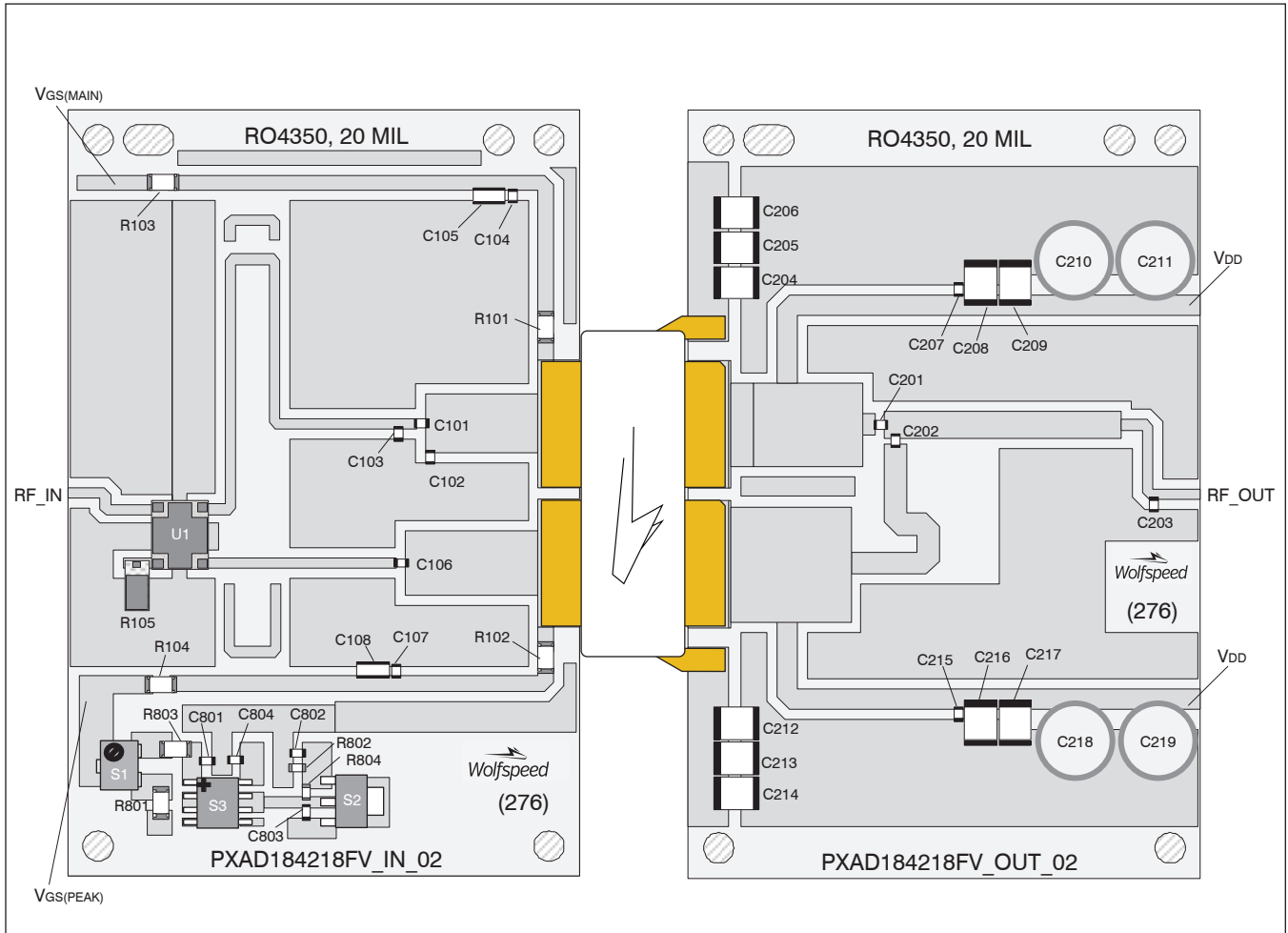
		P <sub>3dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>3dB</sub> [dBm]	P <sub>3dB</sub> [W]	$\eta^D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>3dB</sub> [dBm]	P <sub>3dB</sub> [W]	$\eta^D$ [%]
1805	2.3 - j6.3	1.4 - j3.5	18.4	53.20	210	58.5	2.9 - j3.7	20.6	52.00	157	67.4
1842.5	3.2 - j7.4	1.3 - j3.6	18.1	53.29	213	58.6	2.6 - j3.3	20.2	52.20	167	68.4
1880	5.1 - j8.9	1.4 - j3.7	18.6	53.27	212	58.8	2.7 - j3.2	20.7	52.10	162	68.6

**Peak Side Load Pull Performance** – Pulsed CW signal: 10  $\mu$ s, 10% duty cycle,  $V_{DD} = 28$  V,  $I_{DQ} = 10$  mA, class B

		P <sub>1dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>1dB</sub> [dBm]	P <sub>1dB</sub> [W]	$\eta^D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>1dB</sub> [dBm]	P <sub>1dB</sub> [W]	$\eta^D$ [%]
1805	2.1 - j4.6	1.1 - j3.3	17.1	55.38	345	54.7	2.8 - j2.2	18.7	53.27	212	66.7
1842.5	2.8 - j5.4	1.2 - j3.4	17.4	55.43	349	54.9	2.7 - j 2.2	18.8	53.30	214	66.7
1880	4.4 - j5.6	1.3 - j3.7	17.7	55.42	348	54.6	2.5 - j2.2	19.2	53.33	215	66.3

		P <sub>3dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>3dB</sub> [dBm]	P <sub>3dB</sub> [W]	$\eta^D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>3dB</sub> [dBm]	P <sub>3dB</sub> [W]	$\eta^D$ [%]
1805	2.1 - j4.6	1.2 - j3.6	14.9	56.17	414	56.9	2.8 - j2.6	16.5	54.20	265	66.8
1842.5	2.8 - j5.4	1.2 - j3.7	15	56.20	417	56.2	2.6 - j2.7	16.6	54.40	277	67.1
1880	4.4 - j5.6	1.3 - j3.8	15.6	56.14	411	56.2	2.4 - j2.9	17	54.80	301	66.9

Reference Circuit, 1805 – 1880 MHz



Reference circuit assembly diagram (not to scale)

**Reference Circuit** (cont.)**Reference Circuit Assembly**

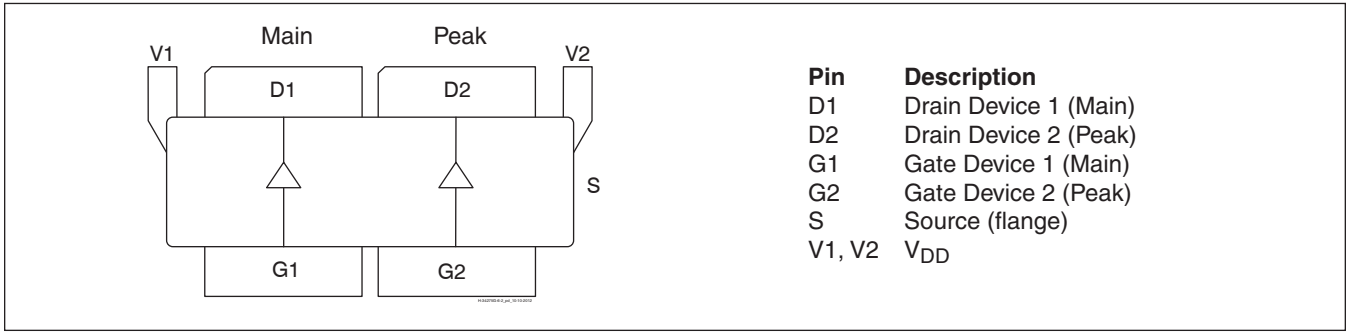
DUT	PXAD184218FV V1
Test Fixture Part No.	LTA/PXAD184218FV V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$ , $f = 1805 - 1880$ MHz
Find Gerber files for this test fixture on the Wolfspeed Web site at <a href="http://www.wolfspeed.com/RF">http://www.wolfspeed.com/RF</a>	

**Components Information**

Component	Description	Manufacturer	P/N
<b>Input</b>			
C101, C106	Capacitor, 22 pF	ATC	ATC800A220JT250T
C102	Capacitor, 1.8 pF	ATC	ATC800A1R8CT250T
C103	Capacitor, 0.6 pF	ATC	ATC800A0R6CT250T
C104, C107	Capacitor, 33 pF	ATC	ATC800A330JT250T
C105, C108	Capacitor, 10 $\mu$ F	Murata Electronics North America	LLL31MR60J106ME01L
R101, R102, R103, R104	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R105	Resistor, 50 ohms	Richardson	C16A50Z4
C801, C802, C803, C804	Capacitor, 1000 pF	AVX Corporation	06031C102KAT2A
R801	Resistor, 100 ohms	Panasonic Electronic Components	ERJ-8GEYJ101V
R802	Resistor, Chip 1.3K ohms	Panasonic Electronic Components	ERJ-3GEYJ132V
R803	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R804	Resistor, CHIP 1.2K ohms	Panasonic Electronic Components	ERJ-3GEYJ122V
S1	Resistor, Variable 2K ohms	Bourns Inc.	3224W-1-202E
S2	Transistor	Diodes Incorporated	BCP5616TA
S3	Voltage Regulator	Texas Instruments	LM78L05ACM
U1	Hybrid Coupler	Anaren	05X3C19P1-05S
<b>Output</b>			
C201	Capacitor, 7.5 pF	ATC	ATC800A7R5JT250T
C202	Capacitor, 33 pF	ATC	ATC800A330JT250T
C203	Capacitor, 0.3 pF	ATC	ATC800A0R3CT250T
C204, C205, C206, C208, C209, C212, C213 C214, C216, C217	Capacitor, 10 $\mu$ F	Taiyo Yuden	UMK325C7106MM-T
C207, C215	Capacitor, 22 pF	ATC	ATC800A220JT250T
C210, C211, C218, C219	Capacitor, 220 $\mu$ F	Panasonic Electronic Components	PCE4444TR-ND



**Pinout Diagram** (top view)



Package Outline Specifications

Package H-37275G-6/2

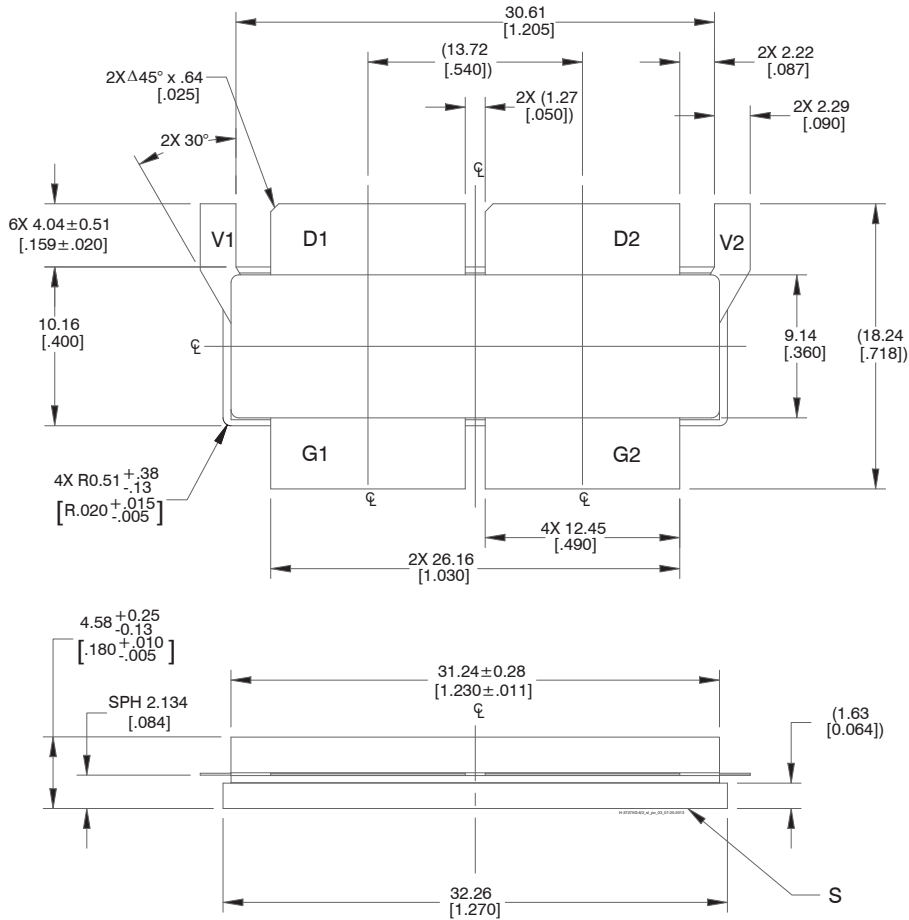


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances  $\pm 0.127$  [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source; V1, V2 –  $V_{DD}$ .
5. Lead thickness:  $0.13 + 0.051/-0.025$  mm [0.005+0.002/-0.001 inch].
6. Gold plating thickness:  $1.14 \pm 0.38$  micron [ $45 \pm 15$  microinch].



## Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2016-04-20	Advance	All	Data Sheet reflects advance specification for product development
02	2016-11-07	Production	All	Data Sheet reflects released product specification
02.1	2016-12-07	Production	1, 4	Revised typo in Features, revised PAE to Drain Eff in Load Pull performance
03	2018-06-25	Production	All	Converted to Wolfspeed Data Sheet

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## Notes

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