

TEMPERATURE SWITCH IC WITH LATCHwww.sii-ic.com

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Rev.3.0_00

The S-8130AA is a temperature switch with a latch function having a built-in semiconductor temperature sensor with the accuracy of $\pm 2.5^{\circ}\text{C}$. The output signal is inverted when the temperature is detected, and latched until a reset signal input or a detection of the power voltage lowering.

Low voltage operation down to 2.2 V is possible and the current consumption is low, 15 μA (typ.), due to CMOS configuration.

The S-8130AA consists of a temperature sensor having the temperature coefficient of $-13\text{ mV}/^{\circ}\text{C}$, a reference voltage source, a comparator, voltage detection circuit, and noise suppression circuit all of which are enclosed in 8-Pin MSOP package.

Since the temperature range of this IC is -40 to $+100^{\circ}\text{C}$, it is possible to achieve the extensive application for temperature control.

■ Features

- Detection temperature : $+60$ to $+95^{\circ}\text{C}$, 5°C step
- Detection accuracy : $\pm 2.5^{\circ}\text{C}$
- V_{SS} grounded temperature voltage output
- Low voltage operation : V_{DD} (min.)= 2.2 V
- Low current consumption : 15 μA typ. ($+25^{\circ}\text{C}$)
- A built-in circuit for preventing malfunction of temperature detection
- Output logic level is fixed by the latch after temperature detection
- Lead-free, halogen-free^{*1}

*1. Refer to “**■ Product Name Structure**” for details.

■ Applications

- Game console
- Electronic devices

■ Package

- 8-Pin MSOP

■ Block diagram

S-8130AAxFN-xxxT2z (Fixed detection temperature)

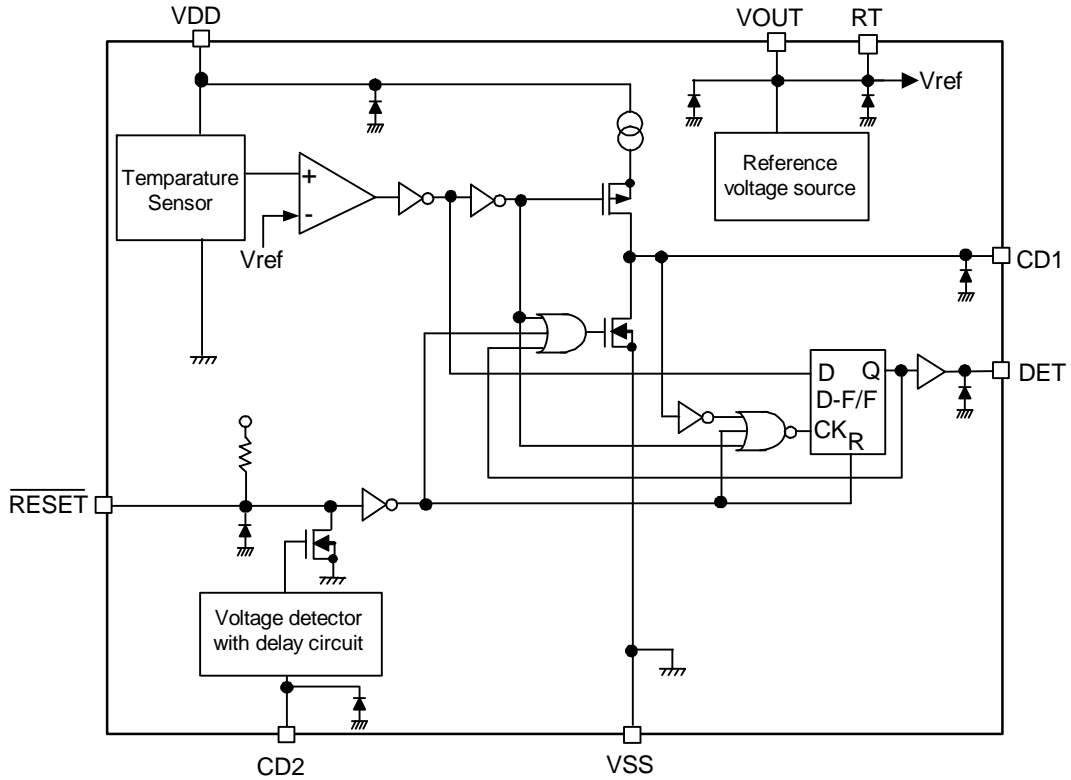
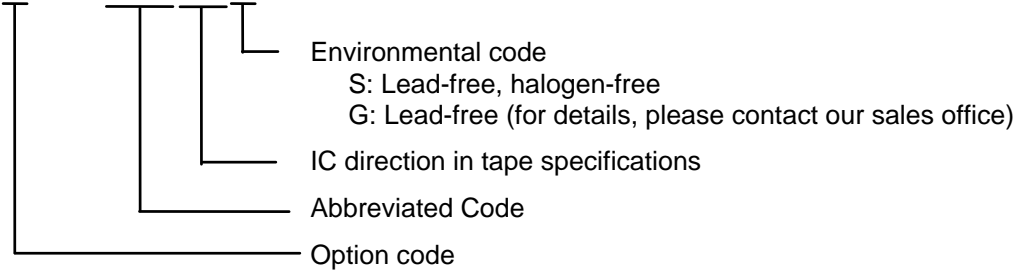


Figure 1

■ Product Name Structure

1. Product name

S - 8130 A A x F N - x x x T 2 x



Option list

- Detection temperature T_{DET} is selectable in 5°C step in the range between 60 and 95°C.
- DET output is selectable active high or active low.
- Release voltage V_{RET} is selectable in 0.1 V step in the range between 2.2 and 3.4 V.
- \overline{RESET} pin is selectable “Pull-up” or “Nch Open Drain”.

2. Package

| Package Name | Drawing Code | | |
|--------------|--------------|--------------|--------------|
| | Package | Tape | Reel |
| 8-Pin MSOP | FN008-A-P-SD | FN008-A-C-SD | FN008-A-R-SD |

3. Product name list

Table 1

| Product name | T_{DET} | DET output | V_{RET} | \overline{RESET} |
|--------------------|-----------|-------------|-----------|--------------------|
| S-8130AAAFN-MAAT2z | 80°C | Active high | 2.4 V | Pull-up |
| S-8130AACFN-MAET2z | 86°C | Active high | 2.9 V | Pull-up |

Remark1. Please contact our sales department for options other than those specified above.

2. z: G or S

■ Pin configuration

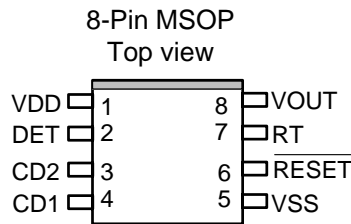


Figure 2

■ Pin Description

Table 2

| Pin No. | Pin Name | Function | Input/Output |
|---------|----------|--|---|
| 1 | VDD | Positive power supply pin | — |
| 2 | DET | Output pin for detection at the defined temperature | CMOS output : Output logic is selectable |
| 3 | CD2 | Capacitor connection pin for delay time setting in voltage detection | Input/Output |
| 4 | CD1 | Capacitor connection pin for time setting of malfunction prevention | Input/Output |
| 5 | VSS | Ground pin | — |
| 6 | RESET | Input/Output pin for reset Active low | Input : CMOS Output : N channel open drain (Pull-up resistance is optional) |
| 7 | RT | Reference voltage input pin (short-circuited to VOUT pin internally) | Input |
| 8 | VOUT | Output pin for reference voltage from the internal comparator | Output |

■ Absolute maximum ratings

Table 3

(Ta = 25 °C unless otherwise specified)

| Parameter | Symbol | Ratings | Unit |
|---|---|--|------|
| Supply voltage (V _{SS} =0.0 V) | V _{DD} | V _{SS} +12 | V |
| Pin voltage | V _{OUT} , V _{RT} , V _{RESET} , V _{DET} , V _{CD1} , V _{CD2} | V _{SS} -0.3 to V _{DD} +0.3 | V |
| Power dissipation | P _D | 300 (When not mounted on board) | mW |
| | | 500*1 | mW |
| Operating temperature | T _{opr} | -40 to +100 | °C |
| Storage temperature | T _{stg} | -55 to +125 | °C |

*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended values for external parts

Table 4

| Parameters | Symbol | Value | Unit |
|-----------------|-----------------|-------|------|
| CD1 capacitance | C _{D1} | 4.7 | nF |
| CD2 capacitance | C _{D2} | 4.7 | nF |

■ **DC Electrical Characteristics**

Table 5

(Ta=25°C, V_{SS}=0 V unless otherwise specified)

| Parameters | Symbol | Conditions | Min. | Typ. | Max. | Unit | |
|--|---|---|-------------------------|-------------------------|-------------------------|--------|----|
| Supply voltage | V _{DD} | — | 2.2 | — | 10.0 | V | |
| Detection temperature | T _D | — | T _{DET} -2.5 | T _{DET} | T _{DET} +2.5 | °C | |
| Output current 1 | I _{DETH} | V _{DD} =3 V Applied to DET pin | V _{DET} =2.2 V | 2 | 4 | — | mA |
| | I _{DETL} | | V _{DET} =0.4 V | 0.5 | 1 | — | mA |
| Input voltage | V _{ONH} | Applied to $\overline{\text{RESET}}$ pin | 0.8 × V _{DD} | — | V _{DD} | V | |
| | V _{ONL} | | V _{SS} | — | 0.2 × V _{DD} | V | |
| Pull-up resistance | R _{OL} | Applied to $\overline{\text{RESET}}$ pin V _{IN} =0 V, V _{DD} =3.0 V | 30 | 100 | 300 | kΩ | |
| Release voltage for voltage detector | V _R | — | V _{RET} × 0.98 | V _{RET} | V _{RET} × 1.02 | V | |
| Hysteresis width for voltage detector | V _{HYS} | — | — | V _{RET} × 0.05 | — | V | |
| Output current for voltage detector | I _{RSTL} | V _{DD} =3.0 V, V _{RESET} =0.5 V Applied to $\overline{\text{RESET}}$ pin | 0.5 | 1 | — | mA | |
| Temperature coefficient for voltage detector | $\frac{\Delta V_{\text{RET}}}{\Delta T_a \cdot V_{\text{RET}}}$ | Ta= -40 to 100°C | — | ±100 | — | ppm/°C | |
| Operating current | I _{DD} | V _{DD} =3.3 V | — | 15 | 30 | μA | |

■ **AC Electrical Characteristics**

Table 6

(Ta=25°C unless otherwise specified)

| Parameters | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|--------------------|---|------|------|------|------|
| Noise filtering time | T _{noise} | C _{D1} =4.7 nF, V _{DD} =3 V | 10 | 30 | 50 | ms |
| Delay time for voltage detector | T _{delay} | C _{D2} =4.7 nF, V _{DD} =3 V | 10 | 30 | 50 | ms |

Definition of the symbols used in the voltage detection circuit

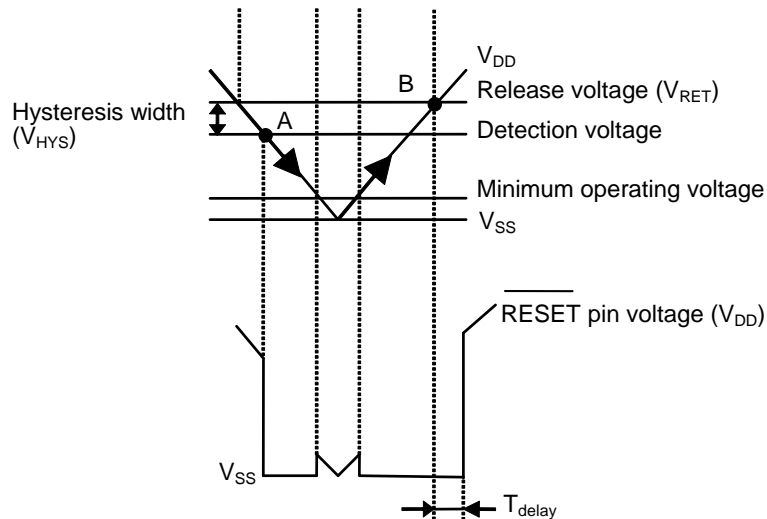


Figure 3

■ Description of Operation

1. Basic operation

S-8130AA series is a temperature switch which detects the temperature and sends a signal to an external device. The users can select a combination of the parameters such as detection temperature and release voltage.

The following is the case that the DET output is active high.

When the power voltage is turned on, the DET pin voltage goes to low since the flip-flop circuit in the detection circuit is cleared by the delayed voltage detection circuit. Temperature detection then starts and the DET pin is held low as long as the temperature is lower than the detection temperature. The temperature rises and when the temperature exceeds the detection temperature; longer than the time defined by the capacitor connected to the CD1 pin, the DET pin goes to high. Once the over-temperature is detected and the DET pin goes to high, the state is held by the flip-flop circuit. In order to release the state the $\overline{\text{RESET}}$ pin voltage should be set to low by the external signal or the power voltage should be set under the detection voltage of the built-in detector to reset the internal circuit.

Using the internal reference voltage and built-in temperature sensor, the accuracy of $\pm 2.5^\circ\text{C}$ in the detection temperature is achieved.

Noise Protection circuit

The noise protection circuit prevents malfunction of the temperature switch caused by noise.

The noise protection circuit starts charging the capacitor connected to the CD1 pin when the output of the internal comparator enters active state due to an external noise or a rapid change in the power voltage. In the normal operation the flip-flop circuit is set when the capacitor is charged to a certain voltage. But in the noise triggered operation the comparator output goes back to inactive state and the CD1 pin voltage is held low since the charging of the capacitor is insufficient. As a result the DET pin is held low and malfunction does not occur.

Noise suppression time, T_{noise} , is determined by the time constant consisting of internal constant current and the capacitance C_{D1} , and calculated by the following equation.

$$T_{\text{noise}} (\text{ms}) = \text{Noise suppression time coefficient} \times C_{D1} (\text{nF})$$

Noise suppression time coefficient (25°C): Typ. 6.4

2. Voltage detection circuit with delay

The delay circuit in the voltage detector provides a delayed output signal to the $\overline{\text{RESET}}$ pin when the power voltage V_{DD} rises and exceeds the release voltage V_R . On the other hand no delay occurs when the power voltage V_{DD} goes lower than the detection voltage, $V_R - V_{HYS}$.

The delay time, T_{delay} , is determined by the time constant consisting of internal constant current and the capacitance C_{D2} , and calculated by the following equation.

$$T_{\text{delay}} (\text{ms}) = \text{Delay coefficient} \times C_{D2} (\text{nF})$$

Delay coefficient (25°C): Min. 4.3, Typ. 6.4, Max. 8.5

- Layout the board wiring so that the current does not flow into or flow out of the CD2 pin to have correct delay time since the impedance of the CD2 pin is high.
- Capacitance of the external capacitor C_{D2} has no limitation as long as its leak current is negligible compared to the internal constant current. The difference occurs in delay time if the capacitor has leak current. When the leak current is larger than the internal constant current, the voltage detection circuit does not release reset.

■ Application circuit

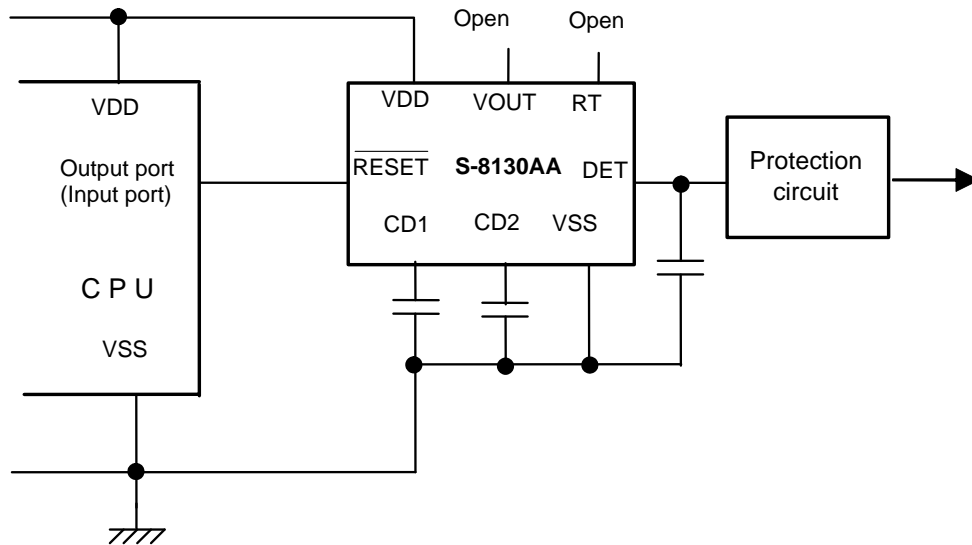


Figure 4

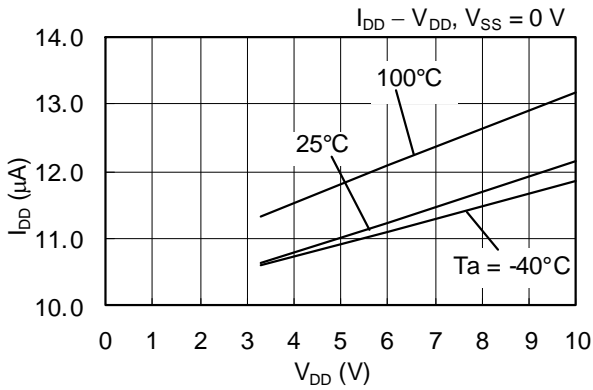
Caution The above connection diagram will not guarantee successful operation. Perform thorough evaluation using actual application to set the constant.

■ Precautions

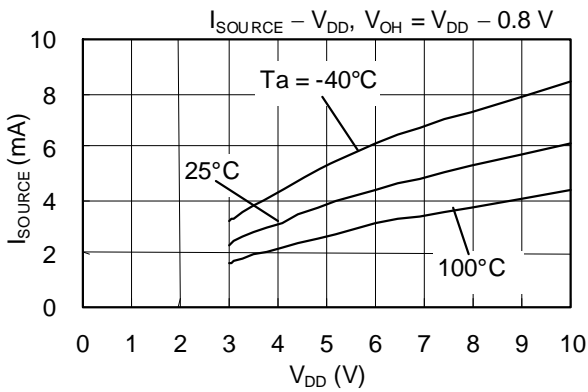
- (1) Since the S-8130AA has a voltage detector inside, control for the $\overline{\text{RESET}}$ pin is not necessary to activate the circuit as seen in **Figure 4**. In this case the $\overline{\text{RESET}}$ pin should be open.
- (2) A capacitor of around 1 μF should be connected to the DET pin to prevent malfunction caused by a noise due to the power on.
- (3) Nothing should be connected to the VOUT pin and the RT pin. These pins should be left open.
- (4) Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

■ Typical Characteristics

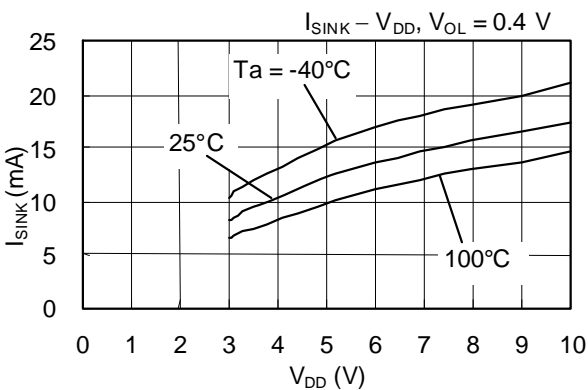
1. Current consumption vs. power voltage

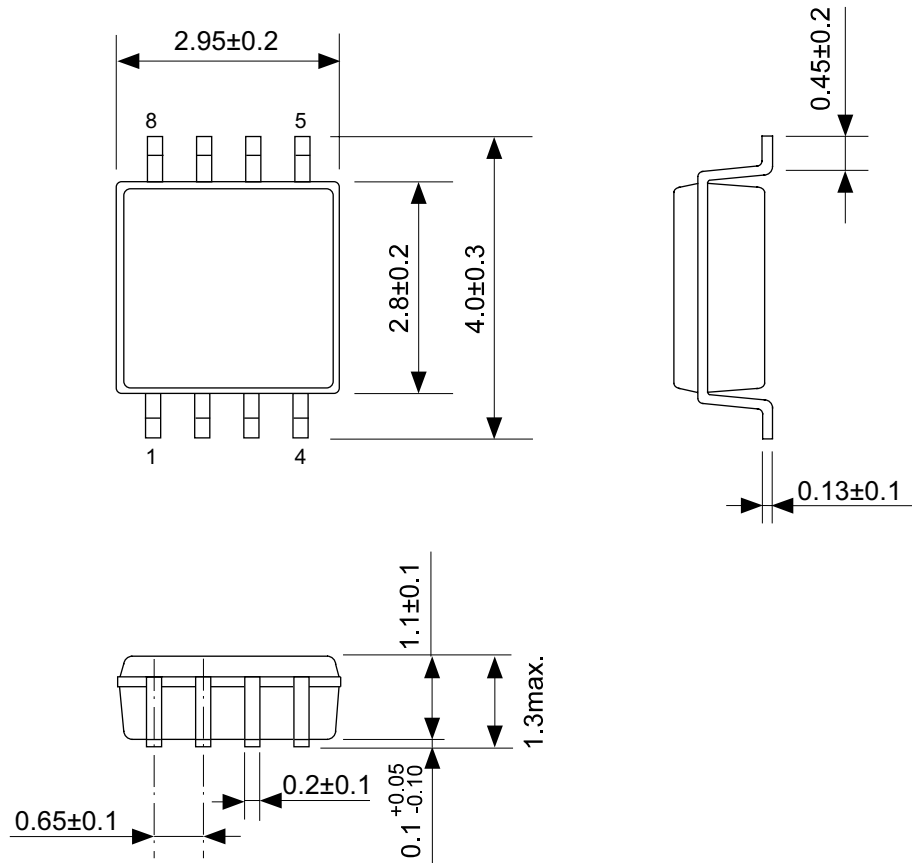


2. DET pin I_{SOURCE} vs. V_{DD} characteristics



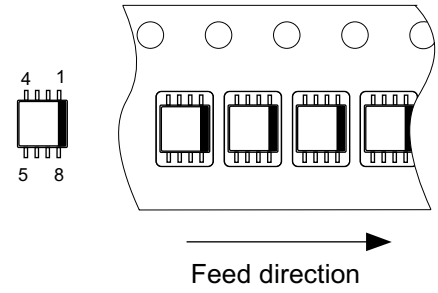
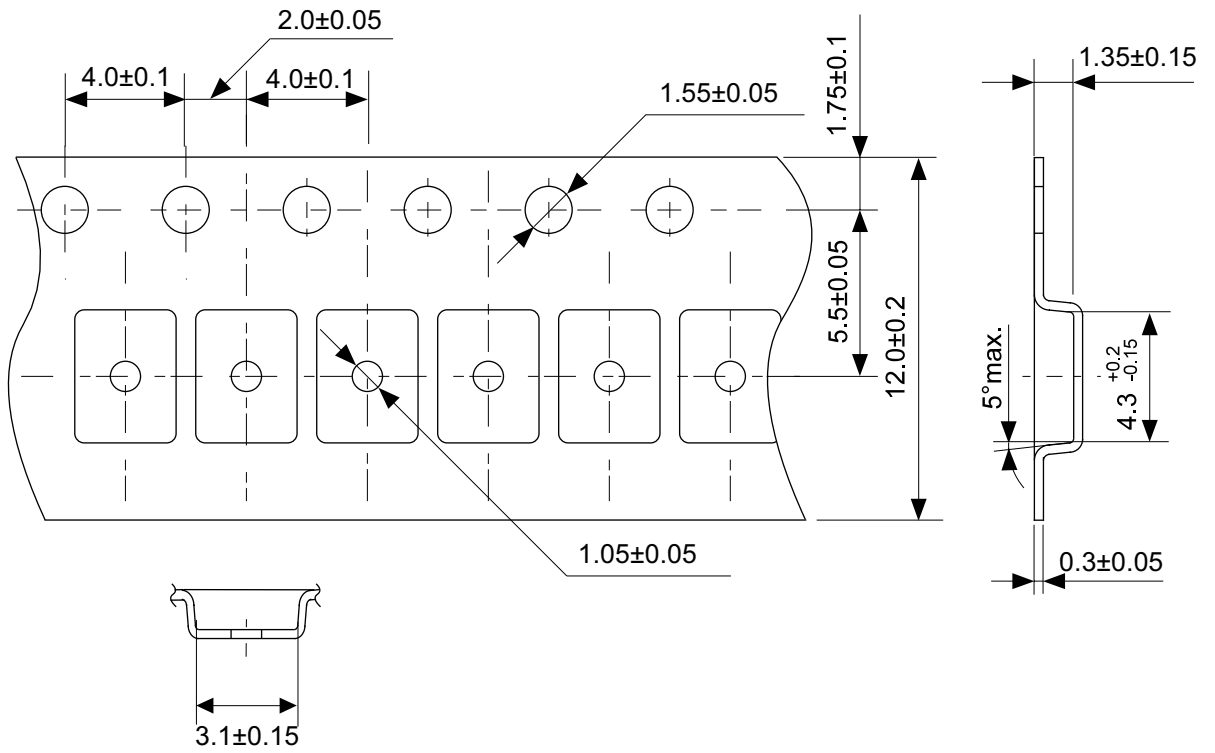
3. DET pin I_{SINK} vs. V_{DD} characteristics





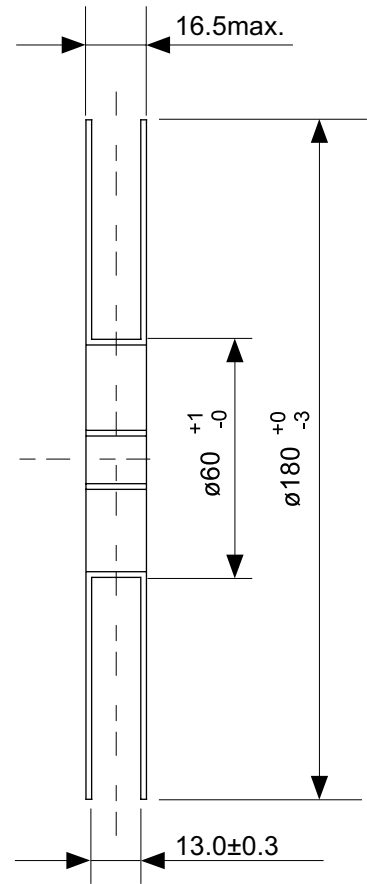
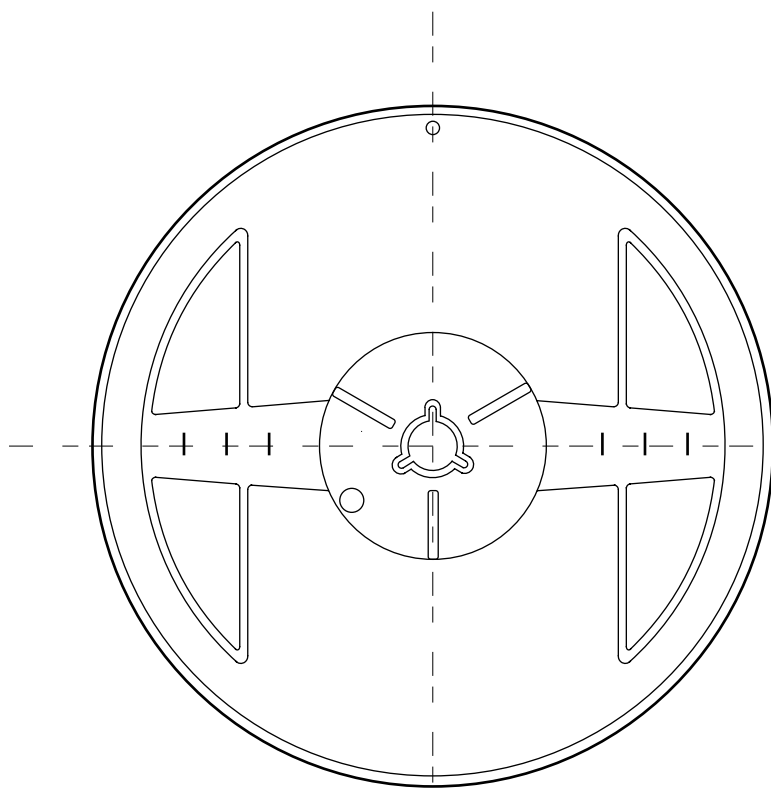
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| | |
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| Seiko Instruments Inc. | |

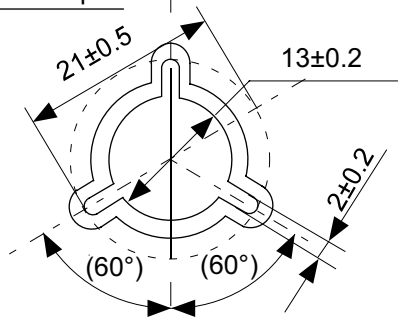


No. FN008-A-C-SD-1.1

| | |
|------------------------|----------------------|
| TITLE | MSOP8-A-Carrier Tape |
| No. | FN008-A-C-SD-1.1 |
| SCALE | |
| UNIT | mm |
| Seiko Instruments Inc. | |



Enlarged drawing in the central part



No. FN008-A-R-SD-1.1

| | | | |
|------------------------|------------------|------|-------|
| TITLE | MSOP8-A-Reel | | |
| No. | FN008-A-R-SD-1.1 | | |
| SCALE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
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