FEDL62Q1300-03
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ML62Q1300 Group

16-bit micro controller

GENERAL DESCRIPTION

ML62Q1300 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory(Flash memory), data memory(RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC generator, DMA controller, Clock generator, Timer, General Purpose Ports, UART, Synchronous serial port, I^2C bus interface unit (Master, Slave), Buzzer, Voltage Level Supervisor(VLS), Successive approximation type A/D converter, D/A converter , Analog comparator, Safety function(IEC60730/60335 Class B) and so on.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP(In-System Programming) function supports the Flash programming in production line.
The ML62Q1300 Group has six packages (16pin - 32pin) and five kinds of memory sizes(16Kbyte - 64Kbyte).

Table 1 ML62Q1300 Group Product List

Program memory	Data memory (RAM)	Data Flash	16pin SSOP16 WQFN16	20pin TSSOP20	24pin WQFN24	32pin TQFP32 WQFN32
64Kbyte	4Kbyte	2Kbyte	—	—	ML62Q1347	ML62Q1367
48Kbyte			—	—	ML62Q1346	ML62Q1366
32Kbyte			—	—	ML62Q1345	ML62Q1365
32Kbyte	2Kbyte		ML62Q1325	ML62Q1335	—	—
24Kbyte			ML62Q1324	ML62Q1334	—	—
16Kbyte			ML62Q1323	ML62Q1333	—	—

FEATURES

- CPU
  - 16-bit RISC CPU: nX-U16/100(A35 core)
  - Instruction system: 16-bit length instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Built-in On-chip debug function
  - Built-in ISP (In-System Programming) function
  - Minimum instruction execution time
    Approximately 30.5 µs (at 32.768 kHz system clock)
    Approximately 62.5ns/41.6ns (at 16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Multiplication : 16bit × 16bit (operation time : 4 cycles)
  - Division : 32bit ÷ 16bit (operation time : 8 cycles)
  - Division : 32bit ÷ 32bit (operation time : 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time : 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time : 4 cycles)
  - Signed or Unsigned is selectable

- Operating voltage and temperature
  - Operating voltage: VDD = 1.6 to 5.5 V (V_{DD} should be 1.8V or over at Power-on)
  - Operating temperature: -40 °C to +105 °C

- Internal memory
  - Program memory area
    Rewrite count: 100 cycles
    Write unit: 32bit(4byte)
    Erase unit: 16Kbyte/1Kbyte
    Erase/Write temperature: 0 °C to +40 °C

  - Data Flash memory area
    Rewrite count 10,000 cycles
    Write unit: 8bit(1byte)
    Erase unit: all area/128byte
    Erase/Write temperature: -40 °C to +85 °C
    Back Ground Operation(CPU can work while erasing and rewriting)

    This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.
    SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.

  - Data RAM area
    Rewrite unit: 8bit/16bit(1byte/2byte)
    Parity check function is available (interrupt / reset are generatable at Parity error)

- Clock
  - Low-speed clock (LSCLK)
    Internal low-speed RC oscillation: Approximately 32.768 kHz
  - High-speed clock (HSCLK)
    PLL oscillation: 2 selectable oscillation frequency (24MHz and 16MHz) by code option
  - Watch Dog Timer (WDT): built-in independent clock for WDT (RC1K: Approximately 1kHz)

- Reset
  - Reset by reset input pin
  - Reset by Power-On Reset
  - Reset by WDT overflow
  - Reset by WDT invalid clear
  - Reset by RAM parity error
  - Reset by unused ROM area access (instruction access)
  - Reset by voltage level supervisor (VLS)
  - Software reset by BRK instruction (reset CPU only)
  - Reset the peripherals individually
  - Collective reset to the all control pins and peripheral circuits

- Power management
  - HALT mode: CPU stops executing instruction, peripheral circuits continue working
  - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits continue working with low-speed clock
  - STOP mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop.
  - STOP-D mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop. The internal logic voltage (V_{DDL}) goes down to reduce the current consumption (RAM data is retained).
  - Clock gear: High-speed system clock frequency can be changed (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of HSCLK)
  - Block Control Function: Powers down the unused function blocks (reset the block or stop supplying the clock)

- Interrupt controller
  - External interrupt ports : max. 8
  - Non-maskable interrupt source: 1 (Internal sources: WDT)
  - Maskable interrupt sources: max.32
  - Four step interrupt levels

- Watchdog timer(WDT)
  - Selectable Operating clock : select RC1K or LSCLK by code option
  - Overflow period: 8selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2s and 8s)
  - Selectable window function (enable or disable): configurable clear enable period (50% or 75% of overflow period)
  - Selectable WDT operation : select Enable or Disable by code option
  - Readable WDT counter : WDT counter monitor function

- DMA(Direct Memory Access) controller
  - Channel: 2channel
  - Transfer unit: 8bit/16bit
  - Transfer count: 1 to 1024
  - Transfer cycle: 2 cycle transfer
  - Transfer address: Fixed addressing mode, inclement addressing mode , and decrement addressing mode
  - Transfer target: Special Function Register (SFR)/RAM → SFR/RAM (Transfer from/to Flash is not supported)
  - Transfer request: External pins, Serial communication unit, Successive approximation type A/D converter, 16bit timer, and Functional timer

- Low-speed Time base counter
  - Generate 8 frequency (128Hz to1Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
  - Selectable 3 interrupts from eight frequency internal pulse signals
  - 1Hz or 2Hz output from general purpose port

- Functional timer
  - Channel: 4 channel
  - Built-in timer, capture, and PWM function by 16 bit counter
  - Built-in Repeat mode, One shot mode is available
  - Two types of PWM output with the same period and different duties, and complementary PWM output with the dead time
  - Monitor input signal duty and the period by capture function
  - Generate periodical interrupts, duty interrupts, and interrupts coincided with set value
  - Counter Start, Stop, Counter clear triggered by an external inputs or Timer
  - Generate Emergency stop and emergency stop interrupt triggered by an external input
  - Same start/stop among different channels of the functional timer
  - Selectable counter clock(external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channels

- 16-bit General timers
  - Channel: Max. 6channel
  - 8 bits timer mode and 16-bit timer mode
  - Same start/stop among different channels of 16bit (8bit) timer
  - Timer output (toggled by overflow)
  - Selectable counter clock (external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channels

- Serial communication unit
  - Synchronous Serial Port (SSIO) mode or UART mode is selectable
  - Channel: 2channel

    < Synchronous Serial Port >
    – Selectable from Master and Slave
    – Selectable from LSB first or MSB first
    – Selectable 8-bit length or 16-bit length

    < UART mode>
    – Full-duplex communication (One Full-duplex UART is configurable as two half-duplex UARTs)
    – 5 to 8 bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits
    – Selectable from Positive logic or Negative logic
    – Selectable from LSB first or MSB first
    – Configurable wide range communication speed
    32.768kHz operation clock : 1bit/s to 4,800 bit/s
    24MHz operation clock : 600bit/s to 3M bit/s
    16MHz operation clock : 300bit/s to 2M bit/s
    – Built-in baud rate generator

- I^2C bus unit (Master / Slave)
  - Selectable from Master mode or Slave mode
  - Channel: 1 channel

    < Master function >
    – Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
    – Handshake (Clock synchronization)
    – 7bit address format (10bit address format is supported)

    < Slave function >
    – Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
    – Clock stretch function
    – 7bit address format

- I^2C bus Master
  - Channel: 1channel
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock synchronization)
  - 7bit address format (10bit address format is supported)

- General-purpose ports (GPIO)
  - I/O port: Max. 28 (Including one pin for on-chip debug and pins for other shared functions)
  - External interrupt port: 8
  - LED driver port : Max. 27
  - Carrier frequency output function (used for IR communication)

- Successive approximation type A/D converter (SA-ADC)
  - Channel: Max.8channel
  - Resolution: 10bit
  - Conversion time: Min. 2.25μs /channel (When the conversion clock speed is 8MHz)
  - Referece voltages are selectable
    (V_{DD} pin / Internal reference voltage(V_{REFI} = Approximately 1.55V) / External reference voltage (V_{REF} pin))
  - Selected channel repeat conversion
  - Dedicated result register for each channel
  - Interrupt determining by upper limit or lower limit threshold of conversion result

- Voltage level supervisor (VLS)
  - Accuracy: ±4%
  - Threshold voltage: 12 selectable (from 1.85V to 4.00V)
  - Functional Voltage level detection reset (VLS reset)
  - Functional Voltage level detection interrupt (VLS0 interrupt)

- Analog comparator
  - Channel: 1channel
  - Selectable interrupt from the comparator output (rising edge or falling edge)
  - Selectable from sampling or without sampling
  - Comparable with external 2 inputs
  - Comparable with external input and internal reference voltage (0.8V)

- D/A converter
  - Channel: Max 1channel
  - Resolution: 8bit
  - Output impedance: 6k ohm(Typ.)
  - R-2R ladder type

- Buzzer
  - 4 buzzer mode (Continuous sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
  - 8 frequencies (4.096kHz to 293Hz)
  - 15 step duty (1/16 to 15/16)
  - Selectable from positive logic buzzer output or negative logic buzzer output

- CRC(Cyclic Redundancy Check) generator
  - Generation equation: $X^{16}+X^{12}+X^5+1$
  - Selectable from LSB first or MSB first
  - Built-in Automatic program memory CRC calculation mode in HALT mode

- Safety Function(IEC60730/60335 Class B)
  - RAM/SFR guard
  - Automatic program memory CRC calculation
  - RAM parity error detection
  - ROM unused area access reset (instruction access)
  - Clock mutual monitoring
  - WDT counter monitoring
  - SA-ADC test
  - UART test
  - Synchronous serial I/O test
  - I^2C bus test
  - GPIO test

- Shipping package

  - 16-pin plastic SSOP
    ML62Q1323/1324/1325 - xxxMB (Blank part: ML62Q1323/1324/1325-NNNMB)
  - 16-pin plastic WQFN
    ML62Q1323/1324/1325 - xxxGD (Blank part: ML62Q1323/1324/1325-NNNGD)
  - 20-pin plastic TSSOP
    ML62Q1333/1334/1335 - xxxTD (Blank part: ML62Q1333/1334/1335-NNNTD)
  - 24-pin plastic WQFN
    ML62Q1345/1346/1347 - xxxGD (Blank part: ML62Q1345/1346/1347-NNNGD)
  - 32-pin plastic TQFP
    ML62Q1365/1366/1367 - xxxTB (Blank part: ML62Q1365/1366/1367-NNNTB)
  - 32-pin plastic WQFN
    ML62Q1365/1366/1367 - xxxGD (Blank part: ML62Q1365/1366/1367-NNNGD)

  xxx: ROM code number

ML62Q1300 Group how to read the part number

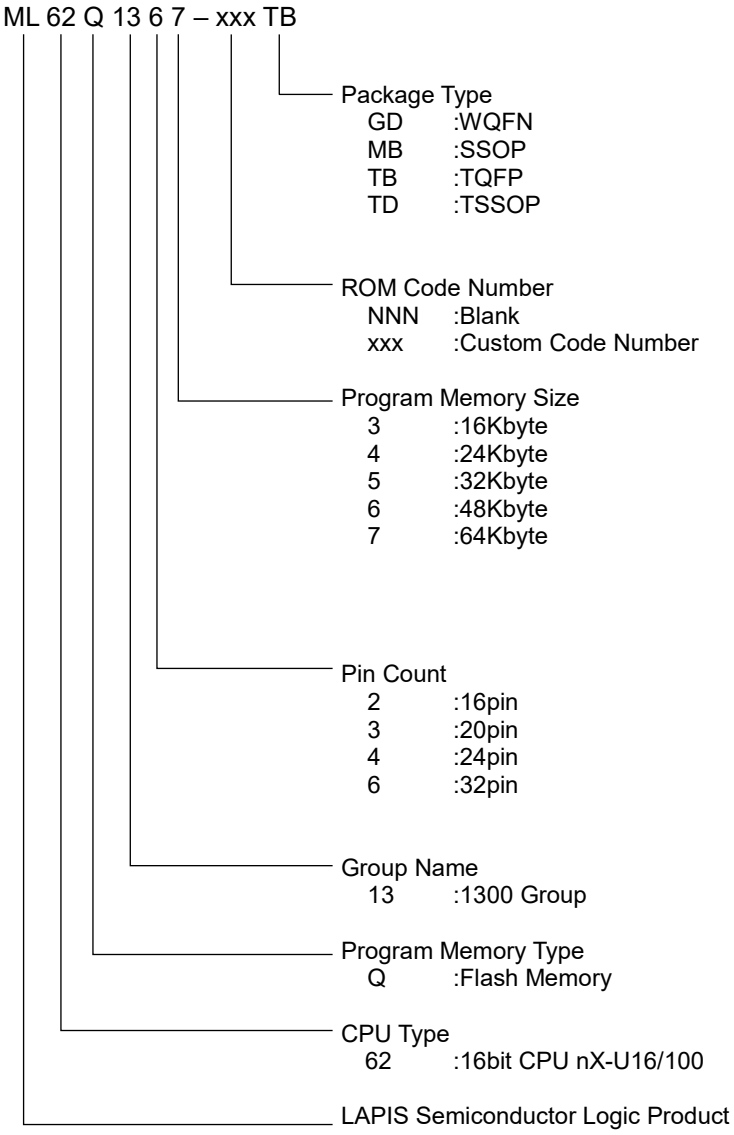


Figure 1 ML62Q1300 Group Part Number

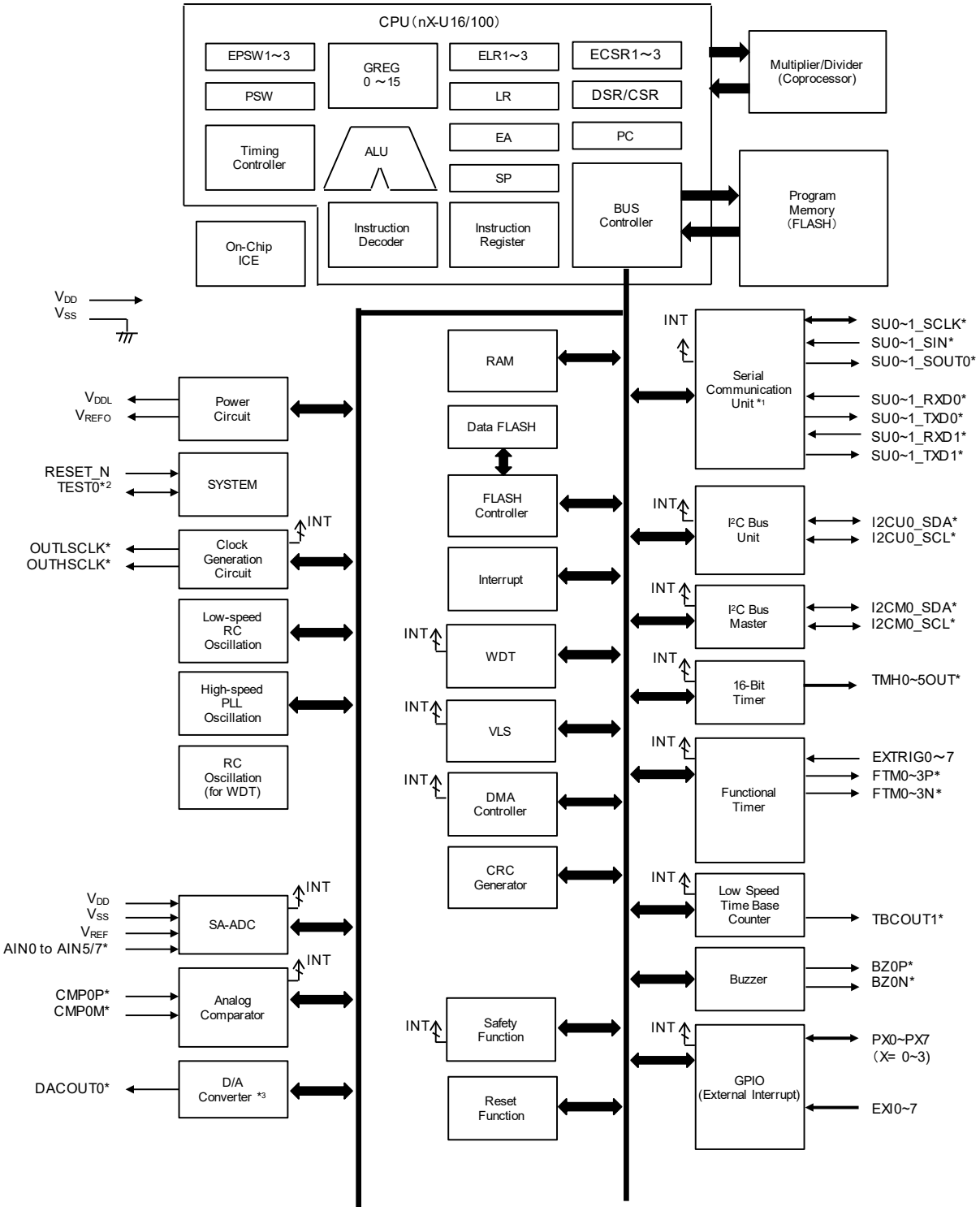
ML62Q1300 Group Main Function List

Table 2 ML62Q1300 Group Main Function List

Part number	Pin					Interrupt		Timer		Serial			Analog			
	Total pin-counts	Power pin counts	Reset Input pin	I/O port	LED drive port	Internal interrupt [source]	External interrupt [port]	Functional Timer [channel]	16-bit Timer [channel] *1	Full-duplex UART or Synchronous serial [channel] *2	I^2C bus unit (Master/Slave) [channel]	I^2C bus interface (Master only) [channel]	10bit Successive type A/D converter [channel]	Analog comparator [channel]	Analog comparator [input pin]	8bit D/A converter [channel]
ML62Q1323	16	3	1	12	11	23	8	4	4	2	1	1	6	1	2	0
ML62Q1324																
ML62Q1325																
ML62Q1333	20			16	15								8			
ML62Q1334																
ML62Q1335																
ML62Q1345	24			20	19	25			6							1
ML62Q1346																
ML62Q1347																
ML62Q1365	32			28	27											
ML62Q1366																
ML62Q1367																

*1 : One 16-bit timer is configurable as two 8-bit timers.
*2 : Full-duplex UART and Synchronous Serial Port can not be used simultaneously in the same channel. One Full-duplex UART is configurable as two half-duplex UARTs.

BLOCK DIAGRAM



* : Indicates the shared function of general ports.
*1 : One channel Full-duplex UART is configurable as two channel Half-duplex UART.
*2 : Not available as the input port when connecting to the on-chip debug emulator.
*3 : ML62Q133x and ML62Q132x does not have the peripheral circuits.

Figure 2 ML62Q1300 Group Block Diagram

PIN CONFIGURATION

Pin Layout of ML62Q1323/1324/1325 16pin SSOP Package

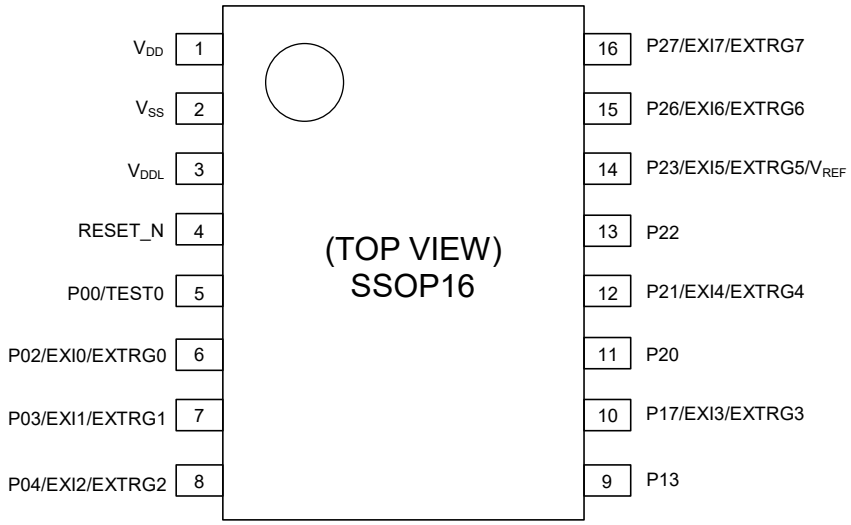


Figure 3 Pin Layout of 16pin SSOP Package

Pin Layout of ML62Q1323/1324/1325 16pin WQFN Package

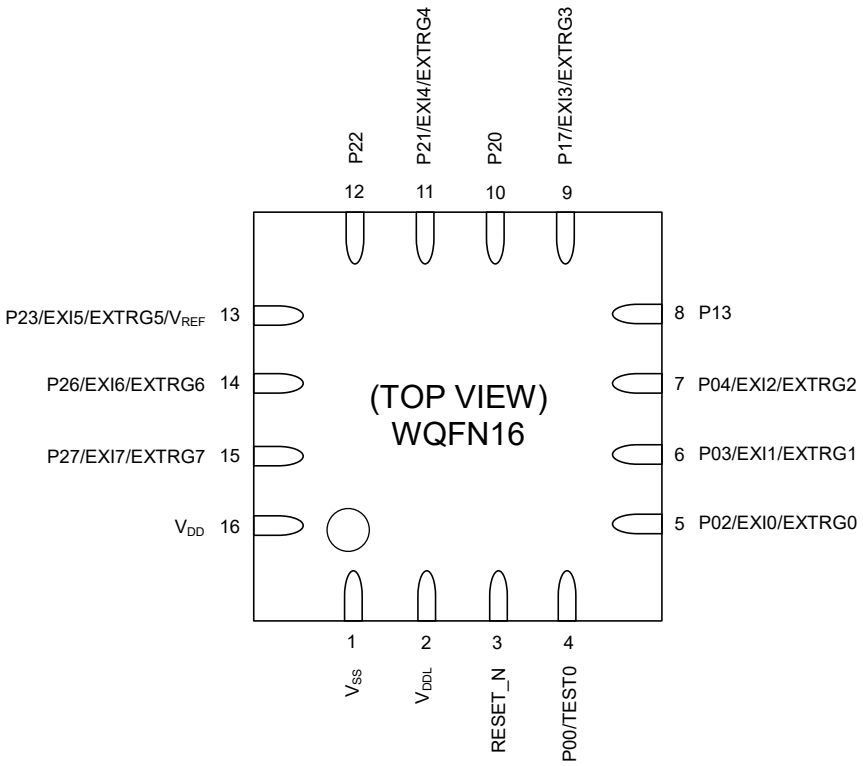


Figure 4 Pin Layout of 16pin WQFN Package

Pin Layout of ML62Q1333/1334/1335 20pin TSSOP Package

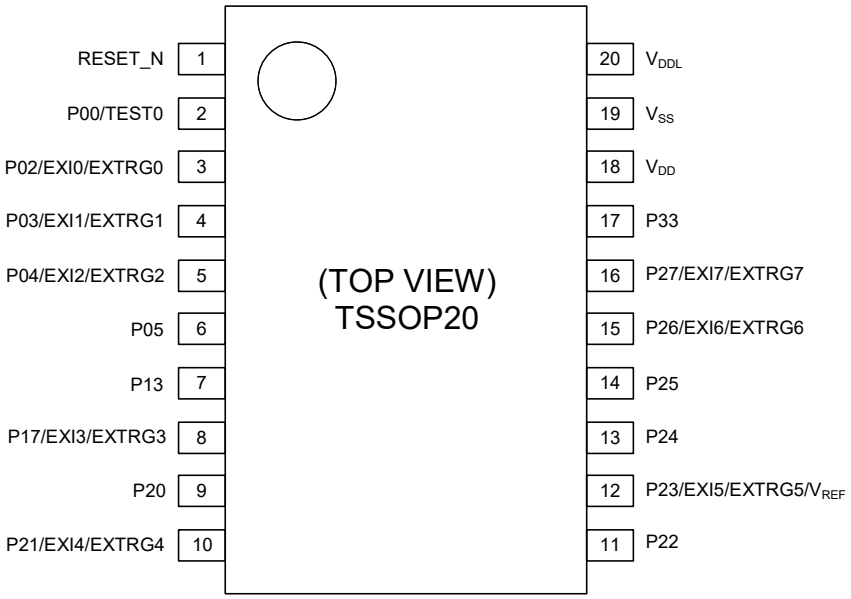


Figure 5 Pin Layout of 20pin TSSOP Package

Pin Layout of ML62Q1345/1346/1347 24pin WQFN Package

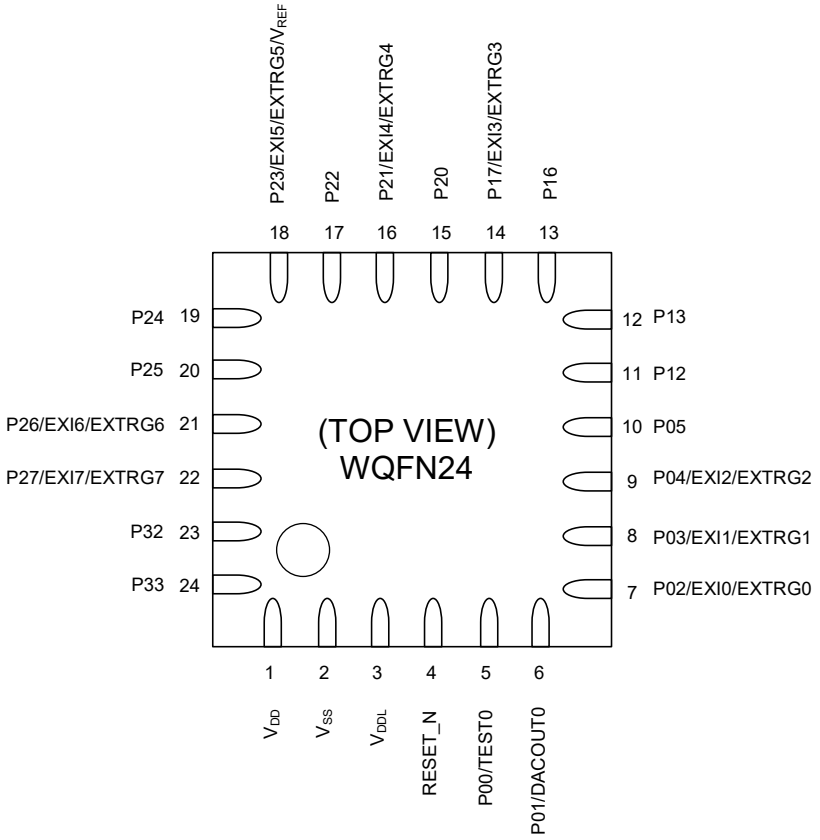


Figure 6 Pin Layout of 24pin WQFN Package

Pin Layout of ML62Q1365/1366/1367 32pin TQFP Package

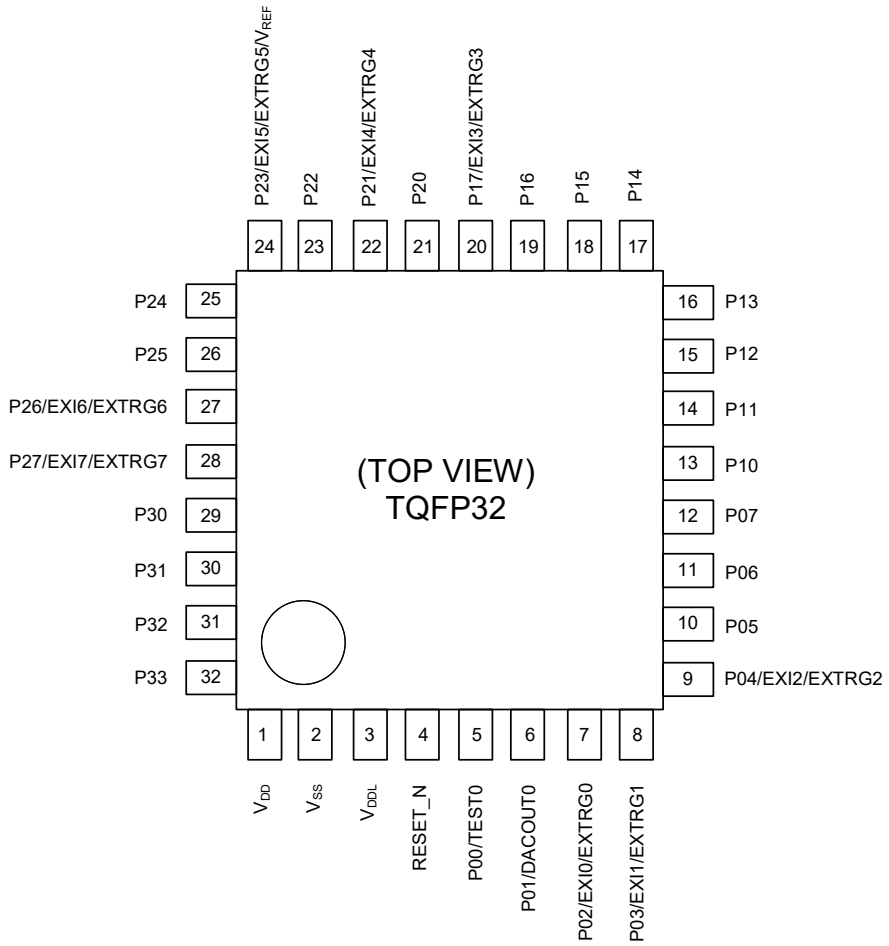


Figure 7 Pin Layout of 32pin TQFP Package

Pin Layout of ML62Q1365/1366/1367 32pin WQFN Package

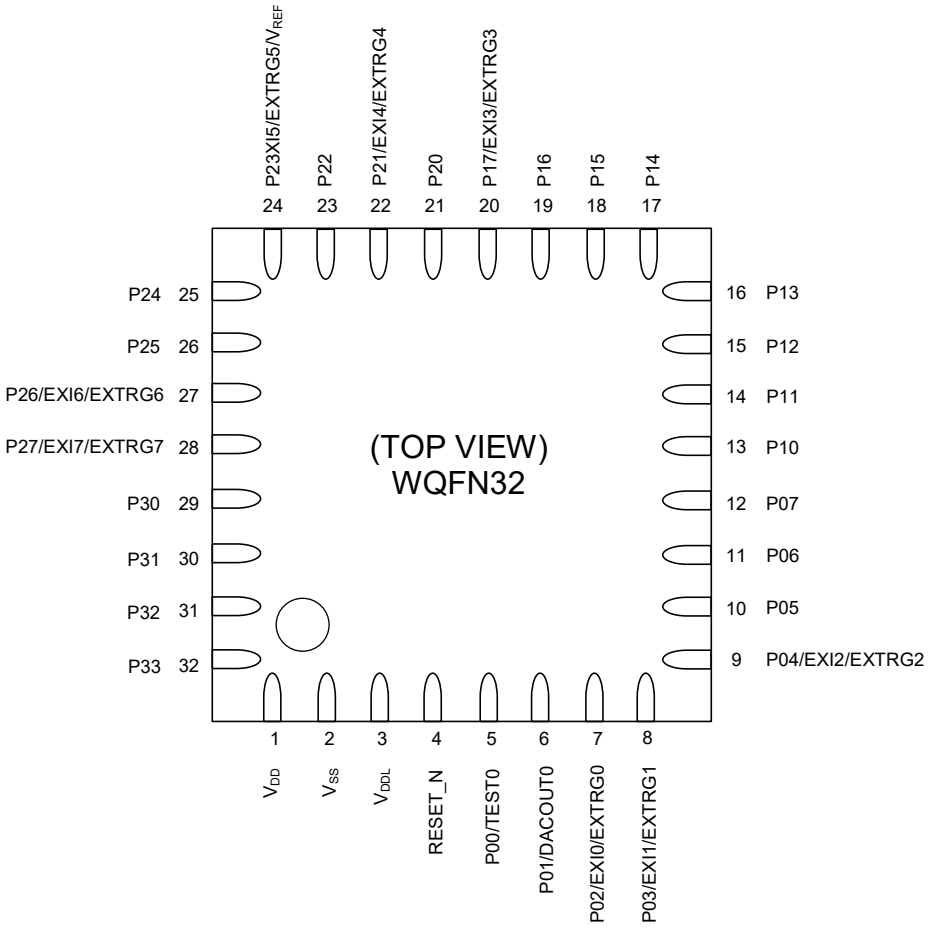


Figure 8 Pin Layout of 32pin WQFN Package

PIN LIST

Table 3 Pin List

Pin No.					Pin name (Primary function)	Primary function Others	2nd function Communications	3rd function Communications	4th function Communications	5th function Timers	6th function Others	7th function Others	8th function ADC
16Pin No.(SSOP)	16Pin No.(WQFN)	20Pin No.(TSSOP)	24Pin No.(WQFN)	32Pin No.(TQFP)(WQFN)									
1	16	18	1	1	V_{DD}	-	-	-	-	-	-	-	-
2	1	19	2	2	V_{SS}	-	-	-	-	-	-	-	-
3	2	20	3	3	V_{DDL}	-	-	-	-	-	-	-	-
4	3	1	4	4	RESET_N	-	-	-	-	-	-	-	-
5	4	2	5	5	P00	TEST0	-	-	-	-	-	-	-
-	-	-	6	6	P01	DACOUT0	-	-	-	-	-	-	-
6	5	3	7	7	P02	EXI0 EXTRG0	SU0_RXD0 SU0_SIN	-	-	FTM0P	OUTLSCLK	CMP0M	-
7	6	4	8	8	P03	EXI1 EXTRG1	SU0_TXD0 SU0_SOUT	SU0_TXD1	I2CU0_SDA	FTM0N	OUTHSCLK	CMP0P	-
8	7	5	9	9	P04	EXI2 EXTRG2	SU0_SCLK	-	I2CU0_SCL	TMH0OUT	-	-	-
-	-	6	10	10	P05	-	-	-	-	-	-	-	-
-	-	-	-	11	P06	-	-	-	I2CM0_SDA	-	-	-	-
-	-	-	-	12	P07	-	SU0_RXD1	SU0_RXD0	I2CM0_SCL	-	-	-	-
-	-	-	-	13	P10	-	SU0_TXD1	-	-	-	-	-	-
-	-	-	-	14	P11	-	SU0_SCLK	-	-	-	-	-	-
-	-	-	11	15	P12	-	SU0_RXD0 SU0_SIN	-	-	TMH4OUT	-	-	-
9	8	7	12	16	P13	-	SU0_TXD0 SU0_SOUT	SU0_TXD1	-	TMH1OUT	-	TMH3OUT	-
-	-	-	-	17	P14	-	-	-	-	-	-	-	-
-	-	-	-	18	P15	-	-	-	I2CU0_SDA	-	-	-	-
-	-	-	13	19	P16	-	SU1_SCLK	-	I2CU0_SCL	TMH5OUT	-	-	-
10	9	8	14	20	P17	EXI3 EXTRG3	SU0_RXD1	SU0_RXD0	-	FTM1P	-	BZ0P	AIN0
11	10	9	15	21	P20		SU0_TXD1	-	-	FTM1N	TBCOUT1	BZ0N	AIN1
12	11	10	16	22	P21	EXI4 EXTRG4	SU1_RXD0 SU1_SIN	-	-	FTM2P	OUTLSCLK	-	AIN2
13	12	11	17	23	P22	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	I2CM0_SDA	FTM2N	OUTHSCLK	-	AIN3
14	13	12	18	24	P23	EXI5 EXTRG5 V_{REF}	SU1_SCLK	-	I2CM0_SCL	TMH2OUT	-	-	V_{REFO}
-	-	13	19	25	P24	-	SU1_RXD0 SU1_SIN	-	-	-	-	-	AIN4
-	-	14	20	26	P25	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	-	-	-	-	AIN5
15	14	15	21	27	P26	EXI6 EXTRG6	SU1_RXD1	SU1_RXD0	I2CU0_SDA	FTM3P	-	BZ0P	AIN6
16	15	16	22	28	P27	EXI7 EXTRG7	SU1_TXD1	-	I2CU0_SCL	FTM3N	TBCOUT1	BZ0N	AIN7
-	-	-	-	29	P30	-	-	-	-	-	-	-	-
-	-	-	-	30	P31	-	-	-	-	-	-	-	-
-	-	-	23	31	P32	-	SU1_RXD1	SU1_RXD0	-	-	-	-	-
-	-	17	24	32	P33	-	SU1_TXD1	-	-	TMH3OUT	-	-	-

PIN DESCRIPTION

Table 4 Pin Description (1/4)

Function	Signal name	Pin name	I/O	Description	Logic
Power	–	V_{SS}	–	Negative power supply pin (-)	–
	–	V_{DD}	–	Positive power supply pin (+). Connect a capacitor C_V between this pin and V_{SS}.	–
	–	V_{DDL}	–	Power supply pin for internal logic (internal regulator's output). Connect a capacitor C_L (1μF) between this pin and V_{SS}.	–
Test	TEST0	P00	I/O	Input for testing, is used as on-chip debug interface and ISP function. P00 is initialized as pull-up input mode by the system reset.	–
System	V_{REFO}	P23	–	Reference voltage output	–
	RESET_N	RESET_N	I	Reset input. Applying "L" level shifts the MCU in system reset mode. Applying "H" level shifts the CPU in program running mode. Used for on-chip debug interface and ISP function. No pull-up resistor is installed.	Negative
	OUTLSCLK	P02 P21	O	Low-speed clock output.	–
	OUTHSCLK	P03 P22	O	High-speed clock output.	–
General port (GPIO)	P00	P00	I/O	General purpose I/O port - High-impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output Not available to use as I/O pin when using for on-chip debug interface or ISP function.	Positive
	P01 – P07	P01 – P07	I/O	General purpose I/O - High-impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output	Positive
	P10 – P17	P10 – P17			
	P20 – P27	P20 – P27			
	P30 – P33	P30 – P33			

Table 4 Pin Description (2/4)

Function	Signal name	Pin name	I/O	Description	Logic
UART	SU0_TXD0	P03	O	Serial communication unit0 UART0 data output	Positive
		P13			
	SU0_RXD0	P02	I	Serial communication unit0 Full-duplex data input Serial communication unit0 UART0 data input	Positive
		P07			
		P12			
		P17			
	SU0_TXD1	P03	O	Serial communication unit0 Full-duplex data output Serial communication unit0 UART1 data output	Positive
		P10			
		P13			
		P20			
	SU0_RXD1	P07	I	Serial communication unit0 UART1 data input	Positive
		P17			
	SU1_TXD0	P22	O	Serial communication unit1 UART0 data output	Positive
		P25			
	SU1_RXD0	P21	I	Serial communication unit1 Full-duplex data input Serial communication unit1 UART0 data input	Positive
		P24			
		P26			
		P32			
	SU1_TXD1	P22	O	Serial communication unit1 Full-duplex data output Serial communication unit1 UART1 data output	Positive
		P25			
		P27			
		P33			
	SU1_RXD1	P26	I	Serial communication unit1 UART1 data input	Positive
		P32			
Synchronous Serial Port	SU0_SIN	P02	I	Serial communication unit0 Synchronous serial data input	Positive
		P12			
	SU0_SCLK	P04	I/O	Serial communication unit0 Synchronous serial clock I/O	Positive
		P11			
	SU0_SOUT	P03	O	Serial communication unit0 Synchronous serial data output	Positive
		P13			
	SU1_SIN	P21	I	Serial communication unit1 Synchronous serial data input	Positive
		P24			
	SU1_SCLK	P16	I/O	Serial communication unit1 Synchronous serial clock I/O	Positive
		P23			
	SU1_SOUT	P22	O	Serial communication unit1 Synchronous serial data output	Positive
		P25			
I^2C Bus	I2CU0_SDA	P03	I/O	I^2C Unit0 (Master and Salve) Data I/O N-channel open drain Connect a pull-up resistor externally	Positive
		P15			
		P26			
	I2CU0_SCL	P04	I/O	I^2C Unit0 (Master and Salve) Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive
		P16			
		P27			
	I2CM0_SDA	P06	I/O	I^2C Master0 Data I/O pin N-channel open drain output Connect a pull-up resistor externally	Positive
		P22			
	I2CM0_SCL	P07	I/O	I^2C Master0 Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive
		P23			

Table 4 Pin Description (3/4)

Function	Signal name	Pin name	I/O	Description	Logic
Functional Timer (FTM)	FTM0P	P02	O	Functional Timer0 P output.	Positive
	FTM0N	P03	O	Functional Timer0 N output.	Negative
	FTM1P	P17	O	Functional Timer1 P output.	Positive
	FTM1N	P20	O	Functional Timer1 N output.	Negative
	FTM2P	P21	O	Functional Timer2 P output.	Positive
	FTM2N	P22	O	Functional Timer2 N output.	Negative
	FTM3P	P26	O	Functional Timer3 P output.	Positive
	FTM3N	P27	O	Functional Timer3 N output.	Negative
	EXTRG0	P02	I	Functional Timer event trigger input	—
	EXTRG1	P03	I	Functional Timer event trigger input	—
	EXTRG2	P04	I	Functional Timer event trigger input	—
	EXTRG3	P17	I	Functional Timer event trigger input	—
	EXTRG4	P21	I	Functional Timer event trigger input	—
	EXTRG5	P23	I	Functional Timer event trigger input	—
	EXTRG6	P26	I	Functional Timer event trigger input	—
	EXTRG7	P27	I	Functional Timer event trigger input	—
16bit General Timer	TMH0OUT	P04	O	16bit General Timer 0 output	Positive
	TMH1OUT	P13	O	16bit General Timer 1 output	Positive
	TMH2OUT	P23	O	16bit General Timer 2 output	Positive
	TMH3OUT	P13	O	16bit General Timer 3 output	Positive
		P33			
	TMH4OUT	P12	O	16bit General Timer 4 output	Positive
	TMH5OUT	P16	O	16bit General Timer 5 output	Positive
	EXTRG0	P02	I	16bit General Timer trigger input	—
	EXTRG1	P03	I	16bit General Timer trigger input	—
Low-Speed Time Base Counter (LTBC)	TBCOUT1	P20	O	Low-speed Time Base Counter 1Hz/2Hz output	Positive
		P27			
Buzzer	BZ0P	P17	O	Buzzer output (positive phase)	Positive
		P26			
	BZ0N	P20	O	Buzzer output (negative phase)	Negative
		P27			

Table 4 Pin Description (4/4)

Function	Signal name	Pin name	I/O	Description	Logic
External Interrupt	EXI0	P02	I	External interrupt 0 input	—
	EXI1	P03	I	External interrupt 1 input	—
	EXI2	P04	I	External interrupt 2 input	—
	EXI3	P17	I	External interrupt 3 input	—
	EXI4	P21	I	External interrupt 4 input	—
	EXI5	P23	I	External interrupt 5 input	—
	EXI6	P26	I	External interrupt 6 input	—
	EXI7	P27	I	External interrupt 7 input	—
Successive approximation type A/D converter	V_{REF}	P23	—	SA-ADC external reference voltage input	—
	AIN0	P17	I	SA-ADC channel 0 input	—
	AIN1	P20	I	SA-ADC channel 1 input	—
	AIN2	P21	I	SA-ADC channel 2 input	—
	AIN3	P22	I	SA-ADC channel 3 input	—
	AIN4	P24	I	SA-ADC channel 4 input	—
	AIN5	P25	I	SA-ADC channel 5 input	—
	AIN6	P26	I	SA-ADC channel 6 input	—
	AIN7	P27	I	SA-ADC channel 7 input	—
Analog comparator	CMP0P	P03	I	Comparator input 0 (noninverting input)	—
	CMP0M	P02	I	Comparator input 0 (inverting input)	—
D/A converter	DACOUT0	P01	O	D/A converter0 output	—

TERMINATION OF UNUSED PINS

Table 5 Termination of unused pins

Pin	pin termination
RESET_N	Connect to V_{DD}
P00/TEST0	Connect to V_{DD} with initial state (pulled-up input mode)
P01 to P07	Open with initial state(Hi-impedance)
P10 to P17	
P20 to P27	
P30 to P33	

Note:
- Terminate unused input pins according to the table 5 in order to avoid unexpected through-current in the pins.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta = +25°C		-0.3 to +2.0	V
Input voltage	V_{IN}	Ta = +25°C		-0.3 to V_{DD}+0.3*1	V
Output voltage	V_{OUT}	Ta = +25°C		-0.3 to V_{DD}+0.3*1	V
"H" level output current	I_{OUTH}	Ta = +25°C	1pin	-40*2	mA
			Total	-150*2	
"L" level output current	I_{OUTL}	Ta = +25°C	1pin	+40	mA
			Total	+150	
Power dissipation	PD	Ta = +25°C		1	W
Storage temperature	T_{STG}	—		-55 to +150	°C

*1 6.5V or lower
*2 The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

[Note]
Stresses above the absolute maximum ratings listed in the above table may cause permanent damage to the device.
These are stress ratings only and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature(Ambient)	Ta	—	-40 to +105	°C
Operating temperature(Chip-Junction)	Tj	—	-40 to +105	°C
Operating voltage	V_{DD}	—	1.6 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.6 to 5.5V	30k to 4M	Hz
		V_{DD} = 1.8 to 5.5V	30k to 25M	
V_{DDL} pin external capacitance	C_L	—	1.0 ±30%	µF

Thermal characteristics

The maximum chip-junction temperature, T_j max, may be calculated using the following equation.

$T_j \max = T_a \max + P_D \max \times \theta_{ja}$
T_a max: $maximum\ ambient\ temperature$
$P_D\ max$: LSI maximum power dissipation
θ_{ja}: $Package\ junction\ to\ ambient$ thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows the each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

Parameter	Symbol	Package type	Value		Unit
			L1	L2	
Thermal resistance	θ_{ja}	SSOP16	90.5	84.3	°C/W
		WQFN16	80.8	74.7	
		TSSOP20	58.2	50.8	
		WQFN24	59.0	51.0	
		WQFN32	50.6	43.5	
		TQFP32	67.6	61.8	

PCB conditions:

PCB name	L1	L2	Unit
PCB size（L / W / T）	114.3 / 76.2 / 1.6	114.3 / 76.2 / 1.6	mm
Number of layer	1	2	layer
Wiring density	60% (top layer)	60%(top and bottom layer)	—
Wind condition	No wind (0m/s)		—

WQFN package's thermal resistance is simulated on the condition that the exposed pad is soldered on the PCB.

Current Consumption 1

Product: ML62Q1323, ML62Q1324, ML62Q1325, ML62Q1333, ML62Q1334, ML62Q1335

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ. *3	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.60	17	μA	1
			Ta = -40 to +105 °C	—		36		
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.75	20	μA	
			Ta = -40 to +105 °C	—		42		
Supply current 2	IDD2	Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating *1). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	3.6	27	μA	
			Ta = -40 to +105 °C	—		44		
Supply current 3	IDD3	CPU: Running with 32kHz RC oscillation clock*1*2 PLL oscillation is stopped.	Ta = -40 to +105 °C	—	17	66	μA	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock*1*2 PLL 16MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	3.1	3.8	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock*1*2 PLL 24MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	4.4	5.3		

*1 LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all “1”

*2 CPU running in wait mode

*3 On the condition of V_{DD}=3.0V, Ta=+25 °C

Current Consumption 2

Product: ML62Q1345, ML62Q1346, ML62Q1347, ML62Q1365, ML62Q1366, ML62Q1367

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ. *3	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.80	18	μA	1
			Ta = -40 to +105 °C	—		40		
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.95	21	μA	
			Ta = -40 to +105 °C	—		45		
Supply current 2	IDD2	Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating *1). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	4.3	33	μA	
			Ta = -40 to +105 °C	—		50		
Supply current 3	IDD3	CPU: Running with 32kHz RC oscillation clock*1*2 PLL oscillation is stopped.	Ta = -40 to +105 °C	—	20	70	μA	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock*1*2 PLL 16MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	4.3	4.8	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock*1*2 PLL 24MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	6.4	7.0		

*1 LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all “1”

*2 CPU running in wait mode

*3 On the condition of V_{DD}=3.0V, Ta=+25°C

On-chip Oscillator

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed RC oscillator frequency accuracy 1 Without software adjustment	f_{RCL1}	Ta= +25°C V_{DD} = 1.8 to 5.5V	Typ -1.0%	32.768	Typ +1.0%	kHz	1
		Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ -2.5%	32.768	Typ +2.5%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ -3.0%	32.768	Typ +3.0%		
		V_{DD} = 1.6 to 1.8V	Typ -3.5%	32.768	Typ -3.5%		
Low-speed RC oscillator frequency accuracy 2 With software adjustment	f_{RCL2}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ -1.0%	32.768	Typ +1.0%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ -1.5%	32.768	Typ +1.5%		
PLL oscillation frequency accuracy 1 Without software adjustment	f_{PLL1}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ -2.5%	16/24	Typ +2.5%	MHz	
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ -3.0%	16/24	Typ +3.0%		
		V_{DD} = 1.6 to 1.8V	Typ -3.5%	16/24	Typ +3.5%		
PLL oscillation frequency accuracy 2 With software adjustment	f_{PLL2}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ -1.0%	16/24	Typ +1.0%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ -1.5%	16/24	Typ +1.5%		
PLL oscillation start time	T_{PLL}	V_{DD} = 1.6 to 5.5V	—	—	2	ms	
1kHz Low-speed RC oscillator (for WDT) frequency accuracy	f_{RC1K}	Ta= -40 to +105°C V_{DD} = 1.6 to 5.5V	0.5	1	2.5	kHz	

Input / Output pin 1

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage1 “H”/”L” level (P00-P07) (P10-P17) (P20-P27) (P30-P33)	VOH1	IOH1=-10mA V_{DD}≥4.5V		V_{DD} -1.5	—	—	V	2
		IOH1=-1mA V_{DD}≥1.6V		V_{DD} -0.5	—	—		
	VOL1	IOL1=+10mA V_{DD}≥4.5V		—	—	1.5		
		IOL1=+1mA V_{DD}≥1.6V		—	—	0.5		
Output voltage2 “L” level (P01-P07) (P10-P17) (P20-P27) (P30-P33)	VOL2	When Nch open drain output mode is selected	IOL2=+15mA V_{DD}≥4.5V	—	—	0.7		
			IOL2=+8mA V_{DD}≥3.0V	—	—	0.5		
			IOL2=+3mA V_{DD}≥2.0V	—	—	0.4		
			IOL2=+2mA V_{DD}≥1.6V	—	—	0.4		

Input / Output pin 2

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	V_{DD}≥4.5V	-10*3*5	—	—	mA	3
			V_{DD}≥1.6V	-1*3*5	—	—		
"H" level output current *1*4	IOH3	Total of 'P00-P07 andP10-P13 or Total of 'P14-P17, P20-P27 and P30-P33 (Duty≤50%)	V_{DD}≥4.5V	-50*5	—	—		
			V_{DD}≥1.6V	-20*5	—	—		
		All pin total (Duty≤50%)	V_{DD}≥4.5V	-100*5	—	—		
			V_{DD}≥1.6V	-40*5	—	—		
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	V_{DD}≥4.5V	—	—	10*3		
			V_{DD}≥1.6V	—	—	1*3		
"L" level output current2 *6	IOL2	1pin (Nch open drain output mode)	V_{DD}≥4.5V	—	—	15*3		
			V_{DD}≥3.0V	—	—	8*3		
			V_{DD}≥2.0V	—	—	3*3		
			V_{DD}≥1.6V	—	—	2*3		
"L" level output total current *2*4	IOL3	Total of P00-P07 and P10-P13 or Total of P14-P17, P20-P27 and P30-P33 (Nch open drain output mode, duty≤50%)	V_{DD}≥4.5V	—	—	60		
			V_{DD}≥3.0V	—	—	40		
			V_{DD}≥2.0V	—	—	15		
			V_{DD}≥1.6V	—	—	10		
		All pin total (Nch open drain output mode, duty≤50%)	V_{DD}≥4.5V	—	—	120		
			V_{DD}≥1.6V	—	—	20		
Output leak (P00-P07) (P10-P17) (P20-P27) (P30-P33)	IOOH	VOH=V_{DD} (High impedance mode)		—	—	+1	μA	
	IOOL	VOL=V_{SS} (High impedance mode)		-1*5	—	—		

*1 Sink-out current from V_{DD} to the output pin, which can guarantee the device operation.
*2 Sink-in current from the output pin to V_{SS}, which can guarantee the device operation.
*3 Do not exceed total current.
*4 The total current is on the condition of Duty≤50%(same applies to IOH1).
When the duty>50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
<For an example> When IOL3=100mA and n=80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
*5 The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*6 These values are satisfied with VOH1, VOL1 and VOL2.

Input / Output pin 3

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input current1 (RESET_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-1*1	—	—		
Input current2 (P00/TEST0)	IIL2	VIL2=V_{SS} (pull-up mode) *2	-1500*1	-300*1	-20*1		
	V/IIL2	VIL2=V_{SS} (pull-up mode) *2	3.7	10	80	kΩ	
	IIH2Z	VIH2=V_{DD} (High impedance mode)	—	—	1	μA	
	IIL2Z	VIL2=V_{SS} (High impedance mode)	-1*1	—	—		
Input current3 (P01-P07) (P10-P17) (P20-P27) (P30-P33)	IIL3	VIL1=V_{SS}(pull-up mode) *2	-250*1	-30*1	-2*1		
	V/IIL3	VIL1=V_{SS} (pull-up mode) *2	22	100	800	kΩ	
	IIH3Z	VIH1=V_{DD} (High impedance mode)	—	—	1	μA	
	IIL3Z	VIL1=V_{SS} (High impedance mode)	-1*1	—	—		
Input voltage1 (RESET_N) (P01-P07) (P10-P17) (P20-P27) (P30-P33)	VIH1	—	0.7 x V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3 x V_{DD}		
Input voltage2 (P00/TEST0)	VIH2	—	0.7 x V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.25 x V_{DD}		
Pin capacitance (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33)	CPIN	f = 10kHz Ta = +25°C	—	—	10	pF	—

*1 The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*2 Measurement conditions: Typ. : V_{DD} = 3.0V, Max. : V_{DD} = 1.6V, Min. : V_{DD} = 5.5V

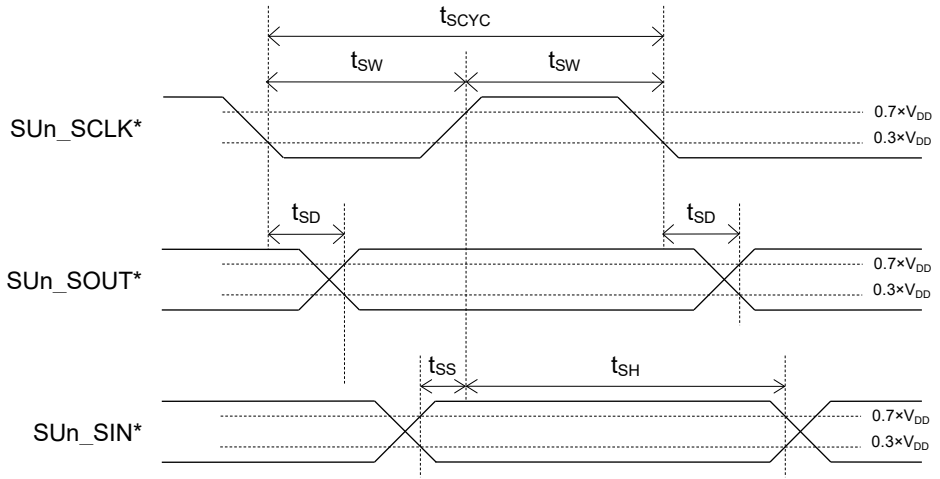
Synchronous Serial Port

Slave mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle	t_{SCYC}	—	1 *2	—	—	µs
SCK input pulse width	t_{SW}	—	0.5 *3	—	—	µs
SOUT output delay time	t_{SD}	V_{DD}=2.4 to 5.5V	—	—	100+ HSCLK*1×3	ns
		V_{DD}=1.8 to 5.5V	—	—	200+ HSCLK*1×3	ns
SIN input setup time	t_{SS}	—	HSCLK*1 x1	—	—	ns
SIN input hold time	t_{SH}	—	80+ HSCLK*1×3	—	—	ns

*1 Cycle of high speed clock
*2 Need input cycles of HSLCK x8 or longer
*3 Need input cycles of HSLCK x4 or longer



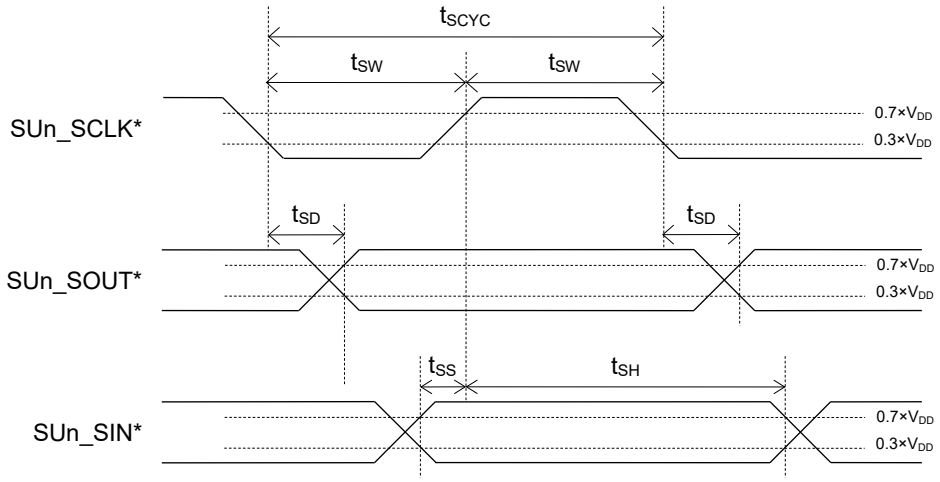
* 2nd to 8th function of port, n=0~1

Master mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK output cycle	t_{SCYC}	—	—	SCLK*[1]	—	ns
SCK output pulse width	t_{SW}	—	SCLK*[1] ×0.4	SCLK*[1] ×0.5	SCLK*[1] ×0.6	ns
SOUT output delay time	t_{SD}	V_{DD}=2.4 to 5.5V	—	—	100	ns
		V_{DD}=1.8 to 5.5V	—	—	160	ns
SIN input setup time	t_{SS}	V_{DD}=2.4 to 5.5V	120	—	—	ns
		V_{DD}=1.8 to 5.5V	180	—	—	ns
SIN input hold time	t_{SH}	V_{DD}=2.4 to 5.5V	80	—	—	ns
		V_{DD}=1.8 to 5.5V	100	—	—	ns

*[1] Clock cycle selected by bit12~8(SnCK4~0) of the serial port n mode register (SIOnMOD)
V_{DD}≥2.4V: min250ns , V_{DD}≥1.8V: min500ns



* 2nd to 8th function of port, n=0~1

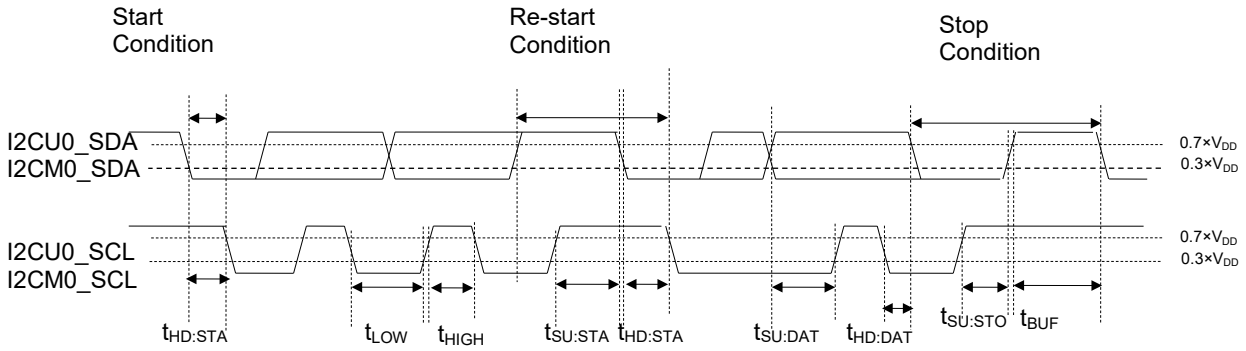
I²C Bus Interface

Standard Mode (100k bit/s)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

When using the I²C as the master, configure the I²C master n mode register (I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

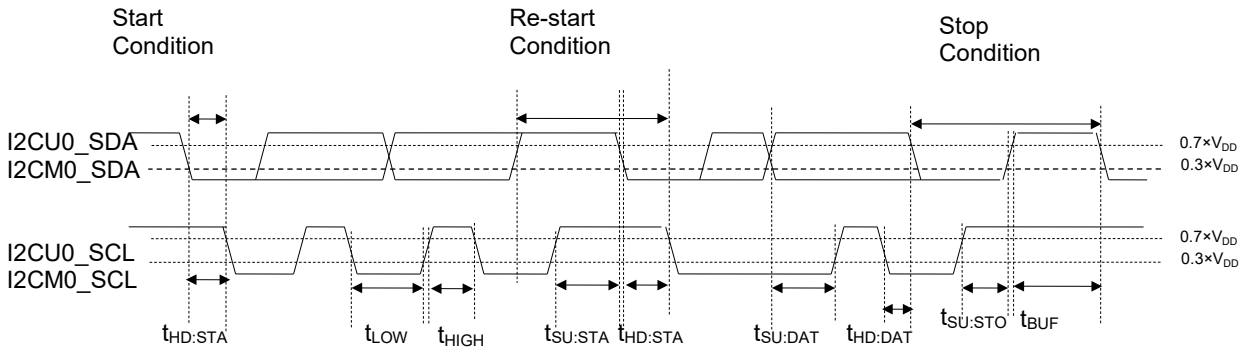


Fast Mode (400k bit/s)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL ”L” level time	t_{LOW}	—	1.3	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

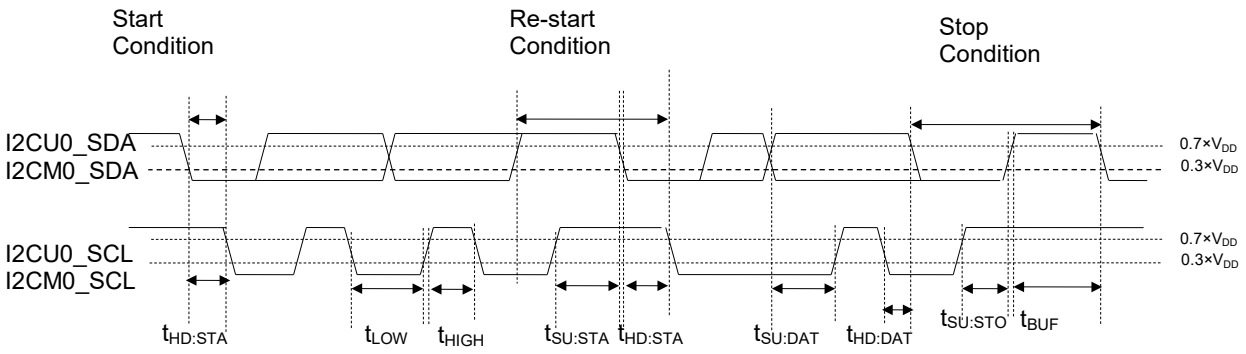


1Mbps Mode (1M bit/s)

(V_{DD}=2.7 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	1000	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.26	—	—	µs
SCL ”L” level time	t_{LOW}	—	0.5	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.26	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.26	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.26	—	—	µs
Bus-free time	t_{BUF}	—	0.5	—	—	µs

When using the I^2C as the master, configure the I^2C master n mode register(I2MnMOD) and I^2C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

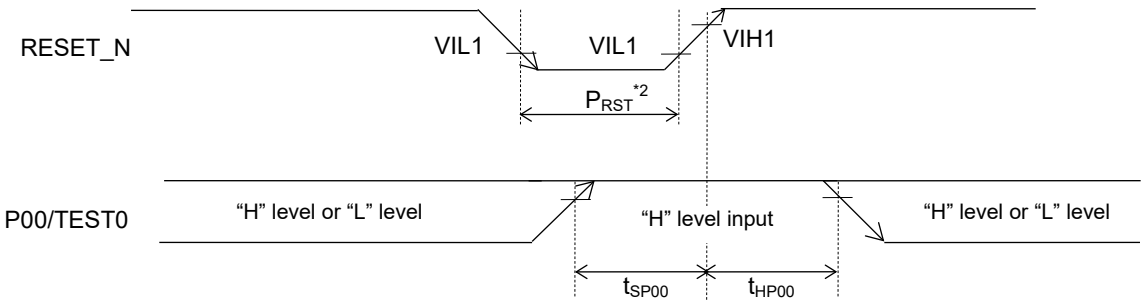


Reset

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Reset pulse width	P_{RST}	—	2	—	—	ms	1
P00 "H" level setup time	t_{SP00}	—	1	—	—	ms	
P00 "H" level hold time *1	t_{HP00}	—	1	—	—	ms	

*1: except ISP mode. Refer to the User's manual "25.4 In-System Programing Function" for the timing in ISP mode.



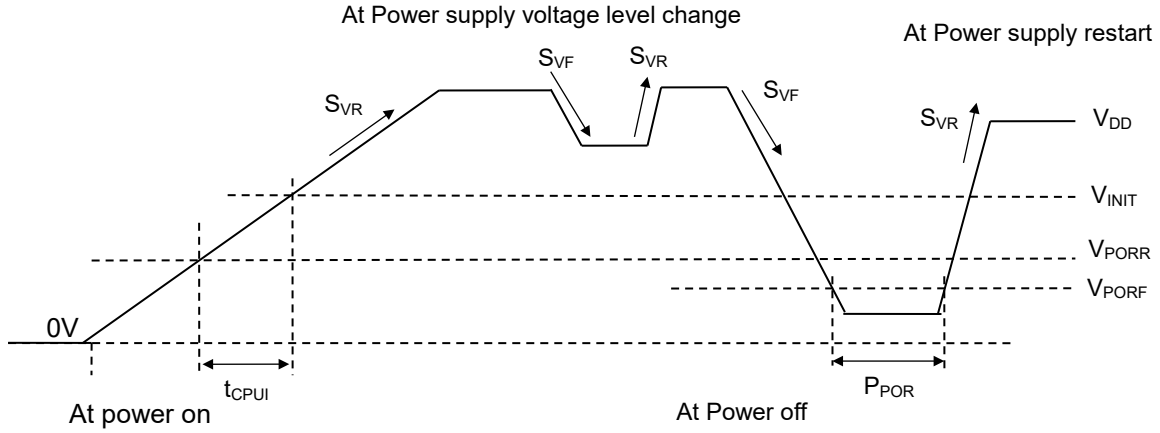
*2: VDD=1.6V or over at power on

Note:
- RESET_N input shorter pulse than the Reset pulse width (P_{RST}) valid time should be avoided. The shorter pulse input may cause unexpected behavior.

Slope of Power supply and Power On Reset

(VSS =0V, –40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Power on rising slope	S_{VR}	—	—	—	60	V/ms	1
Power on falling slope	S_{VF}	—	—	—	2	V/ms	
Power on reset detection voltage	V_{PORR}	At Power up (rising)	1.47	1.57	1.80	V	
	V_{PORF}	At Power down (falling)	1.33	1.49	1.58	V	
Power on reset minimum pulse width	P_{POR}	—	200	—	—	µs	
Power on voltage	V_{INIT}	At power on	1.8	—	—	V	
CPU operation start time (from the release of reset to the CPU starts to run)	t_{CPUI}	—	11	16	—	ms	—



Note:
- If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD}, it may cause the MCU malfunction.
  Apply prevent measurement such as bypass capacitors or external reset input, and so on.
- Start the high-speed clock when the V_{DD} is within the operating voltage.

VLS

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition VLS0LV *1		Min.	Typ.	Max.	Unit	Measuring circuit
VLS threshold voltage *2	V_{VLSR}	00H	Rising	3.86	4.06	4.26	V	1
	V_{VLSF}		Falling	3.84	4.00	4.16		
	V_{VLSR}	01H	Rising	3.57	3.76	3.95		
	V_{VLSF}		Falling	3.55	3.70	3.85		
	V_{VLSR}	02H	Rising	2.94	3.11	3.28		
	V_{VLSF}		Falling	2.92	3.05	3.18		
	V_{VLSR}	03H	Rising	2.85	3.01	3.17		
	V_{VLSF}		Falling	2.83	2.95	3.07		
	V_{VLSR}	04H	Rising	2.75	2.91	3.07		
	V_{VLSF}		Falling	2.73	2.85	2.97		
	V_{VLSR}	05H	Rising	2.66	2.81	2.96		
	V_{VLSF}		Falling	2.64	2.75	2.86		
	V_{VLSR}	06H	Rising	2.56	2.71	2.86		
	V_{VLSF}		Falling	2.54	2.65	2.76		
	V_{VLSR}	07H	Rising	2.46	2.61	2.76		
	V_{VLSF}		Falling	2.44	2.55	2.66		
	V_{VLSR}	08H	Rising	2.37	2.51	2.65		
	V_{VLSF}		Falling	2.35	2.45	2.55		
	V_{VLSR}	09H	Rising	1.98	2.11	2.24		
	V_{VLSF}		Falling	1.96	2.05	2.14		
	V_{VLSR}	0AH	Rising	1.89	2.01	2.13		
	V_{VLSF}		Falling	1.87	1.95	2.03		
	V_{VLSR}	0BH	Rising	1.79	1.91	2.03		
	V_{VLSF}		Falling	1.77	1.85	1.93		
VLS Current	I_{VLS}	—		—	50	—	nA	

*1 Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).

*2 The Data VLS0LV = 0CH~0FH is not available to use, if the data is specified it will the same spec as that 0BH is specified.

Analog Comparator

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Comparator same phase input voltage range	V_{CMR}	—	0.1	—	V_{DD} -1.5	V	1
Comparator0 input offset	V_{CMOF}	Ta=+25°C, V_{DD}=5.0V	—	5	—	mV	
Comparator Reference Voltage	V_{CMREF}	—	0.75	0.8	0.85	V	

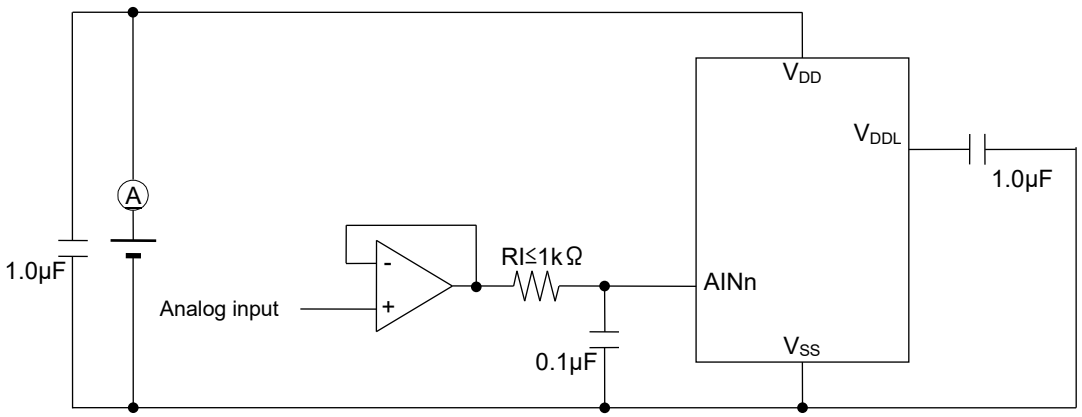
Successive Approximation Type A/D Converter

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n_{AD}	—	—	—	10	bit
Overall error	—	4.5V≤Reference voltage*1≤5.5V	-3.5	1.2	3.5	LSB
Integral non-linearity error	INL_{AD}	2.7V≤ Reference voltage*1≤5.5V	-4	—	4	
		2.2V≤ Reference voltage*1＜2.7V	-6	—	6	
		1.8V≤ Reference voltage*1＜2.2V	-10	—	10	
		Reference voltage =Internal reference voltage	-15	—	15	
Differential non-linearity error	DNL_{AD}	2.7V≤ Reference voltage*1≤5.5V	-3	—	3	
		2.2V≤ Reference voltage*1＜2.7V	-5	—	5	
		1.8V≤ Reference voltage*1＜2.2V	-9	—	9	
		Reference voltage =Internal reference voltage	-14	—	14	
Zero-scale error	ZSE	RI≤1kΩ	-6	—	6	
Full-scale error	FSE	RI≤1kΩ	-6	—	6	
A/D reference voltage	V_{REF}	—	1.8	—	V_{DD}	V
Internal reference voltage	V_{REFI}	—	1.5	1.55	1.6	
Conversion time	t_{CONV}	4.5V≤V_{DD}≤5.5V	2.25	—	427	μs
		2.2V≤V_{DD}≤5.5V	4.5	—	427	
		1.8V≤V_{DD}≤5.5V	18	—	427	

*1 : V_{DD} or P23/V_{REF} is selected for the reference voltage of Successive Approximation Type A/D Converter by setting bit5(VREFP1) and bit4(VREFP0) of SA-ADC TEMP/VREF control register(VREFCON).

The current flows during the ADC sampling as it takes charging. Make the output impedance of the anlog signal source 1kΩ or smaller. Also, putting 0.1uF capacitor on the ADC input pin is recommended to reduce the noise.



D/A Converter

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n_{DA}	—	—	—	8	bit
Conversion cycle	tc	—	10	—	—	µs
Integral non-linearity error	INL_{DA}	RL=4MΩ	-2	—	2	LSB
Differential non-linearity error	DNL_{DA}	RL=4MΩ	-1	—	1	
Output impedance	Ro	DACEN bit of D/A converter enable register =1	3	6	9	kΩ

Reference Voltage Output

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REFO}	—	—	1.55	—	V
Output impedance	R_{VREFO}	—	—	—	500	kΩ

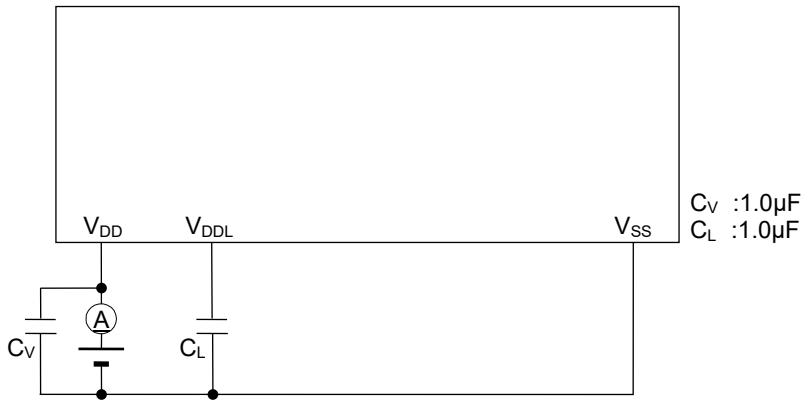
Flash Memory

(V_{SS}= 0V)

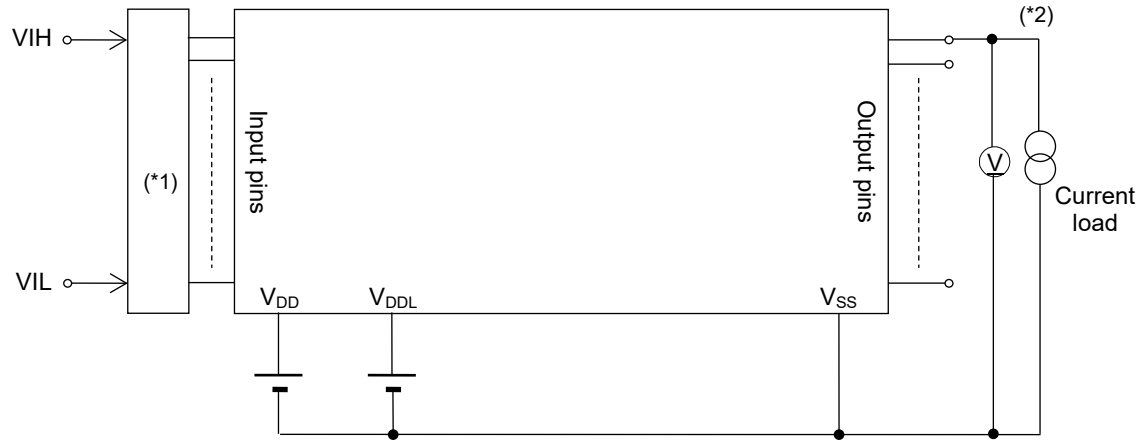
Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		+1.8 to +5.5	V
Maximum rewrite count	CEPD	Data Flash (4Kbyte)		10000	times
	CEPP	Program Flash		100	
Erase unit	—	Block erase	Program Flash	16K	B
			Data Flash	All area	
	—	Sector erase	Program Flash	1K	B
			Data Flash	128	
Erase time (Max.)	—	Block erase / Sector erase		50	ms
Write unit	—	Program Flash		4	B
		Data Flash		1	
Write time (Max.)	—	Program Flash		80	µs
	—	Data Flash		40	
Data retention period	YDR	—		15	years

Measuring circuit

Measuring circuit 1

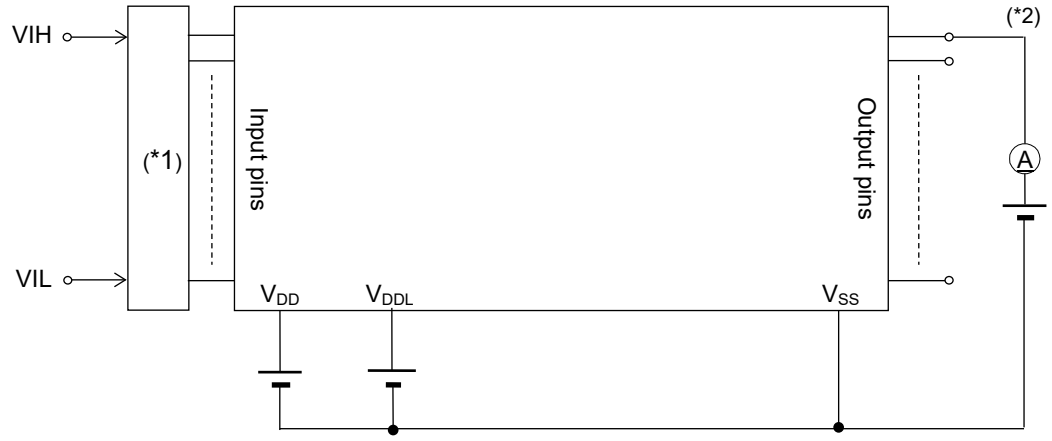


Measuring circuit 2



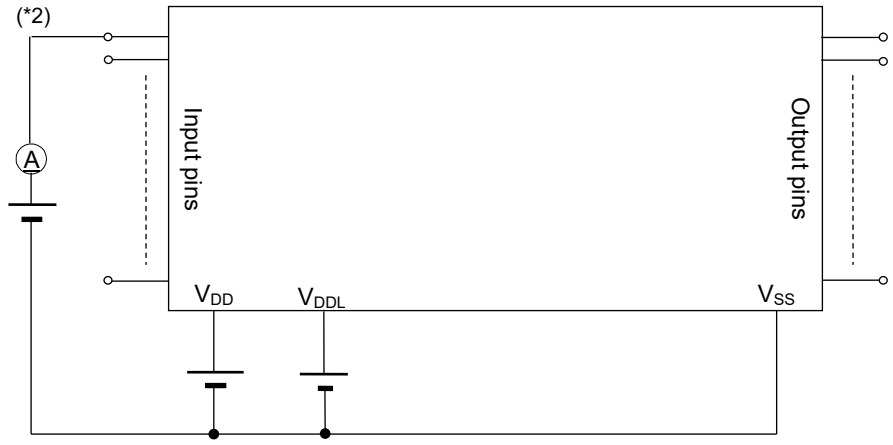
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 3



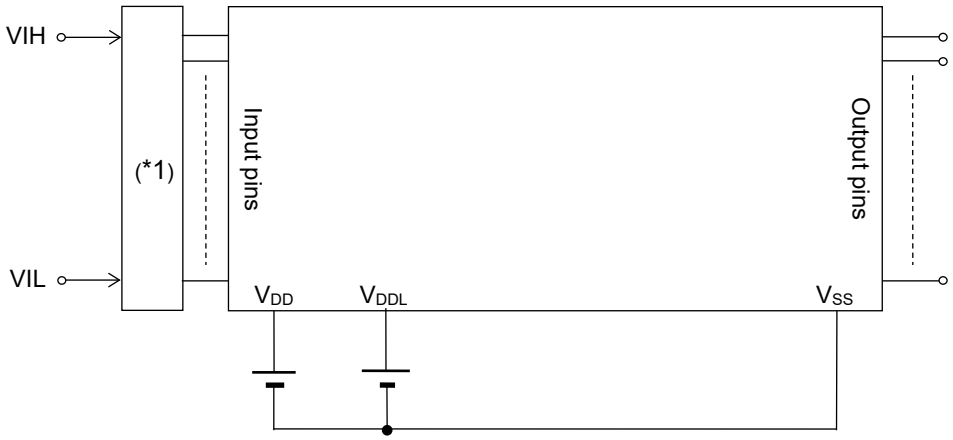
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 4



(*2) Measured connecting specified pins

Measuring circuit 5

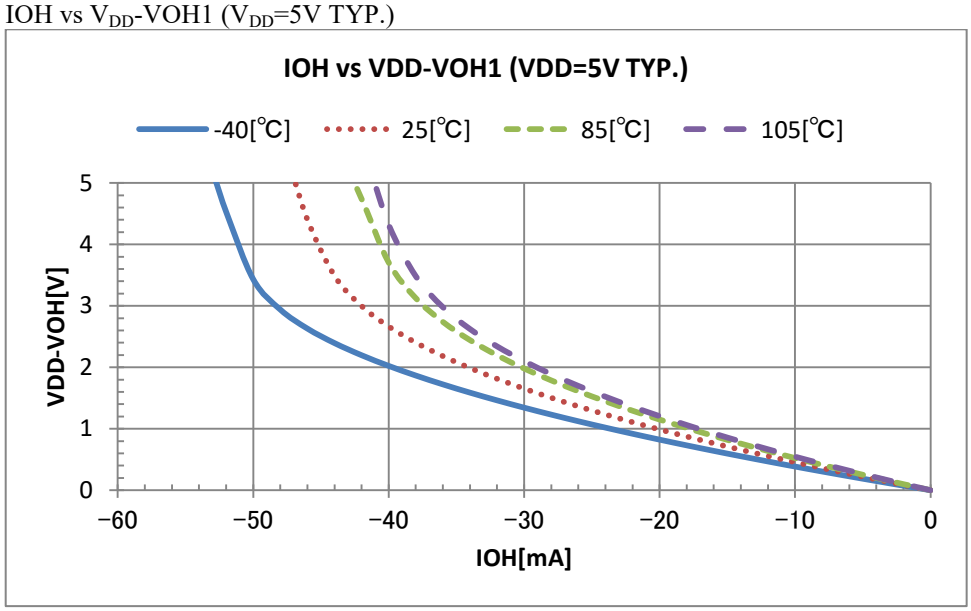


(*1) Input logic circuit to determine the specified measuring conditions

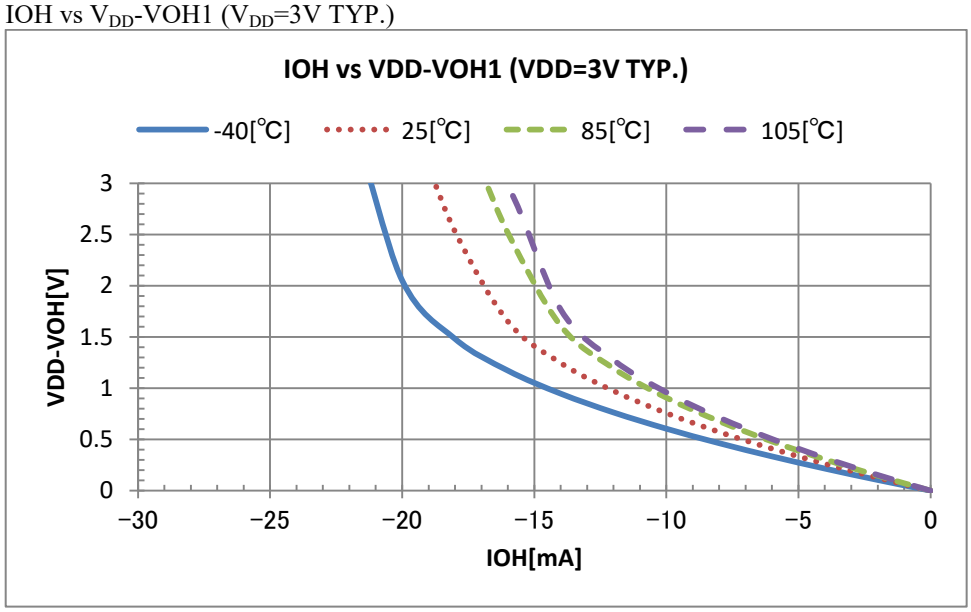
Characteristics graphs

These Graphs on the following pages are references for designing an application.

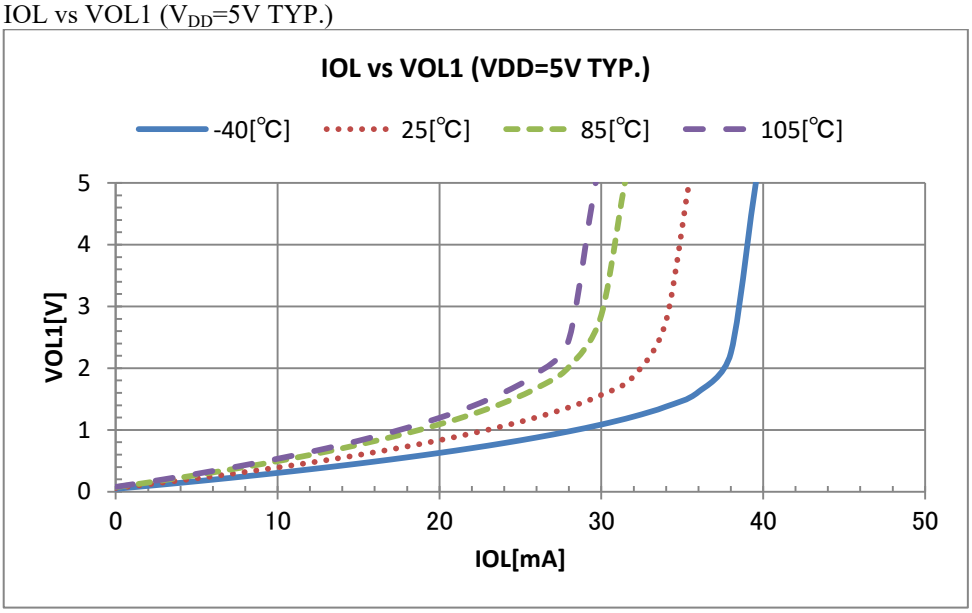
IOH vs V_{DD}-VOH1 (V_{DD}=5V TYP.)



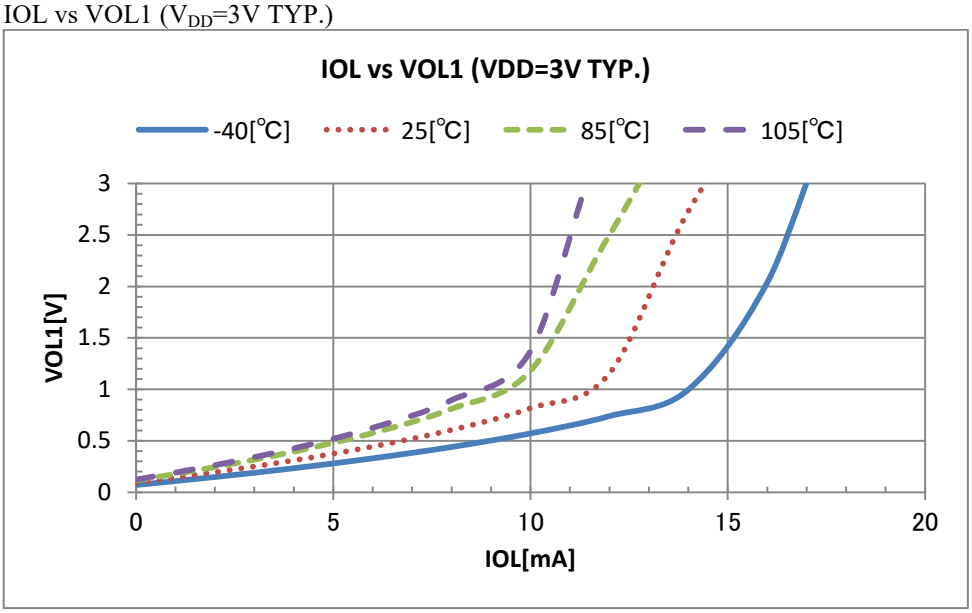
IOH vs V_{DD}-VOH1 (V_{DD}=3V TYP.)



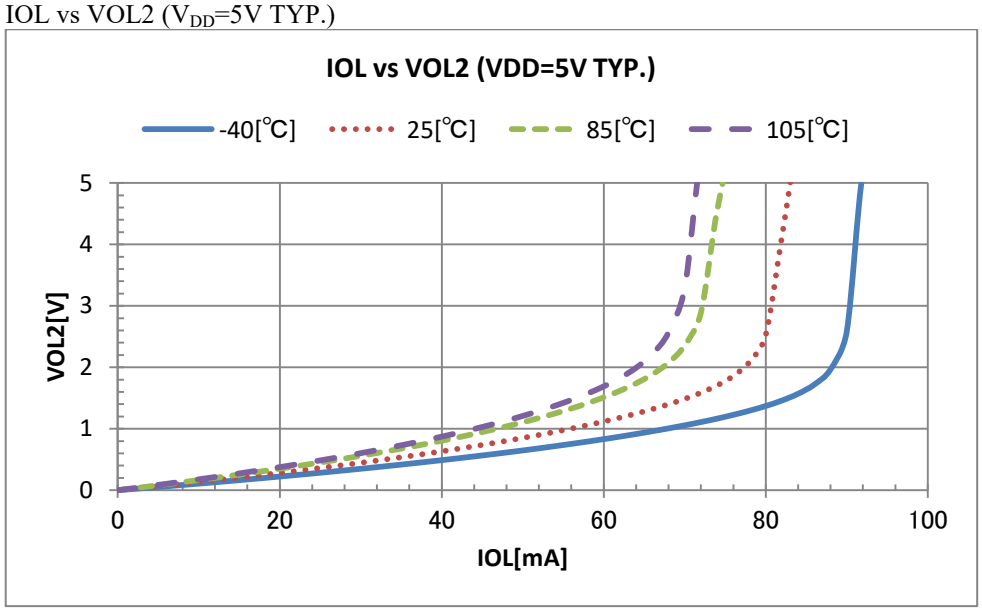
IOL vs VOL1 (V_{DD}=5V TYP.)



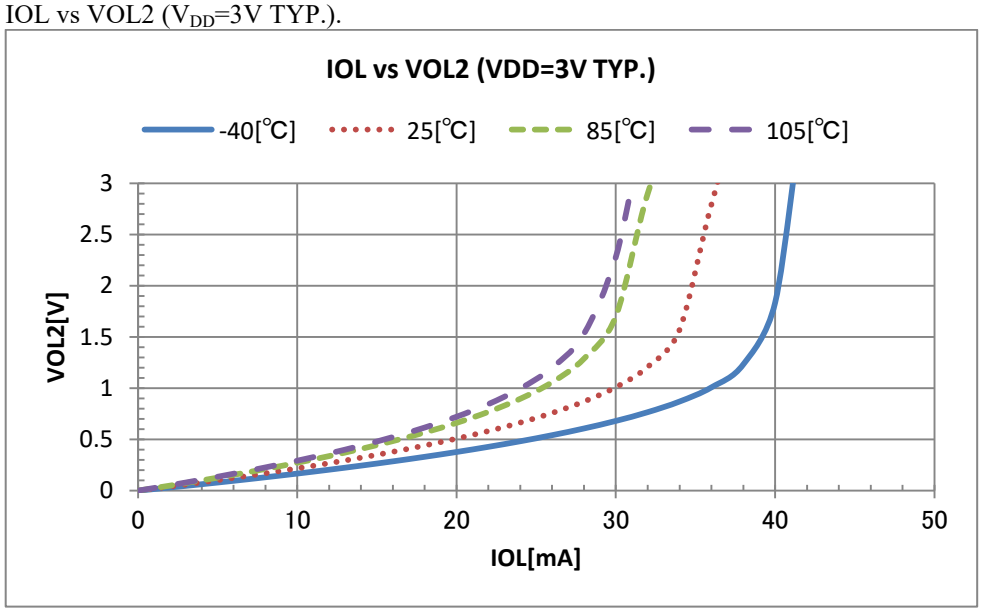
IOL vs VOL1 (V_{DD}=3V TYP.)



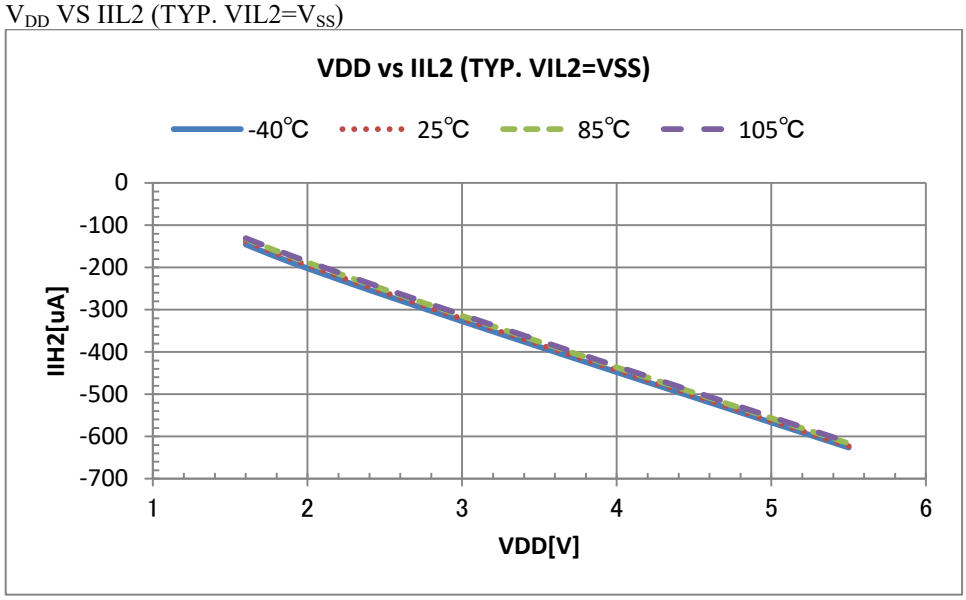
IOL vs VOL2 (V_{DD}=5V TYP.)



IOL vs VOL2 (V_{DD}=3V TYP.).

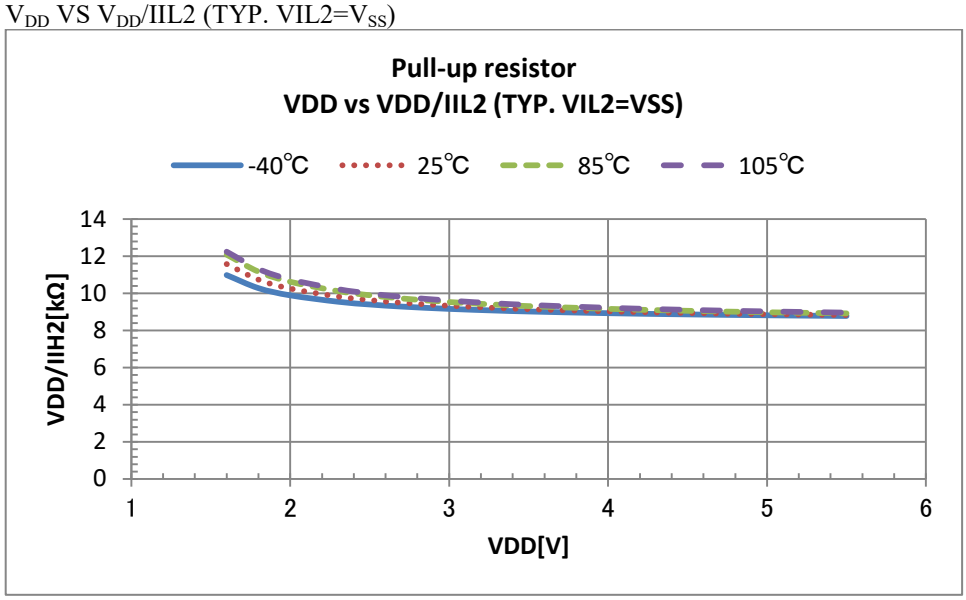


V_{DD} VS IIL2 (TYP. VIL2=V_{SS})

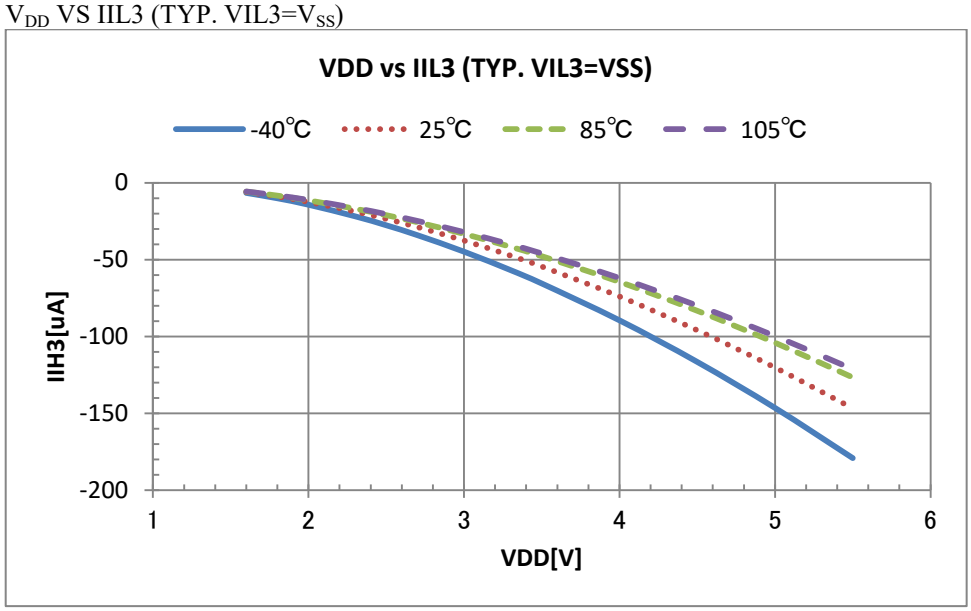


Pull-up resistor

V_{DD} VS V_{DD}/IIL2 (TYP. VIL2=V_{SS})

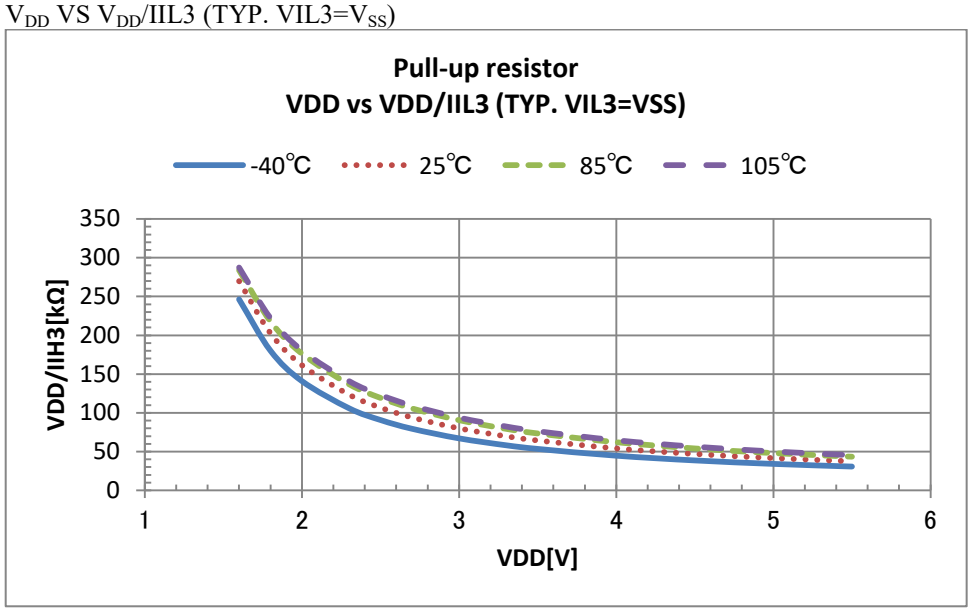


V_{DD} VS IIL3 (TYP. VIL3=V_{SS})

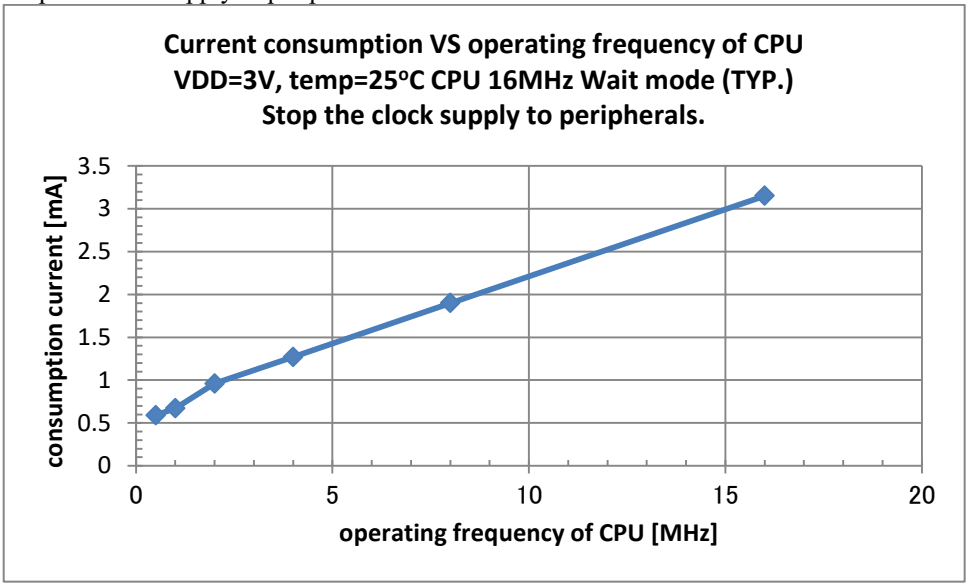


Pull-up resistor

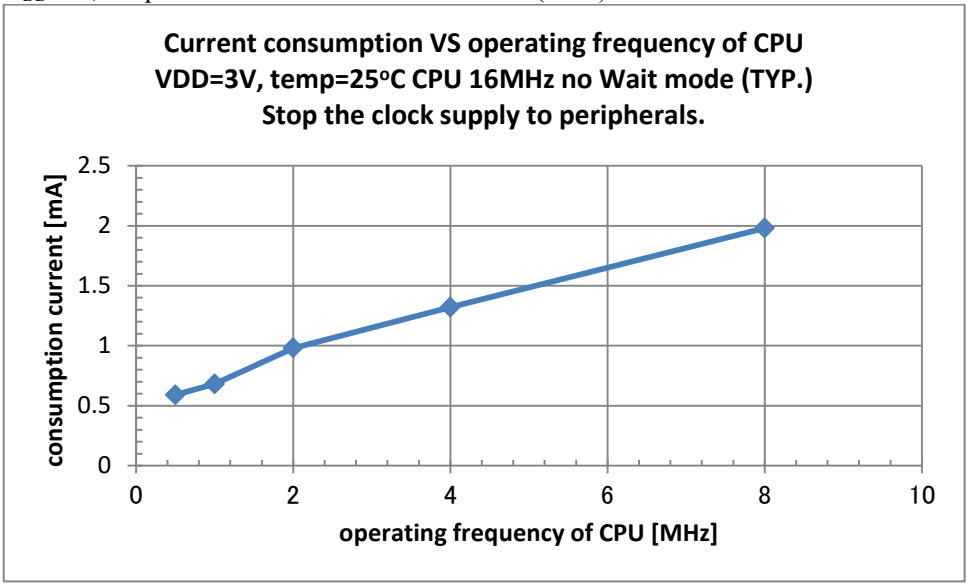
V_{DD} VS V_{DD}/IIL3 (TYP. VIL3=V_{SS})



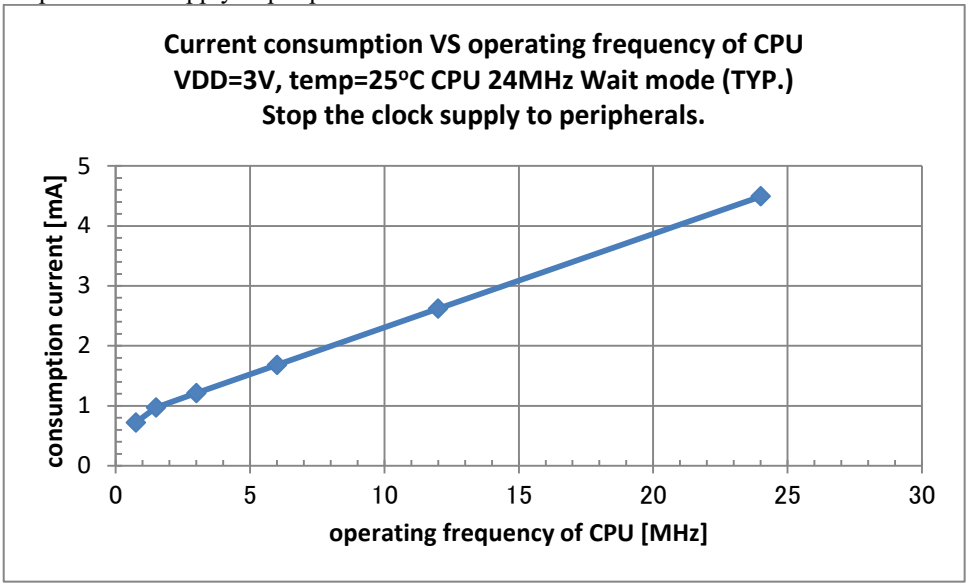
Current consumption VS operating frequency of CPU
V_{DD}=3V, temp=25℃ CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



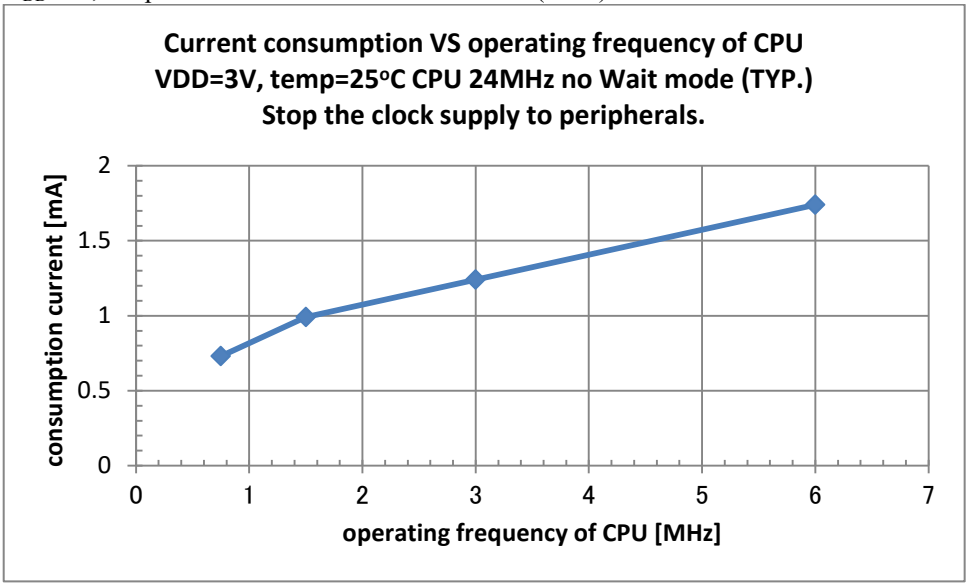
V_{DD}=3V, temp=25℃ CPU 16MHz no Wait mode (TYP.)



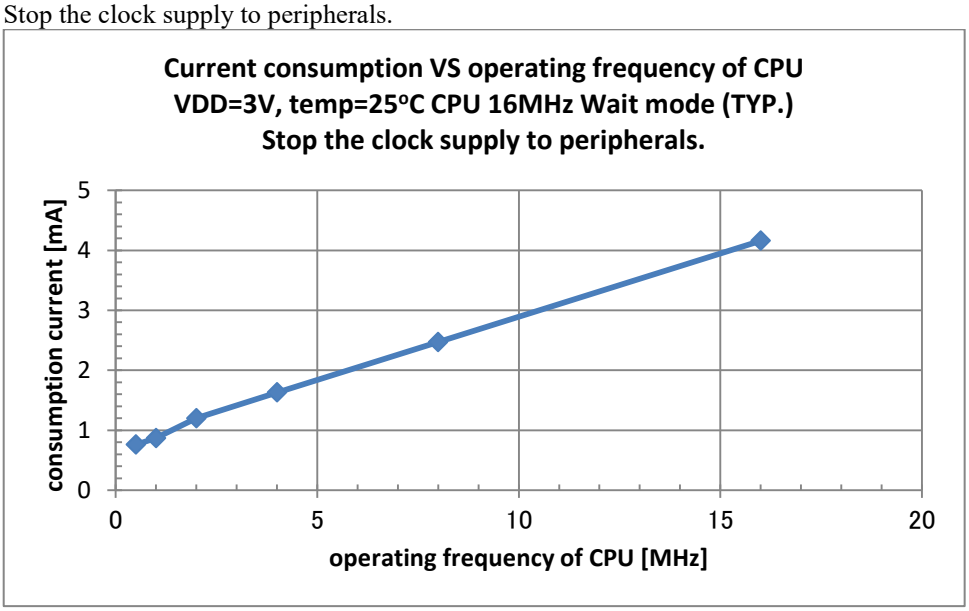
Current consumption VS operating frequency of CPU
V_{DD}=3V, temp=25℃ CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



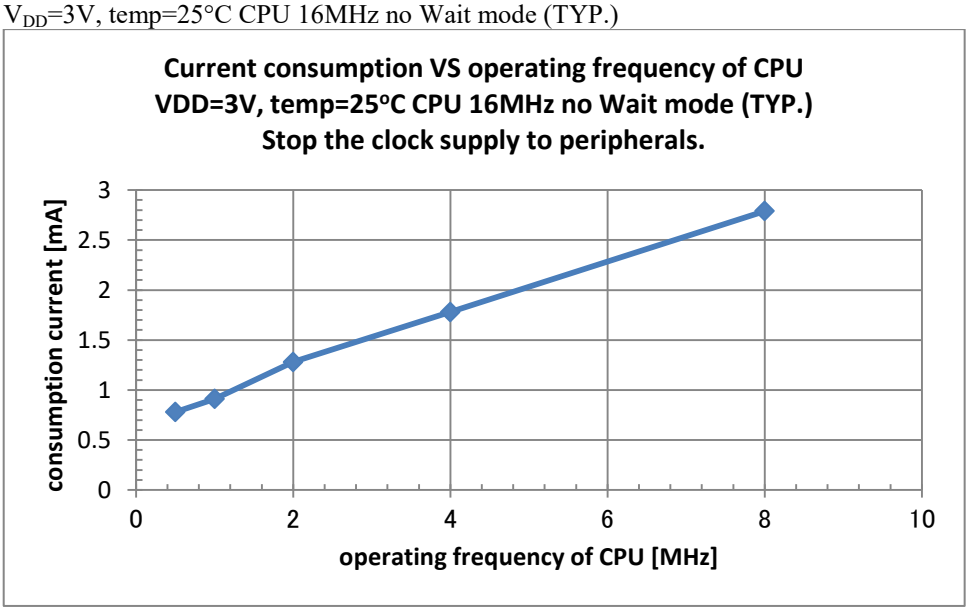
V_{DD}=3V, temp=25℃ CPU 24MHz no Wait mode (TYP.)



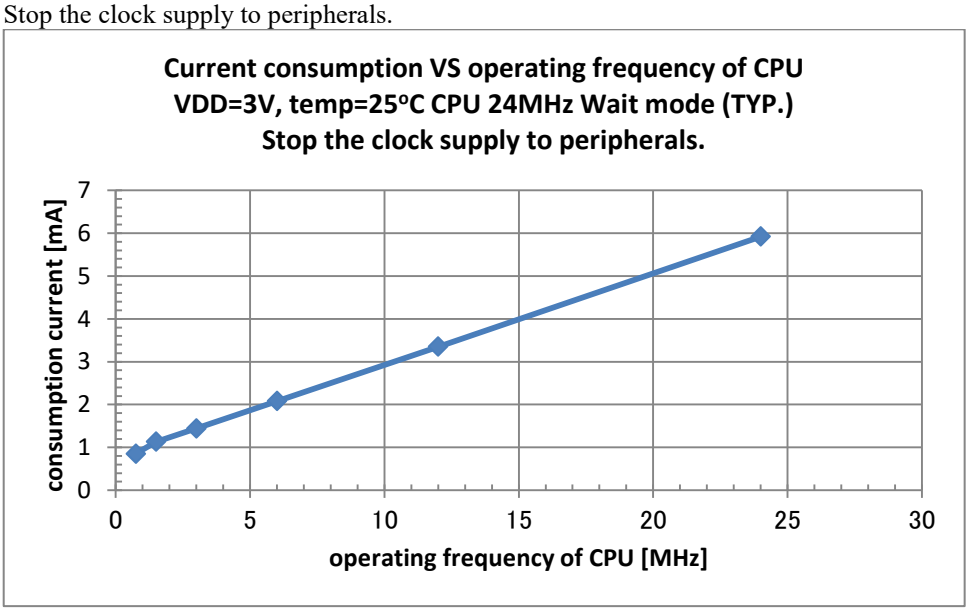
Current consumption VS operating frequency of CPU
V_{DD}=3V, temp=25°C CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



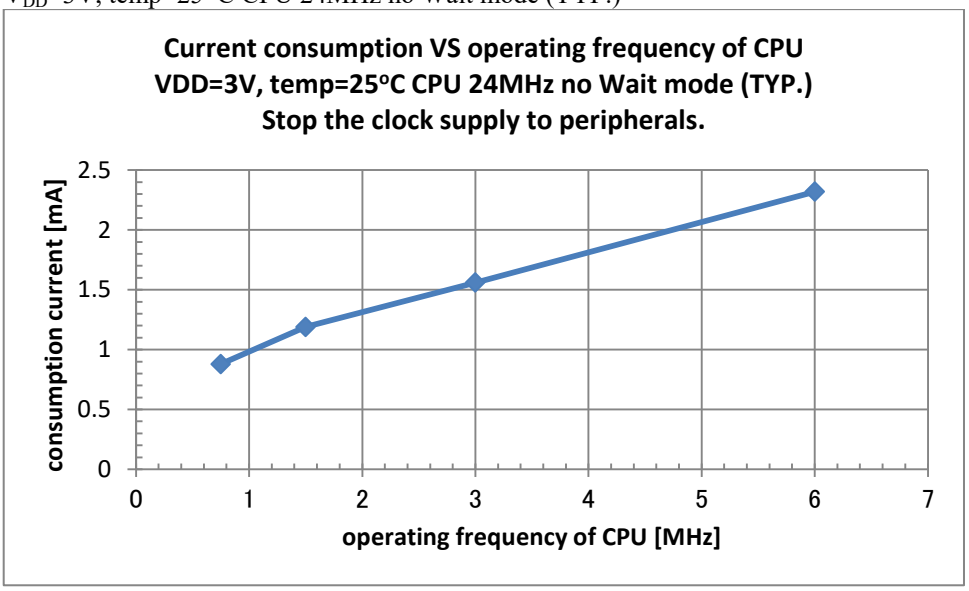
V_{DD}=3V, temp=25°C CPU 16MHz no Wait mode (TYP.)



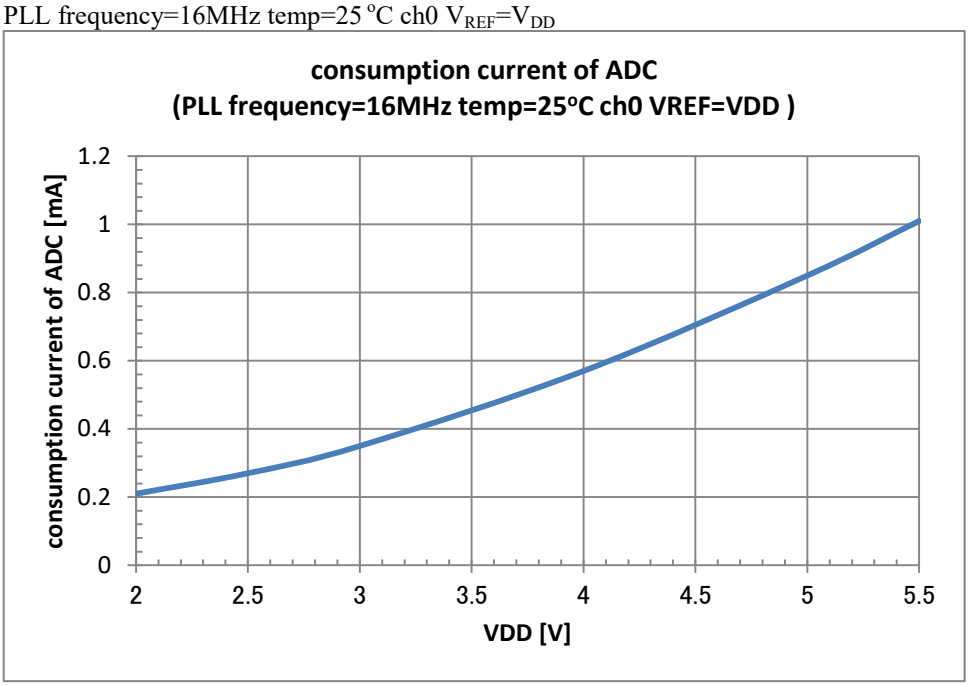
Current consumption VS operating frequency of CPU
V_{DD}=3V, temp=25 °C CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



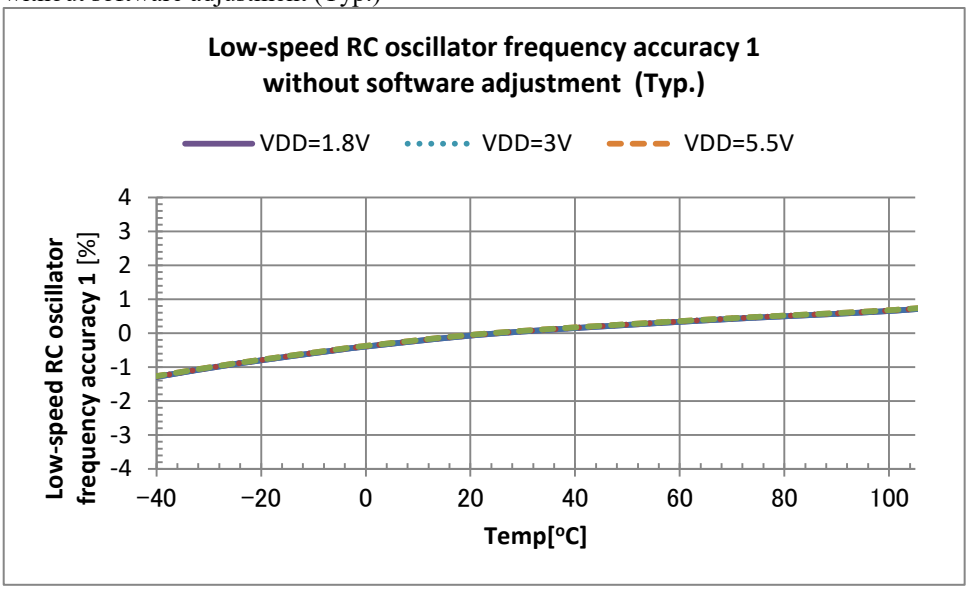
V_{DD}=3V, temp=25 °C CPU 24MHz no Wait mode (TYP.)



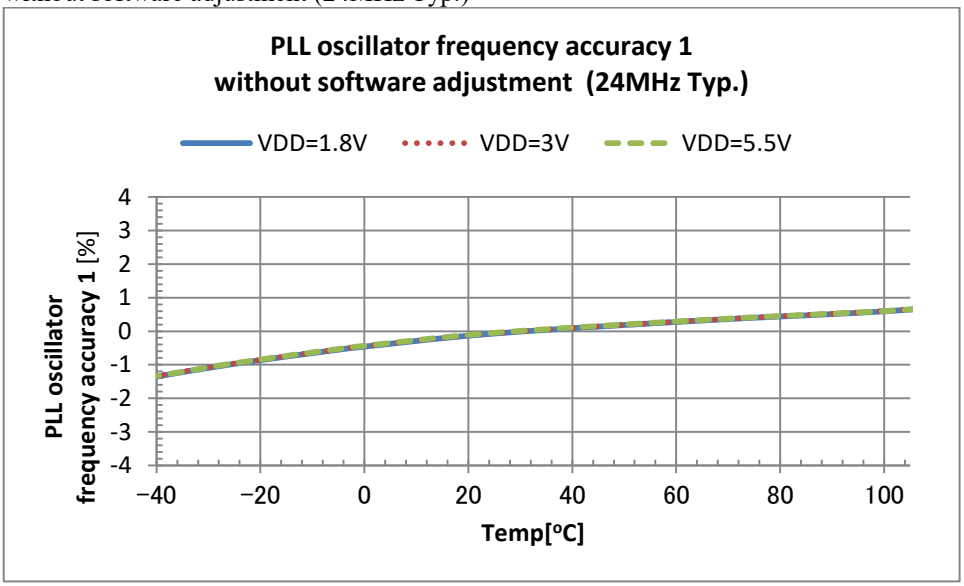
Consumption current of ADC VS operating voltage
PLL frequency=16MHz temp=25 °C ch0 $V_{REF}=V_{DD}$



TEMP VS Low-speed RC oscillator frequency accuracy 1
without software adjustment (Typ.)

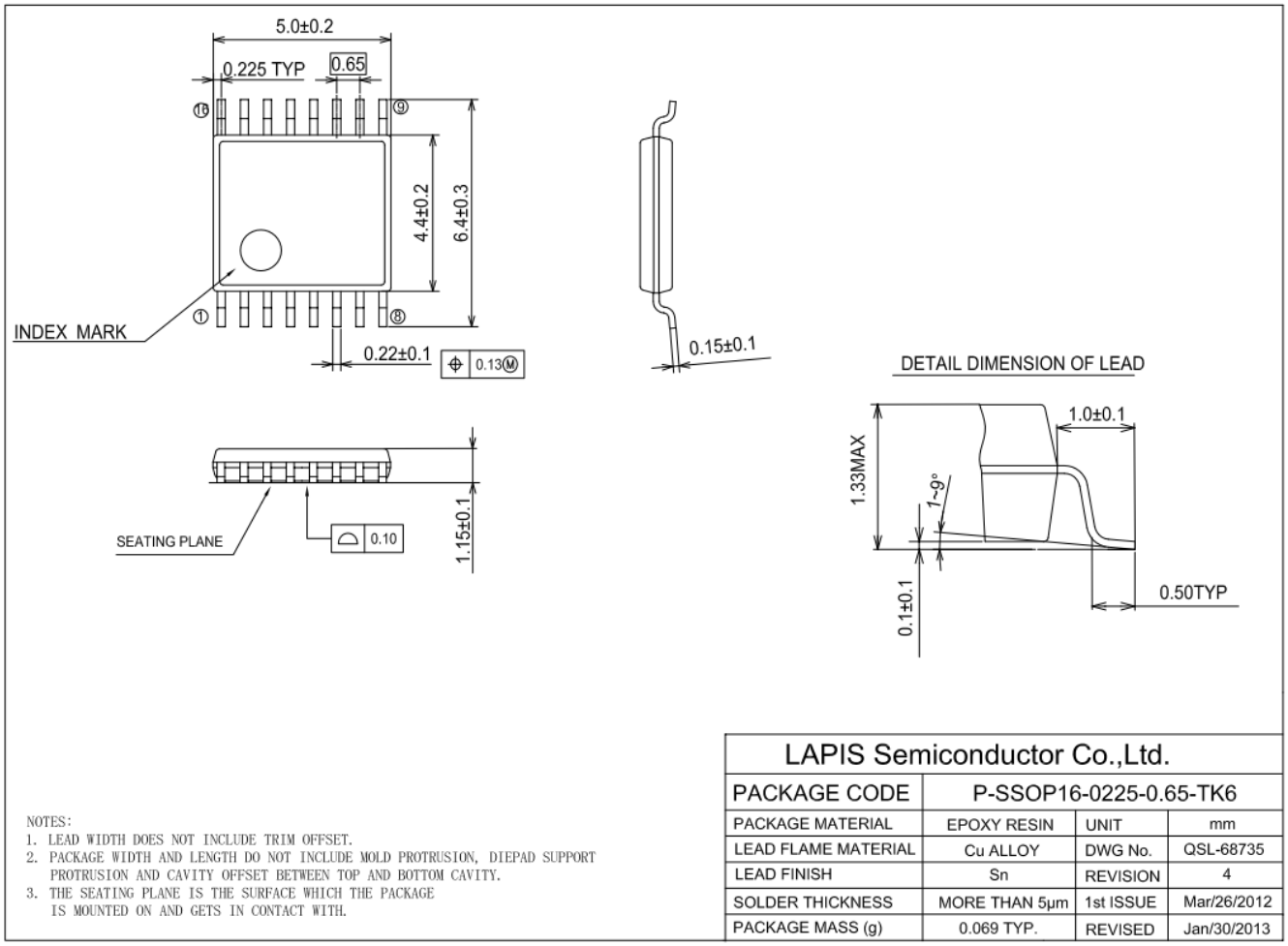


TEMP VS PLL oscillator frequency accuracy 1
without software adjustment (24MHz Typ.)



PACKAGE DIMENSIONS

ML62Q1323/1324/1325 16pin SSOP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

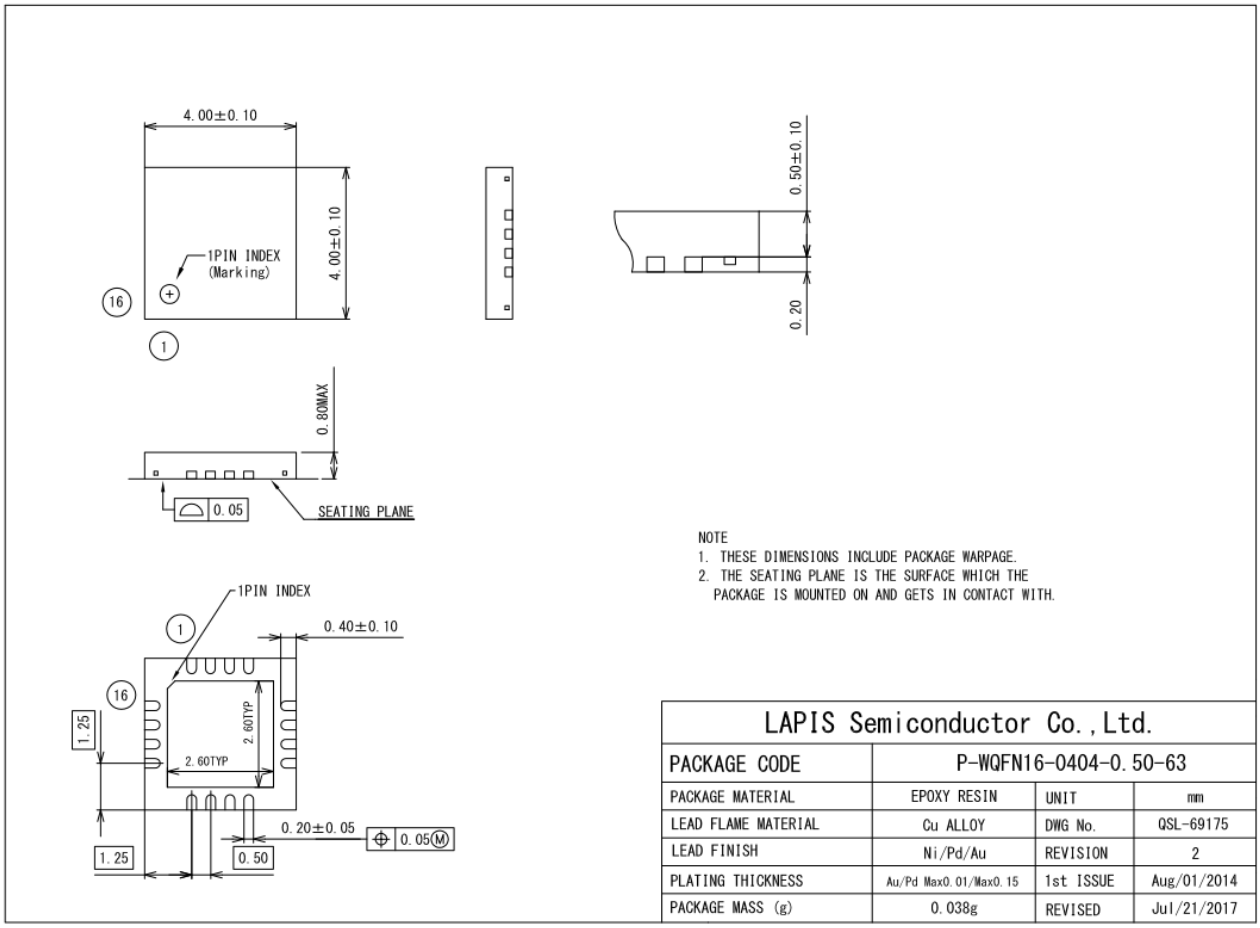
LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-SSOP16-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68735
LEAD FINISH	Sn	REVISION	4
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Mar/26/2012
PACKAGE MASS (g)	0.069 TYP.	REVISED	Jan/30/2013

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1323/1324/1325 16pin WQFN Package



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-WQFN16-0404-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69175
LEAD FINISH	Ni/Pd/Au	REVISION	2
PLATING THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Aug/01/2014
PACKAGE MASS (g)	0.038g	REVISED	Jul/21/2017

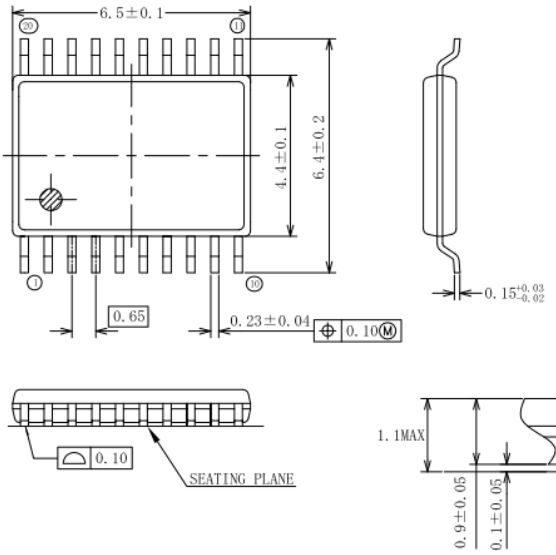
(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad
The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

ML62Q1333/1334/1335 20pin TSSOP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

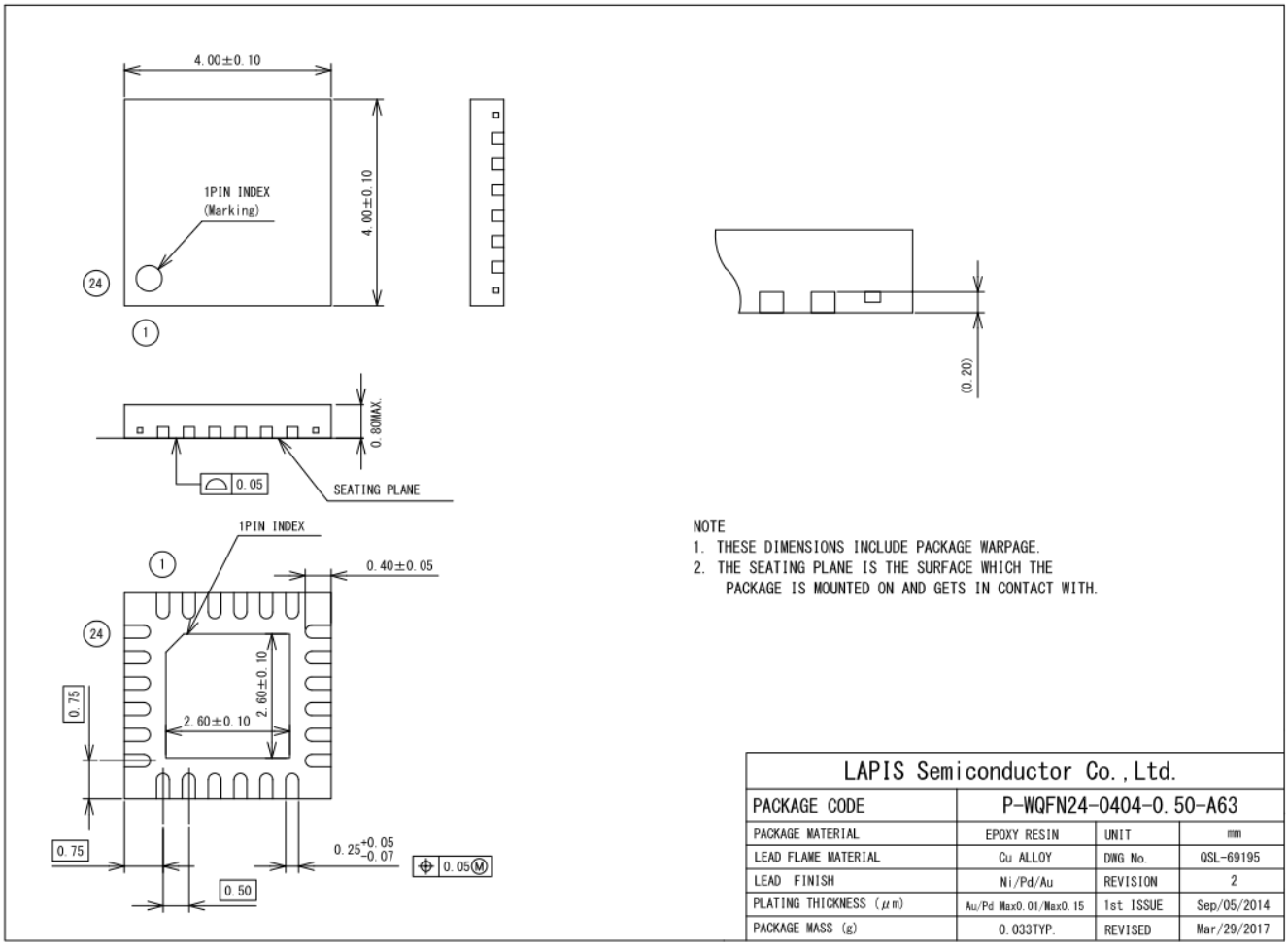
LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TSSOP20-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68909
LEAD FINISH	Sn	REVISION	1
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.08TYP.	REVISED	

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1345/1346/1347 24pin WQFN Package



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-WQFN24-0404-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69195
LEAD FINISH	Ni/Pd/Au	REVISION	2
PLATING THICKNESS (μm)	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/05/2014
PACKAGE MASS (g)	0.033TYP.	REVISED	Mar/29/2017

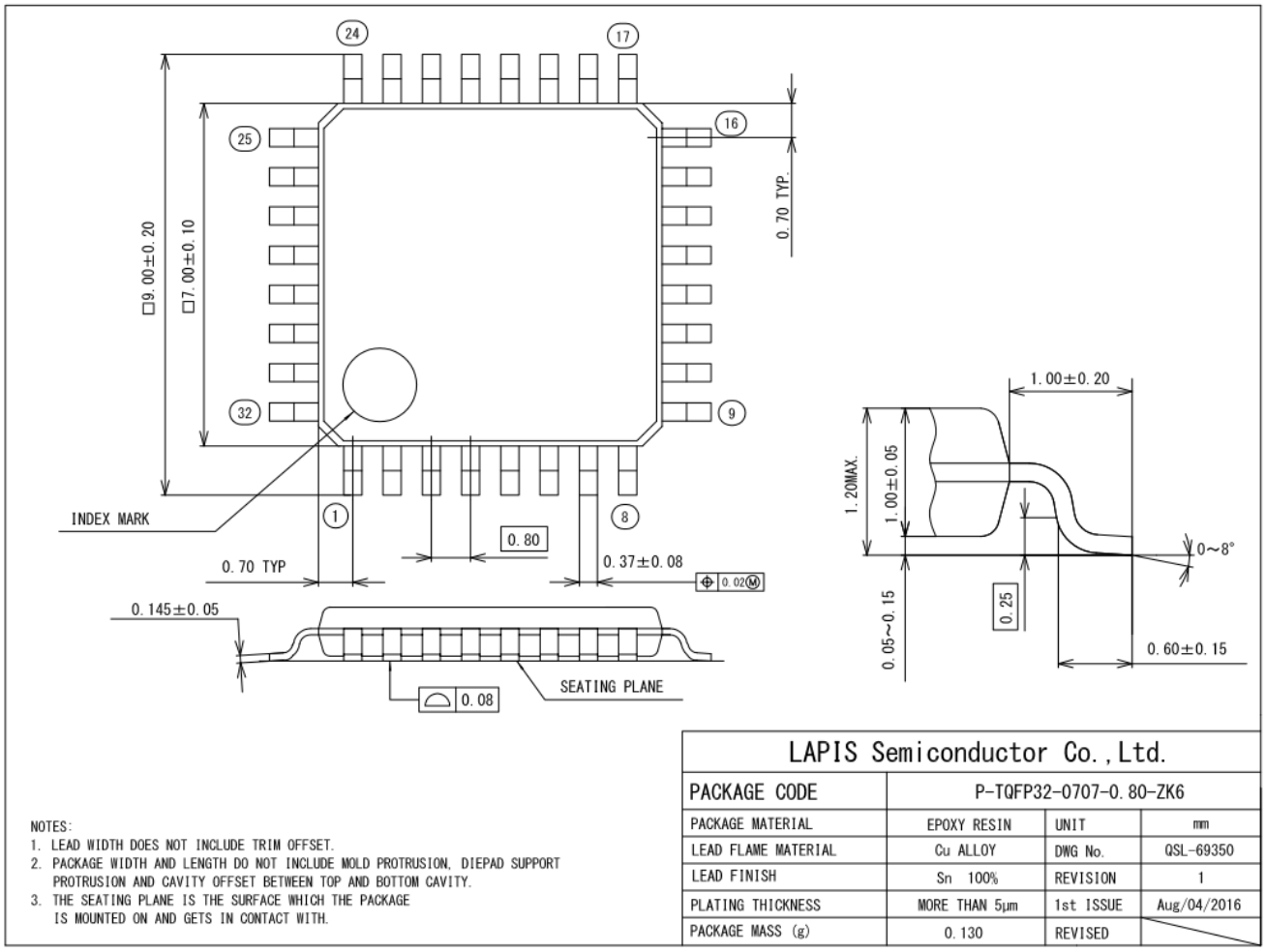
(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad
The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

ML62Q1365/1366/1367 32pin TQFP Package



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP32-0707-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69350
LEAD FINISH	Sn 100%	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Aug/04/2016
PACKAGE MASS (g)	0.130	REVISED	

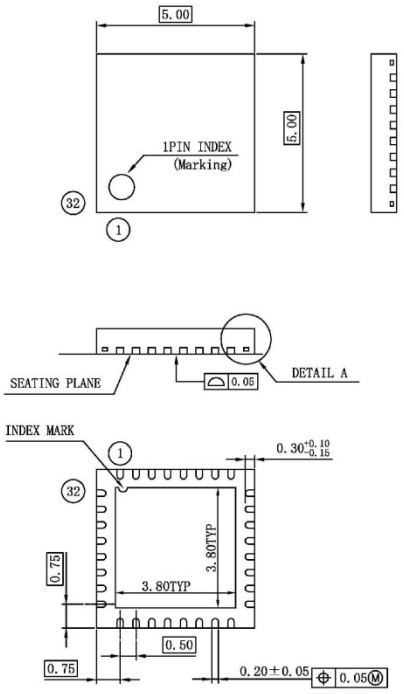
NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

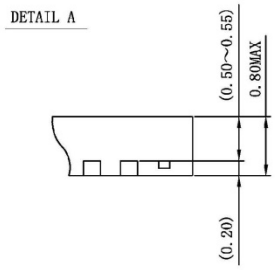
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1365/1366/1367 32pin WQFN Package

P-WQFN32-0505-0.50-A63





Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 max./0.15 max.
Package weight (g)	0.055 TYP.
Rev. No./Last Revised	2/Feb. 4, 2012

LAPIS Semiconductor Co.,Ltd.

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad
The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL62Q1300-01	Nov 15, 2018	-	-	1st Revision.
FEDL62Q1300-02	Sep 27, 2019	1	1	Changed the products status (Table 1 ML62Q1300 Group Product List)
		-	23	Added Current Consumption 1
		26	27	Added comment "*6" to the IOHL.
		46	49	Updated 24MHz Characteristics graph
		-	46,47	Added ML62Q1323/ML62Q1324/ML62Q1325/ML62Q1333/ ML62Q1334/ML62Q1335 Current consumption VS operating frequency of CPU
		*	*	Correction of errors
FEDL62Q1300-03	Mar 25, 2020	21	21	Changed termination of unused pins
		22	22	Added parameter "Operating temperature(Chip-Junction)" in Recommended Operating Conditions
		—	23	Added thermal characteristics section
		34	35	Added comments and notes to the reset characteristics
		34	36	Revised overall of "Power On Reset" section as "Slope of Power supply and Power On Reset" section. The major revisions are Added definitions of Power on rising/falling slope, Power on voltage, CPU operation start time, and added Note.
		*	*	Corrected typo

Notes

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