Octal 14-Bit, Parallel Input, Voltage-Output DAC

AD7841

FEATURES
Eight 14-Bit DACs in One Package
Voltage Outputs
Offset Adjust for Each DAC Pair
Reference Range of ±5 V
Maximum Output Voltage Range of ±10 V
±15 V ± 10% Operation
Clear Function to User-Defined Voltage
44-Lead MQFP Package

APPLICATIONS
Automatic Test Equipment
Process Control
General Purpose Instrumentation

GENERAL DESCRIPTION

The AD7841 contains eight 14-bit DACs on one monolithic chip. It has output voltages with a full-scale range of ±10 V from reference voltages of ±5 V.

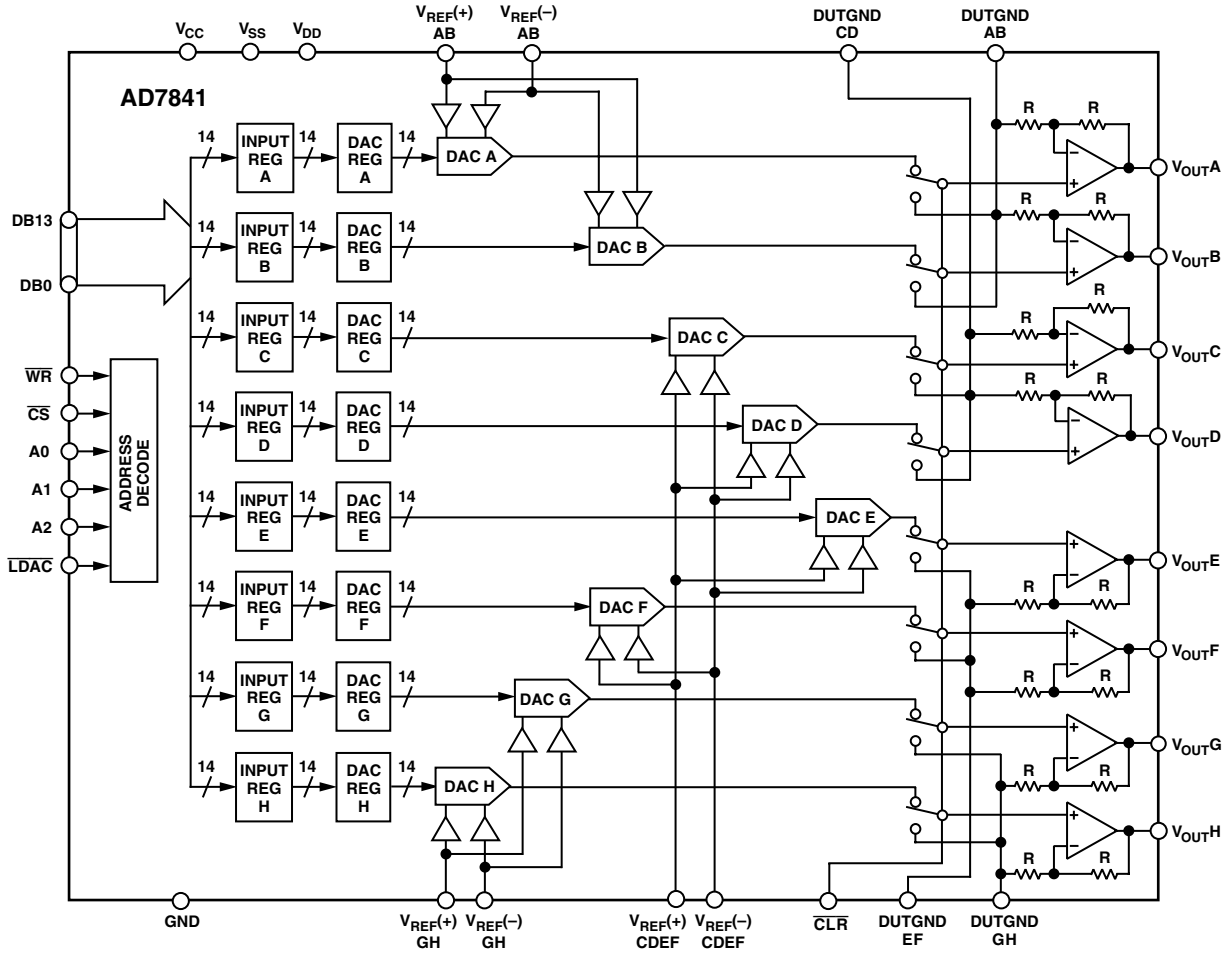
The AD7841 accepts 14-bit parallel loaded data from the external bus into one of the input registers under the control of the $\overline{WR}$, $\overline{CS}$, and DAC channel address pins, A0–A2.

The DAC outputs are updated on reception of new data into the DAC registers. All the outputs may be updated simultaneously by taking the $\overline{LDAC}$ input low.

Each DAC output is buffered with a gain-of-two amplifier into which an external DAC offset voltage can be inserted via the DUTGNDx pins.

The AD7841 is available in a 44-lead MQFP package.

FUNCTIONAL BLOCK DIAGRAM



REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/461-3113

AD7841—SPECIFICATIONS (V_{CC} = 5 V ± 5%; V_{DD} = 15 V ± 10%; V_{SS} = –15 V ± 10%; GND = DUTGND = 0 V; R_L = 5 kΩ and C_L = 50 pF to GND, T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A	B	Unit	Test Conditions/Comments
ACCURACY				
Resolution	14	14	Bits	
Relative Accuracy	±4	±2	LSB max	
Differential Nonlinearity	–0.9/2	±1	LSB max	Guaranteed Monotonic Over Temperature for All Grades
Zero-Scale Error	±8	±8	LSB max	$V_{REF}(+)$ = +5 V, $V_{REF}(–)$ = –5 V. Typically within ±2 LSB
Full-Scale Error	±8	±8	LSB max	$V_{REF}(+)$ = +5 V, $V_{REF}(–)$ = –5 V. Typically within ±2 LSB
Gain Error	±2	±2	LSB typ	$V_{REF}(+)$ = +5 V, $V_{REF}(–)$ = –5 V
Gain Temperature Coefficient[2]	0.5	0.5	ppm FSR/°C typ	
	10	10	ppm FSR/°C max	
DC Crosstalk[2]	120	120	μV max	See Terminology. Typically 75 μV
REFERENCE INPUTS[2]				
DC Input Impedance	100	100	MΩ typ	
Input Current	±1	±1	μA max	Per Input. Typically ±0.03 μA
$V_{REF}(+)$ Range	0/5	0/5	V min/max	
$V_{REF}(–)$ Range	–5/0	–5/0	V min/max	
$[V_{REF}(+) – V_{REF}(–)]$	2/10	2/10	V min/max	For Specified Performance. Can Go as Low as 0 V, but Performance Not Guaranteed
DUTGND INPUTS[2]				
DC Input Impedance	60	60	kΩ typ	
Max Input Current	±0.3	±0.3	mA typ	Per Input
Input Range[3]	–2/+2	–2/+2	V min/max	
OUTPUT CHARACTERISTICS[2]				
Output Voltage Swing	V_{SS} + 2.5 V to V_{DD} – 2.5 V	V_{SS} + 2.5 V to V_{DD} – 2.5 V	V typ	$V_{OUT} = 2 \times (V_{REF}(–) + [V_{REF}(+) – V_{REF}(–)] \times D) – V_{DUTGND}$
Short Circuit Current	15	15	mA max	
Resistive Load	5	5	kΩ min	To 0 V
Capacitive Load	50	50	pF max	To 0 V
DC Output Impedance	0.5	0.5	Ω max	
DIGITAL INPUTS[2]				
V_{INH}, Input High Voltage	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	V max	
I_{INH}, Input Current				Total for All Pins
@ 25°C	±1	±1	μA max	
T_{MIN} to T_{MAX}	±10	±10	μA max	
C_{IN}, Input Capacitance	10	10	pF max	
POWER REQUIREMENTS[4]				
V_{CC}	4.75/+5.25	4.75/+5.25	V min/max	For Specified Performance
V_{DD}	15 V ± 10%	15 V ± 10%	V min/max	For Specified Performance
V_{SS}	–15 V ± 10%	–15 V ± 10%	V min/max	For Specified Performance
Power Supply Sensitivity[2]				
ΔFull Scale/ΔV_{DD}	90	90	dB typ	
ΔFull Scale/ΔV_{SS}	90	90	dB typ	
I_{CC}	0.5	0.5	mA max	$V_{INH} = V_{CC}$, V_{INL} = GND. Dynamic Current
I_{DD}	10	10	mA max	Outputs Unloaded. Typically 8 mA
I_{SS}	10	10	mA max	Outputs Unloaded. Typically 8 mA

NOTES

[1]Temperature range for A and B Versions: –40°C to +85°C.

[2]Guaranteed by characterization. Not production tested.

[3]See DUTGND Voltage Range section.

[4]The AD7841 is functional with power supplies of ±12 V ±10% with reduced output range. Output amplifier requires 2.5 V of head room at the bottom and top ends of the transfer for function. At 12 V supplies it is recommended to restrict the reference range to ±4 V.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to production testing.)

Parameter	A & B Versions	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	31	µs typ	Full-Scale Change to ±1/2 LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s
Slew Rate	0.7	V/µs typ	
Digital-to-Analog Glitch Impulse	230	nV-s typ	Measured with $V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V. DAC Latch Alternately Loaded with 1FFF Hex and 2000 Hex. Not Dependent on Load Conditions
Channel-to-Channel Isolation	99	dB typ	See Terminology
DAC-to-DAC Crosstalk	40	nV-s typ	See Terminology
Digital Crosstalk	0.2	nV-s typ	Feedthrough to DAC Output Under Test Due to Change in Digital Input Code to Another Converter
Digital Feedthrough	0.1	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density @ 1 kHz	200	nV/√Hz typ	All 1s Loaded to DAC. $V_{REF}(+) = V_{REF}(-)$ = 0 V

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1, 2] (V_{CC} = 5 V ± 5%; V_{DD} = 15 V ± 10%; V_{SS} = –15 V ± 10%; GND = DUTGND = 0 V)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	15	ns min	Address to $\overline{WR}$ Setup Time
t_2	0	ns min	Address to $\overline{WR}$ Hold Time
t_3	50	ns min	$\overline{CS}$ Pulsewidth Low
t_4	50	ns min	$\overline{WR}$ Pulsewidth Low
t_5	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_6	0	ns min	$\overline{WR}$ to $\overline{CS}$ Hold Time
t_7	20	ns min	Data Setup Time
t_8	0	ns min	Data Hold Time
t_9	31	µs typ	Settling Time
t_{10}	300	ns max	$\overline{CLR}$ Pulse Activation Time
t_{11}	50	ns min	$\overline{LDAC}$ Pulsewidth Low

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Rise and fall times should be no longer than 50 ns.
Specifications subject to change without notice.

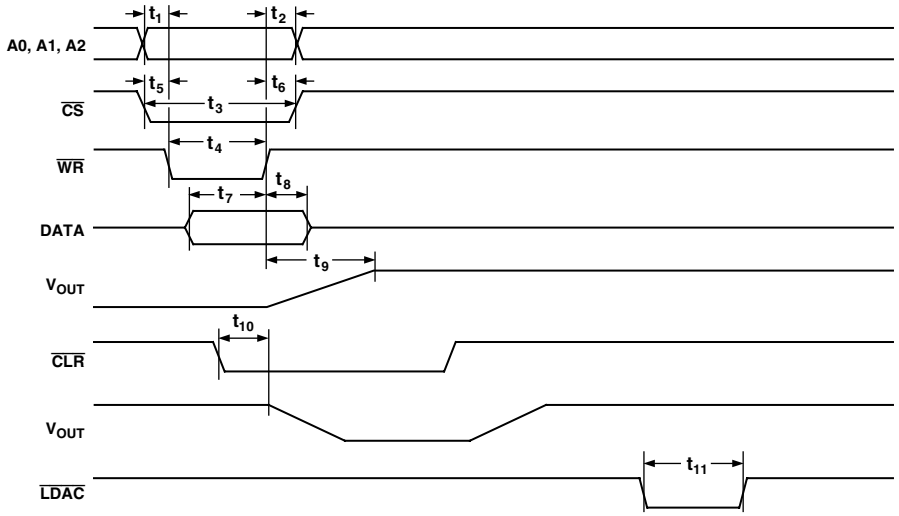


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C unless otherwise noted)

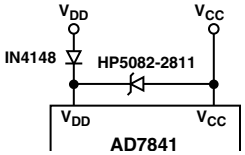
V_{CC} to GND[3] . . . . . –0.3 V, +7 V or V_{DD} + 0.3 V (Whichever Is Lower)
V_{DD} to GND . . . . . –0.3 V, +17 V
V_{SS} to GND . . . . . +0.3 V, –17 V
Digital Inputs to GND . . . . . –0.3 V, V_{CC} + 0.3 V
V_{REF}(+) to V_{REF}(–) . . . . . –0.3 V, +18 V
V_{REF}(+) to GND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{REF}(–) to GND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
DUTGND to GND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{OUT} (A–H) to GND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
MQFP Package
Power Dissipation . . . . . $(T_J Max – T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance . . . . . 95°C/W
Lead Temperature .....JEDEC Industry Standard
Soldering J-STD-020
ESD ..... >4000 V

NOTES

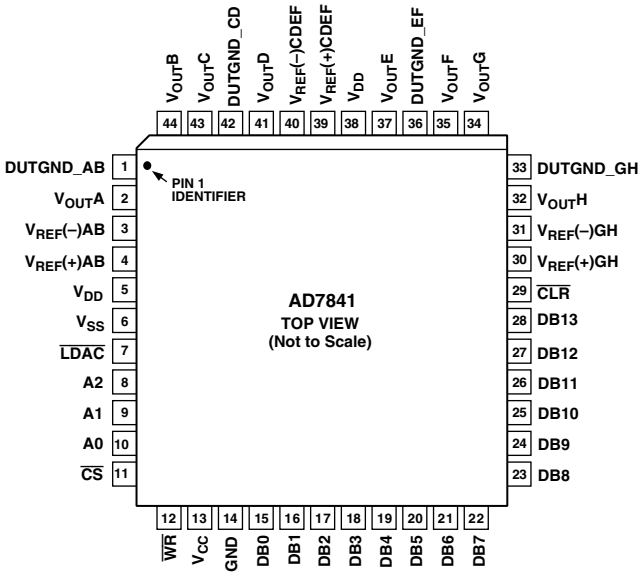
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

[3]V_{CC} must not exceed V_{DD} by more than 0.3 V. If it is possible for this to happen during power supply sequencing, the following diode protection scheme will ensure protection.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	DUTGND_AB	Device Sense Ground for DACs A and B. $V_{OUT}A$ and $V_{OUT}B$ are referenced to the voltage applied to this pin.
2, 44, 43, 41, 37, 35, 34, 32	$V_{OUT}A$ . . $V_{OUT}H$	DAC Outputs.
3, 4	$V_{REF}(-)AB$, $V_{REF}(+)AB$	Reference Inputs for DACs A and B. These reference voltages are referred to GND.
5, 38	V_{DD}	Positive Analog Power Supply; +15 V ± 10% for specified performance.
6	V_{SS}	Negative Analog Power Supply; –15 V ± 10% for specified performance.
7	$\overline{LDAC}$	Load DAC Logic Input (active low). When this logic input is taken low the contents of the registers are transferred to their respective DAC registers. $\overline{LDAC}$ can be tied permanently low enabling the outputs to be updated on the rising edge of $\overline{WR}$.
8, 9, 10	A2, A1, A0	Address inputs. A0, A1 and A2 are decoded to select one of the eight input registers for a data transfer.
11	$\overline{CS}$	Level-Triggered Chip Select Input (active low). The device is selected when this input is low.
12	$\overline{WR}$	Level-Triggered Write Input (active low), used in conjunction with $\overline{CS}$ to write data to the AD7841 data registers. Data is latched into the selected input register on the rising edge of $\overline{WR}$.
13	V_{CC}	Logic Power Supply; 5 V ± 5%.
14	GND	Ground.
15–28	DB0 . . DB12	Parallel Data Inputs. The AD7841 can accept a straight 14-bit parallel word on DB0 to DB13 where DB13 is the MSB and DB0 is the LSB.
29	$\overline{CLR}$	Asynchronous Clear Input (level sensitive, active low). When this input is low, all analog outputs are switched to the externally set potential on the relevant DUTGND pin. The contents of input registers and DAC registers A to H are not affected when the $\overline{CLR}$ pin is taken low. When $\overline{CLR}$ is brought back high, the DAC outputs revert to their original outputs as determined by the data in their DAC registers.
30, 31	$V_{REF}(+)GH$, $V_{REF}(-)GH$	Reference Inputs for DACs G and H. These reference voltages are referred to GND.
33	DUTGND_GH	Device Sense Ground for DACs G and H. $V_{OUT}G$ and $V_{OUT}H$ are referenced to the voltage applied to this pin.
36	DUTGND_EF	Device Sense Ground for DACs E and F. $V_{OUT}E$ and $V_{OUT}F$ are referenced to the voltage applied to this pin.
39	$V_{REF}(+)CDEF$	Reference Inputs for DACs C, D, E and F. These reference voltages are referred to GND.
40	$V_{REF}(-)CDEF$	Reference Inputs for DACs C, D, E and F. These reference voltages are referred to GND.
42	DUTGND_CD	Device Sense Ground for DACs C and D. $V_{OUT}C$ and $V_{OUT}D$ are referenced to the voltage applied to this pin.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in Least Significant Bits.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

DC Crosstalk
Although the common input reference voltage signals are internally buffered, small IR drops in the individual DAC reference inputs across the die can mean that an update to one channel can produce a dc output change in one or another of the channel outputs.

The eight DAC outputs are buffered by op amps that share common V_{DD} and V_{SS} power supplies. If the dc load current changes in one channel (due to an update), this can result in a further dc change in one or another of the channel outputs. This effect is most obvious at high load currents and reduces as the load currents are reduced. With high impedance loads the effect is virtually impossible to measure.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-secs. It is measured with $V_{REF}(+)$ = +5 V and $V_{REF}(-)$ = –5 V and the digital inputs toggled between 1FFFH and 2000H.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input that appears at the output of another DAC. It is expressed in dBs.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is defined as the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog O/P change at another converter. It is specified in nV-secs.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the digital crosstalk and is specified in nV-secs.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins. This noise is digital feedthrough.

DC Output Impedance
This is the effective output source resistance. It is dominated by package lead resistance.

Full-Scale Error
This is the error in DAC output voltage when all 1s are loaded into the DAC latch. Ideally the output voltage, with all 1s loaded into the DAC latch, should be 2 $V_{REF}(+)$ – 1 LSB.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC latch. Ideally the output voltage, with all 0s in the DAC latch should be equal to 2 $V_{REF}(-)$. Zero-scale error is mainly due to offsets in the output amplifier.

Gain Error
Gain Error is defined as (Full-Scale Error) – (Zero-Scale Error).

GENERAL DESCRIPTION

DAC Architecture—General
Each channel consists of a straight 14-bit R-2R voltage-mode DAC. The full-scale output voltage range is equal to twice the reference span of $V_{REF}(+) - V_{REF}(-)$. The DAC coding is straight binary; all 0s produces an output of 2 $V_{REF}(-)$; all 1s produces an output of 2 $V_{REF}(+)$ – 1 LSB.

The analog output voltage of each DAC channel reflects the contents of its own DAC register. Data is transferred from the external bus to the input register of each DAC on a per channel basis.

Bringing the $\overline{CLR}$ line low switches all the signal outputs, $V_{OUT}A$ to $V_{OUT}H$, to the voltage level on the relevant DUTGND pin. When the $\overline{CLR}$ signal is brought back high, the output voltages from the DACs will reflect the data stored in the relevant DAC registers.

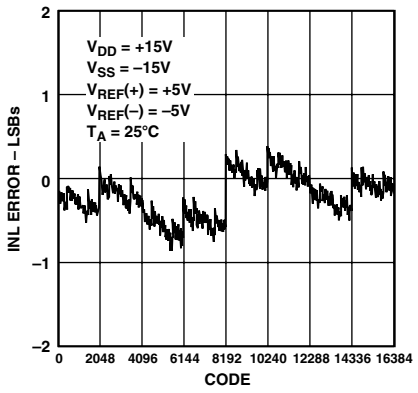
Data Loading to the AD7841
Data is loaded into the AD7841 in straight parallel 14-bit wide words.

The DAC output voltages, $V_{OUT}A - V_{OUT}H$ are updated to reflect new data in the DAC registers.

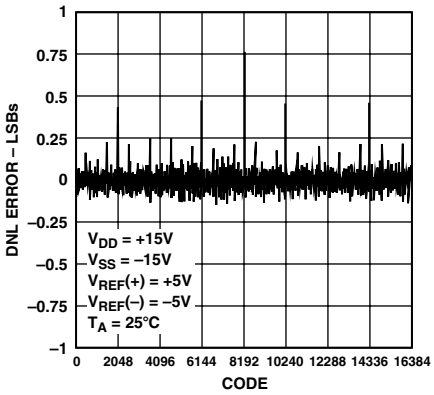
The actual input register being written to is determined by the logic levels present on the device's address lines, as shown in Table I.

Table I. Address Line Truth Table

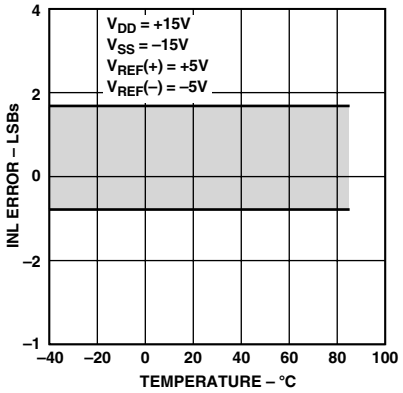
A2	A1	A0	DAC Selected
0	0	0	INPUT REG A (DAC A)
0	0	1	INPUT REG B (DAC B)
0	1	0	INPUT REG C (DAC C)
0	1	1	INPUT REG D (DAC D)
1	0	0	INPUT REG E (DAC E)
1	0	1	INPUT REG F (DAC F)
1	1	0	INPUT REG G (DAC G)
1	1	1	INPUT REG H (DAC H)



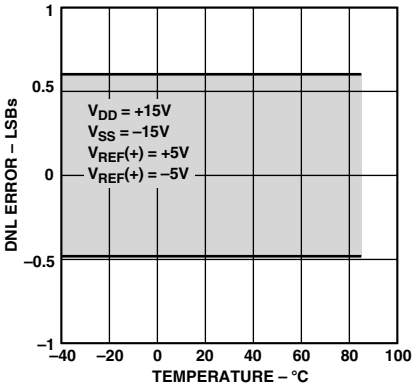
TPC 1. Typical INL Plot



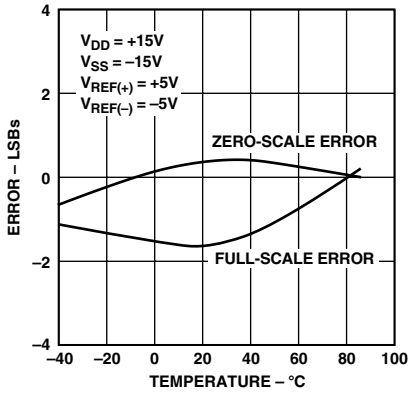
TPC 2. Typical DNL Plot



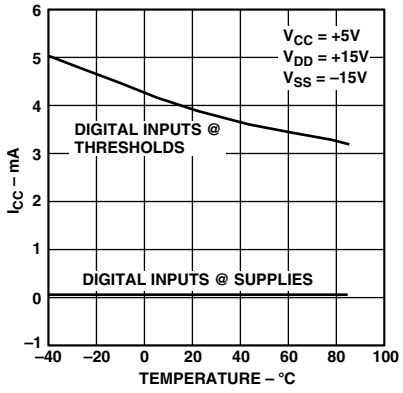
TPC 3. Typical INL Error vs. Temperature



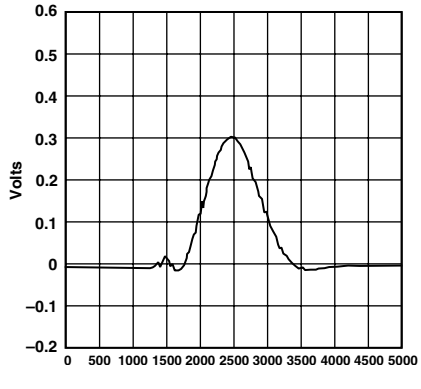
TPC 4. Typical DNL Error vs. Temperature



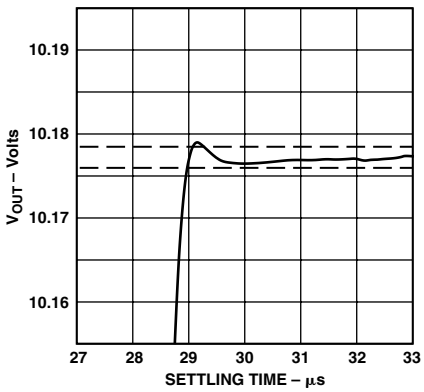
TPC 5. Zero-Scale and Full-Scale Error vs. Temperature



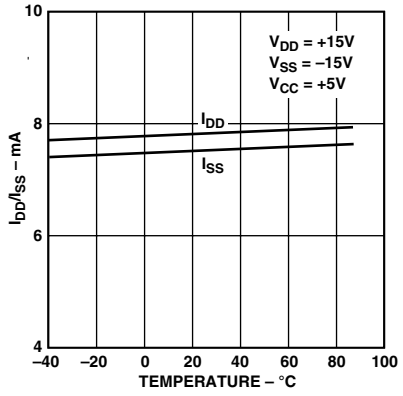
TPC 6. I_{CC} vs. Temperature



TPC 7. Typical Digital-to-Analog Glitch Impulse



TPC 8. Settling Time (+)



TPC 9. I_{DD}, I_{SS} vs. Temperature

Unipolar Configuration

Figure 2 shows the AD7841 in the unipolar binary circuit configuration. The $V_{REF}(+)$ input of the DAC is driven by the AD586, a 5 V reference. $V_{REF}(-)$ is tied to ground. Table II gives the code table for unipolar operation of the AD7841. Other suitable references include the REF02, a precision 5 V reference, and the REF195, a low dropout, micropower precision 5 V reference.

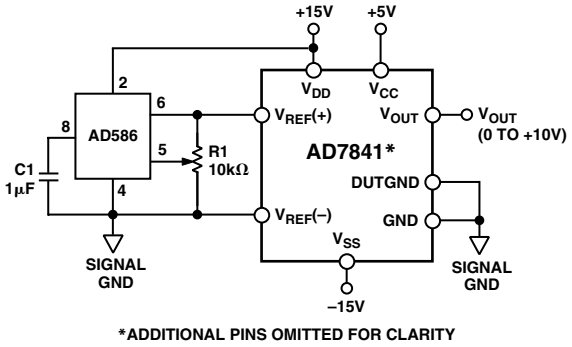


Figure 2. Unipolar 10 V Operation

Offset and gain may be adjusted in Figure 2 as follows: To adjust offset, disconnect the $V_{REF}(-)$ input from 0 V, load the DAC with all 0s and adjust the $V_{REF}(-)$ voltage until V_{OUT} = 0 V. For gain adjustment, the AD7841 should be loaded with all 1s and R1 adjusted until V_{OUT} = 2 $V_{REF}(+)$ – 1 LSB = 10 V(16383/16384) = 9.99939 V.

Many circuits will not require these offset and gain adjustments. In these circuits R1 can be omitted. Pin 5 of the AD586 may be left open circuit and Pin 2 ($V_{REF}(-)$) of the AD7841 tied to 0 V.

Table II. Code Table for Unipolar Operation

Binary Number in DAC Register MSB			LSB	Analog Output (V_{OUT})
11	1111	1111	1111	2 V_{REF} (16383/16384) V
10	0000	0000	0000	2 V_{REF} (8192/16384) V
01	1111	1111	1111	2 V_{REF} (8191/16384) V
00	0000	0000	0001	2 V_{REF} (1/16384) V
00	0000	0000	0000	0 V

NOTES
V= $V_{REF}(+)$; $V_{REF}(-)$ = 0 V for unipolar operation.
For $V_{REF}(+)$ = 5 V, 1 LSB = 10 V/2^{14} = 10 V/16384 = 610 µV.

Bipolar Configuration

Figure 3 shows the AD7841 set up for ±10 V operation. The AD588 provides precision ±5 V tracking outputs that are fed to the $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the AD7841. The code table for bipolar operation of the AD7841 is shown in Table III.

In Figure 3, full-scale and bipolar zero adjustments are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the offset of both the +5 V and –5 V outputs together with respect to ground.

For bipolar-zero adjustment, the DAC is loaded with 1000 . . . 0000 and R3 is adjusted until V_{OUT} = 0 V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until V_{OUT} = 10(8191/8192) V = 9.99878 V.

When bipolar-zero and full-scale adjustment are not needed, R2 and R3 can be omitted. Pin 12 on the AD588 should be connected to Pin 11 and Pin 5 should be left floating.

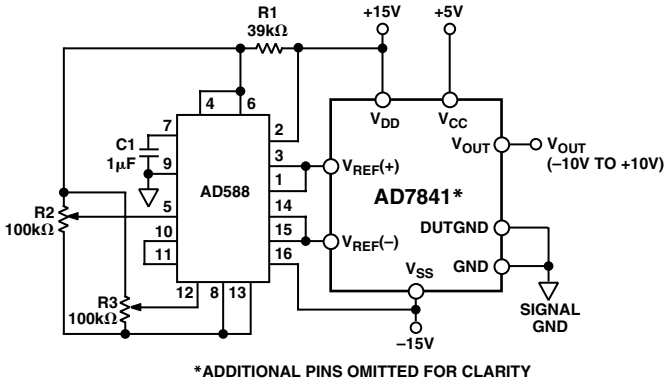


Figure 3. Bipolar ±10 V Operation

Table III. Code Table for Bipolar Operation

Binary Number in DAC Register MSB			LSB	Analog Output (V_{OUT})
11	1111	1111	1111	2[$V_{REF}(-)$ + V_{REF} (16383/16384)] V
10	0000	0000	0001	2[$V_{REF}(-)$ + V_{REF} (8193/16384)] V
10	0000	0000	0000	2[$V_{REF}(-)$ + V_{REF} (8192/16384)] V
01	1111	1111	1111	2[$V_{REF}(-)$ + V_{REF} (8191/16384)] V
00	0000	0000	0001	2[$V_{REF}(-)$ + V_{REF} (1/16384)] V
00	0000	0000	0000	2[$V_{REF}(-)$] V

NOTES
V_{REF} = ($V_{REF}(+)$ – $V_{REF}(-)$).
For $V_{REF}(+)$ = +5 V, and $V_{REF}(-)$ = –5 V, V_{REF} = 10 V, 1 LSB = 2 V_{REF} V/2^{14} = 20 V/16384 = 1.22 mV.

CONTROLLED POWER-ON OF THE OUTPUT STAGE

A block diagram of the output stage of the AD7841 is shown in Figure 4. It is capable of driving a load of 5 kΩ in parallel with 50 pF. G_1 to G_6 are transmission gates used to control the power on voltage present at V_{OUT}. On power up G_1 and G_2 are also used in conjunction with the $\overline{CLR}$ input to set V_{OUT} to the user defined voltage present at the DUTGND pin. When $\overline{CLR}$ is taken back high, the DAC outputs reflect the data in the DAC registers.

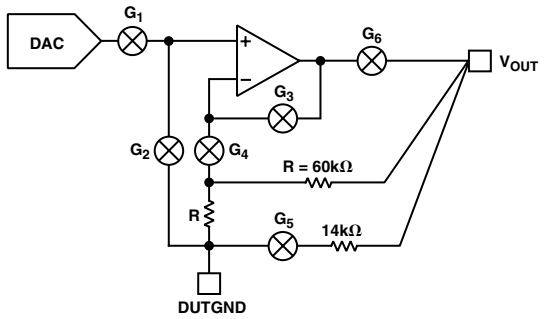


Figure 4. Block Diagram of AD7841 Output Stage

Power-On with $\overline{CLR}$ Low

The output stage of the AD7841 has been designed to allow output stability during power-on. If $\overline{CLR}$ is kept low during power-on, then just after power is applied to the AD7841, the situation is as depicted in Figure 5. G_1, G_4 and G_6 are open while G_2, G_3 and G_5 are closed.

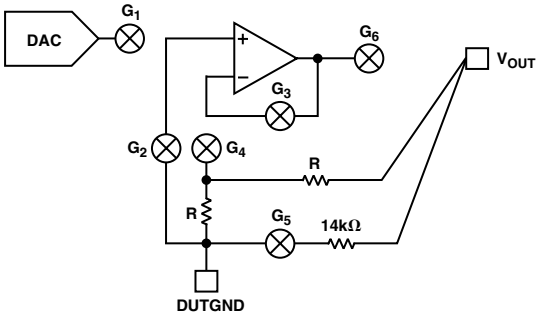


Figure 5. Output Stage with V_{DD} < 7 V or V_{SS} > –3 V; $\overline{CLR}$ Low

V_{OUT} is kept within a few hundred millivolts of DUTGND via G_5 and a 14 kΩ resistor. This thin-film resistor is connected in parallel with the gain resistors of the output amplifier. The output amplifier is connected as a unity gain buffer via G_3, and the DUTGND voltage is applied to the buffer input via G_2. The amplifier's output is thus at the same voltage as the DUTGND pin. The output stage remains configured as in Figure 5 until the voltage at V_{DD} exceeds 7 V and V_{SS} is more negative than –3 V. By now the output amplifier has enough headroom to handle signals at its input and has also had time to settle. The internal power-on circuitry opens G_3 and G_5 and closes G_4 and G_6. This situation is shown in Figure 6. Now the output amplifier is configured in its noise gain configuration via G_4 and G_6. The DUTGND voltage is still connected to the noninverting input via G_2 and this voltage appears at V_{OUT}.

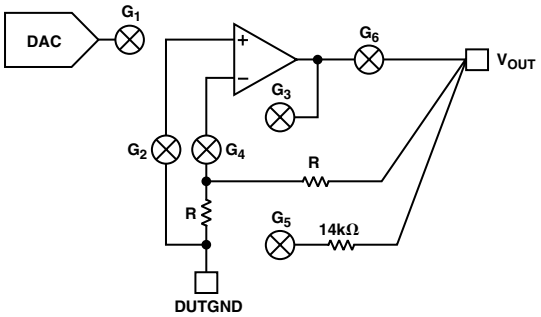


Figure 6. Output Stage with V_{DD} > 7 V and V_{SS} < –3 V; $\overline{CLR}$ Low

V_{OUT} has been disconnected from the DUTGND pin by the opening of G_5, but will track the voltage present at DUTGND via the configuration shown in Figure 6.

When $\overline{CLR}$ is taken back high, the output stage is configured as shown in Figure 7. The internal control logic closes G_1 and opens G_2. The output amr})fier is connected in a noninverting gain-of-two configuration. The voltage that appears on the V_{OUT} pins is determined by the data present in the DAC registers.

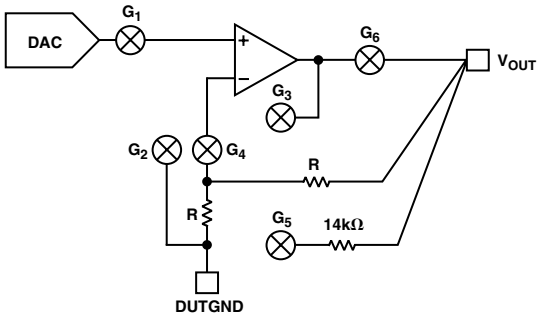


Figure 7. Output Stage After $\overline{CLR}$ Is Taken High

Power-On with $\overline{CLR}$ High

If $\overline{CLR}$ is high on the application of power to the device, the output stages of the AD7841 are configured as in Figure 8 while V_{DD} is less than 7 V and V_{SS} is more positive than –3 V. G_1 is closed and G_2 is open, thereby connecting the output of the DAC to the input of its output amplifier. G_3 and G_5 are closed while G_4 and G_6 are open, thus connecting the output amplifier as a unity gain buffer. V_{OUT} is connected to DUTGND via G_5 through a 14 kΩ resistor until V_{DD} exceeds 7 V and V_{SS} is more negative than –3 V.

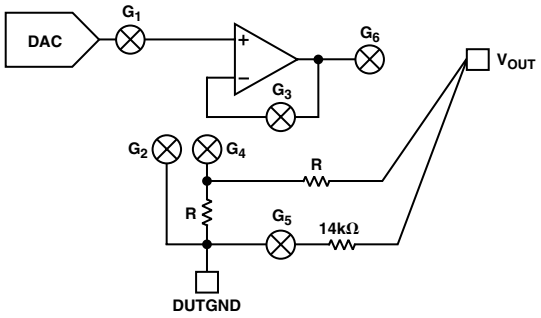


Figure 8. Output Stage Powering Up with $\overline{CLR}$ High While V_{DD} < 7 V or V_{SS} > –3 V

When the difference between the supply voltages reaches 10 V, the internal power-on circuitry opens G_3 and G_5 and closes G_4 and G_6 configuring the output stage as shown in Figure 9.

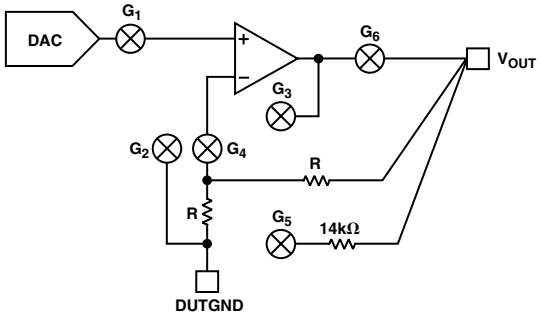


Figure 9. Output Stage Powering Up with $\overline{CLR}$ High When V_{DD} > 7 V and V_{SS} < –3 V

DUTGND Voltage Range

During power-on, the V_{OUT} pins of the AD7841 are connected to the relevant DUTGND pins via G_5 and the 14 kΩ thin-film resistor. The DUTGND potential must obey the max ratings at all times. Thus, the voltage at DUTGND must always be within the range V_{SS} – 0.3 V, V_{DD} + 0.3 V. However, in order that the voltages at the V_{OUT} pins of the AD7841 stay within ±2 V of the relevant DUTGND potential during power-on, the voltage applied to DUTGND should also be kept within the range GND – 2 V, GND + 2 V.

Once the AD7841 has powered on and the on-chip amplifiers have settled, any voltage that is now applied to the DUTGND pin is subtracted from the DAC output, which has been gained up by a factor of two. Thus, for specified operation, the maximum voltage that can be applied to the DUTGND pin increases to the maximum allowable 2 V_{REF}(+) voltage, and the minimum voltage that can be applied to DUTGND is the minimum 2 V_{REF}(–) voltage. After the AD7841 has fully powered on, the outputs can track any DUTGND voltage within this minimum/maximum range.

Power Supply Sequencing

When operating the AD7841, it is important that ground be connected at all times to avoid high current states. The recommended power-up sequence is V_{DD}/V_{SS} followed by V_{CC}. If V_{CC} can exceed V_{DD} on power-up, the diode scheme shown in the absolute maximum ratings section will ensure protection. The reference inputs and digital inputs should be powered up last. Should the references exceed V_{DD}/V_{SS} on power-up, current limiting resistors should be inserted in series with the reference inputs to limit the current to 20 mA. Logic inputs should not be applied before V_{CC}. Current limiting resistors (470 Ω) in series with the logic inputs should be inserted if these inputs come up before V_{CC}.

MICROPROCESSOR INTERFACING

Interfacing the AD7841—16-Bit Interface

The AD7841 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure 10 shows the AD7841 interfaced to a generic 16-bit microcontroller/DSP processor. The lower address lines from the processor are connected to A0, A1 and A2 on the AD7841 as shown. The upper address lines are decoded to provide a chip select signal or an $\overline{\text{LDAC}}$ signal for the AD7841. The fast interface timing of the AD7841 allows direct interface to a wide variety of microcontrollers and DSPs as shown in Figure 10.

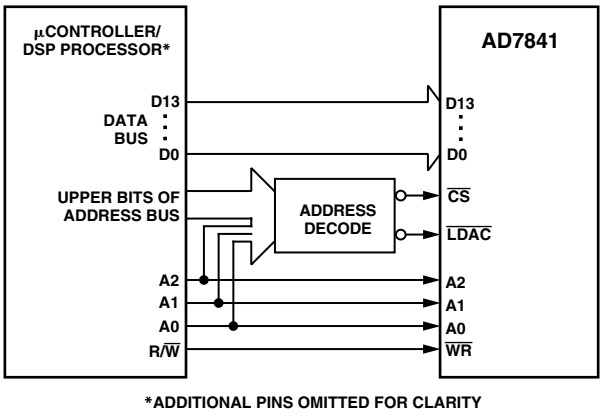


Figure 10. Parallel Interface

APPLICATIONS

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7841 is mounted should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined at only one place. The GND pin of the AD7841 should be connected to the AGND of the system. If the AD7841 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD7841.

Digital lines running under the device should be avoided as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7841 to avoid noise coupling. The power supply lines of the AD7841 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the analog inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but not always possible with a double sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

The AD7841 should have ample supply bypassing located as close to the package as possible, ideally right up against the device. Figure 11 shows the recommended capacitor values of 10 μF in parallel with 0.1 μF on each of the supplies. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

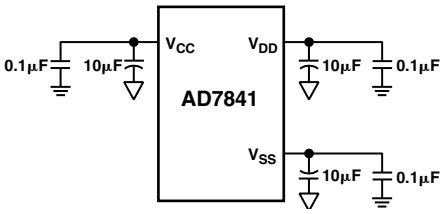


Figure 11. Recommended Decoupling Scheme for AD7841

Automated Test Equipment

The AD7841 is particularly suited for use in an automated test environment. Figure 12 shows the AD7841 providing the necessary voltages for the pin driver and the window comparator in a typical ATE pin electronics configuration. AD588s are used to provide reference voltages for the AD7841. In the configuration shown, the AD588s are configured so that the voltage at Pin 1 is 5 V greater than the voltage at Pin 9 and the voltage at Pin 15 is 5 V less than the voltage at Pin 9.

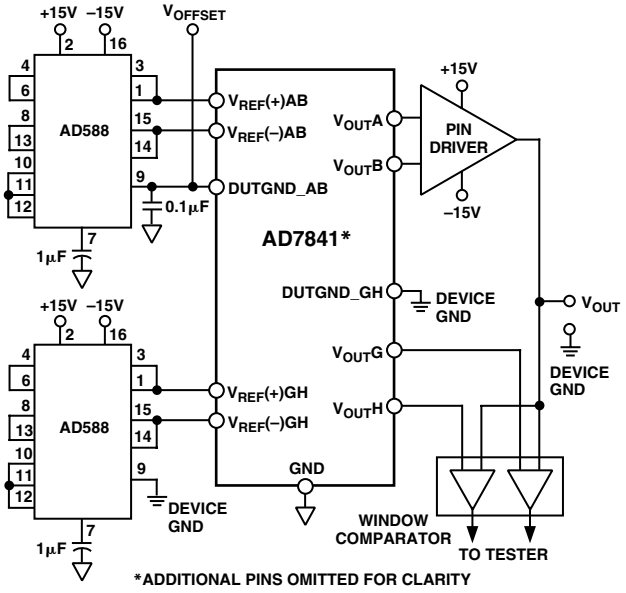


Figure 12. ATE Application

One of the AD588s is used as a reference for DACs A and B. These DACs are used to provide high and low levels for the pin driver. The pin driver may have an associated offset. This can be nulled by applying an offset voltage to Pin 9 of the AD588. First, the code 1000 . . . 0000 is loaded into the DACA latch and the pin driver output is set to the DACA output. The V_{OFFSET} voltage is adjusted until 0 V appears between the pin driver output and DUTGND. This causes both $V_{REF}(+)$ and $V_{REF}(–)$ to be offset with respect to GND by an amount equal to V_{OFFSET}. However, the output of the pin driver will vary from –10 V to +10 V with respect to DUTGND as the DAC input code varies from 000 . . . 000 to 111 . . . 111. The V_{OFFSET} voltage is also applied to the DUTGND pins. When a clear is performed on the AD7841, the output of the pin driver will be 0 V with respect to DUTGND.

The other AD588 is used to provide a reference voltage for DACs G and H. These provide the reference voltages for the window comparator shown in the diagram. Note that Pin 9 of this AD588 is connected to Device GND. This causes $V_{REF}(+)GH$ and $V_{REF}(–)GH$ to be referenced to Device GND. As DAC G and DAC H input codes vary from 000 . . . 000 to 111 . . . 111, $V_{OUT}G$ and $V_{OUT}H$ vary from –10 V to +10 V with respect to Device GND. Device GND is also connected to DUTGND. When the AD7841 is cleared, $V_{OUT}G$ and $V_{OUT}H$ are cleared to 0 V with respect to Device GND.

Programmable Reference Generation for the AD7841 in an ATE Application

The AD7841 is particularly suited for use in an automated test environment. The reference input for the AD7841 octal 14-bit DAC requires three differential references for the eight DACs. Programmable references may be a requirement in some ATE applications as the offset and gain errors at the output of a DAC can be adjusted by varying the voltages on the reference pins of the DAC. To trim offset errors, the DAC is loaded with the digital code 000 . . . 000 and the voltage on the $V_{REF}(–)$ pin is adjusted until the desired negative output voltage is obtained. To trim out gain errors, first the offset error is trimmed. Then the DAC is loaded with the code 111 . . . 111 and the voltage on the $V_{REF}(+)$ pin is adjusted until the desired full-scale voltage minus one LSB is obtained.

It is not uncommon in ATE design, to have other circuitry at the output of the AD7841 that can have offset and gain errors of up to say ±300 mV. These offset and gain errors can be easily removed by adjusting the reference voltages of the AD7841. The AD7841 uses nominal reference values of ±5 V to achieve an output span of ±10 V. Since the AD7841 has a gain of two from the reference inputs to the DAC output, adjusting the reference voltages by ±150 mV will adjust the DAC offset and gain by ±300 mV.

There are a number of suitable 8- and 10-bit DACs available that would be suitable to drive the reference inputs of the AD7841, such as the AD7804, a quad 10-bit digital-to-analog converter with serial load capabilities. The voltage output from this DAC is in the form of $V_{BIAS} \pm V_{SWING}$ and rail-to-rail operation is achievable. The voltage reference for this DAC can be internally generated or provided externally. This DAC also contains an 8-bit SUB DAC which can be used to shift the complete transfer function of each DAC around the V_{BIAS} point. This can be used as a fine trim on the output voltage. In this application two AD7804s are required to provide programmable reference capability for all eight DACs. One AD7804 is used to drive the $V_{REF}(+)$ pins and the second package used to drive the $V_{REF}(–)$ pins.

Another suitable DAC for providing programmable reference capability is the AD8803. This is an octal 8-bit TRIMDAC® and provides independent control of both the top and bottom ends of the TRIMDAC. This is helpful in maximizing the resolution of devices with a limited allowable voltage control range.

TRIMDAC is a registered trademark of Analog Devices, Inc.

The AD8803 has an output voltage range of GND to V_{DD} (0 V to 5 V). To trim the $V_{REF}(+)$ input, the appropriate trim range on the AD8803 DAC can be set using the V_{REFL} and V_{REFH} pins allowing 8 bits of resolution between the two points. This will allow the $V_{REF}(+)$ pin to be adjusted to remove gain errors.

To trim the $V_{REF}(-)$ voltage, some method of providing a trim voltage in the required negative voltage range is required. Neither the AD7804 or the AD8803 can provide this range in normal operation as their output range is 0 V to 5 V. There are two methods of producing this negative voltage. One method is to provide a positive output voltage and then to level shift that analog voltage to the required negative range. Alternatively these DACs can be operated with supplies of 0 V and –5 V, with the V_{DD} pin connected to 0 V and the GND pin connected to –5 V. Now these can be used to provide the negative reference voltages for the $V_{REF}(-)$ inputs on the AD7841. However, the digital signals driving the DACs need to be level-shifted from the 0 V to +5 V range to the –5 V to 0 V range. Figure 13 shows a typical application circuit to provide programmable reference capabilities for the AD7841.

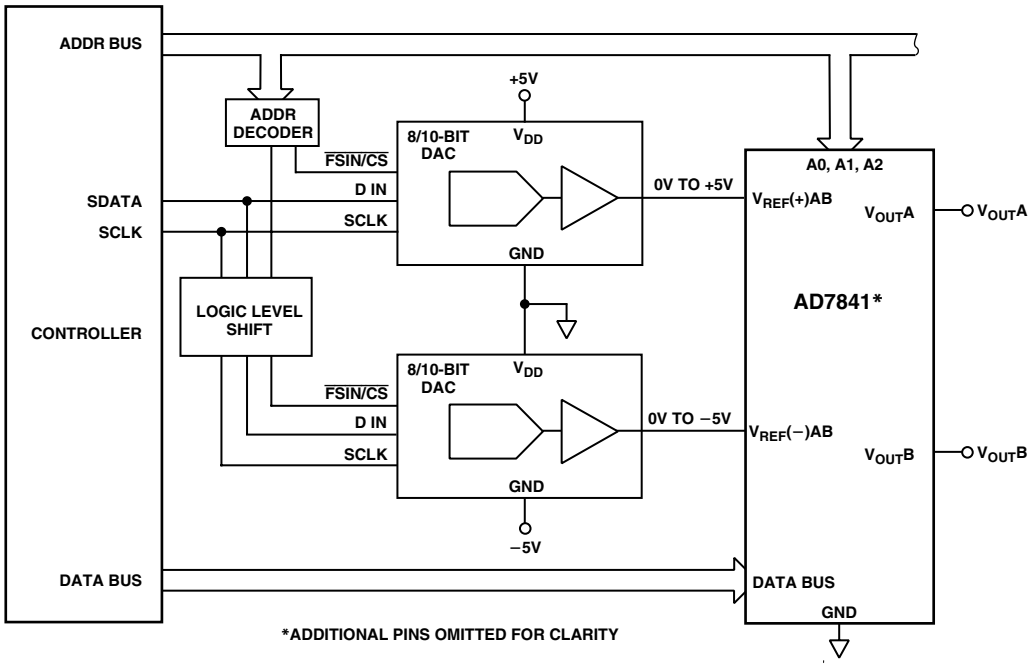
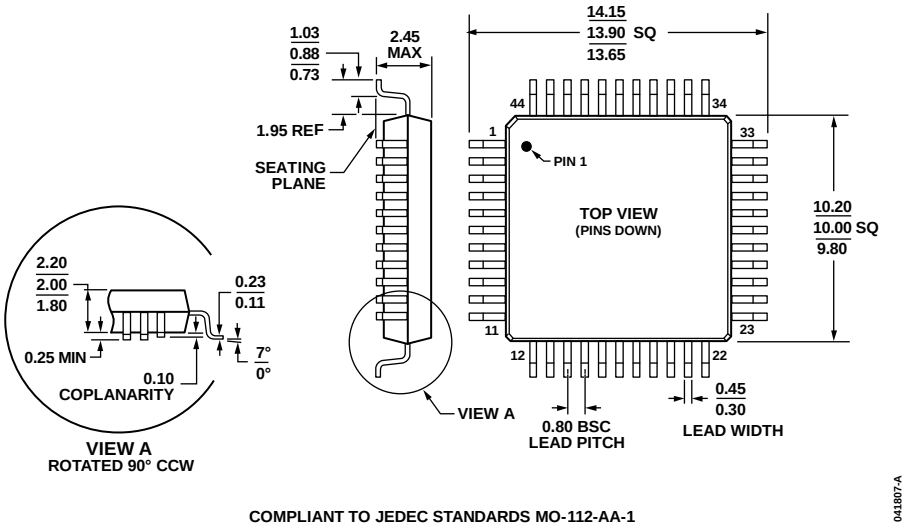


Figure 13. Programmable Reference Generation for the AD7841

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-112-AA-1

Figure 14. 44-Lead Metric Quad Flat Package [MQFP]
(S-44-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Linearity Error (LSBs)	DNL (LSBs)	Temperature Range	Package Description	Package Option
AD7841ASZ	±4	−0.9/+2	−40°C to +85°C	44-Lead Metric Quad Flat Package [MQFP]	S-44-2
AD7841ASZ-REEL	±4	−0.9/+2	−40°C to +85°C	44-Lead Metric Quad Flat Package [MQFP]	S-44-2
AD7841BSZ	±2	±1	−40°C to +85°C	44-Lead Metric Quad Flat Package [MQFP]	S-44-2
AD7841BSZ-REEL	±2	±1	−40°C to +85°C	44-Lead Metric Quad Flat Package [MQFP]	S-44-2
EVAL-AD7841EBZ				Evaluation Board	

[1] Z = RoHS Compliant Part.

REVISION HISTORY

1/11—Rev. A to Rev. B

Changes to Absolute Maximum Ratings, Lead Temperature.....4
Updated Outline Dimensions.....13
Moved and Changes to Ordering Guide.....13

D09645-0-1/11(B)

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