74HC2G08; HCT2G08

Dual 2-input AND gate Rev. 6 — 1 November 2018

Product data sheet

1. General description

The 74HC2G08; 74HCT2G08 is a dual 2-input AND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of $V_{\rm CC}$.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC2G08: CMOS level
 - For 74HCT2G08: TTL level
- · Symmetrical output impedance
- · High noise immunity
- · Low power dissipation
- · Balanced propagation delays
- · Multiple package options
- ESD protection:
 - HBM JESD22-A114E exceeds 2 000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74HC2G08DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads;	SOT505-2				
74HCT2G08DP			body width 3 mm; lead length 0.5 mm					
74HC2G08DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads;	SOT765-1				
74HCT2G08DC			body width 2.3 mm					

4. Marking

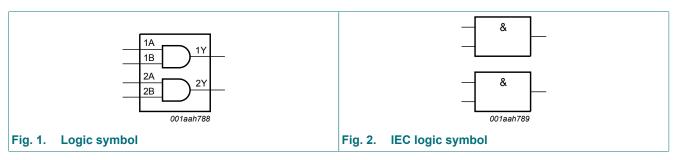
Table 2. Marking code

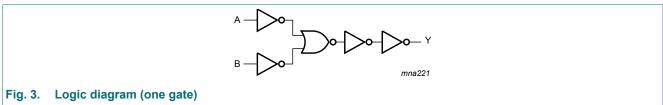
Type number	Marking code[1]
74HC2G08DP	H08
74HCT2G08DP	T08
74HC2G08DC	H08
74HCT2G08DC	Т08

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.



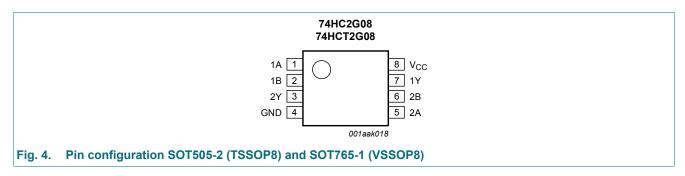
5. Functional diagram





6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Input		Output
nA	nB	nY
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	[1]	-	25	mA
I _{CC}	supply current		[1]	-	50	mA
I _{GND}	ground current		[1]	-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P_D	dynamic power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	300	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter Conditions		74HC2G08			74HCT2G08			Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
	fall rate	V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

^[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K. For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		°C to +8	5°C	-40 °C to +125 °C		Unit	
			Min	Typ[1]	Max	Min	Max	1	
74HC2G	08								
V _{IH}	HIGH-level input	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V	
	voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V	
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V	
V _{IL}	LOW-level input	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V	
	voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V	
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V	
V _{OH}	HIGH-level output	$V_I = V_{IH}$ or V_{IL}							
	voltage	$I_{\rm O}$ = -20 μ A; $V_{\rm CC}$ = 2.0 V	1.9	2.0	-	1.9	-	V	
		$I_{\rm O}$ = -20 μ A; $V_{\rm CC}$ = 4.5 V	4.4	4.5	-	4.4	-	V	
		I_{O} = -20 μ A; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	V	
		I_{O} = -4.0 mA; V_{CC} = 4.5 V	4.13	4.32	-	3.7	-	V	
		I_{O} = -5.2 mA; V_{CC} = 6.0 V	5.63	5.81	-	5.2	-	V	
V _{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}							
	voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V	
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V	
	I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V		
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V	
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V	
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±1.0	-	±1.0	μA	
I _{CC}	supply current	per input pin; $V_1 = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	10	-	20	μΑ	
Cı	input capacitance		-	1.5	-	-	-	pF	
74HCT2	G08						1		
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V	
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V	
V _{OH}	HIGH-level output	$V_I = V_{IH}$ or V_{IL}						+	
	voltage	I_{O} = -20 μ A; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V	
		I_{O} = -4.0 mA; V_{CC} = 4.5 V	4.13	4.32	-	3.7	-	V	
V _{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}							
	voltage	I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V	
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V	
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	-	±1.0	μA	
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	10	-	20	μA	
Δl _{CC}	additional supply current	per input; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V};$ $V_1 = V_{CC} - 2.1 \text{ V};$ $I_0 = 0 \text{ A}$	-	-	375	-	410	μΑ	

Symbol	Parameter	Conditions	-40 °C to +85 °C		o +85 °C -40 °C to +125 °C		+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
Cı	input capacitance		-	1.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions		-40	°C to +85	S°C	-40 °C t	Unit	
			Min	Typ[1]	Max	Min	Max		
74HC2G	08								
t _{pd}	propagation delay	nA and nB to nY; see Fig. 5	[2]						
		V _{CC} = 2.0 V		-	26	95	-	110	ns
		V _{CC} = 4.5 V		-	9	19	-	22	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	9	-	-	-	ns
		V _{CC} = 6.0 V		-	8	16	-	20	ns
t _t	transition time	see Fig. 5	[3]						
		V _{CC} = 2.0 V		-	20	95	-	125	ns
		V _{CC} = 4.5 V		-	7	19	-	25	ns
		V _{CC} = 6.0 V		-	6	16	-	20	ns
C _{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}$	[4]	-	10	-	-	-	pF
74HCT2	G08								
t _{pd}	propagation delay	nA and nB to nY; see Fig. 5	[2]						
		V _{CC} = 4.5 V		-	14	30	-	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	14	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 5</u>	[3]	-	7	19	-	22	ns
C _{PD}	power dissipation capacitance	$V_1 = \text{GND to V}_{CC} - 1.5 \text{ V}$ [4]		-	10	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_t is the same as t_{TLH} and t_{THL} .
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} x V_{CC}^2 x f_i x N + \Sigma (C_L x V_{CC}^2 x f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

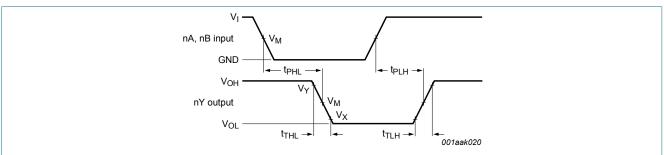
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of outputs.

11.1. Waveforms and test circuit



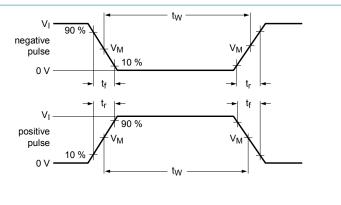
Measurement points are given in Table 9.

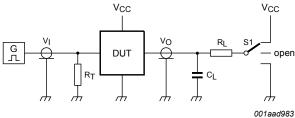
 $\ensuremath{V_{OL}}$ and $\ensuremath{V_{OH}}$ are typical output voltage levels that occur with the output load.

Fig. 5. Propagation delay data input (nA, nB) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Туре	Input	Output			
	V _M	V _M	V _X	V _Y	
74HC2G08	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}	
74HCT2G08	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}	





Test data is given in Table 10.

Definitions for test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 $\ensuremath{\text{C}_{\text{L}}}$ = Load capacitance including jig and probe capacitance.

 R_L = Load resistance.

S1 = Test selection switch.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Туре	Input		Load	S1 position	
	V _I	t _r , t _f	CL	R_L	t _{PHL} , t _{PLH}
74HC2G08	GND to V _{CC}	≤ 6 ns	15 pF, 50 pF	1 kΩ	open
74HCT2G08	GND to 3 V	≤ 6 ns	15 pF, 50 pF	1 kΩ	open

12. Package outline

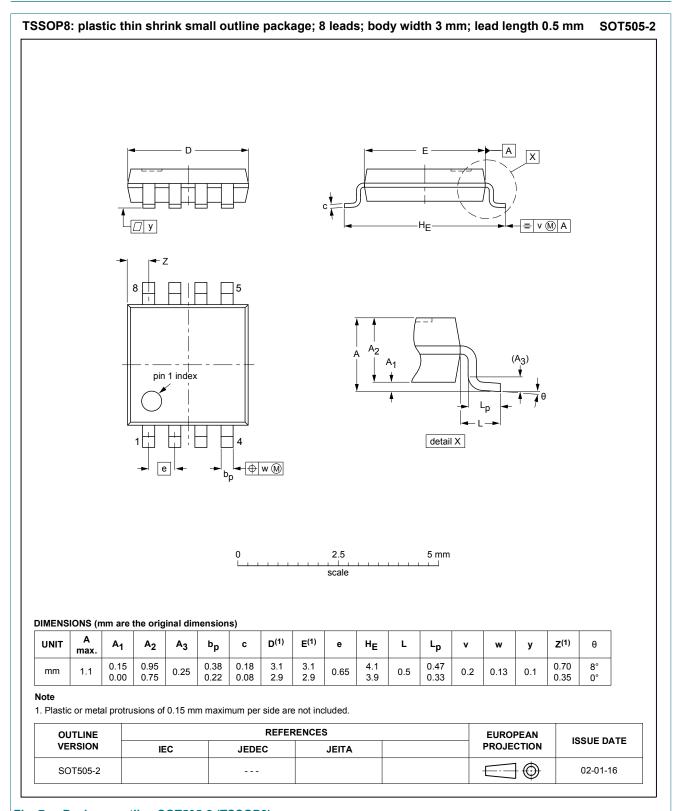


Fig. 7. Package outline SOT505-2 (TSSOP8)

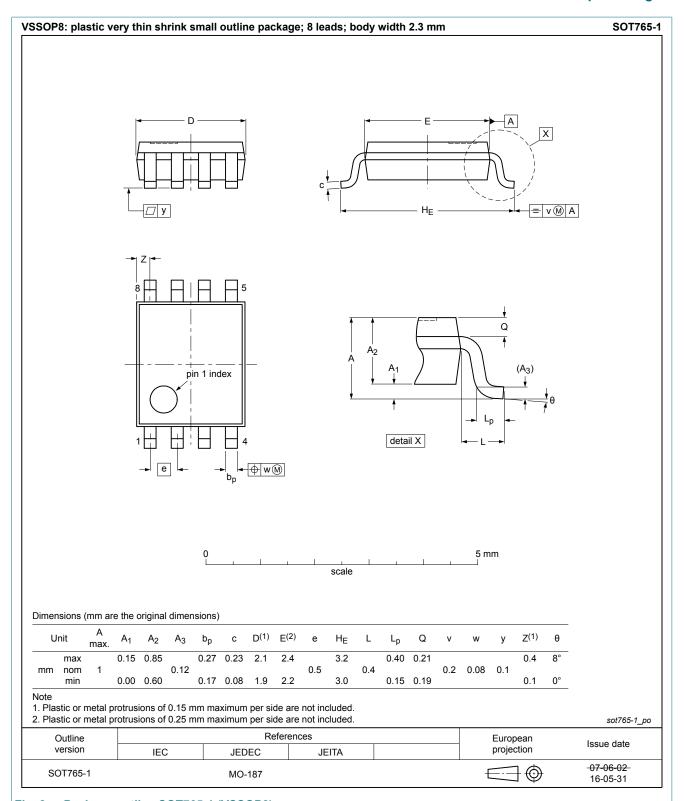


Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74HC_HCT2G08 v.6	20181101	Product data sheet	-	74HC_HCT2G08 v.5		
Modifications:	Nexperia. • Legal texts ha	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC2G08GD and 74HCT2G08GD (SOT996-2/XSON8) removed. 				
74HC_HCT2G08 v.5	20131008	Product data sheet	-	74HC_HCT2G08 v.4		
Modifications:	For type number	For type numbers 74HC2G08GD and 74HCT2G08GD XSON8U has changed to XSON8.				
74HC_HCT2G08 v.4	20090507	Product data sheet	-	74HC_HCT2G08 v.3		
74HC_HCT2G08 v.3	20031022	Product specification	-	74HC_HCT2G08 v.2		
74HC_HCT2G08 v.2	20030203	Product specification	-	74HC_HCT2G08 v.1		
74HC_HCT2G08 v.1	20020710	Product specification	-	-		

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А