MIC2130/1

High Voltage Synchronous Buck Control IC with Low EMI Option

General Description

The MIC2130/1 is a high voltage input PWM synchronous buck controller IC. It is a voltage mode controller with a fast hysteretic control loop (FHyCL) employed during fast line and load transients. The internal gate drivers are designed to drive high current MOSFETs.

The MIC2130/1 can produce output voltages down to 0.7V with input voltage from 8V to 40V. The MIC2130 family of control ICs implements fixed frequency PWM control. The active anti-shoot through drive scheme means a wide range of external MOSFETs may be used while maintaining optimum efficiency.

The MIC2131 is the fully functional version of the family and implements a new feature to minimize EMI. This function is critical for systems that need to be compliant with EMI standards throughout the world.

The MIC2130/1 is available in small size 16-pin 4mm x 4mm MLF® package, as well as 16-pin e-TSSOP at a junction temperature range of –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

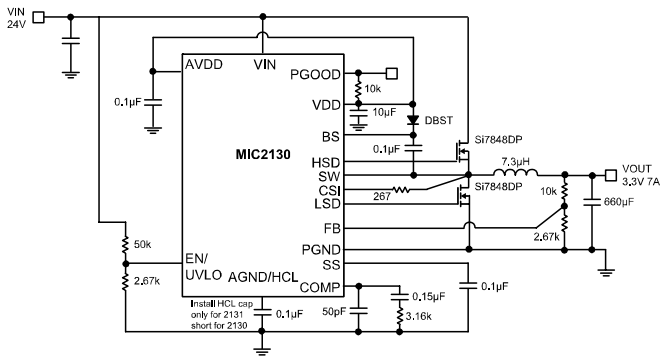
Features

- 8V to 40V input voltage range
- Adjustable output voltages down to 0.7V
- LOW EMI option MIC2131
- Fixed 150kHz and 400kHz frequency options
- Excellent line and load regulation due to fast hysteretic control loop during transients
- Adaptive gate drive allows efficiencies over 95%
- Programmable current limit with no sense resistor
- Senses low-side MOSFET current
- Internal drivers allow 15A output current
- Power Good output allow simple sequencing
- Programmable soft-start pin
- 100% increase in current limit (MIC2131)
- Output over-voltage protection
- Programmable Input UVLO
- 16-pin e-TSSOP and 16-pin 4mm x 4mm MLF®
- Junction temperature range of –40°C to +125°C

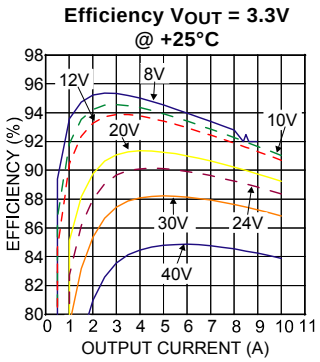
Applications

- Industrial/Medical DC/DC point of use power
- Printer head drivers
- Automotive Systems
- Telecom systems
- LCD/ Plasma TV
- Gaming Machines

Typical Application



MIC2130/1 High Input Voltage Converter



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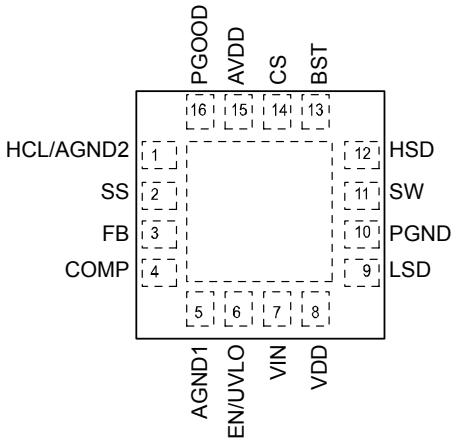
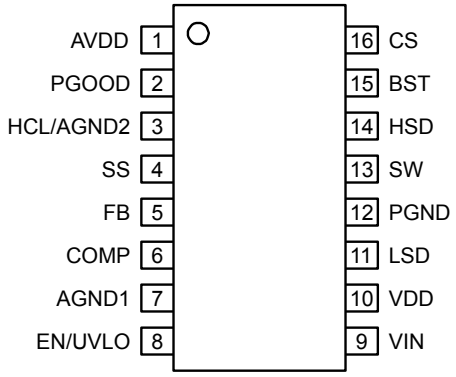
Ordering Information

Part Number	Frequency	Output Voltage	Low EMI	Junction Temp. Range	Package	Lead Finish
MIC2130-1YML	150kHz	Adj.	No	–40° to +125°C	16-Pin 4x4 MLF®	Pb-Free
MIC2130-4YML	400kHz	Adj.	No	–40° to +125°C	16-Pin 4x4 MLF®	Pb-Free
MIC2130-1YTSE	150kHz	Adj.	No	–40° to +125°C	16-Pin e-TSSOP	Pb-Free
MIC2130-4YTSE	400kHz	Adj.	No	–40° to +125°C	16-Pin e-TSSOP	Pb-Free
MIC2131-1YML	150kHz	Adj.	Yes	–40° to +125°C	16-Pin 4x4 MLF®	Pb-Free
MIC2131-4YML	400kHz	Adj.	Yes	–40° to +125°C	16-Pin 4x4 MLF®	Pb-Free
MIC2131-1YTSE	150kHz	Adj.	Yes	–40° to +125°C	16-Pin e-TSSOP	Pb-Free
MIC2131-4YTSE	400kHz	Adj.	Yes	–40° to +125°C	16-Pin e-TSSOP	Pb-Free

Pin Configuration



16-Pin 4mm x 4mm MLF® (ML)



16-Pin e-TSSOP (TS)

Pin Description

Pin Number MLF-16	Pin Number e-TSSOP-16	Pin Name	Pin Function
1	3	HCL* AGND2	High Current Limit (Output): The capacitor on this pin sets the duration of time so that the current limit will be set to 200% of its nominal set current. AGND2 for MIC2130
2	4	SS	Soft Start (Output): Active at Power-up, Enable, and Current Limit recovery.
3	5	FB	Feedback (Output): Input to error amplifier. Regulates to 0.7V.
4	6	COMP	Compensation (Output): Pin for external compensation.
5	7	AGND1	Analog Ground.
6	8	EN/UVLO	Enable (Input): Logic low turns the IC off. When the voltage drops below the band gap reference voltage of the IC the device turns off. This accurate threshold allows the pin to be used as an accurate under voltage lockout.
7	9	VIN	Supply Voltage (Input): 8V to 40V.
8	10	VDD	5V Internal Linear Regulator from VIN. When VIN is <8V, this regulator operates in drop-out mode. Connect external bypass capacitor.
9	11	LSD	Low-Side Drive (Output): High-current driver output for external low-side MOSFET.
10	12	PGND	Power Ground: High current return for ext. Low side driver.
11	13	SW	Switch Node (Output): High current output driver return.
12	14	HSD	High-Side Drive (Output): High current output-driver for ext. high-side MOSFET.
13	15	BST	Boost (Output): Provides voltage for high-side MOSFET driver. The gate drive voltage is higher than the source voltage by VDD minus a diode drop.
14	16	CS	Current Sense (Output): Current-limit comparator non inverting input. The current limit is sensed across the low-side FET during the OFF time. Current limit is set by the resistor in series with the CS pin.
15	1	AVDD	Analog Supply Voltage (internal 5V LDO): Connect external By pass capacitor.
16	2	PGOOD	Power Good (Output): High output when VOUT > 90% nominal.

Note: * indicates that is only used on MIC2131.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) 42V
Boot Strapped Voltage (V_{BST}) ..... V_{IN} + 5V
Logic Inputs 6.5V
EN Input 42V
Ambient Storage Temperature (T_s) ..... –65°C to +150°C
ESD Rating[3] 1.5kV

Operating Ratings[2]

Supply Voltage ($V_{IN1,}$ V_{IN2}) ..... +8V to +40V
Output Voltage Range ..... 0.7V to 0.85V_{IN}
Junction Temperature (T_J) ..... –40°C ≤ T_J ≤ +125°C
Package Thermal Resistance
e-TSSOP (θ_{JA}) ..... 97.5°C/W
e-TSSOP (θ_{JC}) ..... 29.9°C/W
4x4 MLF-16 (θ_{JA}) ..... 50.6°C/W
4x4 MLF-16 (θ_{JC}) ..... 15.8°C/W

Electrical Characteristics[4]

T_J = 25°C; V_{EN} = V_{IN} = 24V; Frequency = 150kHz; V_{OUT} = 3.3V, unless otherwise specified.
Bold values indicate –40°C≤ T_J ≤ +125°C.

Parameter	Condition	Min	Typ	Max	Units
V_{IN}, $V_{EN/UVLO}$, V_{DD} Supply					
Total Supply Current, PWM Mode Supply Current	V_{FB} = 0.7V; Comp = 3V (Outputs switching but excluding external MOSFET gate current.)		4	**7.5**	mA
Shutdown Current	V_{EN} = 0V; V_{IN} = 12V		180	**300**	µA
V_{EN}/UVLO Turn-On Threshold			1.1	**1.3**	V
V_{EN}/UVLO Turn-Off Threshold		**0.7**	1.0		V
V_{IN} UVLO Hysteresis			100		mV
Internal Bias Voltages (AV_{DD},) (I_{DD} = 50mA)		4.6	5	5.3	V
Oscillator/PWM Section					
PWM Frequency	MIC2130/1-1	130	150	170	kHz
PWM Frequency	MIC2130/1-4	360	400	440	kHz
Maximum Duty Cycle	MIC2130/1-1	**92**			%
Maximum Duty Cycle	MIC2130/1-4	**80**			%
Minimum On-Time	**Note 5**		50		ns
Regulation					
Feedback Voltage Reference	(±2%) -40°C to +125°C	**686**	700	**714**	mV
Feedback Bias Current			300	**1000**	nA
Output Voltage Line Regulation	V_{IN} = 8V – 40V		0.03		%/V
Output Voltage Load Regulation	1A ≤ I_{OUT} ≤ 10A		0.5		%
Error Amplifier (each channel)					
DC Gain			70		dB
Output Impedance			2		MΩ
Transconductance		1.2	1.6	2.5	ms
Output Over voltage Protection					
V_{FB} Threshold	(Latches LSD High)	**110**	115	**120**	%Nom
Delay Blanking Time			1		µs
Soft Start/HCL					
Internal Soft Start Source Current		**1**	2.75	**5**	µA
HCL (MIC2131) Pin Voltage High	I_{LIMIT} set to 200% when HCL charges to2.4V		2.4		V

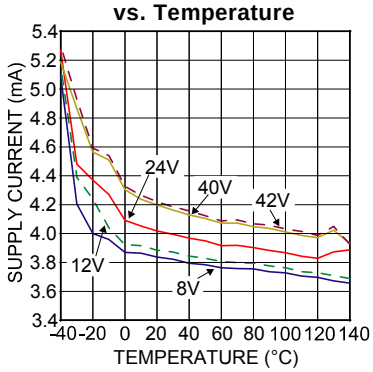
Parameter	Condition	Min	Typ	Max	Units
HCL Low	I_{LIMIT} set to normal when HCL is low		0.5		V
HCL Pin Charge Up Current			2.9		µA
HCL Pin Charge Down Current			12		µA
LOW/EMI					
Frequency Dither Range	Of center freq		±12		%
Current Sense					
CS Over Current Trip Point Program Current		170	200	230	µA
Temperature Coefficient			+2300		ppm/°C
CS Comparator Sense Threshold	(Senses drop across low-side FET)	**–5**	0	**+5**	mV
Power Good					
V_{FB} Threshold		**86**	90	**93**	%Nom
PGOOD Voltage Low	V_{DD} = 5.0V; V_{FB} = 0V; I_{PGOOD} = 1mA		0.1	**0.5**	V
Gate Drivers					
Rise/Fall Time	Into 3000pF Source Sink		 23 16		 ns ns
Output Driver Resistance	HSD: Source; V_{DD} = 5V HSD: Sink; V_{DD} = 5V LSD: Source; V_{DD} = 5V LSD: Sink; V_{DD} = 5V		2 1.47 2.2 2.1		Ω Ω Ω Ω
Driver Non-Overlap Time (Adaptive)	**Note 4**	40	60		ns
Thermal Shutdown Threshold	T_J Increasing		155		°C
	T_J Decreasing		142		°C

Notes:

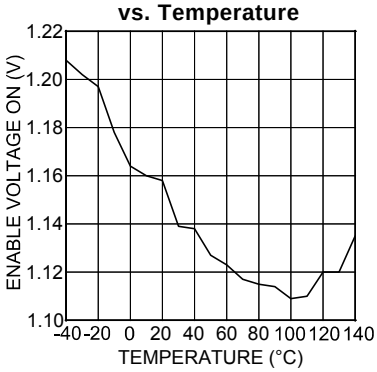
1. Exceeding the absolute maximum rating may damage the device.
2. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(Max)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
3. Devices are ESD sensitive. Handling precautions recommended.
4. Guaranteed by design.
5. Minimum on-time before automatic cycle skipping begins.

Typical Characteristics

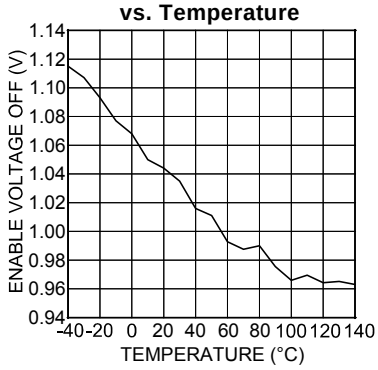
Supply Current vs. Temperature



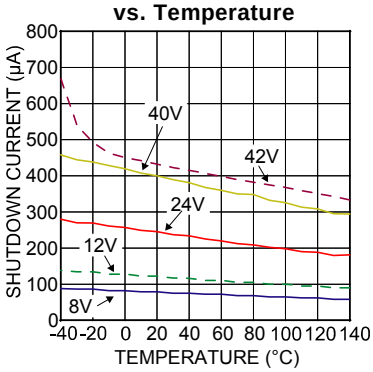
Enable Voltage On vs. Temperature



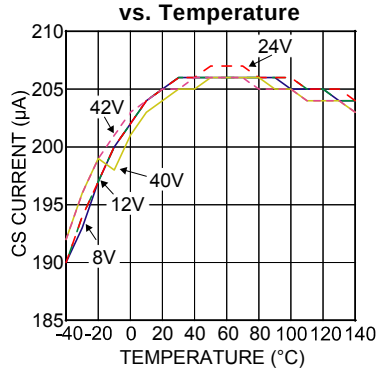
Enable Voltage Off vs. Temperature



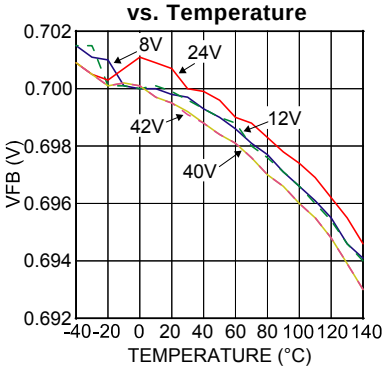
Shutdown Current vs. Temperature



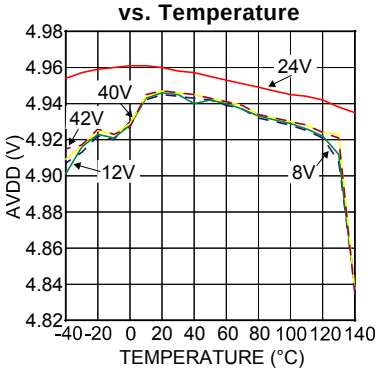
CS Current vs. Temperature



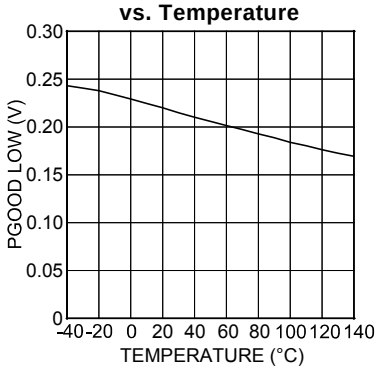
V_{FB} vs. Temperature



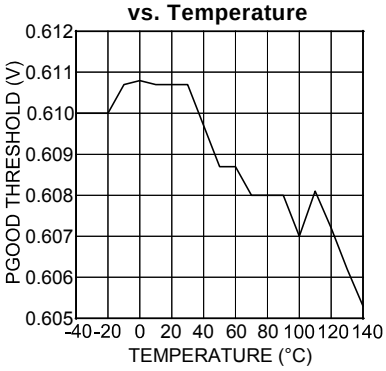
AV_{DD} vs. Temperature



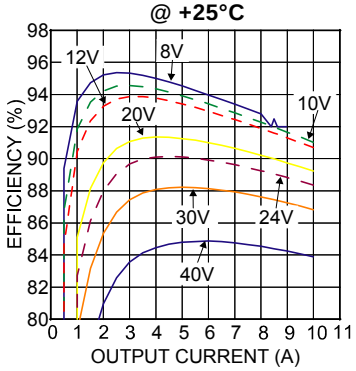
P_{GOOD} Low @ I_{PG} = 1mA vs. Temperature



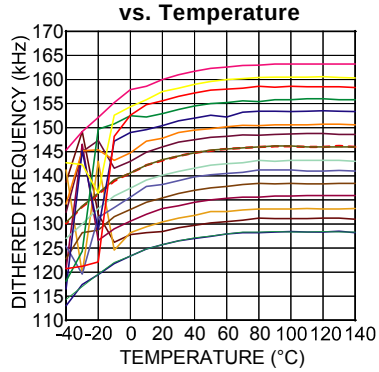
P_{GOOD} Threshold vs. Temperature



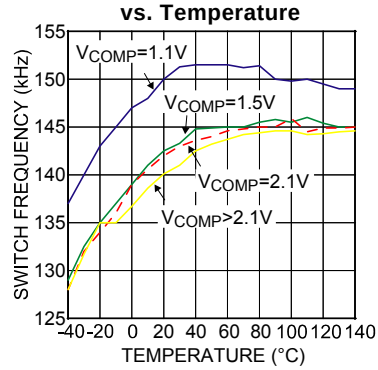
Efficiency V_{OUT} = 3.3V @ +25°C



Dithered (Spread) Frequency vs. Temperature

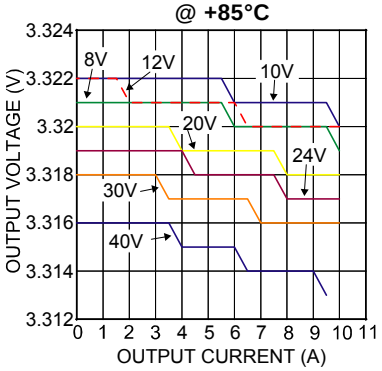


Switch Frequency vs. Temperature

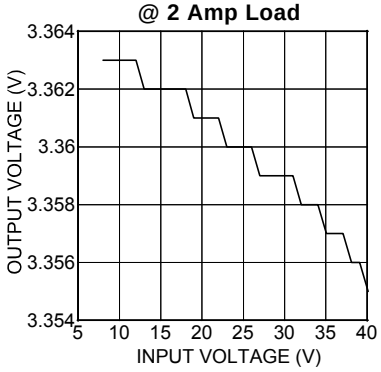


Typical Characteristics (continued)

Load Regulation @ +85°C



Line Regulation @ 2 Amp Load



Functional Diagram

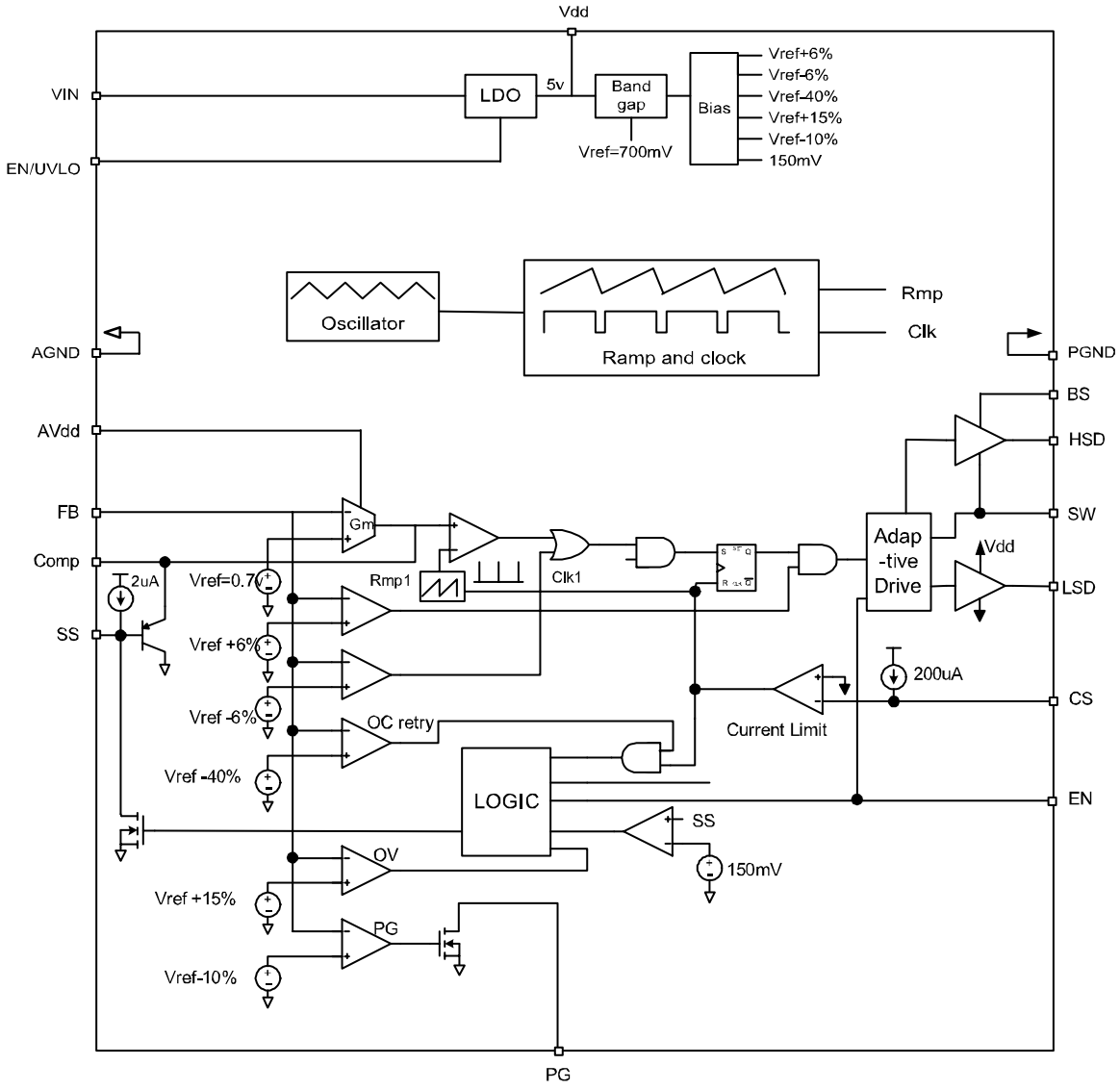


Figure 1. MIC2130/1 Block Diagram

Functional Description

The MIC2130/31 is a voltage mode synchronous buck controller built for optimum speed and efficiency. It is designed for wide input voltage range and for high output power buck converters. Figure 1 shows the block diagram.

The control loop has two stages of regulation. During steady-state to medium output disturbances, the loop operates in fixed frequency, PWM mode while (gm loop), during a large output voltage disturbance (~±6% nominal), the loop becomes hysteretic; meaning that for a short period, the switching MOSFETs are switched on and off continuously until the output voltage returns to it's nominal level. This maximizes transient response for large load steps, while nominally operating in fixed frequency PWM mode. Voltage mode control is used to allow for maximum flexibility and maintains good transient regulation. The operating input voltage range is 8V to 40V and output can be set from 0.7V up to $0.85*V_{IN}$. Start-up surges are prevented using built in soft start circuitry as well as resistor-less (LSD RDS_{ON} is used to sense load current) current sensing for overload protection. Other protection features include UVLO, over voltage latch off protection, Power good signal.

Theory of Operation

A voltage divider monitors the output voltage of the converter then sensed at the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to the internal 0.7V reference and the two inputs are compared to produce an analog error voltage. This error voltage is then fed into the non-inverting input of the PWM comparator and compared to the voltage ramp (1.1V to 2.1V) to create the PWM pulses. The PWM pulses propagate through to the MOSFET drivers which drive the external MOSFETs to create the power switching waveform at the set D (duty cycle). This is then filtered by a power inductor and low ESR capacitor to produce the output voltage where $V_{OUT} \approx D*V_{IN}$. As an example, due to a load increase or an input voltage drop, the output voltage will instantaneously drop. This will cause the error voltage to rise, resulting in wider pulses at the output of the PWM comparator. The higher Duty Cycle power switching waveform will cause an associated rise in output voltage and will continue to rise until the feedback voltage is equal to the reference and the loop is again in equilibrium. As with any control system, it is necessary to compensate this feedback loop (by selecting the R and C values at the comp pin) in order to keep the system stable. One of the tradeoffs for stability is reduced transient regulation performance. However, the MIC2130/31 has an additional feature to correct this problem. The MIC2130/31 family features a fast hysteretic control loop (FHyCL) which bypasses the gm amp and the feedback compensation network during fast line and load transients.

The fast hysteretic control loop (FHyCL) operates during large transients to provide excellent line and load regulation. Hysteretic mode is invoked when the output voltage is detected to be ±6% of its regulated value. If the input voltage step or output load step is large enough to cause a 6% deviation in V_{OUT}, then the additional hysteretic control loop functions to return the output voltage to its nominal set point in the fastest time possible. This is limited only by the time constant of the power inductor and output capacitor (an order of magnitude faster than the gm loop). This scheme is not used during normal operation because it creates switching waveforms whose frequency is dependant on V_{IN}, passive component values and load current. Due to its large noise spectrum it is only used during surges to keep switching noise at a known, fixed frequency.

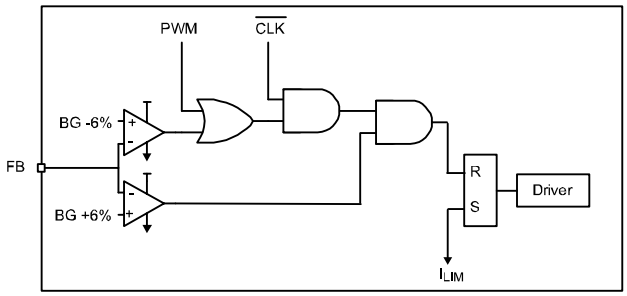


Figure 2. Hysteric Block Diagram

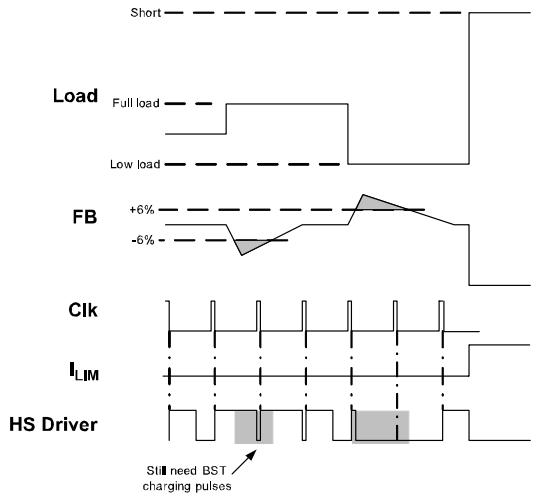


Figure 3. Hysteric Waveforms

Soft Start

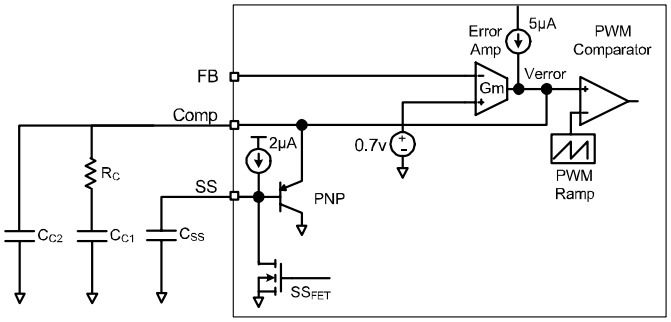


Figure 4. Soft Start Circuit

At startup, the Soft-start MOSFET (SS_{FET}) is released and C_{SS} starts to charge at the rate $dV_{SS}/dt–2\mu A/C_{SS}$. The PNP transistor's emitter (COMP) starts to track V_{SS} (plus a junction voltage ≈0.65). When (COMP) reaches the lower end of the PWM ramp voltage at 1.10V, switching pulses will begin to drive the power MOSFETs. This voltage rise continues on the COMP pin until the control loop reaches the regulation point. During this soft start period, the gate drive pulses to the MOSFET will start at the minimum pulse width and increase up to the duty cycle D required for regulation. The COMP voltage can be anywhere from 1.1V to 2.1V which corresponds to a duty cycle D of 0-85%. V_{SS} will however, continue to rise as the PNP base-emitter junction becomes reverse biased. The SS pin is allowed to rise to 2.5V (four diode drops) max to allow fast response to fault conditions. During large over current or short circuit conditions, i.e., where current limit is detected and V_{OUT} is <60% of nominal, the SS_{FET} is momentarily switched on. This discharges C_{SS} to ~150mV at which point, it re-starts the soft start cycle once again. During soft start, hysteretic comparators are disabled.

Duty Cycle D can be written in terms of V_{COMP}

$D = (0.85) \times V_{COMP} – (0.935)$ or $V_{COMP} = (D + 0.935)/0.85$

Example: $V_{IN} = 12V$; $V_{OUT} = 3.3V$; $D = V_{OUT}/V_{IN} = 0.275$

$V_{COMP} = 1.424V$; i.e. the steady-state DC Value of V_{COMP} when D = 0.275

T1 is the time for V_{COMP} to charge up to 1.1V, therefore, V_{SS} is one diode drop below V_{COMP}.

T2 is the time for V_{COMP} to charge up to (D + 0.935)/ 0.85 + 1.1V.

Soft Start time = T1 + T2

Where

T1 = (1.1-Vdiode) x C_{SS}/2µA; the time until output pulsing starts at minimum duty.

And,

T2 = (1/0.85) x D x C_{SS}/ 2µA; the time until output pulsing increases to D.

The compensation capacitors at the COMP pin (C_{COMP} = Cc1+Cc2 in Figure 4) will also need to charge up to V_{COMP}. This charging time starts as soon as MOSFET (SS_{FET}) is released. Depending upon the size of the C_{COMP}, the charging time could be greater than T1+T2. C_{COMP} could be used for the Soft Start cap by leaving SS pin open.

Tc_{COMP} = (1/0.85) x D x C_{COMP}/5µA: The time until output pulsing increases to D.

Protection

There exits four different types of output protection.

1. Output "hard short" over current
2. Output "soft short" over current
3. Output under voltage
4. Output over voltage

Current Limit

The MIC2130/31 uses the RDS_{ON} of the low-side MOSFET to sense overcurrent conditions. The lower MOSFET is used because it displays much lower parasitic oscillations during switching then the upper MOSFET. Using the low-side MOSFET RDS_{ON} as a current sense is an excellent method for circuit protection. This method will avoid adding cost, board space and power losses taken by discrete current sense resistors.

Hard Short

Generally, the MIC2130/31 current limit circuit acts to provide a fixed maximum output current until the resistance of the load is so low that the voltage across it is no longer within regulation limits. At this point (60% of nominal output voltage), the part employs Hiccup mode. During Hiccup mode, the output pulses stop and the soft start cap is discharged and soft start mode begins. After the soft start time, if the output voltage is still 60% low, then the process repeats again and continues until the short is removed. Hard short current mode is initiated to protect down stream loads from excessive current and also reduces overall power dissipation in the PWM converter components during a fault.

Soft Short

Before "Hard Short" mode (also called "hiccup mode") occurs "soft short" current limiting is provided to prevent system shutdown or disturbance if the overload is only marginal. When the load current exceeds the current limit by only a few ma for a short time (milliseconds) then the hard short mode is not desired. Instead, the "Soft Short" loop is used. When the current limit comparator senses an over current it then starts to discharge the SS Cap with a 40µA current source. The current limit comparator gets reset every cycle so if the short still exist during the next cycle then the SS cap will continue to get discharged with the 40µA current source. The comp pin follows the SS pin (Figure 4) and the gm control loop will lower the output voltage accordingly for as long as the short exists. So, instead of shutting down the output as in a hard short, the output is gently and slightly reduced until the over current condition discontinues. If however the short increase to the point of lowering the output to 60%, then hard short will result. The fast hysteretic control loop (FHyCL) is initiated by a 6% drop in output voltage and it is not desired during an over current condition therefore, the FHyCL feature will

be disabled during an over current condition.

Under Voltage

A ±6% comparator monitors the output voltage and will initiate the fast hysteretic control loop (FHyCL) to regulate the output. A comparator monitors the output voltage and sets PGOOD true when the output reaches 90% of the regulated output.

Over Voltage

If the voltage at the FB pin is detected to be 15% higher than nominal for >2µs, then the controller is stopped from switching immediately and latched off. Switching can be re-started by taking EN below the channel's enable threshold and re-enabling or re-cycling power to the IC.

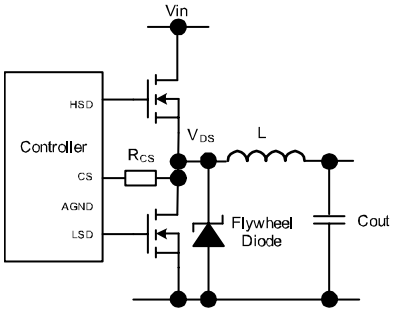


Figure 5.

During the normal operation of a synchronous Buck regulator, as the lower MOSFET is switched on, its drain voltage will become negative with respect to ground as the inductor current continues to flow from Source-to-Drain. This negative voltage is proportional to output load current, inductor ripple current and MOSFET RDS_{ON}.

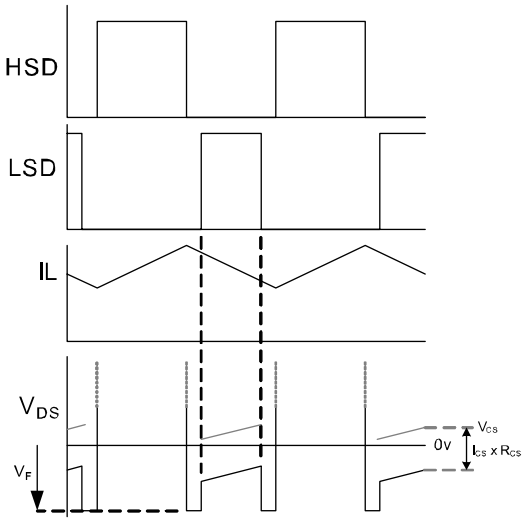


Figure 6.

The larger the inductor current, the more negative V_{DS} becomes. This is utilized for the detection of over current by passing a known fixed current source (200µA) through a resistor R_{CS} which sets up an offset voltage such that when 200µA x R_{CS} = I_{DRAIN} x RDS_{ON} the MIC2130/31's over current trigger is set. This disables the next high side gate drive pulse. After missing the high side pulse, the over current (OC) trigger is reset. If on the next low side drive cycle, the current is still too high i.e., V_{CS} is ≤ 0V, another high side pulse is missed and so on. Thus reducing the overall energy transferred to the output and V_{OUT} starts to fall. As this successive missing of pulses results in an effectively lower switching frequency, power inductor ripple currents can get very high if left unlimited. The MIC2130/31 therefore limits Duty Cycle during current limit to prevent currents building up in the power inductor and output capacitors.

Current Limit Setting

The Simple Method

R_{CS} = I_{OUT} x $RDS_{ON(max)}$/200µA.

Accurate Method

For designs where ripple current is significant when compared to $I_{OUT,}$ or for low duty cycle operation, calculating the current setting resistor R_{CS} should take into account that one is sensing the peak inductor current and that there is a blanking delay of approximately 100ns.

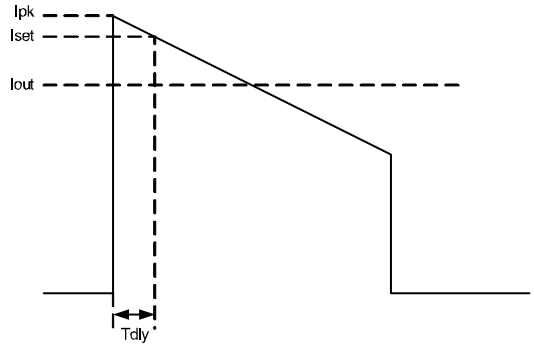


Figure 7.

$$I_{PK} = I_{OUT} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{V_{OUT} \cdot (1 - D)}{F_{SWITCH} \cdot L}$$

$$I_{SET} = I_{PK} - \frac{V_{OUT} \cdot T_{DLY}}{L}$$

$$R_{CS} = \frac{I_{SET} \cdot RDS_{ON(\max)}}{I_{CS(\min)}}$$

D = Duty Cycle

F_{SWITCH} = Switching Frequency

L = Power inductor value

T_{DLY} = Current limit blanking time ~ 100ns

$I_{CS(min)}$ = 180µA

Example:

Consider a 12V to 3.3V @ 5A converter with 7.3µH power inductor and 93% efficiency at a 5A load and an LSD FET of RDS_{ON} of 10mΩ (typical values).

$$D = \frac{V_{OUT}}{V_{IN} \cdot Efficiency}$$

$$I_{RIPPLE} = \frac{3.3 \cdot (1 - 0.306)}{150kHz \cdot 7.3\mu H} = 2.1A$$

$$I_{PK} = 5 + \frac{2.1}{2} = 6.05A$$

$$I_{SET} + 6.05 - \frac{3.3 \cdot 100ns}{7.3\mu H} = 6.00A$$

$$R_{CS} = \frac{6.00 \cdot 10m\Omega}{180\mu A} = 333\Omega \qquad \text{(332 std. value)}$$

Using the simple method here would result in a current limit point lower than desired.

This equation sets the minimum current limit point of the converter, but maximum will depend upon the actual inductor value and RDS_{ON} of the MOSFET under current limit conditions. This could be in the region of 50% higher and should be considered to ensure that all the power components are within their thermal limits unless thermal protection is implemented separately.

HCL (MIC2131 only)

The high current limit (HCL) is a function of the MIC2131 only. It allows for twice the output load current (for a time T determined by the HCL cap) before the current limit comparator trips. During the time T, the current sense current source (200µA nominal) is increased to 400µA.

T = CHCL * 2/13µ = CHCL * 153.85 *1e3

Where CHCL is the cap at the HCL pin

Frequency Dithering

The MIC2131 has an additional useful feature. The switching frequency is dithered ±12% in order to spread the frequency spectrum over a wider range to lower the EMI noise peaks generated by the switching components. A pseudo random generator is used to generate the ±dithering which further reduces the EMI noise peaks.

Power Good Output

The power good output (PG) will go high only when output is above 90% of the nominal set output voltage.

VDD Regulator

The internal regulator provides a regulated 5V for supplying the analog circuit power (AV_{DD}). V_{DD} also powers the MOSFET drivers. V_{DD} is designed to operate at input voltages down to 8V. The AV_{DD} supply should be connected to V_{DD} through an RC filter to provide decoupling of the switching noise generated by the MOSFET drivers taking large current pulses from the V_{DD} regulator.

Gate Drivers

The MIC2130/31 is designed to drive both high side and low side N-Channel MOSFETs to enable high switching speeds with the lowest possible losses. The high side MOSFET gate driver is supplied by a bootstrap capacitor CBST connected at the SW pin and the BST pin. A high speed diode (a Schottky diode is recommended) between the V_{DD} pin and BST pin is required as shown in Figure 8. This provides the high side MOSFET with a constant VGS drive voltage equal to V_{DD} - V_{DIODE}.

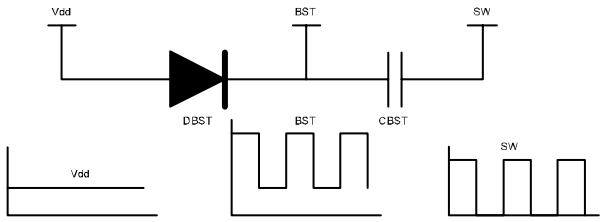
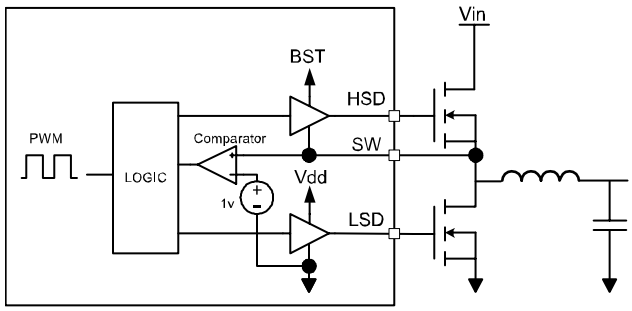


Figure 8.

When HSD goes high, this turns on the high side MOSFET and the SW node rises sharply. This is coupled through the bootstrap capacitor CBST and Diode DBST becomes reverse biased. The MOSFET Gate is held at V_{DD}-V_{DIODE} above the Source for as long as CBST remains charged. This bias current of the High side driver is <10mA so a 0.1µF to1 µF is sufficient to hold the gate voltage with minimal droop for the power stroke (High side switching) cycle, i.e. ∆BST = 10mA x 6µs / 0.1µF = 567mV. When the low side driver turns on every switching cycle, any lost charge from CBST is replaced via DBST as it becomes forward biased. Therefore minimum BST voltage is V_{DD} – 0.5V.

The Low side driver is supplied directly from V_{DD} at nominal 5V.

Adaptive Gate Drive



There is a period when both driver outputs are held off ('dead time') to prevent shoot through current flowing. Shoot through current flows if both MOSFETS are on momentarily as the same time and reduces efficiency and can destroy the FETs. This dead time must be kept to a minimum to reduce losses in the free wheeling diode which could either be an external Schottky diode placed across the lower MOSFET or the internal Schottky diode implemented in some MOSFETs. It is not recommended, for high current designs, to rely on the intrinsic body diode of the power MOSFET. These typically have large forward voltage drops and a slow reverse recovery characteristic which will add significant losses to the regulator. Dependant upon the MOSFETs used, the dead time could be required to be 150ns or 20ns. The MIC2130/31 solves this variability issue by using an adaptive gate-drive scheme.

When the High side driver is turned off, the inductor forces the voltage at the switching node (low side MOSFET drain) towards ground to keep current flowing. When the SW pin is detected to have reached 1V, the top MOSFET can be assumed to be off and the low side driver output is immediately turned on. There is also a short delay between the low side drive turning off and the high side driver turning on. This is fixed at ~80ns to allow for large gate charge MOSFETs to be used.

Application Information

Passive Component Selection Guide

Transition losses in the power MOSFETs are not defined by inductor value. However, the inductor value is responsible for the ripple current which causes some of the resistive losses. These losses are proportional to I_{RIPPLE}^2. Minimizing inductor ripple current therefore reduces resistive losses and can be achieved by choosing a larger value inductor. This will generally improve efficiency by reducing the RMS current flowing in all of the power components. The actual value of inductance is really defined by space limitations, RMS rating (I_{RMS}) and saturation current (I_{SAT}) of available inductors. If we look at the newer flat wire inductors, these have higher saturation current ratings than the RMS current rating for lower values and as inductance value increases, these figures get closer in value. This mirrors what happens in the converter with I_{SAT} analogous to the maximum peak switch current and I_{RMS} analogous to output current. As inductance increases, so $I_{SWITCHpk}$ tends towards I_{OUT}. This is a characteristic that makes these types of inductor optimal for use in high power buck converters such as MIC2130/31.

To determine the I_{SAT} and I_{RMS} rating of the inductor, we should start with a nominal value of ripple current. This should typically be no more than $I_{OUT(max)}/2$ to minimize MOSFET losses due to ripple current mentioned earlier. Therefore:

$$L_{MIN} \sim 2\frac{V_O}{I_O \cdot F_{SWITCH}} \cdot \left(1 - \frac{V_O}{V_{IN} \cdot Efficiency}\right)$$

$IL_{RMS} > 1.04 \times I_{OUT(max)}$

$IL_{SAT} > 1.25 \times I_{OUT(max)}$

Any value chosen above L_{MIN} will ensure these ratings are not exceeded.

In considering the actual value to choose, we need to look at the effect of ripple on the other components in the circuit. The chosen inductor value will have a ripple current of:

$$I_{RIPPLE} \sim \frac{(1-D)}{F_{SWITCH}} \cdot \frac{V_{OUT}}{L}$$

This value should ideally be kept to a minimum, within the cost and size constraints of the design, to reduce unnecessary heat dissipation.

Output Capacitor Selection

The output capacitor (C_{OUT}) will have the full inductor ripple current IL_{RMS} flowing through it. This creates the output switching noise which consists of two main components:

$$V_{OUTPK-PK} \approx \underbrace{I_{RIPPLE} \cdot ESR}_{\substack{ESR \\ Noise}} + \underbrace{\frac{I_{RIPPLE} \cdot T_{ON}}{2 \cdot C_{OUT}}}_{\substack{Capacitor \\ Noise}}$$

If therefore, the need is for low output voltage noise (e.g., in low output voltage converters), V_{OUT} ripple can be directly reduced by increasing inductor value, Output capacitor value or reducing ESR.

For tantalum capacitors, ESR is typically >40mΩ which usually makes loop stabilization easier by utilizing a pole-zero (type II) compensator.

Due to the many advantages of multi-layer ceramic capacitors, among them, cost, size, ripple rating and ESR, it can be useful to use these in many cases. However, one disadvantage is the CV product. This is lower than tantalum. A mixture of one tantalum and one ceramic can be a good compromise which can still utilize the simple type II compensator.

With ceramic output capacitors only, a double-pole, double-zero (type III) compensator is required to ensure system stability. Loop compensation is described in more detail later in the data sheet.

Ensure the RMS ripple current rating of the capacitor is above $I_{RIPPLE} \cdot 0.6$ to improve reliability.

Input Capacitor Selection

The input filter needs to supply the load current when the high-FET is on and should to limit the ripple to the desire value. The C_{IN} ripple rating for a converter is typically $I_{OUT}/2$ under worst case duty cycle conditions of 50%.

$$IRMS_{CIN} = I_{OUT} \times \sqrt{D \times (1-D)}$$

Where $D = V_{OUT}/(V_{IN}xeff)$

It is however, also important to closely decouple the Power MOSFETs with 2 x 10µF Ceramic capacitors to reduce ringing and prevent noise related issues from causing problems in the layout of the regulator. The ripple rating of C_{IN} may therefore be satisfied by these decoupling capacitors as they allow the use of perhaps one more ceramic or tantalum input capacitor at the input voltage node to decouple input noise and localize high di/dt signals to the regulator input.

Power MOSFET Selection

The MIC2130/31 drives N-channel MOSFETs in both the high-side and low-side positions. This is because the switching speed for a given RDS_{ON} in the N-Channel device is superior to the P-Channel device.

There are different criteria for choosing the high- and low-side MOSFETs and these differences are more significant at lower duty cycles such as 12V to 1.8V conversion. In such an application, the high-side MOSFET is required to switch as quickly as possible to minimize transition losses (power dissipated during rise

and fall times). Whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When duty cycle approaches 50%, the current carrying capability of the upper MOSFET starts to become critical also and can sometimes require external high current drivers to achieve the necessary switching speeds.

MOSFET loss = Static loss + Transition loss

Static loss (Ps) = I_{FETRMS}^2 x RDS_{ON}

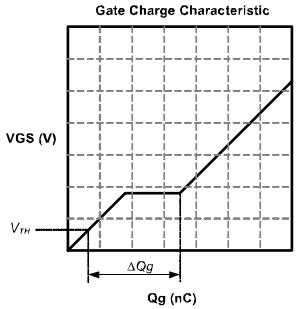
Transition loss (Pt) = I_{OUT} x (tr+tf) x V_{DSOFF} x F_{SWITCH}/2

tr + tf = Rise time + Fall time

Due to the worst case driver currents of the MIC2130/31, the value of tr + tf simplifies to:

tr + tf (ns) = ∆Qg (nC)

∆Qg can be found in the MOSFET characteristic curves



V_{DSOFF} = Voltage across MOSFET when it is off

$$I_{FETRMS} = \sqrt{D \cdot \frac{(I_X^2 + I_X \cdot I_Y + I_Y^2)}{3}}$$

$I_X = I_{OUT} - I_{RIPPLE}/2$

$I_Y = I_{OUT} + I_{RIPPLE}/2$

D_on = T_{ON} x F_{SWITCH} high-side FET on time

D_off = T_{ON} x F_{SWITCH} low-side FET on time

D_on = D = $V_O/(V_{IN}$ x eff) since it changes depending on which MOSFET we are calculating losses for.

High-side FET T_{ON} = D_on/F_{SWITCH}

The lower MOSFET is not on for the whole time that the upper MOSFET is off due to the fixed 80ns high side driver delay. Therefore, there is an 80ns term subtracted from the lower FET on time equation.

Low-side FET T_{ON} = (1-D_on)/F_{SWITCH} – 80ns

There are many MOSFET packages available which have varying values of thermal resistance and can therefore dissipate more power if there is sufficient airflow or heat sink externally to remove the heat. However, for this exercise we can assume a maximum dissipation of 1.2W per MOSFET package. This can be altered if the final design has higher allowable package dissipation.

Look at lower MOSFET first:

Pdis_max = 1.2 W = Ps + Pt

For the low side FET, Pt is small because VDS_{OFF} is clamped to the forward voltage drop of the Schottky diode. Therefore:

$RDS_{ON(max)}$ ~ 1.2/I_{FETRMS}^2

Example: For 12V to 1.8V @ 10A

$RDS_{ON(max)}$ < 14mΩ

It is important to remember to use the $RDS_{ON(max)}$ figure for the MOSFET at the maximum temperature to help prevent thermal runaway (as the temperature increases, the RDS_{ON} increases).

$\Delta Qg_{(max)}$ should be limited so that the low side MOSFET is off within the fixed 80ns delay before the high side driver turns on.

High side MOSFET:

For the high side FET, the losses should ideally be evenly spread between transition and static losses. Use the C of the V_{IN} range to balance the losses.

Pt = Pdis_max/2 = 0.6 = I_{OUT} x ∆Qg x V_{INMID} x F_{SWITCH}/2

$\Delta Qg_{(max)}$ < 0.6 x 2 / (I_{OUT} x V_{INMID} x F_{SWITCH})

RDSon is calculated similarly for the high side MOSFET:

$RDS_{ON(max)}$ ~ 0.6 / I_{FETRMS}^2

Using previous example:

$\Delta Qg_{(max)}$ < 20nC

$RDS_{ON(max)}$ < 35mΩ

Note that these are maximum values based upon thermal limits and are not targeted at the highest efficiency. Selection of lower values is recommended to achieve higher efficiency designs.

Limits to watch out for:

Qg_{TOTAL} < 1500 nC/V_{IN}

Total of both high side and low side MOSFET Qg value at VGS = 5V for both channels.

Example: @ $V_{IN(max)}$ = 13.2V,

Qg_{TOTAL} < 1500/13.2 = 114nC

ΔQg_{LOW} < 120nC

Maximum turn on gate charge for the low side MOSFET to ensure proper turn off before high side MOSFET is switched on.

Control Loop Stability and Compensation

Figure 10 shows the simplified system schematic. The internal transconductance error amplifier is used for compensating the voltage feedback loop by placing a capacitor (C1) in series with a resistor (R1) and another capacitor C2 in parallel from the COMP pin-to-ground. (Note: Ceramic output caps may require type III compensation).

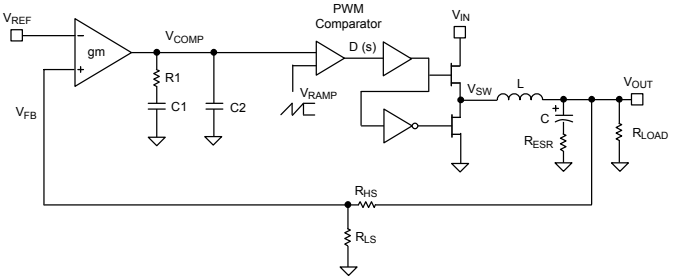


Figure 10 Simplified System Schematic

In order to have a stable system when the gain of T(s) = 1 $\Rightarrow$ (0db) the phase has to be greater (less negative) than -180°. The amount the phase is greater than -180° is called the phase margin, typically 30 to 60 and is a key parameter predicting the stability of the system and how much overshoot and undershoot the system exhibits during transients.

The open loop transfer function is:

$T(s) = G_{ea}(s) \times G_{PWMcomp}(s) \times G_{Pwrs}(s) \times G_{flt}(s) \times H_{fb}(s)$

And the phase is:

$$\angle T(s) = \theta_T(s) = \theta_{ea} + \theta_{PWMcomp} + \theta_{PwrS} + \theta_{Flt} + \theta_{fb}$$

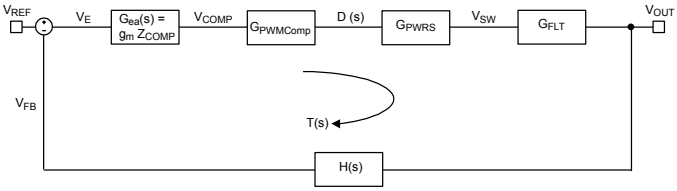


Figure 11 System Block Diagram

In the system block diagram in figure 11

$G_{ea}(s) = g_m \times Z_{comp}$ Gain of the Error amp

where g_m =1.5ms and

$$Z_{comp} = \left(R1 + \frac{1}{sC_1}\right) \| \left(\frac{1}{sC_2}\right)$$

$$G_{PWMcomp}(s) = \frac{\Delta D}{\Delta V_{comp}} = \frac{D_{Max}}{\Delta V_{ramp}} = \frac{0.85}{2.1 - 1.1} = 0.85$$

Gain of the PWM comparator

$$G_{PwrS}(s) = \frac{\Delta V_{SW}}{\Delta d(s)} = \frac{V_{Out}}{\Delta d(s) * D} = \frac{V_{Out}}{D_{Max} * D}$$ Gain of the Power Stage

$$G_{Flt}(s) = \frac{1 + sR_{esr}C_{out}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$ Gain of the Filter

where:

$$Q = \frac{E_{stored}}{E_{Lost}} = \frac{R_{Load}}{\sqrt{L/C_{out}}}$$ (Parallel loaded)

and

$$\omega_0 = \frac{1}{\sqrt{LC_{out}}} \qquad F_{esr} = \frac{1}{2\pi R_{esr}C_{out}}$$

$$H(s) = \frac{R_{LS}}{R_{LS} + R_{HS}} = \frac{V_{ref}}{V_{out}}$$ Gain of the feedback network

For simplicity, combine the PWM comparator gain and the Power stage gain and call it the modulator gain.

$$G_{Mod}(s) = G_{PWMcomp}(s) * G_{PWRsw}(s)$$

$$= \frac{D_{Max}}{\Delta V_{ramp}} * \frac{V_{out}}{D * D_{Max}} = \frac{V_{out}}{\Delta V_{ramp} * D}$$ therefore;

$T(s) = G_{ea}(s) \times G_{Mod}(s) \times G_{flt}(s) \times H_{fb}(s)$ and

$$\theta_T(s) = \theta_{ea} + \theta_{Mod} + \theta_{flt} + \theta_{fb}$$

The phase of the open loop is the phase of all the blocks in the loop added together.

The phase of T(s) is

$$\theta_T(s) = \theta_{ea} + \theta_{PWMcomp} + \theta_{PwrS} + \theta_{Flt} + \theta_{fb}$$

$$\theta_T(s) = \theta_{ea} + \theta_{Mod} + \theta_{fb}$$

Where $\theta_{ea} = -\theta_{pole0} + \theta_{Zero1} - \theta_{pole1}$

θ_{pole0} = phase lag due to the pole at the origin

θ_{Zero1} =phase lead due to Zero1

θ_{pole1} = phase lag due to pole1

$\theta_{PWMcomp} = 0°$, $\theta_{PwrS} = 0°$ $\theta_{fb} = 0°$ therefore;

$\theta_{Mod} = 0°$

The phase of the filter includes the complex poles of LC and the Zero caused by the ESR of the C_{OUT}.

The filter has 2 poles at F_0 and a zero at F_{esr}

$\theta_{Flt} = -180°$ at F_0 and +90° at F_{esr}

Example:

V_{IN} = 24V; V_{OUT} = 3.3V; I_{OUT} = 10A; L = 7.3µH; C_{OUT} = 660µF; Resr = 40mΩ; Fsw = 150KHz

The gain and phase of the modulator and filter is: $G_{Mod}(s)$ x $G_{flt}(s)$

This is the gain $\frac{V_{OUT}}{V_{comp}}(s)$ in Figure 12

A computer generated plot of $G_{Mod}(s)$ x $G_{flt}(s)$ is shown in Figure 12.

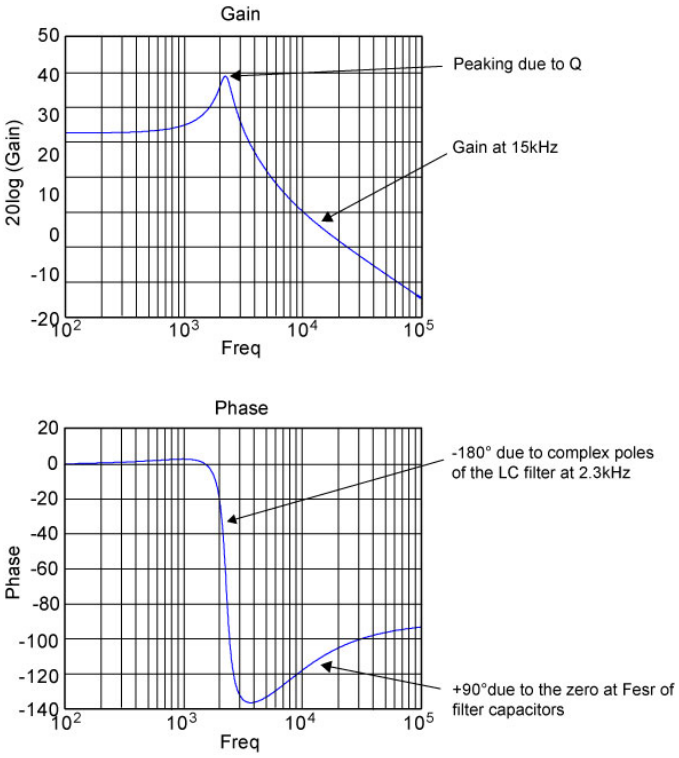


Figure 12. Modulator Transfer Function

There is a -180° phase change near F_0. At frequencies greater then F_0 the phase increases towards -90° due to the zero of F_{esr}. The phase effects of poles and zeros start a decade below and finish a decade above the frequency of a pole or zero. Therefore, at the frequency of a pole or zero the phase effect is only half of the final value. At the complex pole 2.3kHz the phase is -90 and would be -180 at 23kHz if not for the +90 phase lead of the zero at around 6kHz due to the esr of the filter capacitors. (Actually, the phase gain plots reach their final values asymptotically).

By inspecting Figure 12 the DC and low frequency gain of G_{Mod} = 20Log(0.85 x 24) = 26.2db; F_0 = 2.3kHz; F_{esr} = 6kHz and Q is 13.6db.

The peak Gain equals the low freq gain plus the Q = 26.2 + 13.6 = 39.9db.

It is desired that T(s) (the open loop transfer function) have a cross over frequency (Fco) of 1/10 the Switching frequency at 15kHz. It is require that $\angle T(j2\pi Fco)$ (the phase of T(s) at Fco), to be greater than -180° by at least the phase margin. By inspecting the Gain plot of $G_{Mod}(s)$ at 15kHz, $G_{Mod}(s)$ has a gain of about 3.9db.

Therefore, to make T(j2πFco) = 1→ 0db;

$T(s) = G_{ea}(s) \times G_{Mod}(s) \times H_{fb}(s) = 1$ at Fco

H_{fb} = Vref/Vout = 0.7/3.3 = 0.212 → -13.5db

$|G_{ea}|_{db} = |T|_{db} - |G_{Mod}|_{db} - |H_{fb}|_{db}$ = 0-3.9db – (-13.5db) = 9.6db ⇒3.02 The error amp needs 9db of gain at Fco.

Therefore $g_m \times Z_{Comp}$ = 3.02 at 15kHz.

The location of the error amp's zero and poles are selected in order to achieve the desired phase margin of T(s). For the maximum phase boost at the cross over Frequency (Fco), place the first Zero1 of the EA at Fco/10 since the effect of its phase boost will be at the maximum at Fco. Likewise, place the pole of the EA at least 10 x Fco so the effects of its phase lag will be at a minimum at Fco. Therefore, use R1 = 2k; C1 = 0.068µF; C2 = 470pF.

g_m Error Amplifier

Usually, it is undesirable to have high error amplifier gain at high frequencies otherwise high frequency noise spikes at large amplitude would be present at the output. Hence, gain should be permitted to fall off at high frequencies. At low frequency, it is desired to have high open-loop gain to attenuate the power line ripple. Thus, the error amplifier gain should be allowed to increase rapidly at low frequencies.

The transfer function for the internal gm error amplifier with R1, C1, and C2 at the comp pin is given by the following equation:

$$G_{ea}(s) = g_m \cdot \left[\frac{1 + R1 \cdot s \cdot C1}{s \cdot (C1 + C2) \cdot \left(1 + R1 \cdot \frac{C1 \cdot C2 \cdot s}{C1 \cdot C2}\right)} \right]$$

The above equation can be simplified by assuming C2<C1,

$$G_{ea}(s) = g_m \cdot \left[\frac{1 + R1 \cdot s \cdot C1}{s \cdot (C1) \cdot (1 + R1 \cdot C2 \cdot s)} \right]$$

From the above transfer function, one can see that R1 and C1 introduce a zero and R1 and C2 a pole at the following frequencies:

F_{zero1}= 1/2 π × R1 × C1 F_{pole1} = 1/2 π × C2 × R1

$F_{pole@origin}$ = 1/2 π × C1

Figure 14 shows the gain and phase curves for the above transfer function with R1 = 2k, C1 = 0.068µF, C2 = 470pF, and gm = 0.0015Ω–1. It can be seen that at 15kHz, the error amplifier exhibits approximately 9.6db of gain and 170° of phase. Figure 13 shows the open loop transfer function T(s) with these compensation values. It has a cross over frequency of 15KHz and phase margin of 60˚.

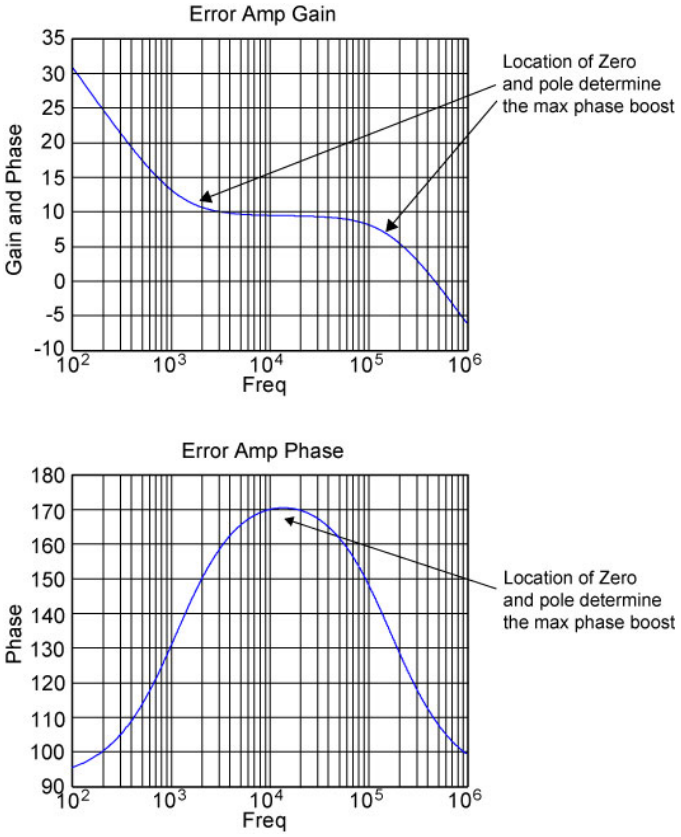


Figure 13. Error Amp Gain and Phase

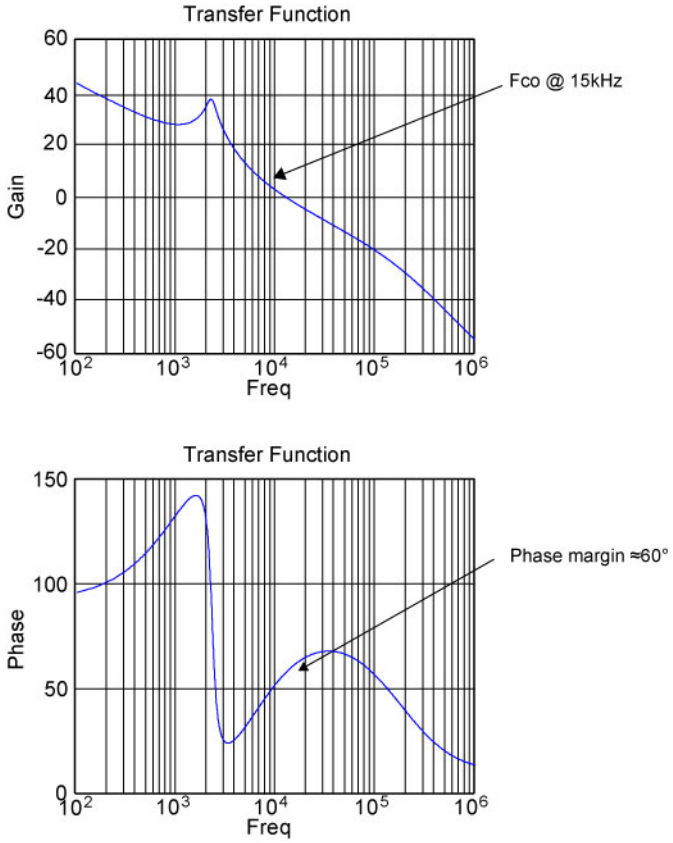
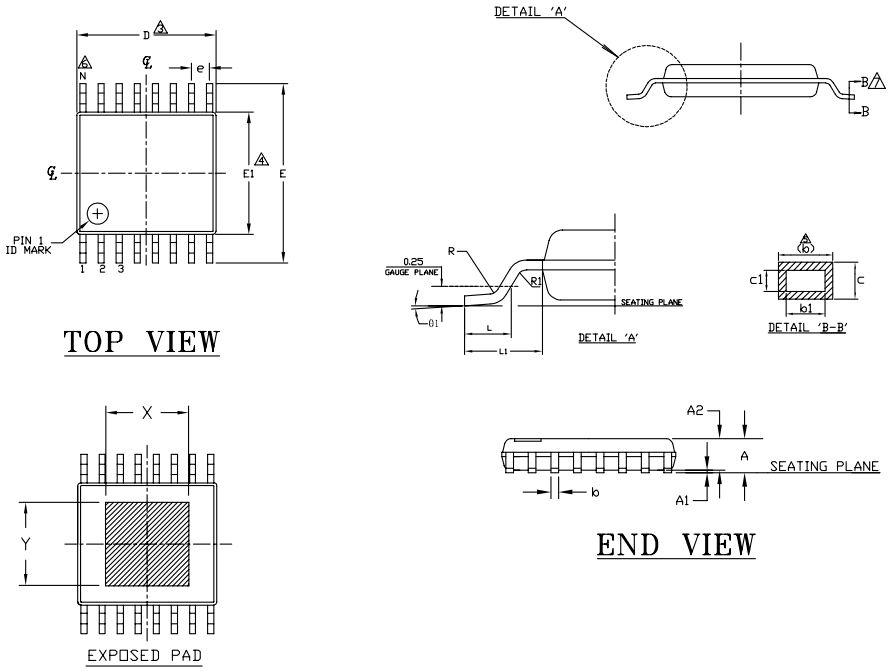


Figure 14. The Open Loop T(s) Gain and Phase

Package Information



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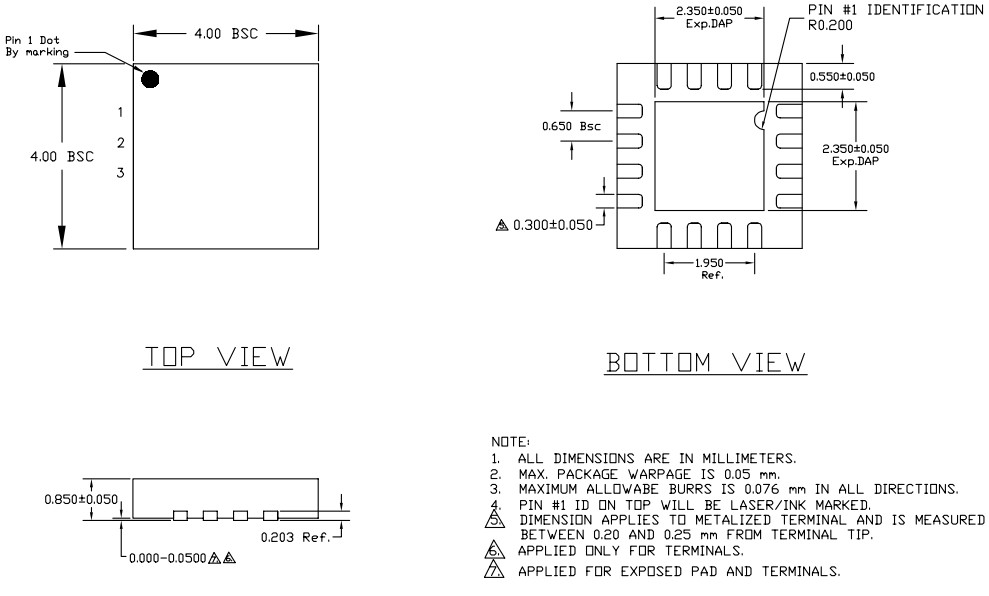

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