Product data sheet

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 plastic package intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- · Direct interfacing to logic level ICs
- · Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- · Planar passivated for voltage ruggedness and reliability
- · Triggering in all four quadrants
- · Very sensitive gate

3. Applications

- General purpose low power phase control
- · General purpose low power switching
- Solid-state relay

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DRM}	repetitive peak off- state voltage		-	-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{lead} ≤ 50 °C; <u>Fig. 1</u> ; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	-	0.6	A
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	-	8	Α
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms	-	-	8.8	A
Tj	junction temperature		-	-	125	°C
Static chara	acteristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + G+;$ $T_j = 25 \text{ °C; } Fig. 7$	-	1	5	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + G-;$ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{}$	-	2	5	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2-\text{ G-;} $ $T_j = 25 \text{ °C; } Fig. 7$	-	2	5	mA

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	4	7	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	1	10	mA
V _T	on-state voltage	I _T = 0.85 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.4	1.9	V
Dynamic chara	acteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 110 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	30	45	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 600 V; T_j = 50 °C; dI_{com}/dt = 0.3 A/ms; I_T = 0.84 A; gate open circuit	-	5	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2		T2
2	G	gate		G sym051
3	T1	main terminal 1	TO-92 (SOT54)	Sylnost

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
MAC97A8	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54			

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{lead} ≤ 50 °C; <u>Fig. 1</u> ; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	0.6	Α
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	8	Α
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	8.8	Α
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	0.32	A²s
dl _T /dt	rate of rise of on-state current	I _G = 20 mA; T2+ G+	-	50	A/µs
		I _G = 20 mA; T2+ G-	-	50	A/µs
		I _G = 20 mA; T2- G-	-	50	A/µs
		I _G = 20 mA; T2- G+	-	10	A/µs
I _{GM}	peak gate current		-	1	Α
P_{GM}	peak gate power		-	5	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		-	125	°C

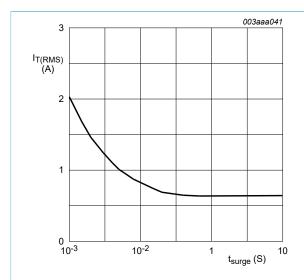


Fig. 1. RMS on-state current as a function of surge duration; maximum values

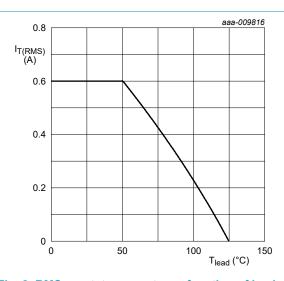


Fig. 2. RMS on-state current as a function of lead temperature; maximum values

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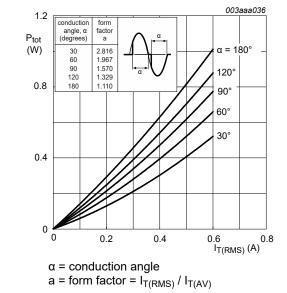


Fig. 3. Total power dissipation as a function of RMS onstate current; maximum values

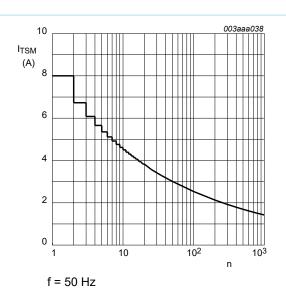


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

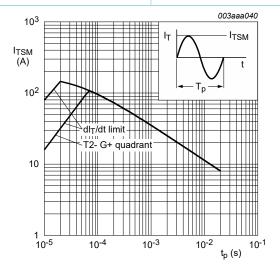


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

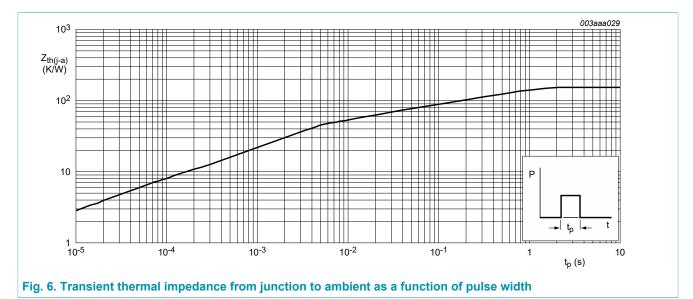
 $t_p \le 20 \text{ ms}$

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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-lead)}	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
		half cycle	-	-	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics				,	
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	1	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ \text{ G-};$ $T_j = 25 \text{ °C}; Fig. 7$	-	2	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	2	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	4	7	mA
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	1	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 8}}{}$	-	5	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 8}}{}$	-	1	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 8}}{}$	-	2	10	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	1	10	mA
V_{T}	on-state voltage	I _T = 0.85 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.4	1.9	V
V_{GT}	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	-	0.9	1.5	V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_j = 110 ^{\circ}\text{C};$ Fig. 11	0.1	0.7	-	V
I _D	off-state current	V _D = 600 V; T _j = 110 °C	-	3	100	μΑ
Dynamic ch	naracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 110 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	30	45	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 600 V; T_j = 50 °C; dI_{com}/dt = 0.3 A/ms; I_T = 0.84 A; gate open circuit	-	5	-	V/µs
t _{gt}	gate-controlled turn-on time	I_{TM} = 1 A; V_D = 600 V; I_G = 25 mA; $dI_G/$ dt = 5 A/µs	-	2	-	μs

3

2

1

-60

T_{L(25°C)}

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T_j (°C)

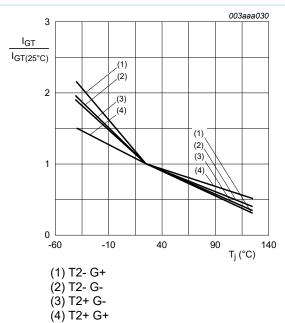


Fig. 8. Normalized latching current as a function of junction temperature

-10

40



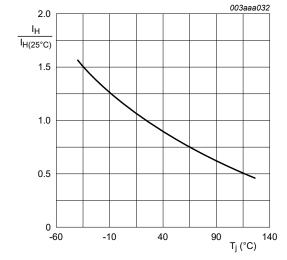
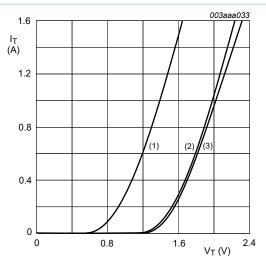


Fig. 9. Normalized holding current as a function of junction temperature



 V_o = 1.45 V; R_s = 0.1875 Ω (1) T_j = 125 °C; typical values (2) T_j = 125 °C; maximum values (3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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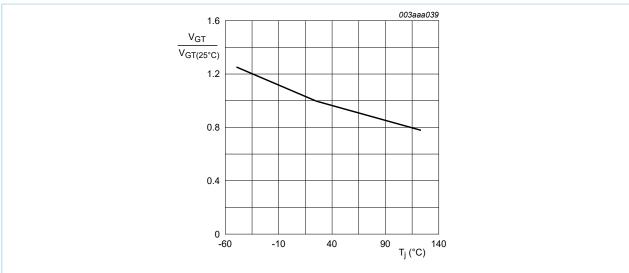


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

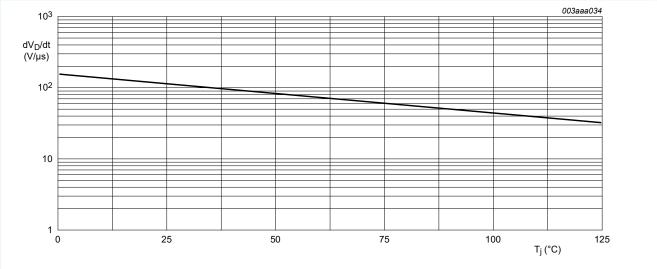
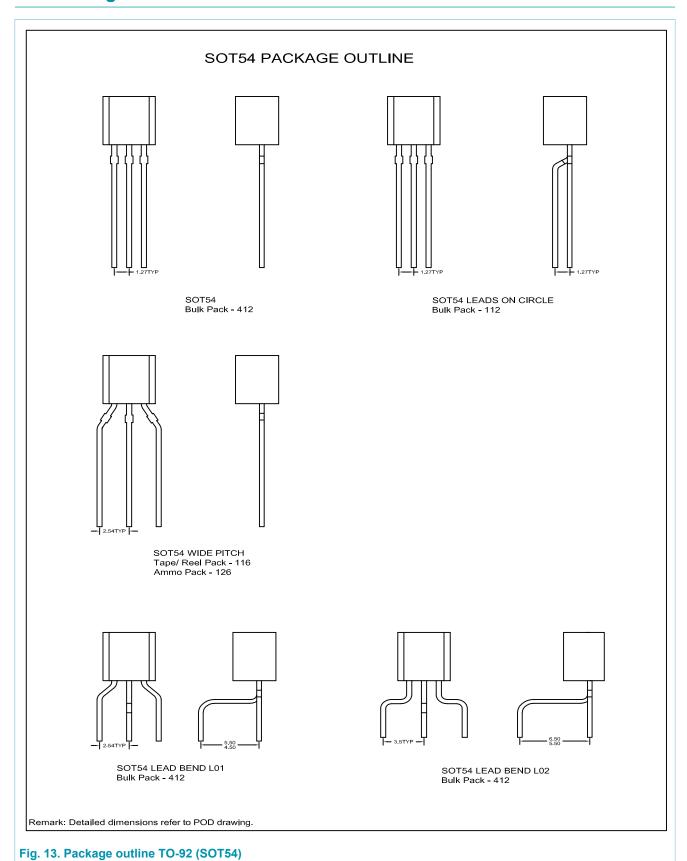


Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline



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11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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For more information, please visit: http://www.ween-semi.com
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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А