



ATP405 — General-Purpose Switching Device Applications

N-Channel Silicon MOSFET

Features

- ON-resistance $R_{DS(on)}=25m\Omega$ (typ.)
- 10V drive
- Input capacitance $C_{iss}=4000pF$ (typ.)
- Halogen free compliance

Specifications

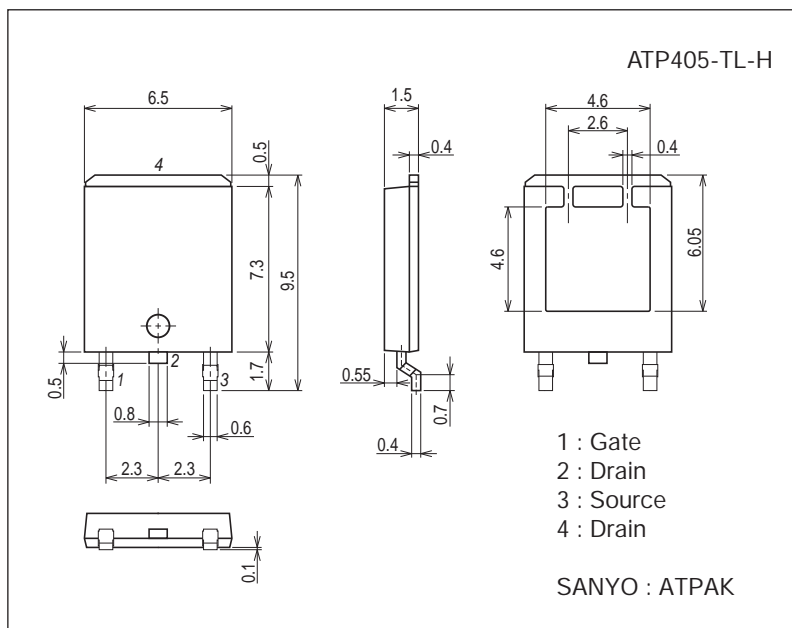
Absolute Maximum Ratings at $T_a=25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		100	V
Gate-to-Source Voltage	V_{GSS}		± 20	V
Drain Current (DC)	I_D		40	A
Drain Current (Pulse)	I_{DP}	$PW \leq 10\mu s$, duty cycle $\leq 1\%$	160	A
Allowable Power Dissipation	P_D	$T_c=25^\circ C$	70	W
Channel Temperature	T_{ch}		150	$^\circ C$
Storage Temperature	T_{stg}		-55 to +150	$^\circ C$
Avalanche Energy (Single Pulse) *1	E_{AS}		148	mJ
Avalanche Current *2	I_{AV}		40	A

Note : *1 $V_{DD}=30V$, $L=100\mu H$, $I_{AV}=40A$
 *2 $L \leq 100\mu H$, Single pulse

Package Dimensions

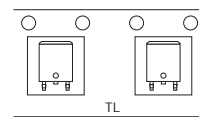
unit : mm (typ)
 7057-001



Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

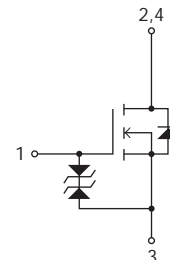
Packing Type: TL



Marking



Electrical Connection

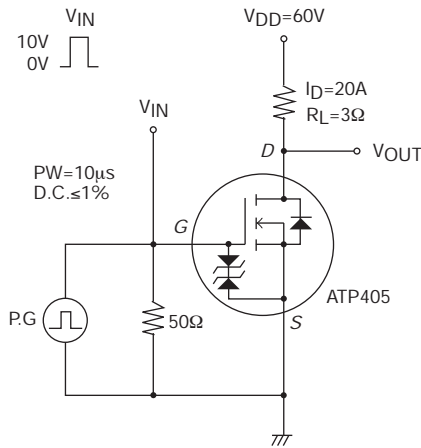


ATP405

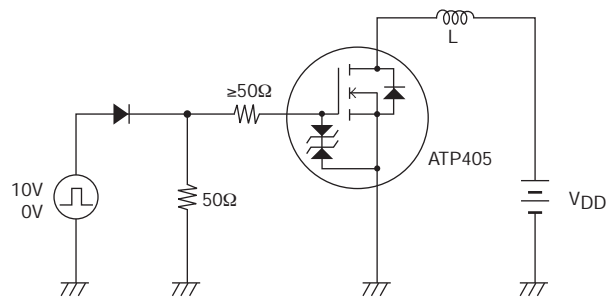
Electrical Characteristics at $T_a=25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=1\text{mA}, V_{GS}=0\text{V}$	100			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$			10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 16\text{V}, V_{DS}=0\text{V}$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS}=10\text{V}, I_D=1\text{mA}$	2.0		3.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS}=10\text{V}, I_D=20\text{A}$		62		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)}$	$I_D=20\text{A}, V_{GS}=10\text{V}$		25	33	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS}=20\text{V}, f=1\text{MHz}$		4000		pF
Output Capacitance	C_{oss}				300	pF
Reverse Transfer Capacitance	C_{rss}				170	pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		38		ns
Rise Time	t_r			125		ns
Turn-OFF Delay Time	$t_{d(off)}$			220		ns
Fall Time	t_f			150		ns
Total Gate Charge	Q_g		$V_{DS}=60\text{V}, V_{GS}=10\text{V}, I_D=40\text{A}$		68	
Gate-to-Source Charge	Q_{gs}			14		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			15		nC
Diode Forward Voltage	V_{SD}	$I_S=40\text{A}, V_{GS}=0\text{V}$		0.9	1.2	V

Switching Time Test Circuit

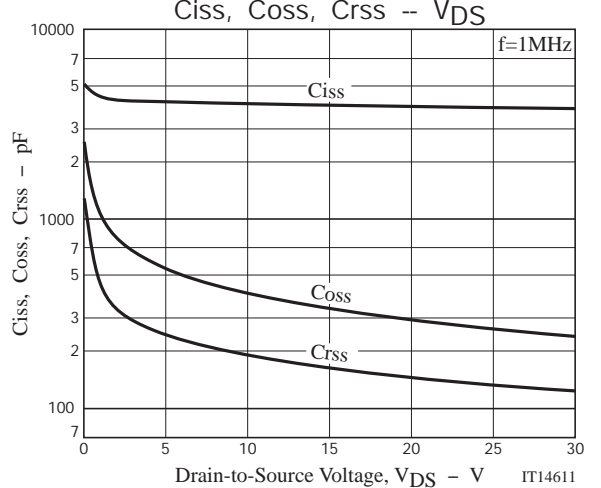
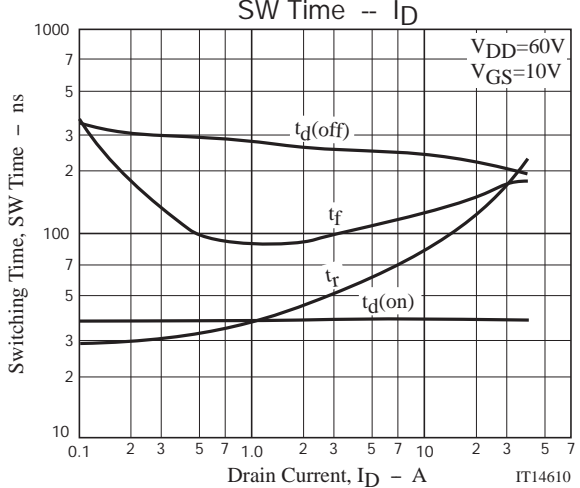
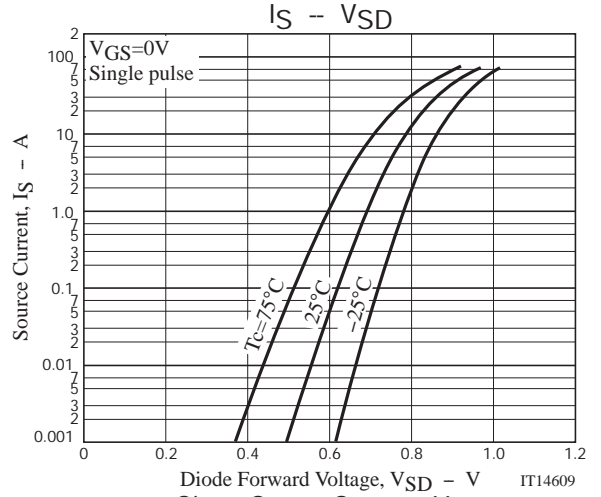
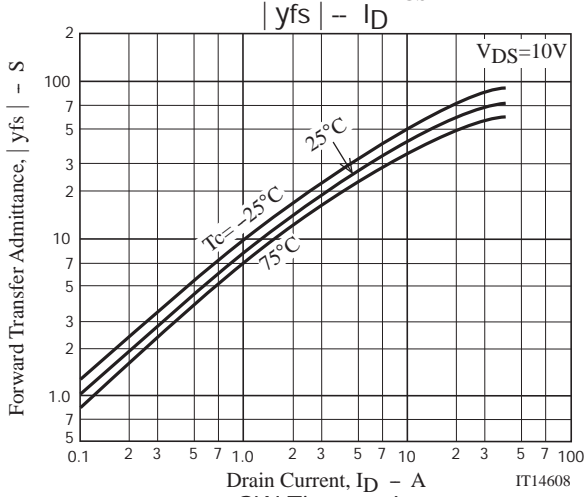
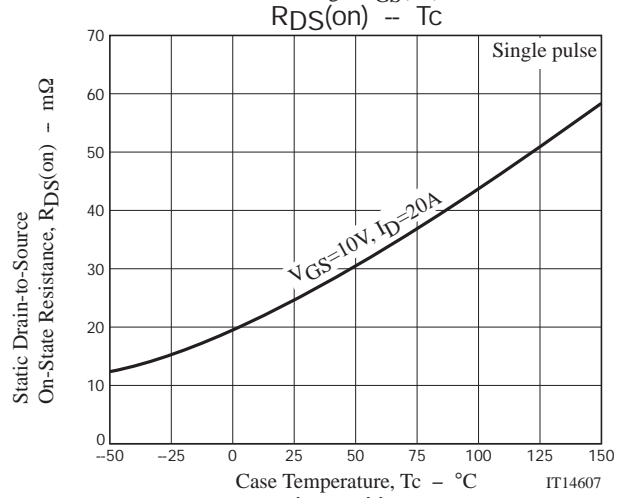
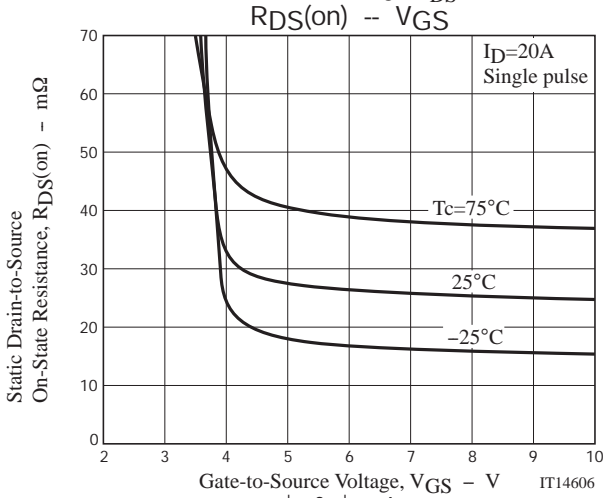
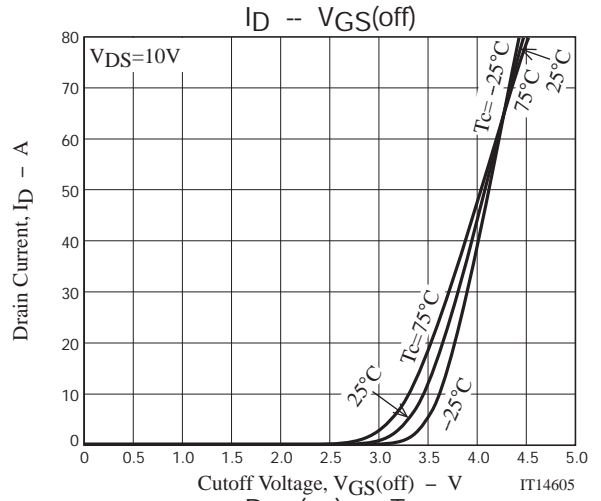
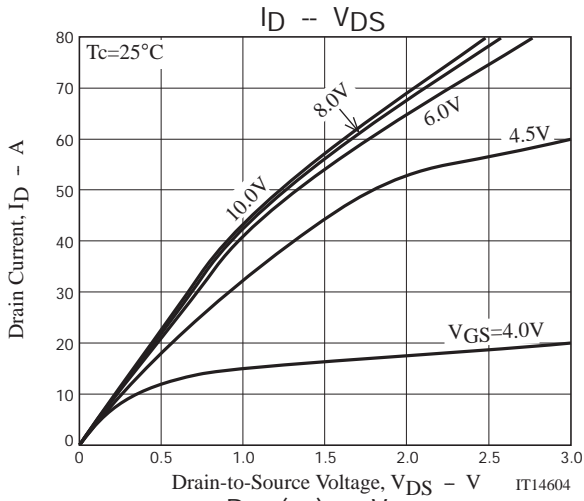


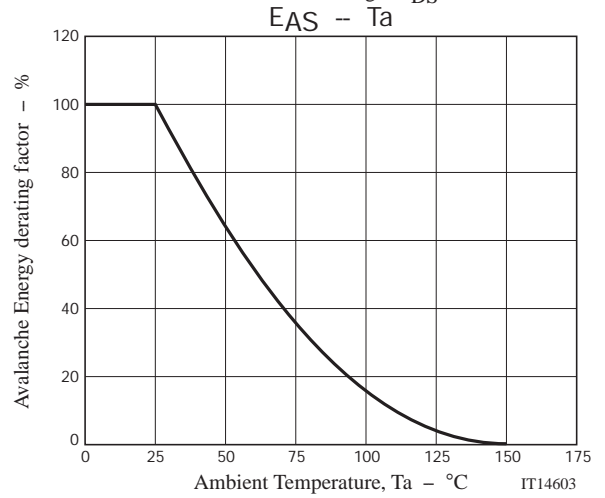
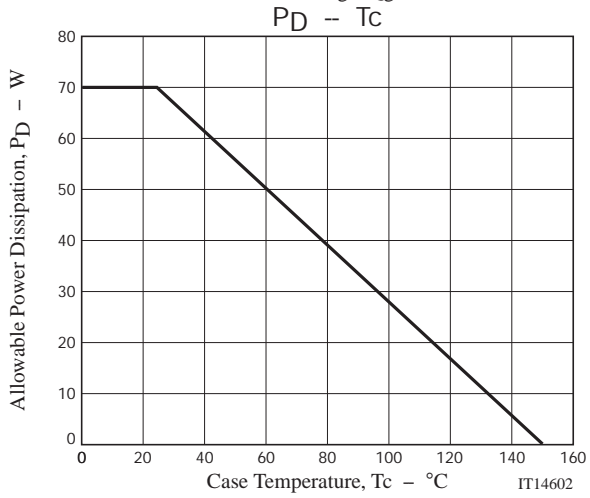
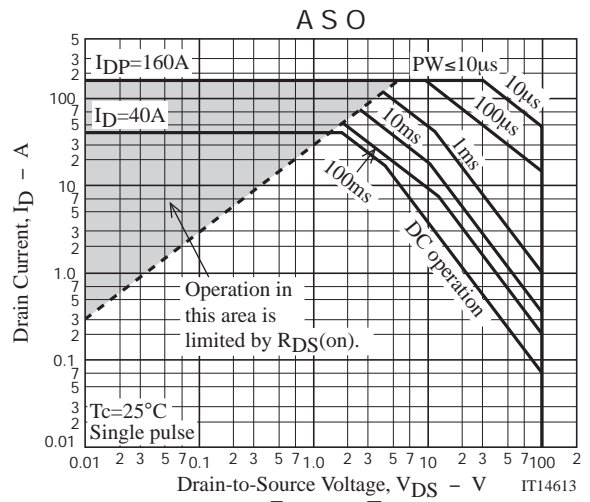
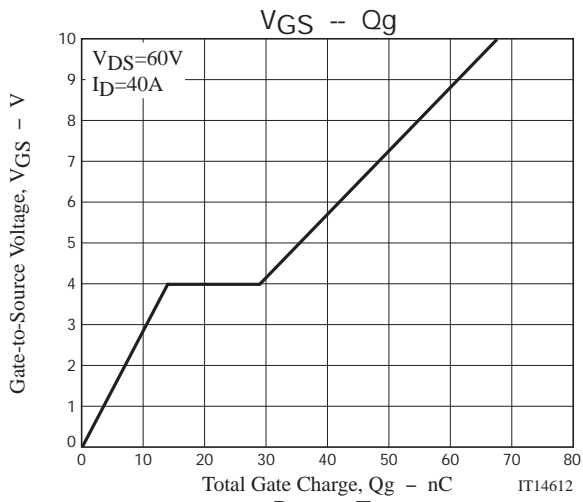
Avalanche Resistance Test Circuit



Ordering Information

Device	Package	Shipping	memo
ATP405-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free





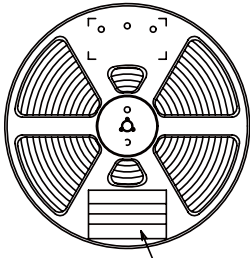
Taping Specification

ATP405-TL-H

1. Packing Format (TL)

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

Packing method



Reel label

Reel label, Inner box label
(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

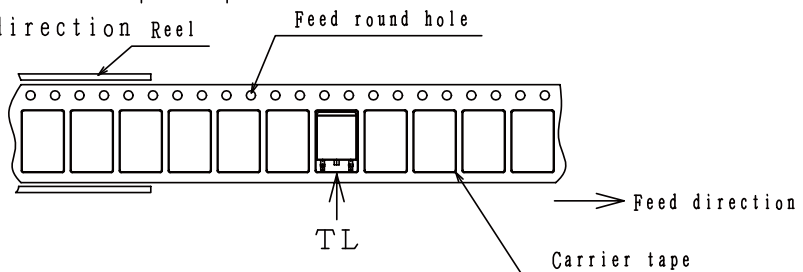
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel

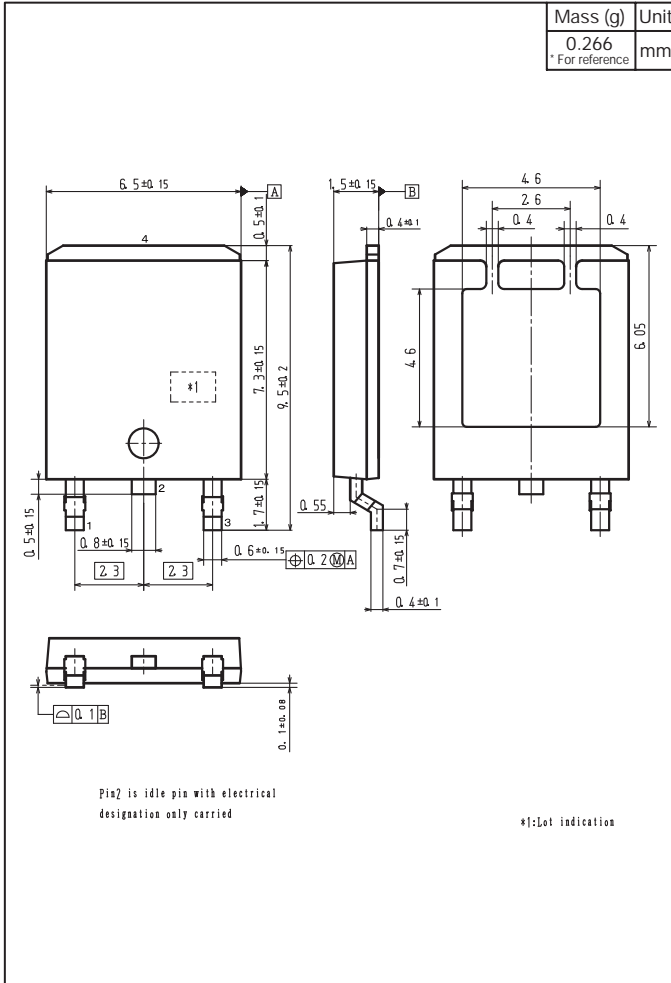


The one electrode terminals on feed hole side...TL

ATP405

Outline Drawing

ATP405-TL-H



Land Pattern Example



Note on usage : Since the ATP405 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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