GS6150 Multi-Rate 6G UHD-SDI Reclocker

Gennum Products

Key Features

- SMPTE ST 2081, ST 424, ST 292, and ST 259-C compliant
- Supports retiming data at rates of 125Mb/s, 270Mb/s, 1.485 and 1.485/1.001Gb/s, 2.97 and 2.97/1.001Gb/s, 5.94 and 5.94/1.001Gb/s
- Supports retiming of DVB-ASI signals
- Automatic or Manual Rate Selection
  - Detected rate indication in Auto Mode
- 4:1 input selector patented technology
- Option of two reclocked data outputs
- Four configurable GPIO pins with ability to output device status, including:
  - Lock Detect
  - Loss of Signal (LOS)
  - Low/High bit-rate indication for slew-rate control of SDI cable drivers
- On-chip 100Ω differential input and output termination
- Bypass support for rates up to 5940Mb/s
  - Manual Bypass function
  - Configurable automatic Bypass when not locked
- Option to use external reference or operate referenceless
- Cascading reference buffer supports multiple reclockers using a single reference source
- Input signal equalization and output signal de-emphasis to compensate for trace dielectric losses
- Single power supply operation at 1.8V
- 130mW typical power consumption (150mW with second output enabled)
- Pb-free and RoHS compliant
- Operating temperature range: -40°C to 85°C

Applications

- SMPTE ST 2081, SMPTE ST 424, SMPTE ST 292, SMPTE ST 259-C coaxial cable serial digital interfaces
- EN50083-9 DVB-ASI interfaces
- MADI standard

Description

The GS6150 is a low-power, multi-rate serial digital reclocker designed to automatically recover the embedded clock from a digital video signal and re-time the incoming video data.

The GS6150 will recover the embedded clock signal and re-time the data from 6G UHD-SDI signals compliant with SMPTE ST 2081. In addition, it can also re-time SMPTE ST 259-C, SMPTE ST 292, SMPTE ST 424 or DVB-ASI compliant digital video signals as well as MADI audio streams.

The GS6150 features four high-speed differential signal inputs feeding a 4:1 input selector. Input termination is on-chip for seamless matching to 100Ω differential transmission lines. The input selector is a component of a video switching system with tightly constrained timing requirements.

The GS6150 includes programmable trace equalization to compensate for high-frequency losses associated with board-level interconnect.

Two CML outputs interface seamlessly to devices with a CML input reference between 1.2V and 2.5V. Programmable output swing and de-emphasis provide flexibility in managing signal integrity of the output signals.

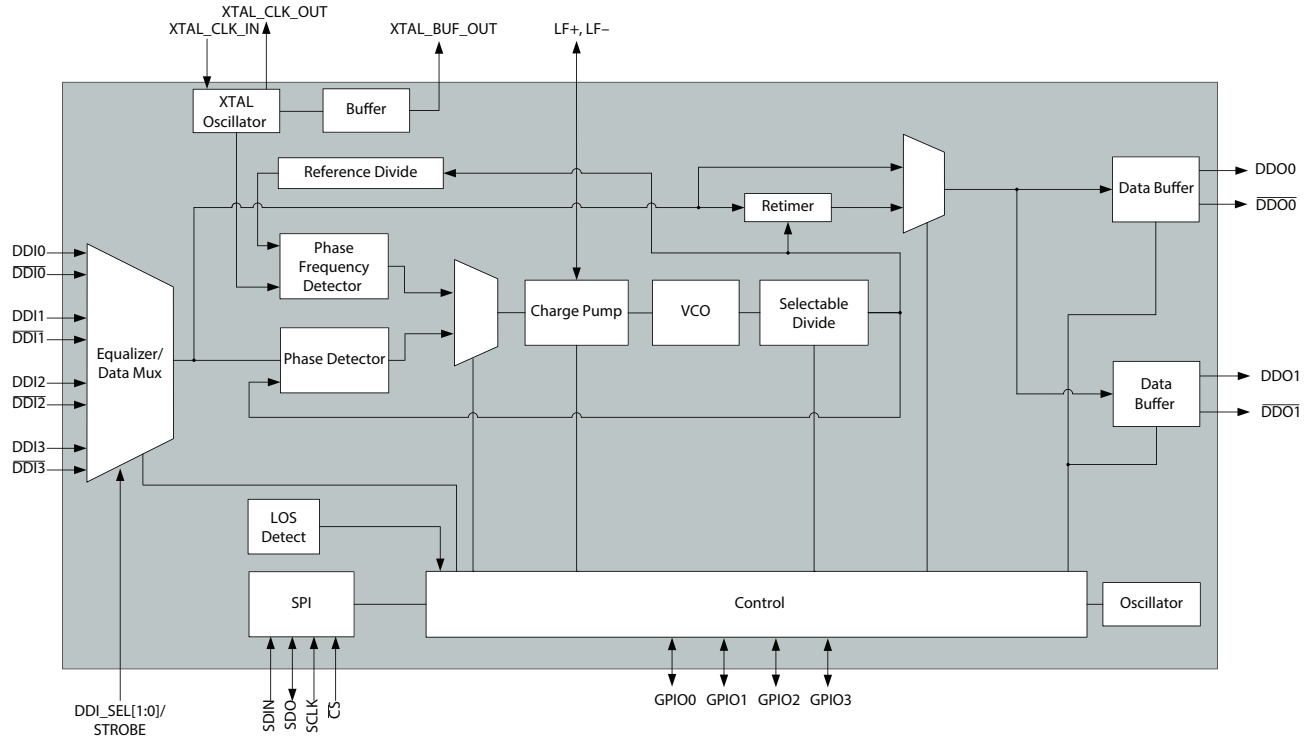
The GS6150 can operate in either automatic rate detection or manual rate selection mode. In auto mode the device will automatically detect and lock onto incoming data signals at any supported rate.

The device can operate without an external 27MHz frequency reference. For applications which require rapid signal lock, an external 27MHz reference may be used to set the VCO frequency when not locked to the input signal. The presence of an external reference crystal is automatically detected by the device.

In systems that require passing of non-supported data rates, the GS6150 can be configured to either automatically or manually enter a bypass mode in order to pass the signal without reclocking.

A four-wire serial Gennum Serial Peripheral Interface (GSPI) facilitates configuration and status monitoring of the device. Multiple GS6150 devices can be daisy-chained together with a single 4-pin connection to the host system.

This device is Pb-free, and the encapsulation compound does not contain halogenated flame retardant. This component and all homogenous sub-components are RoHS compliant.



GS6150 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
2	024967	—	March 2015	Updated Table 2-2 and Table 2-3. Updated Section 4.11 and Section 5. Updated to Final Data Sheet.
1	022115	—	September 2014	Changed product title. Updated Table 5-1 format. Updates throughout Table 2-2 and Table 2-3. Added Section 4.5.5. Updated Table 5-1.
0	016784	—	December 2013	New Document

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1. Pin Out

1.1 Pin Assignment

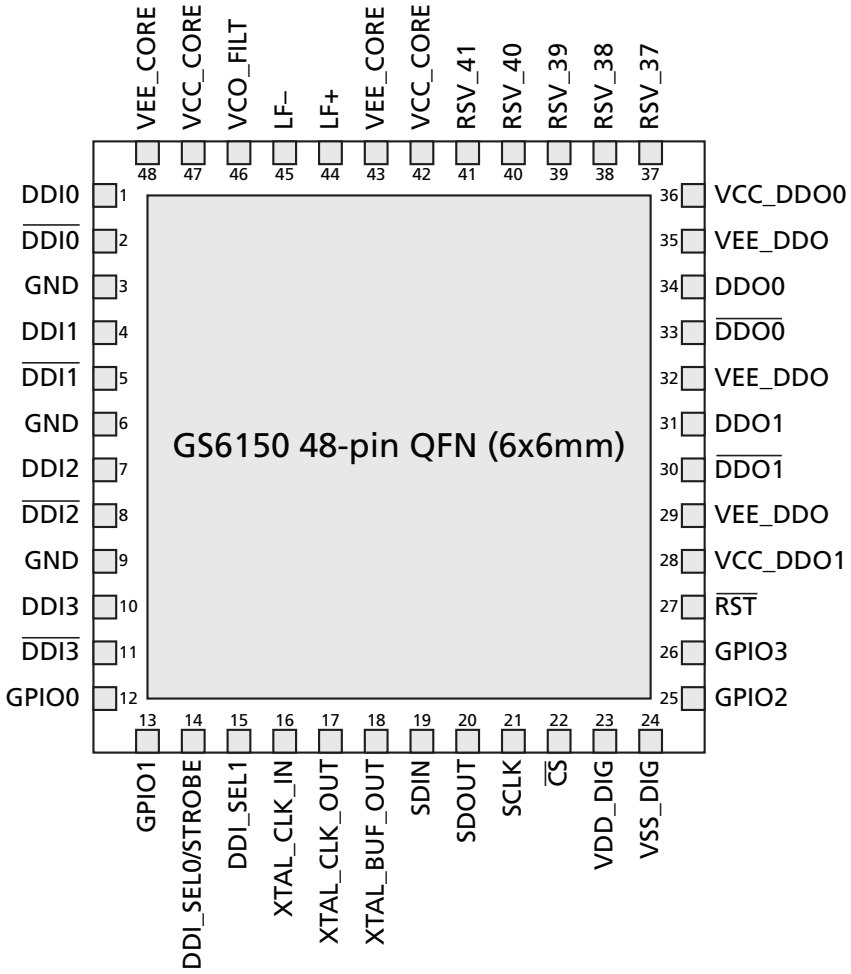


Figure 1-1: GS6150 Pin Out

1.2 Pin Descriptions

Table 1-1: GS6150 Pin Descriptions

Pin Number	Name	Type	Description
1, 2	DDI0, $\overline{\text{DDI0}}$	Input	Serial Digital Differential Input 0.
3, 6, 9	GND	Power	Input channel isolation. Connect to ground or leave unconnected.
4, 5	DDI1, $\overline{\text{DDI1}}$	Input	Serial Digital Differential Input 1.
7, 8	DDI2, $\overline{\text{DDI2}}$	Input	Serial Digital Differential Input 2.
10, 11	DDI3, $\overline{\text{DDI3}}$	Input	Serial Digital Differential Input 3.
12	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Signal options are: LOS (output; default) LOCKED LBR_HBR RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE This pin is configured using the GPIO0_SELECT and GPIO0_IO_SELECT bits in the GPIO_CONTROL_REG_0 register.
13	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Signal options are: LOS LOCKED (output; default) LBR_HBR RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE This pin is configured using the GPIO1_SELECT and GPIO1_IO_SELECT bits in the GPIO_CONTROL_REG_0 register.

Table 1-1: GS6150 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
14, 15	DDI_SEL0/STROBE, DDI_SEL1	Logic Input	Input selection control. Used to select the high-speed input for processing through the device. Refer to Table 4-1 for details on input selection.
16	XTAL_CLK_IN	Input	Reference Crystal Pin/27MHz clock input. Connect to an external circuit as shown in Figure 6-1: GS6150 Typical Application Circuit or to a digital clock source (XTAL_BUF_OUT of another GS6150 or GS6151). Connect to ground if operating referenceless.
17	XTAL_CLK_OUT	Output	Reference Crystal Pin. Connect to a external circuit as shown in Figure 6-1: GS6150 Typical Application Circuit, or leave unconnected if XTAL_CLK_IN is driven by an external clock source or if XTAL_CLK_IN is connected to ground (referenceless).
18	XTAL_BUF_OUT	Output	Buffered clock reference output. Leave unconnected if not used to drive 27MHz clock input of another device.
19	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Refer to 4.11 GSPI Host Interface for more details.
20	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Refer to 4.11 GSPI Host Interface for more details.
21	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Refer to 4.11 GSPI Host Interface for more details.
22	$\overline{CS}$	Digital Input	Chip select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-low input. Refer to 4.11 GSPI Host Interface for more details.
23	VDD_DIG	Power	Most positive power supply for the internal logic Connect to 1.8V.
24	VSS_DIG	Power	Most negative power supply for the internal logic Connect to ground.

Table 1-1: GS6150 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
25	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Signal options are: LOS LOCKED LBR_HBR (output; default) RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE This pin is configured using the GPIO2_SELECT and GPIO2_IO_SELECT bits in the GPIO_CONTROL_REG_1 register.
26	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Signal options are: LOS LOCKED LBR_HBR RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE (input; default) This pin is configured using the GPIO3_SELECT and GPIO3_IO_SELECT bits in the GPIO_CONTROL_REG_1 register.
27	$\overline{\text{RST}}$	Digital Input	Reset pin. If set LOW, all blocks set to default conditions and inputs/outputs set to high impedance. If HIGH, normal operation of the device resumes. By default, internally pulled HIGH.
28	VCC_DDO1	Power	Most positive power supply connection for the DDO1/$\overline{\text{DDO1}}$ output driver. Connect to any voltage between 1.2V and 2.5V.
29, 32, 35	VEE_DDO	Power	Most negative power supply connections for the output drivers. Connect to ground.
30, 31	$\overline{\text{DDO1}}$, DDO1	Output	Differential serial data output 1.
33, 34	$\overline{\text{DDO0}}$, DDO0	Output	Differential serial data output 0.
36	VCC_DDO0	Power	Most positive power supply connection for the DDO0/$\overline{\text{DDO0}}$ output driver. Connect to any voltage between 1.2V and 2.5V.

Table 1-1: GS6150 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
37	RSV_37	Power Decoupling	Connect through decoupling capacitor to ground.
38	RSV_38	Power	Connect to 1.8V.
39	RSV_39	Power	Connect to ground.
40, 41	RSV_40, RSV_41	Input	Leave unconnected.
42	VCC_CORE	Power	Most positive power supply connection to the analog core Connect to 1.8V.
43	VEE_CORE	Power	Most negative power supply connection to the analog core Connect to ground.
44	LF+	Passive	Connect to LF– through C_{LF} Refer to Figure 6-1: GS6150 Typical Application Circuit.
45	LF–	Passive	Connect to LF+ through C_{LF} Refer to Figure 6-1: GS6150 Typical Application Circuit.
46	VCO_FILT	Power	External decoupling for the VCO. Refer to Figure 6-1: GS6150 Typical Application Circuit.
47	VCC_CORE	Power	Most positive power supply connection for the analog core Connect to 1.8V.
48	VEE_CORE	Power	Most negative power supply connection to the analog core Connect to ground.
—	Center Pad	Power	Ground pad on bottom of package.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage – Core (VCC_CORE, VDD_DIG)	–0.5 to +2.1V_{DC}
Supply Voltage – Output Driver (VCC_DDO0, VCC_DDO1)	–0.5 to +2.8V_{DC}
Input ESD Voltage	4kV
Storage Temperature Range (T_S)	–50ºC to +125ºC
Operating Temperature Range (T_A)	–40ºC to +85ºC
Input Voltage Range (any input pin)	–0.3 to (V_{CC_CORE} + 0.3)V_{DC}
Solder Reflow Temperature	+260ºC

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= –40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage – Core (VCC_CORE, VDD_DIG)	V_{CC_CORE}, V_{DD_DIG}	—	1.710	1.8	1.890	V	
Supply Voltage – Output Driver (VCC_DDO0, VCC_DDO1)	V_{CC_DDO0}, V_{CC_DDO1}	—	1.140	—	2.625	V	

Table 2-2: DC Electrical Characteristics (Continued)

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= –40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Power	P_D	Data Rate 6G, DDO1/$\overline{\text{DDO1}}$ disabled	—	140	185	mW	1, 2
		Data Rate <6G, DDO1/$\overline{\text{DDO1}}$ disabled	—	130	170	mW	1, 2
		Data Rate 6G, Default Settings, DDO1/$\overline{\text{DDO1}}$ enabled	—	210	280	mW	3, 4
		Data Rate <6G, Default Settings, DDO1/$\overline{\text{DDO1}}$ enabled	—	190	255	mW	3, 4
		Maximum Supply and Power Settings	—	280	360	mW	5
Power (Sleep operation)	P_{SLEEP}	—	—	20	35	mW	
Power (Standby operation)	$P_{STANDBY}$	—	—	80	110	mW	
Supply Current - Output Driver	I_{CC_DDO0}, I_{CC_DDO1}	Output Swing Register Setting = 0000_b	—	4.8	7	mA	6, 7
		Output Swing Register Setting= 0100_b	—	7.5	12	mA	6, 7
		Output Swing Register Setting = 1100_b	—	15	22	mA	6, 7
Supply Current - Core	I_{CC_CORE}	Output De-emphasis Disabled Data Rate 6G	—	82	—	mA	8
		Output De-emphasis Disabled Data Rate 3G	—	74	—	mA	8
		Output De-emphasis Enabled Data Rate 6G	—	90	—	mA	8
		Output De-emphasis Enabled Data Rate 3G	—	81	—	mA	8
Supply Current - Digital	I_{CC_DIG}	External Crystal Referenced	—	7	12	mA	
Serial Input Termination		Differential	75	100	125	Ω	
Serial Output Termination		Differential	75	100	125	Ω	
Serial Input Common Mode Voltage	V_{CMIN}	—	0.9	—	V_{CC_CORE} - 50mV	V	9, 10

Table 2-2: DC Electrical Characteristics (Continued)

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= –40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, CLK, GPIO[0:3])	V_{IH}	—	0.65* VDD_DIG	—	VDD_DIG	V	
	V_{IL}	—	0	—	0.35* VDD_DIG	V	
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -2mA	VDD_DIG – 0.45	—	—	V	
	V_{OL}	I_{OL} = 2mA	—	—	0.45	V	

Notes:

1. Normal operation in referenceless mode, minimum output swing with de-emphasis disabled
2. VCC_DDO0/1 = 1.2V
3. The swing is default and de-emphasis is on
4. VCC_DDO0/1 = 1.8V
5. DDO0/$\overline{DDO0}$ and DDO1/$\overline{DDO1}$ set to maximum swing setting, external crystal reference used
6. Consumption per enabled DDO output
7. Refer to Table 4-3 for the exact register settings for each ΔV_{DDO} output swing listed
8. For two enabled outputs
9. Maximum input voltage level = 1.8V ± 5%
10. Up to a maximum swing of 800mV

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= –40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Data Rate (Bypass)	DR_{BYPASS}	Bypass mode enabled	3	—	5940	Mb/s	1
Input Sensitivity	ΔV_{SDI}	Differential	200	—	800	mV_{ppd}	
Output Voltage Swing	ΔV_{DDO}	Output Swing Register Setting = 0100_b	310	410	510	mV_{ppd}	2
		Output Swing Register Setting = 1100_b	600	800	1000	mV_{ppd}	2
Serial Input Jitter Tolerance	IJT	Square wave modulation	0.8	—	—	UI	
PLL Lock Time — Asynchronous	t_{ALOCK}	Referenceless	—	—	50	ms	
		With External Reference (MADI enabled)	—	—	30	ms	
		With External Reference (MADI disabled)	—	—	20	ms	

Table 2-3: AC Electrical Characteristics (Continued)

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= –40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Lock Time — Synchronous	t_{SLOCK}	Referenceless	—	—	10	µs	
		With External Reference	—	—	10	µs	
Serial Data (DDO0 and DDO1) Output Rise And Fall Time	$t_{riseDDO}$	20% ~ 80% rising edge into 50Ω load	—	—	70	ps	
	$t_{fallDDO}$	20% ~ 80% falling edge into 50Ω load	—	—	70	ps	
Rise And Fall Time Mismatch (DDO0 and DDO1)	—	—	—	—	15	ps	
Duty Cycle Distortion (DDO0 and DDO1)	—	Data Rate 6G	—	—	10	%	
	—	Data Rate < 6G	—	—	5	%	
Serial Data Output Jitter Intrinsic	$t_{OJ(125Mb/s)}$	BW = Nominal PRN 2^{23} – 1 test pattern	—	0.02	0.03	UI_{P-P}	3, 4
	$t_{OJ(270Mb/s)}$		—	0.02	0.03	UI_{P-P}	3, 4
	$t_{OJ(1485Mb/s)}$		—	0.03	0.06	UI_{P-P}	3, 4
	$t_{OJ(2970Mb/s)}$		—	0.04	0.09	UI_{P-P}	3, 4
	$t_{OJ(5940Mb/s)}$		—	0.07	0.13	UI_{P-P}	3, 4
	$t_{OJ(BYPASS)}$		—	0.06	0.09	UI_{P-P}	3, 4
PLL Loop Bandwidth	$BW_{LOOP(125Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	37	—	kHz	
		PLL_LOOP_BANDWIDTH = 00010	—	74	—	kHz	
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	148	—	kHz	
		PLL_LOOP_BANDWIDTH = 01000	—	296	—	kHz	
		PLL_LOOP_BANDWIDTH = 10000	—	590	—	kHz	
	$BW_{LOOP(270Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	80	—	kHz	
		PLL_LOOP_BANDWIDTH = 00010	—	160	—	kHz	
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	320	—	kHz	
		PLL_LOOP_BANDWIDTH = 01000	—	640	—	kHz	
		PLL_LOOP_BANDWIDTH = 10000	—	1.28	—	MHz	

Table 2-3: AC Electrical Characteristics (Continued)

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A = –40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	$BW_{LOOP(1485Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	438	—	kHz	
		PLL_LOOP_BANDWIDTH = 00010	—	875	—	kHz	
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	1.75	—	MHz	
		PLL_LOOP_BANDWIDTH = 01000	—	3.5	—	MHz	
		PLL_LOOP_BANDWIDTH = 10000	—	7	—	MHz	
	$BW_{LOOP(2970Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	875	—	kHz	
		PLL_LOOP_BANDWIDTH = 00010	—	1.75	—	MHz	
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	3.5	—	MHz	
		PLL_LOOP_BANDWIDTH = 01000	—	7.0	—	MHz	
		PLL_LOOP_BANDWIDTH = 10000	—	14.0	—	MHz	
	$BW_{LOOP(5940Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	1.75	—	MHz	
		PLL_LOOP_BANDWIDTH = 00010	—	3.5	—	MHz	
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	7.0	—	MHz	
		PLL_LOOP_BANDWIDTH = 01000	—	14.0	—	MHz	
		PLL_LOOP_BANDWIDTH = 10000	—	28.0	—	MHz	

Note:

1. Edge detection method for LOS detection should be used for data rates below 20Mb/s
2. Refer to Table 4-3 for the exact register settings for each ΔV_{DDO} output swing listed
3. Jitter measured using an oscilloscope according to SMPTE RP-184
4. Accumulated jitter measured peak to peak differential over 2000 hits

3. Input/Output Circuits

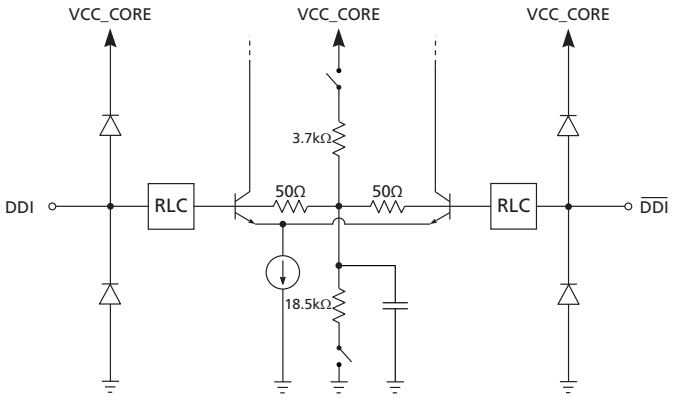


Figure 3-1: DDI0, $\overline{\text{DDI0}}$, DDI1, $\overline{\text{DDI1}}$, DDI2, $\overline{\text{DDI2}}$, DDI3, $\overline{\text{DDI3}}$ Serial Digital Differential Inputs

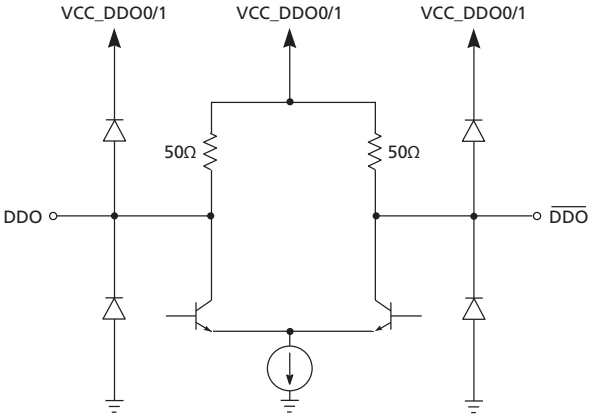


Figure 3-2: DDO0, $\overline{\text{DDO0}}$, DDO1, $\overline{\text{DDO1}}$ Serial Digital Differential Output

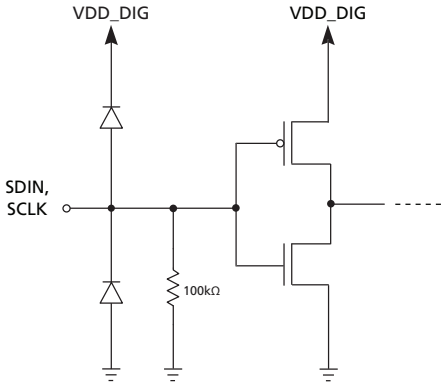


Figure 3-3: SDIN and SCLK

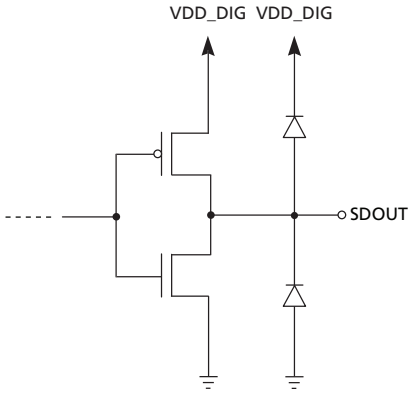


Figure 3-4: SDOUT

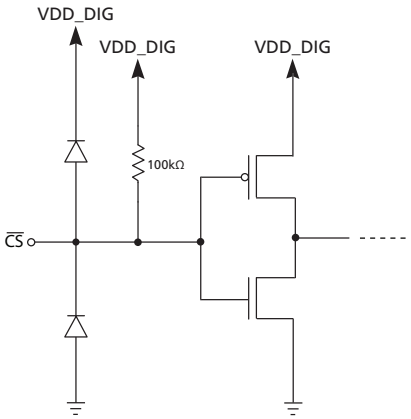


Figure 3-5: $\overline{\text{CS}}$

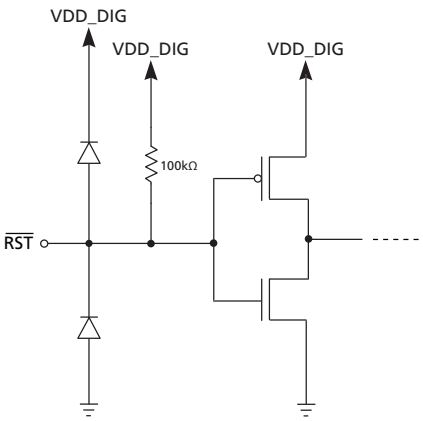


Figure 3-6: $\overline{\text{RST}}$

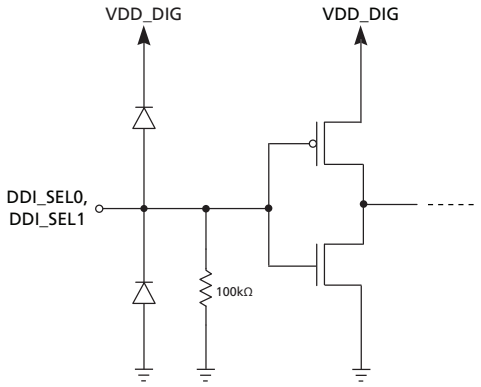


Figure 3-7: DDI_SEL0/STROBE and DDI_SEL1

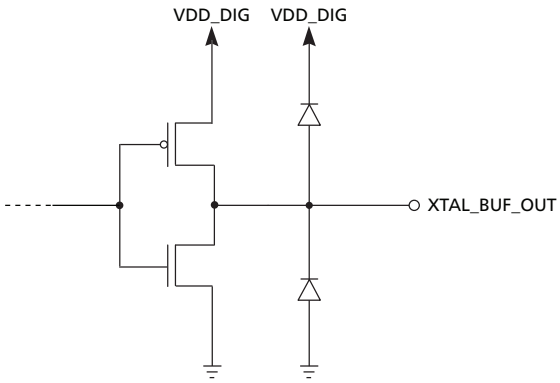


Figure 3-8: XTAL_BUF_OUT

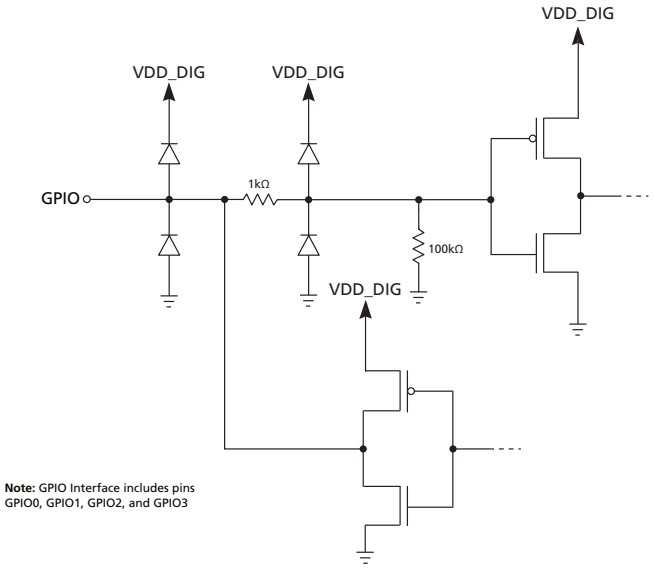


Figure 3-9: General Purpose Inputs/Outputs (GPIO)

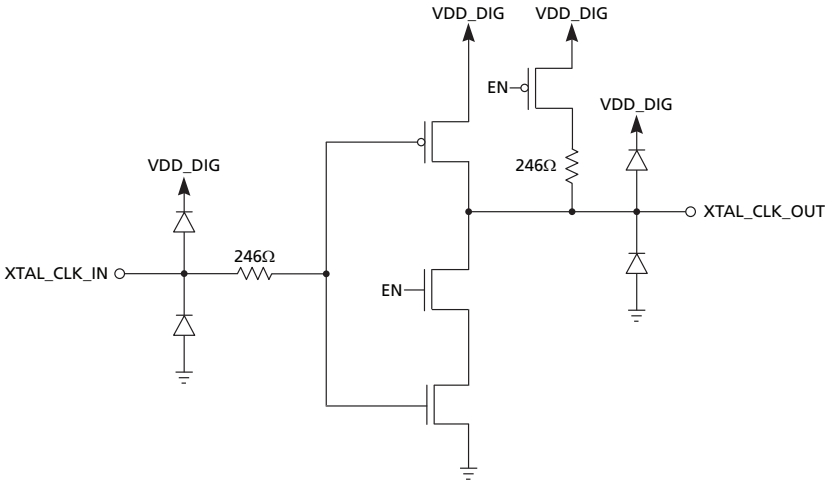


Figure 3-10: XTAL_CLK_IN and XTAL_CLK_OUT

4. Detailed Description

The GS6150 is a multi-standard reclocker for serial digital SDTV SDI and DVB-ASI signals operating at 270Mb/s, HDTV SDI signals operating at 1.485Gb/s and 1.485/1.001Gb/s, 3G SDI signals operating at 2.97Gb/s and 2.97/1.001Gb/s, and 6G UHD-SDI signals operating at 5.94Gb/s and 5.94/1.001Gb/s and MADI audio streams at 125Mb/s.

4.1 Serial Data Inputs

The GS6150 features four 100Ω terminated differential input buffers.

A serial data input signal may be connected to any of the following input pin pairs of the device: DDI0/$\overline{\text{DDI0}}$, DDI1/$\overline{\text{DDI1}}$, DDI2/$\overline{\text{DDI2}}$, and DDI3/$\overline{\text{DDI3}}$.

By default, the self-biasing circuit at the input is enabled to allow AC coupling to upstream devices. To enable DC coupling of the inputs, the user must disable the self-biasing network by setting bits 4:4 through 5:5 to 0 in the register 7_h: DDI[0:1]_TRACE_EQ_DC_TERM_ENABLE.

In order to select DC coupling, please ensure that the output common mode of the upstream device is in range of the input common mode voltage range shown in Table 2-2.

The serial digital input buffer is capable of operation with any binary coded signal that meets the input signal level requirements defined below, with any data rate between 3Mb/s and 5.94Gb/s.

4.1.1 Input Trace Equalization

The GS6150 features adjustable trace equalization to compensate for PCB trace dielectric losses up to half the maximum supported data rate, or 3GHz. The equalization has three settings: the LOW (default) setting is optimized for compensating the high-frequency losses associated with 0-7dB of trace loss at 1.5GHz for data rates of 2.97Gb/s and below, and for 0-10dB of trace loss at 3GHz for 5.94Gb/s. The HIGH setting is optimized for trace loss between 7-14dB at 1.5GHz for data rates 2.97Gb/s and below. The 0dB or EQ_BYPASS setting may be used in systems with negligible trace loss. These settings are selected using the DDI0_TRACE_EQ_CONTROL, DDI1_TRACE_EQ_CONTROL, DDI2_TRACE_EQ_CONTROL and DDI3_TRACE_EQ_CONTROL bits in the INPUT_CONTROL_REG_0 register at address 5_h.

The default state of the device is input trace equalization on all inputs set to LOW.

4.1.2 Input Selection

The GS6150 incorporates a 4:1 input selector which allows the connection of four independent streams of video/data.

The selector is controllable in three separate ways:

1. The DDI_SEL0 and DDI_SEL1 pins can be used to select the input.
2. A GSPI accessible register can be used to select the input, with the state change occurring as soon as the register value changes.
3. A GSPI accessible register can be used to select the input, with a rising edge on the STROBE pin triggering a change to the next state.

Since these states are mutually exclusive, the DDI_SEL0 pin is shared with the STROBE function.

In the case of using the DDI_SEL0/STROBE and DDI_SEL1 pins (#1 above) or the STROBE pre-select method (#3 above), the input selector will switch within 1µs of the change of state on the corresponding pin(s). This strict timing requirement is not maintained when using GSPI register selection (#2 above).

Each of the device's four inputs is selected as shown in Table 4-1.

Table 4-1: Pin and Register Settings for Input Selection

Register Settings			Pin Settings		Differential High-speed Input Selected
INPUT_SELECTION_CONTROL 7_h[9:8]	DDI_SELECT 7_h[11]	DDI_SELECT 7_h[10]	DDI_SEL1	DDI_SEL0/ STROBE	
X0 (default)	X	X	LOW	LOW	DDI0, $\overline{\text{DDI0}}$
X0 (default)	X	X	LOW	HIGH	DDI1, $\overline{\text{DDI1}}$
X0 (default)	X	X	HIGH	LOW	DDI2, $\overline{\text{DDI2}}$
X0 (default)	X	X	HIGH	HIGH	DDI3, $\overline{\text{DDI3}}$
01	0	0	X	X	DDI0, $\overline{\text{DDI0}}$
01	0	1	X	X	DDI1, $\overline{\text{DDI1}}$
01	1	0	X	X	DDI2, $\overline{\text{DDI2}}$
01	1	1	X	X	DDI3, $\overline{\text{DDI3}}$
11	0	0	X	on LOW-to-HIGH transition	DDI0, $\overline{\text{DDI0}}$
11	0	1	X	on LOW-to-HIGH transition	DDI1, $\overline{\text{DDI1}}$
11	1	0	X	on LOW-to-HIGH transition	DDI2, $\overline{\text{DDI2}}$
11	1	1	X	on LOW-to-HIGH transition	DDI3, $\overline{\text{DDI3}}$

Note: 'X' indicates 'Do Not Care'

The DDI_SEL0/STROBE and DDI_SEL1 pins include internal pull-downs, which pulls the input voltage LOW if either pin is unconnected.

When using the STROBE pre-select method (#3 above), the pre-selected input buffer and trace EQ is powered up in advance of the STROBE pulse.

4.2 Reference Clock

The GS6150 can operate with or without an external frequency reference. For applications requiring rapid asynchronous locking, a 27MHz reference or crystal is required.

The PLL lock times for both referenceless and external crystal reference operation are given in Table 2-3: AC Electrical Characteristics.

If a reference is connected to the XTAL_CLK_IN pin or a crystal is connected to the XTAL_CLK_IN and XTAL_CLK_OUT pins of the device, it will automatically be used as the reference frequency for rapid asynchronous lock. If XTAL_CLK_IN is not connected to a crystal, XTAL_CLK_OUT must be left unconnected.

The XTAL_CLK_IN pin operates correctly when connected directly to the XTAL_BUF_OUT from another GS6150, or a 27MHz output of a different device.

4.3 Signal Monitoring

The GS6150 measures and reports the following signal status and quality monitoring parameters:

- Loss of Signal
- Lock Detection
- Rate Detection
- Low/High Bit Rate Detection

4.3.1 Loss of Signal Detection

LOS (Loss of Signal) detection is an active HIGH output available to the application on any of the GPIO[3:0] multi-function status and control pins. It is selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 and GPIO_CONTROL_REG_1 registers. It is the default output of the GPIO0 pin.

LOS indicates when the serial digital signal selected by the input selector is invalid. This function is always active.

Two methods can be used to detect loss of signal: strength (default) and edge. Either method can be selected with LOS_DETECTION_METHOD bits of register PLL_CONTROL.

When strength detection is used as the method of LOS detection the corresponding GPIO pin will be HIGH (signal lost) when the input signal amplitude within a predefined window falls below the threshold set by the bits DDI[0:3]_LOS_THRESHOLD_CONTROL in the LOS_CONTROL_REG_1 and LOS_CONTROL_REG_2 registers. The LOS threshold hysteresis can be set by the LOS_HYSTERESIS bits in the LOS_CONTROL_REG_0 register at address F_h.

The corresponding GPIO pin will be LOW (signal present) when the input signal amplitude within a predefined window is above the defined threshold.

The method of strength detection is measurement of the average rectified differential voltage on the input pins. The strength detection method is therefore inherently dependent on the input signal's eye shape, particularly the rise/fall times of the input signal relative to the data rate. Additionally, the circuit has a lower bandwidth limit of operation (20Mb/s) below which it is recommended that the edge detection method is used. The absolute value of the threshold can be determined for any input swings according to Equation 4-1 below:

$$\text{Threshold} = \frac{1.9\text{mV} \times (\text{DDI[0..3]_LOS_THRESHOLD_CONTROL}) \times 53}{(\text{DEVICE_SPECIFIC_LOS_THRESHOLD})} \qquad \text{Equation 4-1}$$

where DEVICE_SPECIFIC_LOS_THRESHOLD specifies the LOS threshold value for a 100mV input swing at SD-rate specific to each device. The other rates scale according to the fractional relationship given in Figure 4-1 and Figure 4-2 below.

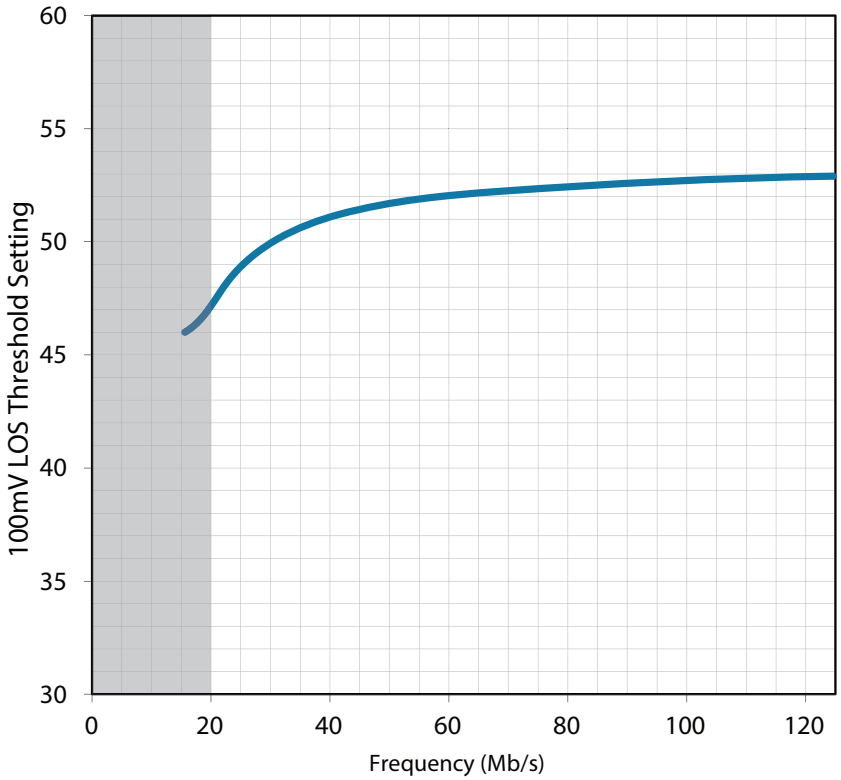


Figure 4-1: LOS Threshold at 100mV Input Swing vs. Low Frequency Rates for a Nominal DEVICE_SPECIFIC_LOS_THRESHOLD of 53

Note: Edge detection method is recommended for signals in shaded areas.

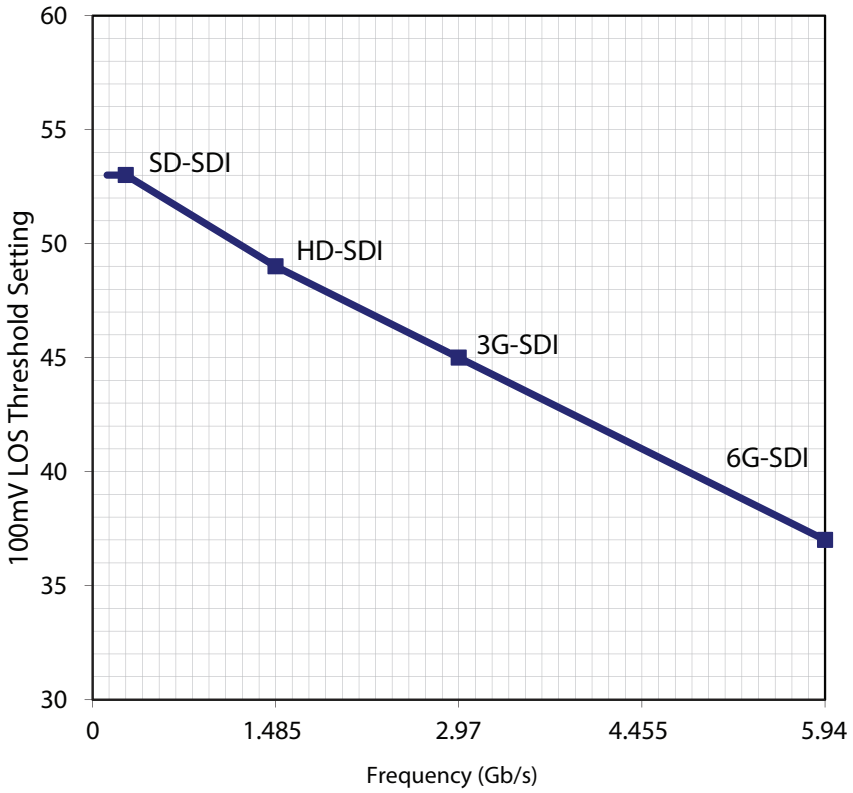


Figure 4-2: LOS Threshold at 100mV Input Swing vs. SDI Data Rates for a Nominal DEVICE_SPECIFIC_LOS_THRESHOLD of 53

Strength detection is unaffected by the Trace EQ settings in INPUT_CONTROL_REG_0.

When edge detection is used as the method of LOS detection the corresponding GPIO pin will be HIGH (signal lost) when no transitions are detected on the selected input. The corresponding GPIO pin will be LOW (signal present) when transitions are detected on the input. The LOS status is also available through the LOS bit in the PLL_STATUS register, and as a sticky status through the LOS_STICKY bit in the STICKY_STATUS register at address 50_h.

4.3.2 Lock Detection

The GS6150 lock detection circuitry outputs a LOCKED status signal which indicates that the CDR has achieved phase lock to the incoming data stream. The LOCKED signal is an active HIGH output available to the application on any of the GPIO[3:0] multi-function status and control pins. It is selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 and GPIO_CONTROL_REG_1 registers. By default, LOCKED is output on GPIO1.

The LOCKED status is available from the LOCKED bit in the PLL_STATUS register, and the LOCK_LOST_STICKY bit in the STICKY_STATUS register indicates whether lock has been lost since the bit was last cleared.

To optimize systems with high DCD and/or high residual ISI the LOCK_SAMPLE bit of the PD_CONTROL register should be set to 1_b in conjunction with reducing the Loop Bandwidth.

4.3.2.1 Synchronous and Asynchronous Lock Time

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes.

The synchronous lock time is defined as the time it takes the device to lock to a signal which has been momentarily interrupted.

The asynchronous and synchronous lock times are defined in Table 2-3: AC Electrical Characteristics.

To qualify for synchronous lock time, the maximum interruption time of the signal is 10µs for a 270Mb/s signal. 1.485Gb/s, 2.97Gb/s, and 5.94Gb/s signals, as well as their f/1.001 components have a maximum interruption time of 6µs. The new signal, after interruption, must have the same frequency as the original signal but can have arbitrary phase.

4.3.3 Rate Detection

The GS6150 can be manually forced to lock to a specific supported data rate, or automatically search for and lock to supported rates. The selection between manual and automatic rate selection is through the FORCE_PLL_RATE and FORCE_PLL_RATE_ENABLE bits of the PLL_CONTROL register at address $4C_h$. By default the device is set to automatically search for supported SDI rates.

When set to automatically detect supported data rates, the device repeatedly cycles through each supported rate that is enabled through the RATE_ENABLE_5G94, RATE_ENABLE_2G97, RATE_ENABLE_1G485, RATE_ENABLE_270M and RATE_ENABLE_125M bits of the PLL_CONTROL register, until the device phase locks to one of the enabled rates. If lock is lost the rate search resumes, continuously testing for each rate in sequence until lock is regained.

The device reports the current data rate setting of the automatic rate search state machine through the DETECTED_RATE bits in the PLL_STATUS register at address $4F_h$. Each bit of DETECTED_RATE is also available to output through the GPIO pins, selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 register. The supported rates that the DETECTED_RATE bits can output are shown in Table 4-2 below.

Table 4-2: Automatic Rate Detection - Supported Data Rates

DETECTED_RATE	Data Rate
000	125Mb/s – MADI
001	270Mb/s – SD
010	1.485Gb/s – HD
011	2.97Gb/s – 3G
100	5.94Gb/s – 6G

4.3.4 Low/High Bit Rate Detection for Slew Rate Control

A status output named LBR_HBR is provided to control the slew rate selection input of a downstream SDI cable driver. It can be connected to the SD_EN input of drivers such as the GS6080 or GS6081 using the Semtech recommended application circuit.

When this signal is HIGH, the data rate is 270Mb/s (SD) or 125Mb/s (MADI). This signal is LOW for all other supported data rates, and when the GS6150 is operating in Bypass Mode or any time the device is not locked.

The LBR_HBR output signal is available to the application on any of the GPIO[3:0] multifunction status and control pins. It is selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 and GPIO_CONTROL_REG_1 registers. By default, LBR_HBR is output on GPIO2.

4.4 Low Power Modes

The device can be programmed via the GSPI to operate in two different low power modes. SLEEP mode has minimum power consumption at the expense of recovery time upon de-assertion of the FORCE_PWRDN_SLEEP bit. STANDBY mode has higher power consumption relative to SLEEP mode but minimizes time to return to operation on de-assertion of the FORCE_PWRDN_STANDBY bit. The features affected by each mode are outlined below.

SLEEP mode:

- LOS detection remains functional
- The GSPI remains functional
- The reference oscillator remains functional

STANDBY mode:

- LOS detection remains functional
- The GSPI remains functional
- The reference oscillator remains functional
- The VCO and PLL remains functional so as to minimize the lock time when a signal is detected
- The rate detector remains set to the last valid data rate. On detection of a signal, the last valid rate is tested first by the rate detect state machine

The device can be programmed to automatically enter into SLEEP or STANDBY mode when LOS is asserted by programming the AUTO_PWRDN_DISABLE bit in the PWRDN_CONTROL register at address 17_h. The AUTO_PWRDN_MODE bit in the same register selects which mode, SLEEP or STANDBY, is entered into upon assertion of LOS.

4.5 Serial Data Output

The GS6150 has two current-mode differential output drivers, each capable of driving up to $1V_{pp}$ differential into an external 100Ω differential load.

The output drivers operate with any binary coded signal with supported data rates up to 5.94Gb/s. This is applicable to both the serial data (DDO, $\overline{DDO}$) and serial data (DDO1, $\overline{DDO1}$) outputs of the device.

4.5.1 Output Impedance

Each of the GS6150's output buffers include two on-chip, 50Ω termination resistors.

4.5.2 Output Signal Interface Levels

The serial digital outputs operate within specification with an output CML power supply of 1.2V to 2.5V.

4.5.3 Adjustable Output Swing

Through the GSPI, the output swing can be set in the range from approximately $230mV_{ppd}$ to $930mV_{ppd}$ in $45mV_{ppd}$ increments, when the outputs are terminated with 50Ω loads. For the exact values, please see Table 4-3 below.

The output swing for each data rate is controlled using the bits in the DRIVER_CONTROL_REG_3, DRIVER_CONTROL_REG_4, DRIVER_CONTROL_REG_5, and DRIVER_CONTROL_REG_6 registers at addresses $1C_h$ through $1F_h$.

The device automatically adjusts the swing setting depending on the state of the device (i.e. detected rate, bypass mode, or mute). There are separate register controls for mute, bypass and each data rate.

Table 4-3: Serial Digital Output Swing Settings

Register Setting (See Note 1)	Min	Typ	Max	Units
0000_b	175	230	290	mV
0001_b	205	275	345	mV
0010_b	245	325	405	mV
0011_b (default)	280	370	460	mV
0100_b	310	410	510	mV
0101_b	345	460	575	mV
0110_b	380	510	640	mV
0111_b	420	560	700	mV

Table 4-3: Serial Digital Output Swing Settings (Continued)

Register Setting (See Note 1)	Min	Typ	Max	Units
1000_b	455	605	760	mV
1001_b	490	655	820	mV
1010_b	530	705	880	mV
1011_b	565	755	945	mV
1100_b	600	800	1000	mV
1101_b	630	840	1050	mV
1110_b	670	890	1110	mV
1111_b	700	930	1160	mV

Note:

1. Applicable registers that can be programmed with the values shown above are DDO0_SWING_1G485, DDO0_SWING_270M, DDO0_SWING_125M, DDO0_SWING_BYPASS, DDO0_SWING_MUTE, DDO0_SWING_5G94, DDO0_SWING_2G97, DDO1_SWING_1G485, DDO1_SWING_270M, DDO1_SWING_125M, DDO1_SWING_BYPASS, DDO1_SWING_MUTE, DDO1_SWING_5G94, and DDO1_SWING_2G97

4.5.4 Output De-emphasis

The GS6150 features adjustable output de-emphasis to compensate for PCB dielectric trace loss. Each output can be independently set to a different de-emphasis setting for each detected rate through controls found in the DRIVER_CONTROL_REG_1 and DRIVER_CONTROL_REG_2 registers.

The effect of de-emphasis, illustrated in Figure 4-3, is to attenuate the swing of bits that do not follow a bit transition (V_{DE}). The swing of bits that do follow a bit transition (V_{nom}) is set by the output swing registers found in Section 4.5.3 and do not depend on the de-emphasis settings.

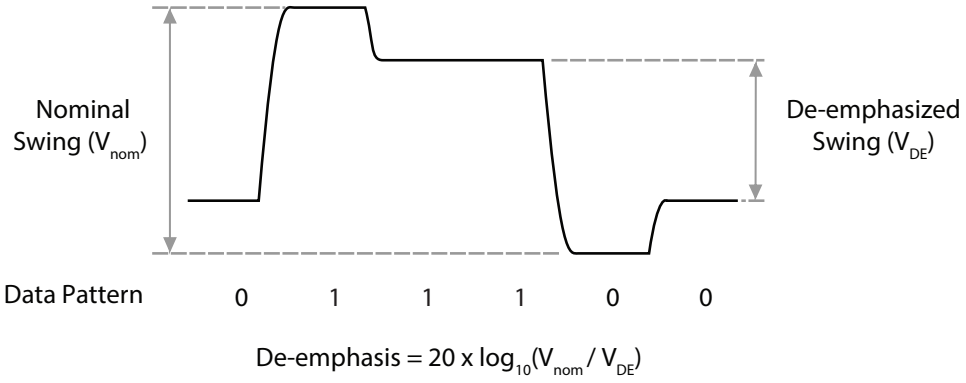


Figure 4-3: De-emphasis Waveform

The default de-emphasis settings for each rate are given in the register descriptions for DRIVER_CONTROL_REG_1 and DRIVER_CONTROL_REG_2 in Table 5-1. De-emphasis is disabled on both outputs in Bypass mode, when the output is muted, or when the device is not locked.

4.5.5 Output Common Mode Voltage

The output common mode voltage level (V_{CMOUT}) is a function of the output voltage swing, the output driver supply voltage (V_{CC_DDO}) and how the transmission line is terminated. If the outputs are terminated through 50Ω resistors to a voltage V_{TERM} equal to V_{CC_DDO}, as shown in Figure 4-5 below, the output common mode voltage is given by the following expression:

$$V_{CMOUT} = V_{CC_DDO} - \frac{\Delta V_{DDO}}{4} \qquad \text{Equation 4-2}$$

If the differential outputs are terminated across a 100Ω resistor, as shown in Figure 4-4 below, the output common mode voltage is given by the following expression:

$$V_{CMOUT} = V_{CC_DDO} - \frac{\Delta V_{DDO}}{2} \qquad \text{Equation 4-3}$$

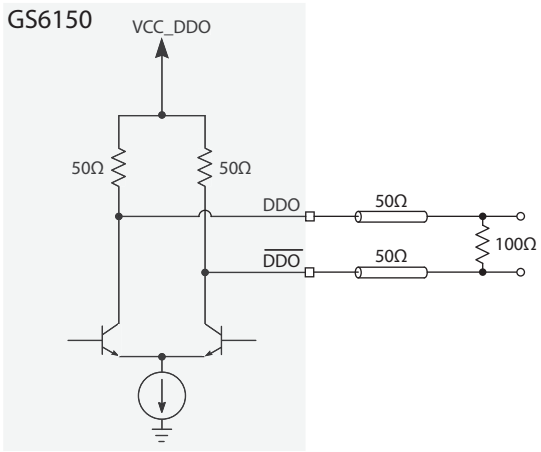


Figure 4-4: 100Ω Parallel Output Termination

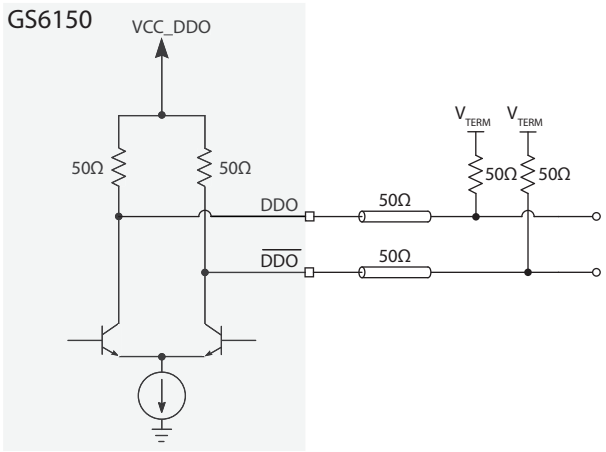


Figure 4-5: 50Ω Termination to V_{TERM}

4.6 Output Mute, Disable, and Data Selection

The GS6150 outputs can each be individually muted using the DDO0_MUTE and DDO1_MUTE bits in the DRIVER_CONTROL_REG_0 register at address 19_h.

Each output can also be independently disabled through either register or GPIO control. When disabled each pin of the output is pulled to V_{CC_DDO}. Register DRIVER_CONTROL_REG_0 contains both register based disable bits (DDO0_DISABLE, DDO1_DISABLE) and bits for selection between register and GPIO control (DDO0_DISABLE_SELECT, DDO1_DISABLE_SELECT). For GPIO control refer to Section 4.10.

By default DDO0, $\overline{\text{DDO0}}$ is enabled/disabled through register control and set to enabled. DDO1, $\overline{\text{DDO1}}$ is enabled/disabled through GPIO3 and set to output data.

4.7 Bypass Mode

In CDR Bypass mode, the GS6150 passes the input data to the outputs, bypassing the retiming functionality.

There are two bits in the control registers that control the bypass function: MANUAL_BYPASS and AUTO_BYPASS in the RECLOCKER_BYPASS register at address 20_h. The MANUAL_BYPASS bit is inactive (set to 0) by default. The AUTO_BYPASS bit is active (set to 1) by default, and places the GS6150 reclocker into bypass mode when the PLL is not locked to a data rate. The bypass function does not affect the trace equalization function of the device.

Note: If MANUAL_BYPASS is active, it overrides the AUTO_BYPASS bit setting.

4.8 DVB-ASI

The GS6150 has the ability to reclock DVB-ASI signals at 270Mb/s. All relevant settings and control registers that apply to SD-SDI signals at 270Mb/s are also compatible with DVB-ASI signals at 270Mb/s.

4.9 Device Power Up

4.9.1 Power on Reset (POR)

The GS6150 features an on-chip power-on-reset that places all registers and internal state machines into their known, default states when the chip is powered up.

4.9.2 Reset Pin ($\overline{\text{RST}}$)

When the $\overline{\text{RST}}$ pin is set LOW, all functional blocks are set to their default conditions and high-speed data and digital functionality is suspended. When it is set HIGH, normal operation of the device resumes 0.5ms after the LOW-to-HIGH transition of the signal. This pin is not required at power up and may be left unconnected.

4.10 GPIO Pins Configuration

The GS6150 has four GPIO pins that can each be configured as outputs for various internal status signals, or as inputs to disable either output-driver through pin control. The bits GPIO[0:3]_IO_SELECT are used to configure the GPIO pins as outputs (0) or inputs (1). The signals that are output or input on the GPIO pins are selected on GPIO_CONTROL_REG_0 and GPIO_CONTROL_REG_1. The signals that can be output on the GPIO pins are listed in Table 4-4 below.

Table 4-4: GPIO Status Outputs

GPIO[0:3]_SELECT	Parameter	Description
0000	LOS	Loss of signal indication - High when there is no detected signal on the selected DDI input
0001	LOCKED	Phase lock indication - High when the CDR has phase-locked to a valid input signal
0010	LBR_HBR	Low bit-rate/High bit-rate - High when the part is locked to the SD data rate; low for all other data rates and in bypass.
0101	RATE_DET0	Rate Detect - Three bits used in conjunction that represent the data rate detected by the rate search state machine. Refer to Table 4-2 for rate encoding details.
0110	RATE_DET1	
0111	RATE_DET2	
1000	LOCKED_125M	High when the rate search state machine is locked to a MADI data rate (125Mb/s)
1001	LOCKED_270M	High when the rate search state machine is locked to an SD data rate (270Mb/s)
1010	LOCKED_1G485	High when the rate search state machine is locked to an HD data rate (1.485Gb/s)
1011	LOCKED_2G97	High when the rate search state machine is locked to a 3G data rate (2.97Gb/s)
1100	LOCKED_5G94	High when the rate search state machine is locked to a 6G data rate (5.94Gb/s)
1101	RATE_CHANGE	When a change in the data rate is detected by the rate search state machine, the RATE_CHANGE signal is pulsed high for a duration of 37ns

The signals that can be input on the GPIOs are listed in Table 4-5 below.

Table 4-5: GPIO Signal Inputs

GPIO[0:3]_SELECT	Parameter	Description
0000	DDO0_DISABLE	Disables serial data output 0 ($\overline{\text{DDO0}}$, DDO0)
0001	DDO1_DISABLE	Disables serial data output 1 ($\overline{\text{DDO1}}$, DDO1)

By default, the GPIO pins are configured to the following parameters:

GPIO0: LOS (output)
GPIO1: LOCKED (output)
GPIO2: LBR_HBR (output)
GPIO3: DDO1_DISABLE (input)

4.11 GSPI Host Interface

The GS6150 is controlled via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (SDIN pin), serial data output signal (SDOUT pin), an active-low chip select ($\overline{CS}$ pin) and a burst clock (SCLK pin).

The GS6150 is a slave device, therefore the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

It is strongly recommended to connect the GSPI pins of the GS6150 to a host/system processor/controller or FPGA to facilitate optimization of the device to meet specific application requirements. Modification of many device settings is only facilitated through the GSPI of the GS6150, and is not available on external pins.

4.11.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-low signal provided by the host processor to the GS6150.

The high-to-low transition of this pin marks the start of serial communication to the GS6150.

The low-to-high transition of this pin marks the end of serial communication to the GS6150.

There is an option for each device to use a separate unique Chip Select signal from the host processor or for up to 32 devices to be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in the GSPI Command Word will respond to communication from the host processor (unless the B'CAST ALL bit in the GSPI Command Word is set to 1).

4.11.2 SDIN Pin

The SDIN pin is the GSPI serial data input pin of the GS6150.

The 16-bit Command and Data Words from the host processor or from the SDOUT pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is low.

4.11.3 SDOUT Pin

The SDOUT pin is the GSPI serial data output of the GS6150.

All data transfers out of the GS6150 to the host processor or to the SDIN pin of other connected devices occur from this pin.

By default at power up or after system reset, the SDOUT pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data

Word portion for read operations to the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the SDOUT pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.11.3.1 GSPI Link Disable Operation

It is possible to disable the direct SDIN to SDOUT (Loop-Through) connection by writing a value of 1 to the GSPI_LINK_DISABLE bit in REGISTER_0. When disabled, any data appearing at the SDIN pin will not appear at the SDOUT pin and the SDOUT pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd_GSPI_config}$ (5 SCLK cycles).

Table 4-6: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	SDIN pin is looped through to the SDOUT pin
1	Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.

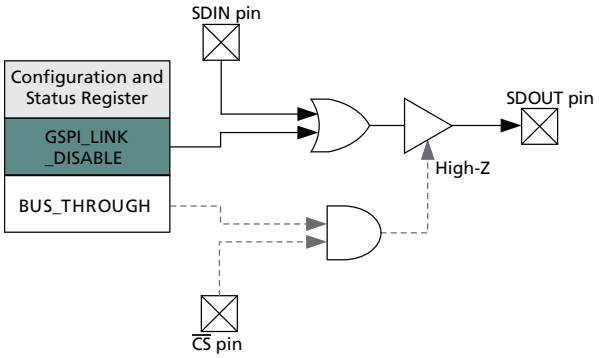


Figure 4-6: GSPI_LINK_DISABLE Operation

4.11.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS6150 can share a common PCB trace with other GSPI devices for SDOUT output.

When configured for Bus-Through operation, by setting GSPI_BUS_THROUGH_ENABLE bit to 1, the SDOUT pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the SDOUT pin will be driven and will follow regular read and write operation as described in Section 4.11.3.

Multiple chains of GS6150 devices can share a single SDOUT bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ($\overline{CS}$).

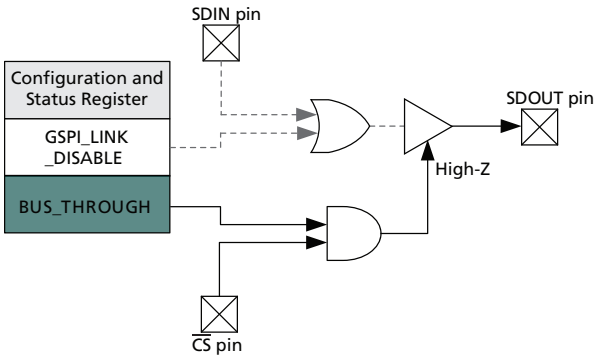


Figure 4-7: GSPI_BUS_THROUGH_ENABLE Operation

4.11.4 SCLK Pin

The SCLK pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS6150 SDIN pin on the rising edge of SCLK. Serial data is clocked out of the device from the SDOUT pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

The maximum interface clock rate is 27MHz.

4.11.5 Command Word Description

All GSPI accesses are a minimum of 32 bits in length (a 16-bit Command Word followed by a 16-bit Data Word) and the start of each access is indicated by the high-to-low transition of the chip select ($\overline{CS}$) pin of the GS6150.

The format of the Command Word and Data Words are shown in Figure 4-8.

Data received immediately following this high-to-low transition will be interpreted as a new Command Word.

4.11.5.1 R/$\overline{W}$ bit - B15 Command Word

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

4.11.5.2 B'CAST ALL - B14 Command Word

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B'CAST ALL is set to 1, the following Data Word (AUTOINC = 0) or Data Words (AUTOINC = 1) are written to the register specified by the ADDRESS field of the Command Word (and subsequent addresses when AUTOINC = 1), regardless of the setting of the UNIT ADDRESS(es).

When B'CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of the Command Word write the Data Word to the register specified by the ADDRESS field of the Command Word.

4.11.5.3 EMEM - B13 Command Word

When the EMEM bit is 1 the Address Word is extended to 23 bits to allow access to registers located in the extended memory space.

When the EMEM bit is 0, the address word is limited to 7 bits.

4.11.5.4 AUTOINC - B12 Command Word

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a low-to-high transition on the $\overline{CS}$ pin is detected.

When AUTOINC is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in HOST_CONFIG.

4.11.5.5 UNIT ADDRESS - B11:B7 Command Word

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed DEVICE_UNIT_ADDRESS in HOST_CONFIG.

By default at power-up or after a device reset, the DEVICE_UNIT_ADDRESS is set to 00h

4.11.5.6 ADDRESS - B6:B0 Command Word

If the extended memory is not being accessed (EMEM = 0), the 7 bits of the ADDRESS field are used to select one of 128 register addresses in the device in single read or write access mode, or to set the starting address for read or write accesses in Auto-Increment Mode.

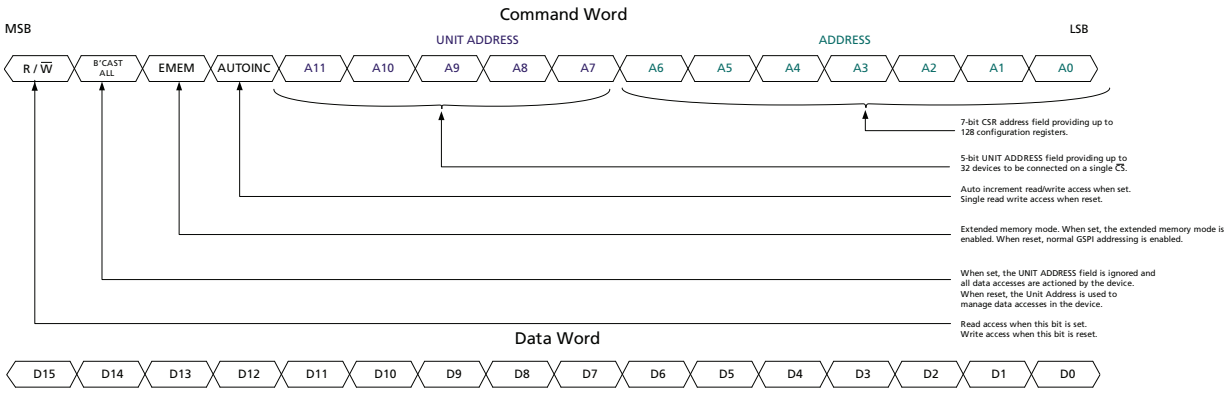


Figure 4-8: Command and Data Word Format

When EMEM is set to 1, the Address Word is extended to 23 bits. The Command and Data Word format will be extended by another 16 bits, and is shown in Figure 4-9 below.

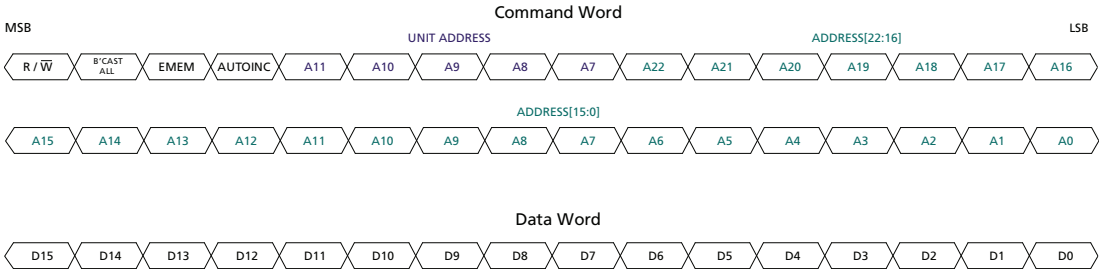


Figure 4-9: Command and Data Word Format with EMEM set to 1

4.11.6 GSPI Transaction Timing

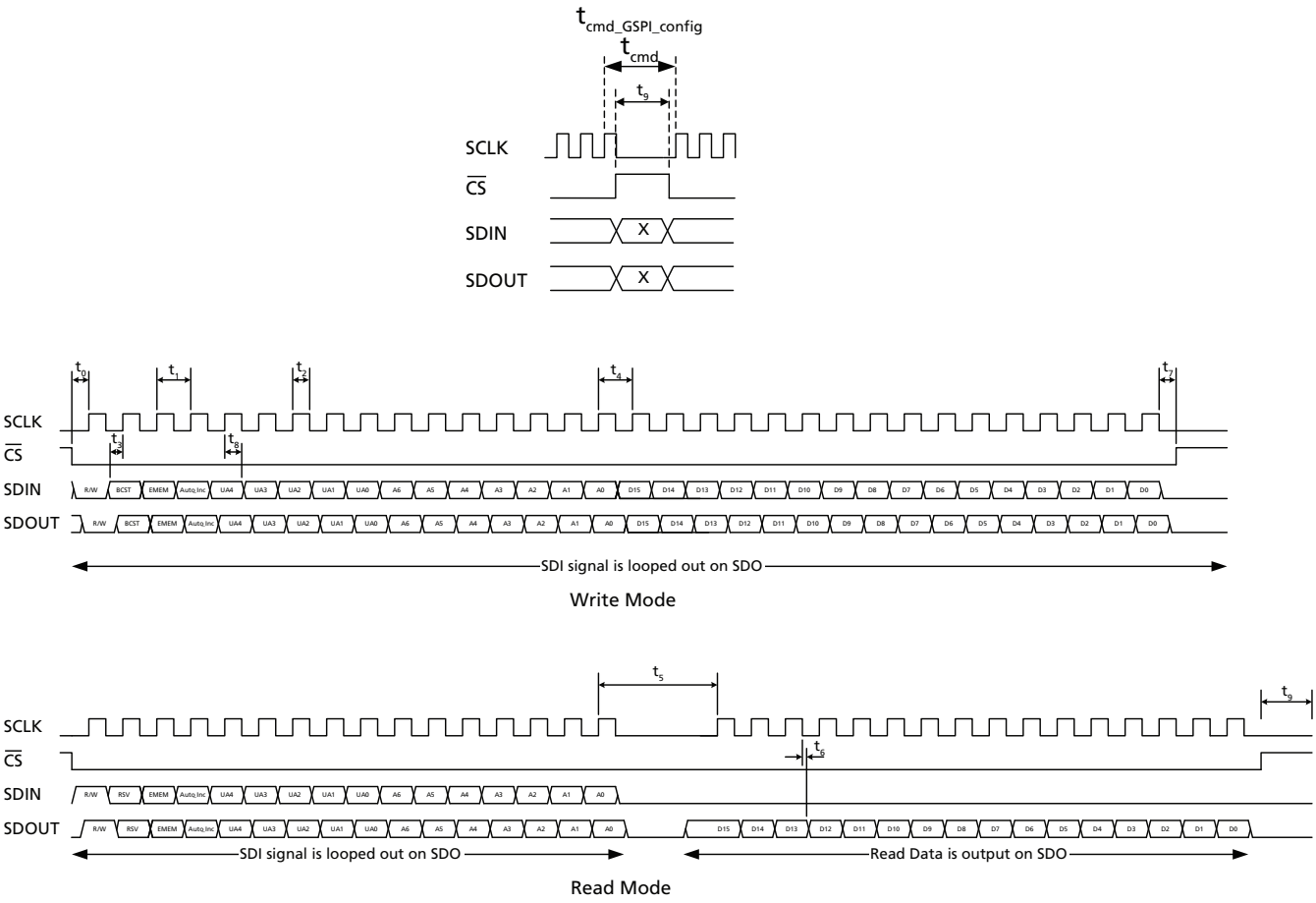


Figure 4-10: GSPI External Interface Timing

Table 4-7: GSPI Timing Parameters

Parameter	Symbol	Equivalent SCLK Cycles (at 27MHz)	Min	Typ	Max	Units
SCLK frequency			—	—	27	MHz
CS low before SCLK rising edge	t_0		2.0	—	—	ns
SCLK period	t_1		37	—	—	ns
SCLK duty cycle	t_2		40	50	60	%
Input data setup time	t_3		2.7	—	—	ns
SCLK idle time -write	t_4	1	37	—	—	ns
SCLK idle time - read	t_5	5	161.0	—	—	ns

Table 4-7: GSPI Timing Parameters (Continued)

Parameter	Symbol	Equivalent SCLK Cycles (at 27MHz)	Min	Typ	Max	Units
Inter-command delay time	t_{cmd}	4	120.0	—	—	ns
Inter-command delay time (after GSPI configuration write)	$t_{cmd_GSPI_conf}$[1]	5	162.0	—	—	ns
SDO after SCLK falling edge	t_6		—	—	7.5	ns
CS high after final SCLK falling edge	t_7		0.0	—	—	ns
Input data hold time	t_8		1.0	—	—	ns
$\overline{CS}$ high time	t_9		57.0	—	—	ns
SDIN to SDOUT combinational delay			—	—	5.0	ns
Max. chips daisy chained at max SCLK frequency	When host clocks in SDOUT data on rising edge of SCLK		—	—	1	GS6150 chips
Max. frequency for 32 daisy-chained devices			—	—	2.1	MHz
Max. chips daisy-chained at max. SCLK frequency	When host clocks in SDOUT data on falling edge of SCLK		—	—	3	GS6150 chips
Max. frequency for 32 daisy-chained devices			—	—	2.2	MHz

Note:

1. $t_{cmd_GSPI_conf}$ inter-command delay must be used whenever modifying HOST_CONFIG register at address 0x00

4.11.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-11 to Figure 4-15.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 32-bits long, consisting of a Command Word and a single Data Word. The read or write cycle begins with a high-to-low transition of the $\overline{CS}$ pin. The read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 4 SCLK clock cycles. After modifying values in HOST_CONFIG, the inter-command delay time, $t_{cmd_GSPI_config}$, is a minimum of 5 SCLK clock cycles.

For read access, the time from the last bit of the Command Word to the start of the data output, as defined by t_5, corresponds to no less than 5 SCLK clock cycles at 27MHz.

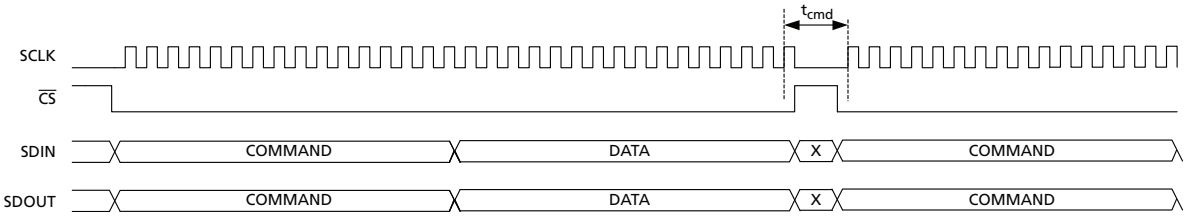


Figure 4-11: GSPI Write Timing – Single Write Access with Loop-Through Operation (default)

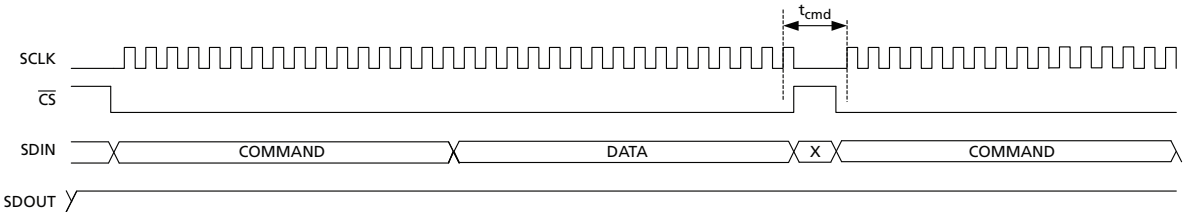


Figure 4-12: GSPI Write Timing – Single Write Access with GSPI Link-Disable Operation

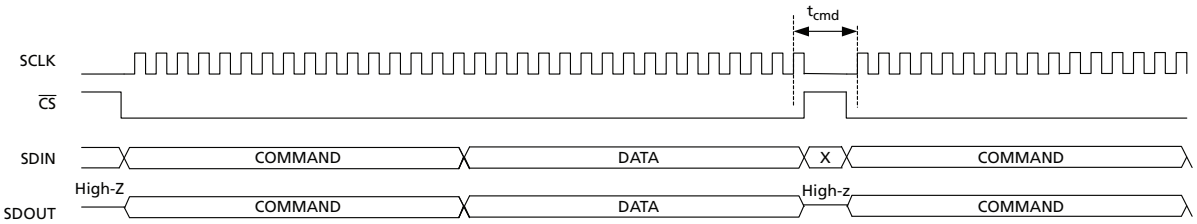


Figure 4-13: GSPI Write Timing – Single Write Access with Bus-Through Operation

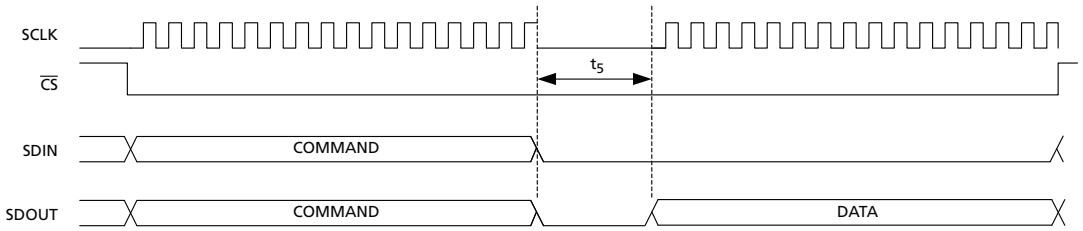


Figure 4-14: GSPI Read Timing – Single Read Access with Loop-Through Operation (default)

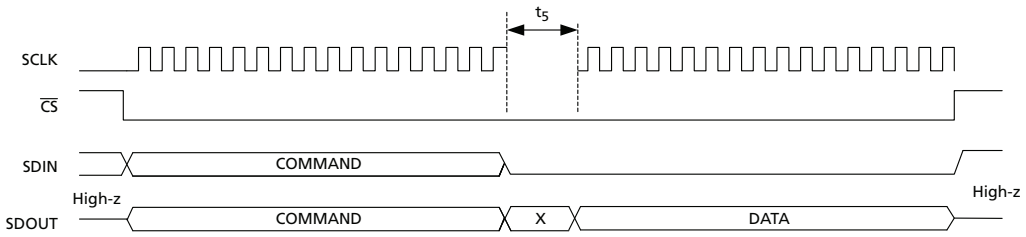


Figure 4-15: GSPI Read Timing – Single Read Access with Bus-Through Operation

4.11.8 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-16 to Figure 4-20.

Auto-increment mode is enabled by the setting of the AUTOINC bit of the Command Word.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a high-to-low transition of the $\overline{CS}$ pin, and consists of a Command Word and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

Note: Writing to HOST_CONFIG using Auto-increment access is not allowed.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of the first Command Word to the start of the data output of the first Data Word as defined by t_5, will be no less than 5 SCLK cycles at 27MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

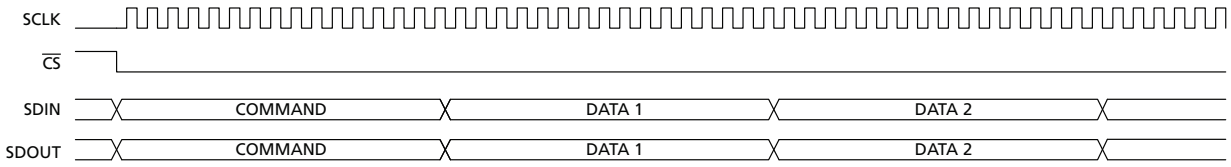


Figure 4-16: GSPI Write Timing – Auto-Increment with Loop-Through Operation (default)

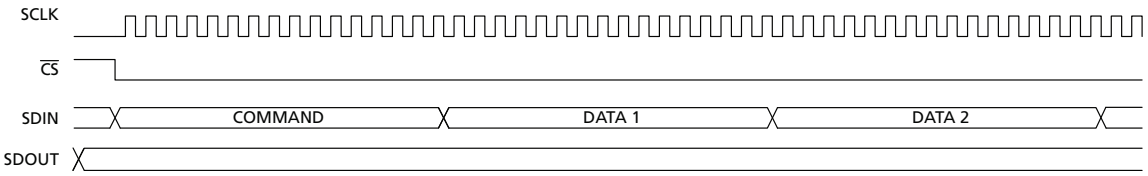


Figure 4-17: GSPI Write Timing – Auto-Increment with GSPI Link Disable Operation

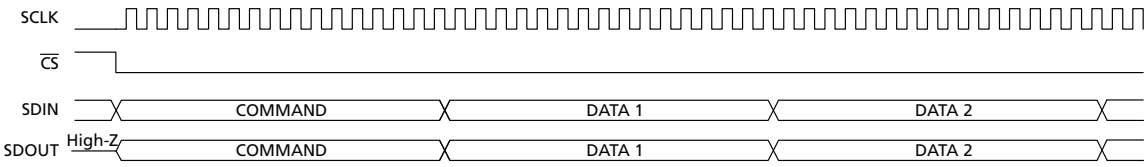


Figure 4-18: GSPI Write Timing – Auto-Increment with Bus-Through Operation

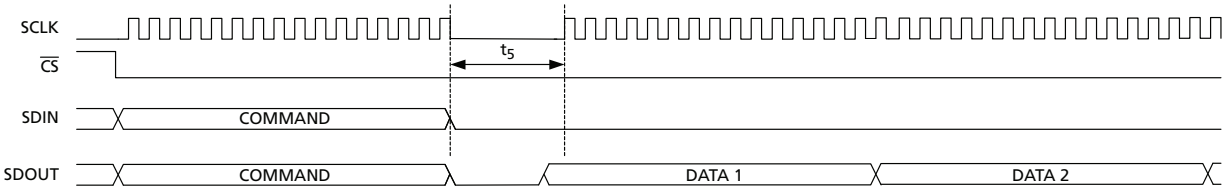


Figure 4-19: GSPI Read Timing – Auto-Increment Read with Loop-Through Operation (default)

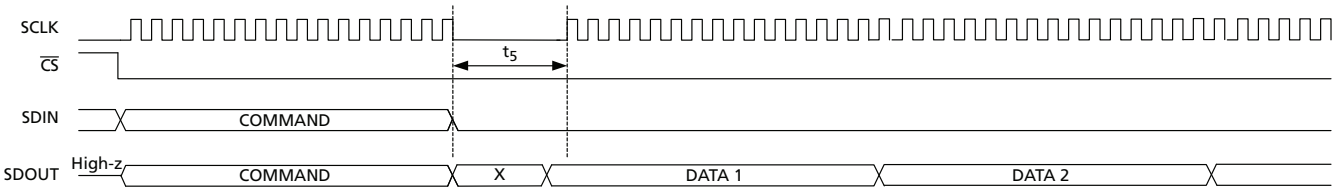


Figure 4-20: GSPI Read Timing – Auto-Increment Read with Bus-through Operation

4.11.9 Setting a Device Unit Address

Multiple (up to 32) GS6150 devices can be connected to a common Chip Select ($\overline{CS}$) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common $\overline{CS}$ can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default at power up or after a device reset, the DEVICE_UNIT_ADDRESS of each device is set to 0h and the SDIN->SDOUT non-clocked loop-through for each device is enabled.

These are the steps required to set the DEVICE_UNIT_ADDRESS of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting HOST_CONFIG (ADDRESS = 0), with the GSPI_LINK_DISABLE bit set to 1 and the DEVICE_UNIT_ADDRESS field set to 0. This disables the direct SDIN->SDOUT non-clocked path for all devices on chip select.

2. Write to Unit Address 0 selecting HOST_CONFIG (ADDRESS = 0), with the GSPI_LINK_DISABLE bit set to 0 and the DEVICE_UNIT_ADDRESS field set to a unique Unit Address. This configures DEVICE_UNIT_ADDRESS for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use DEVICE_UNIT_ADDRESS value 0.
3. Repeat step 2 using new, unique values for the DEVICE_UNIT_ADDRESS field in HOST_CONFIG until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd_GSPI_conf}$ delay must be observed after every write that modifies HOST_CONFIG.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the DEVICE_UNIT_ADDRESS in HOST_CONFIG

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's SDOUT connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final SDOUT outputs connected to a single application host processor input.

4.11.10 Default GSPI Operation

By default at power up or after a device reset, the GS6150 is set for Loop-Through Operation and the internal DEVICE_UNIT_ADDRESS field of the device is set to 0.

Figure 4-21 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS6150 for non-extended memory accesses (EMEM = 0).

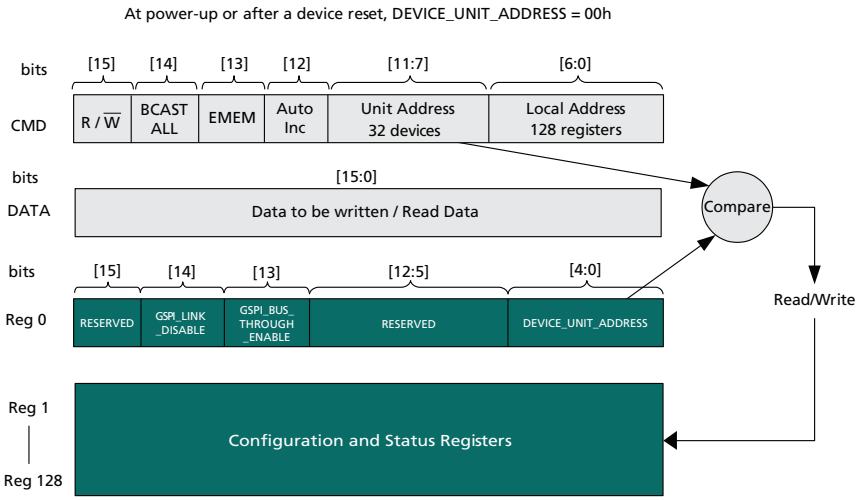


Figure 4-21: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word for write access (R/$\overline{W}$ = 0) to the local registers 0h-80h; set Auto Increment; set the Unit Address field in the Command Word to match the configured DEVICE_UNIT_ADDRESS which will be zero. Write the Command Word.
2. Write the Data Word to be written to the first register.
3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above with the exception of step 1, where the Command Word is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of the Command Word must always match DEVICE_UNIT_ADDRESS for an access to be accepted by the device. Changing DEVICE_UNIT_ADDRESS to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration.)

5. Host Interface Register Map

Table 5-1: Register Descriptions - Standard Address Space

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
0_h	HOST_CONFIG	RSVD	15:15	RW	0_h	Reserved. Do not change.
		GSPI_LINK_DISABLE	14:14	RW	0_h	GSPI loop-through disable.
		GSPI_BUS_THROUGH_ ENABLE	13:13	RW	0_h	GSPI bus-through enable.
		RSVD	12:5	RW	0_h	Reserved. Do not change.
		DEVICE_UNIT_ADDRESS	4:0	RW	0_h	Device address programmed by application.
1_h	DEVICE_INFO	RSVD	15:8	RO	1_h	Reserved.
		DEVICE_VERSION_ID	7:0	RO	-	Device Version Identifier.
2_h	GPIO_CONTROL_ REG_0	RSVD	15:14	RW	0_h	Reserved. Do not change.
		GPIO1_IO_SELECT	13:13	RW	0_h	GPIO1 Input/Output Select 0_b: Output 1_b: Input
		RSVD	12:11	RW	0_h	Reserved. Do not change.
		GPIO1_SELECT	10:7	RW	1_h	GPIO1 Signal Selection If GPIO1_IO_SELECT is set to 0: 0000_b: LOS 0001_b: LOCKED (default) 0010_b: LBR_HBR 0011_b: Reserved 0100_b: Reserved 0101_b: RATE_DET0 0110_b: RATE_DET1 0111_b: RATE_DET2 1000_b: LOCKED_125M 1001_b: LOCKED_270M 1010_b: LOCKED_1G485 1011_b: LOCKED_2G97 1100_b: LOCKED_5G94 1101_b: RATE_CHANGE If GPIO1_IO_SELECT is set to 1: 0000_b: DDO0_DISABLE 0001_b: DDO1_DISABLE
		GPIO0_IO_SELECT	6:6	RW	0_h	GPIO0 Input/Output Select 0_b: Output 1_b: Input
		RSVD	5:4	RW	0_h	Reserved. Do not change.

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
2_h	GPIO_CONTROL_REG_0	GPIO0_SELECT	3:0	RW	0_h	GPIO0 Signal Selection If GPIO0_IO_SELECT is set to 0: 0000_b: LOS (default) 0001_b: LOCKED 0010_b: LBR_HBR 0011_b: Reserved 0100_b: Reserved 0101_b: RATE_DET0 0110_b: RATE_DET1 0111_b: RATE_DET2 1000_b: LOCKED_125M 1001_b: LOCKED_270M 1010_b: LOCKED_1G485 1011_b: LOCKED_2G97 1100_b: LOCKED_5G94 1101_b: RATE_CHANGE If GPIO0_IO_SELECT is set to 1: 0000_b: DDO0_DISABLE 0001_b: DDO1_DISABLE

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
3_h	GPIO_CONTROL_REG_1	RSVD	15:14	RW	0_h	Reserved. Do not change.
		GPIO3_IO_SELECT	13:13	RW	1_h	GPIO3 Input/Output Select 0_b: Output 1_b: Input
		RSVD	12:11	RW	0_h	Reserved. Do not change.
		GPIO3_SELECT	10:7	RW	1_h	GPIO3 Signal Selection If GPIO3_IO_SELECT is set to 0: 0000_b: LOS 0001_b: LOCKED 0010_b: LBR_HBR 0011_b: Reserved 0100_b: Reserved 0101_b: RATE_DET0 0110_b: RATE_DET1 0111_b: RATE_DET2 1000_b: LOCKED_125M 1001_b: LOCKED_270M 1010_b: LOCKED_1G485 1011_b: LOCKED_2G97 1100_b: LOCKED_5G94 1101_b: RATE_CHANGE If GPIO3_IO_SELECT is set to 1: 0000_b: DDO0_DISABLE 0001_b: DDO1_DISABLE (default)
		GPIO2_IO_SELECT	6:6	RW	0_h	GPIO2 Input/Output Select 0_b: Output 1_b: Input

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
		RSVD	5:4	RW	0_h	Reserved. Do not change.
3_h	GPIO_CONTROL_ REG_1	GPIO2_SELECT	3:0	RW	2_h	GPIO2 Signal Selection If GPIO2_IO_SELECT is set to 0: 0000_b: LOS 0001_b: LOCKED 0010_b: LBR_HBR (default) 0011_b: Reserved 0100_b: Reserved 0101_b: RATE_DET0 0110_b: RATE_DET1 0111_b: RATE_DET2 1000_b: LOCKED_125M 1001_b: LOCKED_270M 1010_b: LOCKED_1G485 1011_b: LOCKED_2G97 1100_b: LOCKED_5G94 1101_b: RATE_CHANGE If GPIO2_IO_SELECT is set to 1: 0000_b: DDO0_DISABLE 0001_b: DDO1_DISABLE
4_h	RESERVED	RSVD	15:0	RW	$1C_h$	Reserved. Do not change.
5_h	INPUT_CONTROL_ REG_0	DDI3_TRACE_EQ_CONTROL	7:6	RW	0_h	DDI3 Trace-EQ Configuration 00_b: OFF 01_b: 0dB/EQ BYPASS 10_b: LOW 11_b: HIGH
		DDI2_TRACE_EQ_ CONTROL	5:4	RW	0_h	DDI2 Trace-EQ Configuration 00_b: OFF 01_b: 0dB/EQ BYPASS 10_b: LOW 11_b: HIGH
		DDI1_TRACE_EQ_ CONTROL	3:2	RW	0_h	DDI1 Trace-EQ Configuration 00_b: OFF 01_b: 0dB/EQ BYPASS 10_b: LOW 11_b: HIGH
		DDI0_TRACE_EQ_ CONTROL	1:0	RW	0_h	DDI0 Trace-EQ Configuration 00_b: OFF 01_b: 0dB/EQ BYPASS 10_b: LOW 11_b: HIGH

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
6_h	RESERVED	RSVD	15:0	RW	0_h	Reserved. Do not change.
7_h	INPUT_CONTROL_REG_2	RSVD	15:12	RW	0_h	Reserved. Do not change.
		DDI_SELECT	11:10	RW	0_h	Input Selection 00_b: DDI0 01_b: DDI1 10_b: DDI2 11_b: DDI3 Used when INPUT_SELECTION_CONTROL is set to 01_b or 11_b
		INPUT_SELECTION_CONTROL	9:8	RW	0_h	Determines the source for the input selection block. $X0_b$: Use DDI_SEL0_STROBE and DDI_SEL1 pins. 01_b: Use DDI_SELECT bits 11_b: Use DDI_SELECT bits; update occurs on low-to-high transition of DDI_SEL0_STROBE pin.
		DDI3_TRACE_EQ_DC_TERM_ENABLE	7:7	RW	1_h	Enable DDI3 on-chip Trace-EQ DC termination. 0_b: Disabled 1_b: Enabled
		DDI2_TRACE_EQ_DC_TERM_ENABLE	6:6	RW	1_h	Enable DDI2 on-chip Trace-EQ DC termination. 0_b: Disabled 1_b: Enabled
		DDI1_TRACE_EQ_DC_TERM_ENABLE	5:5	RW	1_h	Enable DDI1 on-chip Trace-EQ DC termination. 0_b: Disabled 1_b: Enabled
		DDI0_TRACE_EQ_DC_TERM_ENABLE	4:4	RW	1_h	Enable DDI0 on-chip Trace-EQ DC termination. 0_b: Disabled 1_b: Enabled
		RSVD	3:0	RW	0_h	Reserved. Do not change.
8_h	RESERVED	RSVD	15:0	ROCW	—	Reserved. Do not change.
9_h	RESERVED	RSVD	15:0	RO	—	Reserved.
A_h	RESERVED	RSVD	15:0	RO	—	Reserved.
B_h	RESERVED	RSVD	15:0	RO	—	Reserved.
C_h	RESERVED	RSVD	15:0	RO	—	Reserved.

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
D_h	RESERVED	RSVD	15:0	RO	—	Reserved.
E_h	RESERVED	RSVD	15:0	RO	—	Reserved.
F_h	LOS_CONTROL_REG_0	RSVD	15:10	RW	0_h	Reserved. Do not change.
		LOS_THRESHOLD_CONTROL_ENABLE	9:9	RW	0_h	Enables LOS threshold adjustment based on the settings in the DDI[3:0]_LOS_THRESHOLD_CONTROL bits in the LOS_CONTROL_REG_1 and LOS_CONTROL_REG_2 registers. 0_b: Default internal thresholds are used 1_b: Thresholds used in the LOS_CONTROL_REG_1 and LOS_CONTROL_REG_2 registers
		LOS_DEASSERT_TIME	8:7	RW	2_h	LOS De-Assert Time Delay: 00_b: 2.30µs 01_b: 1.50µs 10_b: 1.20µs 11_b: 0.90µs
		LOS_ASSERT_TIME	6:5	RW	2_h	LOS Assert Time Delay: 00_b: 68µs 01_b: 64µs 10_b: 62µs 11_b: 61µs
		LOS_HYSTERESIS	4:1	RW	0_h	LOS Threshold Hysteresis Adjustment: 0000_b: 0 dB 0001_b: 0.32 dB 0010_b: 0.64 dB 0011_b: 0.98 dB 0100_b: 1.34 dB 0101_b: 1.70 dB 0110_b: 2.09 dB 0111_b: 2.49 dB 1000_b: 2.84 dB 1001_b: 3.28 dB 1010_b: 3.74 dB 1011_b: 4.23 dB 1100_b: 4.75 dB 1101_b: 5.30 dB 1110_b: 5.89 dB 1111_b: 6.53 dB
		LOS_PWRDN_OVERRIDE	0:0	RW	0_h	Override the internal power-down control for the LOS circuit. 0_b: LOS active 1_b: LOS powered down

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
10_h	LOS_CONTROL_REG_1	DDI1_LOS_THRESHOLD_CONTROL	15:8	RW	$5A_h$	LOS signal threshold for input DDI1 at device pins is: $1.9mV_{ppd}$ x DDI1_LOS_THRESHOLD_CONTROL x (53/DEVICE_SPECIFIC_LOS_THRESHOLD) (All above values are in decimal)
		DDI0_LOS_THRESHOLD_CONTROL	7:0	RW	$5A_h$	LOS signal threshold for input DDI0 at device pins is: $1.9mV_{ppd}$ x DDI0_LOS_THRESHOLD_CONTROL x (53/DEVICE_SPECIFIC_LOS_THRESHOLD) (All above values are in decimal)
11_h	LOS_CONTROL_REG_2	DDI3_LOS_THRESHOLD_CONTROL	15:8	RW	$5A_h$	LOS signal threshold for input DDI3 at device pins is: $1.9mV_{ppd}$ x DDI3_LOS_THRESHOLD_CONTROL x (53/DEVICE_SPECIFIC_LOS_THRESHOLD) (All above values are in decimal)
		DDI2_LOS_THRESHOLD_CONTROL	7:0	RW	$5A_h$	LOS signal threshold for input DDI2 at device pins is: $1.9mV_{ppd}$ x DDI2_LOS_THRESHOLD_CONTROL x (53/DEVICE_SPECIFIC_LOS_THRESHOLD) (All above values are in decimal)
12_h	LOS_STATUS	RSVD	15:8	RO	—	Reserved.
		DEVICE_SPECIFIC_LOS_THRESHOLD	7:0	RO	—	Trimmed setting to achieve LOS threshold of $100mV_{ppd}$
13_h	RESERVED	RSVD	15:0	RW	280_h	Reserved. Do not change.
14_h	RESERVED	RSVD	15:0	RO	—	Reserved.
15_h	REF_CLK_CONTROL	RSVD	15:3	RW	0_h	Reserved. Do not change.
		XTAL_BUF_OUT_ENABLE	2:2	RW	1_h	Enables/Disables the reference buffer output. 0_b: XTAL_BUF_OUT disabled 1_b: XTAL_BUF_OUT enabled
		RSVD	1:1	RW	0_h	Reserved. Do not change.
		RSVD	0:0	RW	0_h	Reserved. Do not change.
16_h	REF_CLK_STATUS	RSVD	15:1	RO	—	Reserved.
		XTAL_CLK_DET	0:0	RO	-	Indicates whether an external 27MHz reference is being used by the device or its internal oscillator. 0_b: Internal oscillator being used 1_b: External crystal being used

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
17_h	PWRDN_ CONTROL	AUTO_PWRDN_MODE	3:3	RW	0_h	Selects the low power mode, SLEEP or STANDBY that is entered into when AUTO_PWRDN_DISABLE is set to 0 and LOS is asserted. 0_b: SLEEP mode is selected (default) 1_b: STANDBY mode is selected
		FORCE_PWRDN_STANDBY	2:2	RW	0_h	Forces the device into STANDBY mode when FORCE_PWRDN_SLEEP is set to 0. 0_b: Device not in STANDBY mode 1_b: Device in STANDBY mode
		FORCE_PWRDN_SLEEP	1:1	RW	0_h	Forces the device into SLEEP mode when AUTO_PWRDN_DISABLE is set to 1. 0_b: Device not in SLEEP mode 1_b: Device in SLEEP mode When FORCE_PWRDN_SLEEP is set to 1, it takes precedence over the FORCE_PWRDN_STANDBY bit.
		AUTO_PWRDN_DISABLE	0:0	RW	1_h	Disables Auto Powerdown mode which automatically enters SLEEP or STANDBY mode when LOS is asserted. 0_b: Device automatically enters SLEEP or STANDBY when LOS is 1 1_b: Device only enters SLEEP or STANDBY when FORCE_PWRDN_SLEEP or FORCE_PWRDN_STANDBY are set to 1
18_h	RESERVED	RSVD	15:0	RO	—	Reserved.

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
19_h	DRIVER_CONTROL_REG_0	RSVD	15:8	RW	0_h	Reserved. Do not change.
		RSVD	7:7	RW	1_h	Reserved. Do not change.
		AUTO_LOS_MUTE_ENABLE	6:6	RW	0_h	Auto-Mute Enable on LOS. 0_b: Output is unaffected by LOS 1_b: Output is muted when LOS is asserted
		DDO1_MUTE	5:5	RW	0_h	Mute control for the DDO1 output. 0_b: DDO1 output not muted 1_b: DDO1 output muted Output across DDO1 and $\overline{DDO1}$ is static and of magnitude DDO1_SWING_MUTE/2 when DDO1_DISABLE is set to 0.
		DDO0_MUTE	4:4	RW	0_h	Mute control for the DDO0 output. 0_b: DDO0 output not muted 1_b: DDO0 output muted Output across DDO0 and $\overline{DDO0}$ is static and of magnitude DDO0_SWING_MUTE/2 when DDO0_DISABLE is set to 0.
		DDO1_DISABLE	3:3	RW	0_h	Disable control for the DDO1 output. 0_b: DDO1 output not disabled 1_b: DDO1 output disabled Output of both DDO1 and $\overline{DDO1}$ is VCC_DDO1. This bit takes precedence over DDO1_MUTE.
		DDO0_DISABLE	2:2	RW	0_h	Disable control for the DDO0 output. 0_b: DDO0 output not disabled 1_b: DDO0 output disabled Output of both DDO0 and $\overline{DDO0}$ is VCC_DDO0. This bit takes precedence over DDO0_MUTE.
		DDO1_DISABLE_SELECT	1:1	RW	0_h	Controls whether DDO1 is disabled using an assigned GPIO pin or the DDO1_DISABLE bit. 0_b: DDO1 is disabled using assigned GPIO 1_b: DDO1 is disabled using the DDO1_DISABLE bit
		DDO0_DISABLE_SELECT	0:0	RW	1_h	Controls whether DDO0 is disabled using an assigned GPIO pin or the DDO0_DISABLE bit. 0_b: DDO0 is disabled using assigned GPIO 1_b: DDO0 is disabled using the DDO0_DISABLE bit

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$1A_h$	DRIVER_CONTROL_REG_1	RSVD	15:15	RW	0_h	Reserved. Do not change.
		DDO0_DEEMPHASIS_5G94	14:12	RW	2_h	De-emphasis control for 5.94Gb/s (6Gb/s UHD-SDI) signals output on DDO0 000_b: 0dB 001_b: 0.3dB 010_b: 0.6dB (default) 011_b: 2.3 B 100_b: 4.0dB 101_b: 6.6dB 110_b: 10.0dB
		DDO0_DEEMPHASIS_2G97	11:9	RW	1_h	De-emphasis control for 2.97Gb/s (3Gb/s SDI) signals output on DDO0 000_b: 0dB 001_b: 0.4dB (default) 010_b: 1.5dB 011_b: 3.2dB 100_b: 4.9dB 101_b: 7.6dB 110_b: 11.0dB
		DDO0_DEEMPHASIS_1G485	8:6	RW	1_h	De-emphasis control for 1.485Gb/s (HD-SDI) signals output on DDO0 000_b: 0dB 001_b: 1.1dB (default) 010_b: 2.4dB 011_b: 4.0dB 100_b: 5.7dB 101_b: 8.2dB 110_b: 11.5dB
		DDO0_DEEMPHASIS_270M	5:3	RW	0_h	De-emphasis control for 0.27Gb/s (SD-SDI) signals output on DDO0 000_b: 0dB (default) 001_b: 1.2dB 010_b: 2.5dB 011_b: 4.1dB 100_b: 6.0dB 101_b: 8.5dB 110_b: 12.0dB
		DDO0_DEEMPHASIS_125M	2:0	RW	0_h	De-emphasis control for 0.125Gb/s (MADI) signals output on DDO0 000_b: 0dB (default) 001_b: 1.2dB 010_b: 2.5dB 011_b: 4.1dB 100_b: 6.0dB 101_b: 8.5dB 110_b: 12.0dB

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
		RSVD	15:15	RW	0_h	Reserved. Do not change.
		DDO1_DEEMPHASIS_5G94	14:12	RW	2_h	De-emphasis control for 5.94Gb/s (6Gb/s UHD-SDI) signals output on DDO1 000_b: 0dB 001_b: 0.3dB 010_b: 0.6dB (default) 011_b: 2.3 B 100_b: 4.0dB 101_b: 6.6dB 110_b: 10.0dB
		DDO1_DEEMPHASIS_2G97	11:9	RW	1_h	De-emphasis control for 2.97Gb/s (3Gb/s SDI) signals output on DDO1 000_b: 0dB 001_b: 0.4dB (default) 010_b: 1.5dB 011_b: 3.2dB 100_b: 4.9dB 101_b: 7.6dB 110_b: 11.0dB
$1B_h$	DRIVER_CONTROL_REG_2	DDO1_DEEMPHASIS_1G485	8:6	RW	1_h	De-emphasis control for 1.485Gb/s (HD-SDI) signals output on DDO1 000_b: 0dB 001_b: 1.1dB (default) 010_b: 2.4dB 011_b: 4.0dB 100_b: 5.7dB 101_b: 8.2dB 110_b: 11.5dB
		DDO1_DEEMPHASIS_270M	5:3	RW	0_h	De-emphasis control for 0.27Gb/s (SD-SDI) signals output on DDO1 000_b: 0dB (default) 001_b: 1.2dB 010_b: 2.5dB 011_b: 4.1dB 100_b: 6.0dB 101_b: 8.5dB 110_b: 12.0dB
		DDO1_DEEMPHASIS_125M	2:0	RW	0_h	De-emphasis control for 0.125Gb/s (MADI) signals output on DDO1 000_b: 0dB (default) 001_b: 1.2dB 010_b: 2.5dB 011_b: 4.1dB 100_b: 6.0dB 101_b: 8.5dB 110_b: 12.0dB

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$1C_h$	DRIVER_CONTROL_REG_3	RSVD	15:12	RW	0_h	Reserved. Do not change.
		DDO0_SWING_1G485	11:8	RW	3_h	Differential swing (amplitude) control for 1.485Gb/s (HD-SDI) signals output on DDO0. For details refer to Section 4.5.3.
		DDO0_SWING_270M	7:4	RW	3_h	Differential swing (amplitude) control for 0.27Gb/s (SD-SDI) signals output on DDO0. For details refer to Section 4.5.3.
		DDO0_SWING_125M	3:0	RW	3_h	Differential swing (amplitude) control for 0.125Gb/s (MADI) signals output on DDO0. For details refer to Section 4.5.3.
$1D_h$	DRIVER_CONTROL_REG_4	DDO0_SWING_BYPASS	15:12	RW	3_h	Differential swing (amplitude) control for unlocked signals output on DDO0 (when reclocker is operating in BYPASS mode). For details refer to Section 4.5.3. Takes precedence over rate-specific swing controls
		DDO0_SWING_MUTE	11:8	RW	3_h	Differential static amplitude control for DDO0 when the output is muted. For details refer to Section 4.5.3. Takes precedence over rate-specific swing controls and bypass swing control
		DDO0_SWING_5G94	7:4	RW	3_h	Differential swing (amplitude) control for 5.94Gb/s (6G UHD-SDI) signals output on DDO0. For details refer to Section 4.5.3.
		DDO0_SWING_2G97	3:0	RW	3_h	Differential swing (amplitude) control for 2.97Gb/s (3Gb/s SDI) signals output on DDO0. For details refer to Section 4.5.3.
$1E_h$	DRIVER_CONTROL_REG_5	RSVD	15:12	RW	0_h	Reserved. Do not change.
		DDO1_SWING_1G485	11:8	RW	3_h	Differential swing (amplitude) control for 1.485Gb/s (HD-SDI) signals output on DDO1. For details refer to Section 4.5.3.
		DDO1_SWING_270M	7:4	RW	3_h	Differential swing (amplitude) control for 0.27Gb/s (SD-SDI) signals output on DDO1. For details refer to Section 4.5.3.
		DDO1_SWING_125M	3:0	RW	3_h	Differential swing (amplitude) control for 0.125Gb/s (MADI) signals output on DDO1. For details refer to Section 4.5.3.

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$1F_h$	DRIVER_CONTROL_REG_6	DDO1_SWING_BYPASS	15:12	RW	3_h	Differential swing (amplitude) control for unlocked signals output on DDO1 (when reclocker is operating in BYPASS mode). For details refer to Section 4.5.3. Also applies when the device is not locked. Takes precedence over rate-specific swing controls
		DDO1_SWING_MUTE	11:8	RW	3_h	Differential static amplitude control for DDO1 when the output is muted. For details refer to Section 4.5.3. Takes precedence over rate-specific swing controls and bypass swing control
		DDO1_SWING_5G94	7:4	RW	3_h	Differential swing (amplitude) control for 5.94Gb/s (6G UHD-SDI) signals output on DDO1. For details refer to Section 4.5.3.
		DDO1_SWING_2G97	3:0	RW	3_h	Differential swing (amplitude) control for 2.97Gb/s (3Gb/s SDI) signals output on DDO1. For details refer to Section 4.5.3.
20_h	RECLOCKER_BYPASS	RSVD	15:2	RW	0_h	Reserved. Do not change.
		MANUAL_BYPASS	1:1	RW	0_h	Used to manually bypass the retiming block in the reclocker. 0_b: Retimer not bypassed 1_b: Retimer bypassed The assertion of MANUAL_BYPASS takes precedence irrespective of the setting of AUTO_BYPASS
		AUTO_BYPASS	0:0	RW	1_h	Selects between automatic and manual bypass of the retiming block when the reclocker is not locked. 0_b: Auto-Bypass is disabled 1_b: Auto-Bypass is enabled Even if AUTO_BYPASS is asserted, the assertion of MANUAL_BYPASS will still cause the retimer to be bypassed.
21_h	PD_CONTROL	RSVD	15:7	RW	1_h	Reserved. Do not change.
		LOCK_SAMPLE	6:6	RW	0_h	Selects sampling method for LOCK DETECTION 0_b: Strict sampling 1_b: High-jitter sampling
		RSVD	5:1	RW	2_h	Reserved. Do not change.
		POLARITY_INVERT	0:0	RW	0_h	—

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
22_h	RESERVED	RSVD	15:0	RW	4208_h	Reserved. Do not change.
23_h	RESERVED	RSVD	15:0	RW	0_h	Reserved. Do not change.
24_h	RESERVED	RSVD	15:0	ROSW	0_h	Reserved. Do not change.
25_h	RESERVED	RSVD	15:0	RW	0_h	Reserved. Do not change.
26_h	RESERVED	RSVD	15:0	RW	2_h	Reserved. Do not change.
27_h	RESERVED	RSVD	15:0	RW	$A8B_h$	Reserved. Do not change.
28_h	RESERVED	RSVD	15:0	RW	3_h	Reserved. Do not change.
29_h	RESERVED	RSVD	15:0	RW	3_h	Reserved. Do not change.
$2A_h$	RESERVED	RSVD	15:0	RW	3_h	Reserved. Do not change.
$2B_h$	RESERVED	RSVD	15:0	RW	2_h	Reserved. Do not change.
$2C_h$	RESERVED	RSVD	15:0	RO	0_h	Reserved.
$2D_h$	RESERVED	RSVD	15:0	RO	0_h	Reserved.
$2E_h$	RESERVED	RSVD	15:0	RO	0_h	Reserved.
$2F_h$	RESERVED	RSVD	15:0	RO	0_h	Reserved.
30_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
31_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
32_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
33_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
34_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
35_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
36_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
37_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
38_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
39_h	RESERVED	RSVD	15:0	RW	2_h	Reserved. Do not change.
$3A_h$	RESERVED	RSVD	15:0	ROSW	0_h	Reserved. Do not change.
$3B_h$	RESERVED	RSVD	15:0	RW	0_h	Reserved. Do not change.
$3C_h$	RESERVED	RSVD	15:0	RW	2_h	Reserved. Do not change.
$3D_h$	RESERVED	RSVD	15:0	RW	$A8B_h$	Reserved. Do not change.

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$3E_h$	RESERVED	RSVD	15:0	RW	3_h	Reserved. Do not change.
$3F_h$	RESERVED	RSVD	15:0	RW	3_h	Reserved. Do not change.
40_h	RESERVED	RSVD	15:0	RW	0_h	Reserved. Do not change.
41_h	RESERVED	RSVD	15:0	RO	0_h	Reserved. Do not change.
42_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
43_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
44_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
45_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
46_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
47_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
48_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
49_h	RESERVED	RSVD	15:0	RO	0_h	Reserved.
$4A_h$	RESERVED	RSVD	15:0	RO	0_h	Reserved.
$4B_h$	RESERVED	RSVD	15:0	RO	0_h	Reserved.

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$4C_h$	PLL_CONTROL	RSVD	15:12	RW	0_h	Reserved. Do not change.
		LOS_DETECTION_METHOD	11:10	RW	1_h	Determines the source of CARRIER_DETECT. 00_b: Edge detection 01_b: Strength detection
		FORCE_PLL_RATE	9:7	RW	1_h	Force the PLL to retime a specific data rate. 000_b: Reserved 001_b: 0.270Gb/s 010_b: 1.485Gb/s 011_b: 2.97Gb/s 100_b: 5.94Gb/s 101_b: Reserved 110_b: Reserved 111_b: Reserved Used when FORCE_PLL_RATE_ENABLE is set to 1.
		FORCE_PLL_RATE_ENABLE	6:6	RW	0_h	Enables the forced PLL rate override set using the FORCE_PLL_RATE bits.
		RATE_ENABLE_125M	5:5	RW	0_h	Enables auto-detection of 0.125Gb/s (MADI) signals 0_b: 0.125Gb/s signals will not be detected 1_b: 0.125Gb/s signals will be detected
		RATE_ENABLE_5G94	4:4	RW	1_h	Enables auto-detection of 5.94Gb/s (6G UHD-SDI) signals. 0_b: 5.94Gb/s signals will not be detected 1_b: 5.94Gb/s signals will be detected
		RATE_ENABLE_2G97	3:3	RW	1_h	Enables auto-detection of 2.97Gb/s (3G SDI) signals. 0_b: 2.97Gb/s signals will not be detected 1_b: 2.97Gb/s signals will be detected
		RATE_ENABLE_1G485	2:2	RW	1_h	Enables auto-detection of 1.485Gb/s (HD-SDI) signals. 0_b: 1.485Gb/s signals will not be detected 1_b: 1.485Gb/s signals will be detected
		RATE_ENABLE_270M	1:1	RW	1_h	Enables auto-detection of 0.27Gb/s (SD-SDI) signals. 0_b: 0.27Gb/s signals will not be detected 1_b: 0.27Gb/s signals will be detected
		PLL_SOFT_RESET	0:0	RW	0_h	Synchronous soft-reset for the PLL rate detection state machine. 0_b: Normal operation of the PLL rate detection state machine 1_b: Resets the PLL rate detection state machine

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$4D_h$	RESERVED	RSVD	15:0	RW	110_h	Reserved. Do not change.
$4E_h$	RESERVED	RSVD	15:0	RW	110_h	Reserved. Do not change.
$4F_h$	PLL_STATUS	RETIMER_BYPASS	15:15	RO	—	Indicates whether the retimer is active or bypassed. 0_b: Retimer is active 1_b: Retimer is bypassed
		LBR_HBR	14:14	RO	—	Indicates high-bit-rate versus low-bit-rate. 0_b: Input data rate is 5.94Gb/s, 2.97Gb/s, 1.485Gb/s, or BYPASS 1_b: Input data rate is 270Mb/s or 125Mb/s
		DETECTED_RATE	13:11	RO	—	Indicates the current rate found by the PLL rate detection state machine. 000_b: 0.125Gb/s 001_b: 0.270Gb/s 010_b: 1.485Gb/s 011_b: 2.97Gb/s 100_b: 5.94Gb/s 101_b: Reserved 110_b: Reserved 111_b: Reserved
		RSVD	10:10	RO	—	Reserved.
		LOCKED	9:9	RO	—	Indicates if the CDR is locked or unlocked. 0_b: CDR is unlocked 1_b: CDR is locked
		LOS	8:8	RO	—	Indicates whether or not the CDR has lost the signal. 0_b: Signal is present 1_b: Loss of signal
		RSVD	7:0	RO	—	Reserved.

Table 5-1: Register Descriptions - Standard Address Space (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
50_h	STICKY_STATUS	STANDBY_STICKY	11:11	ROCW	—	Sticky bit indicating that the device entered STANDBY mode at least once. 0_b: Device has not entered STANDBY mode since this bit was last cleared 1_b: Devices has entered STANDBY mode since this bit was last cleared
		SLEEP_STICKY	10:10	ROCW	—	Sticky bit indicating that the device entered SLEEP mode at least once 0_b: Device has not entered SLEEP mode since this bit was last cleared 1_b: Device has entered SLEEP mode since this bit was last cleared
		RETIMER_BYPASS_STICKY	9:9	ROCW	—	Sticky bit indicating that the retimer is/has been bypassed. 0_b: Retimer has not been bypassed since this bit was last cleared 1_b: Retimer has been bypassed since this bit was last cleared This bit is cleared by writing any value to it.
		LBR_HBR_STICKY	8:8	ROCW	—	Sticky bit indicating that the rate is/has been 270Mb/s (low bit-rate). 0_b: Rate has not been 270Mb/s since this bit was last cleared 1_b: Rate has been 270Mb/s since this bit was last cleared This bit is cleared by writing any value to it.
		RATE_CHANGE_STICKY	7:7	ROCW	—	Sticky bit indicating that a rate change has occurred. 0_b: Rate has not changed since this bit was last cleared 1_b: Rate has changed since this bit was last cleared This bit is cleared by writing any value to it.
		LOCK_LOST_STICKY	6:6	ROCW	—	Sticky bit indicating that lock was lost. 0_b: Lock has not been lost since this bit was last cleared 1_b: Lock has been lost since this bit was last cleared This bit is cleared by writing any value to it.
		RSVD	5:5	ROCW	—	Reserved.
		LOS_STICKY	4:4	ROCW	—	Sticky bit indicating a loss of signal. 0_b: Signal has not been lost since this bit was last cleared 1_b: Signal has been lost since this bit was last cleared This bit is cleared by writing any value to it.
		RSVD	3:0	ROCW	—	Reserved.

Table 5-2: Register Descriptions - Extended Address Space

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value (Dec)	Description
		RSVD	15:5	RW	4_h	Reserved. Do not change.
$E4_h$	PLL_LBW_ CONTROL_ REG_0	PLL_LOOP_BANDWIDTH	4:0	RW	4_h	Sets the rate specific PLL loop-bandwidth when the device is locked. 00001_b: Nominal / 4 00010_b: Nominal / 2 00100_b: Nominal (default) 01000_b: Nominal x 2 11100_b: Nominal x 4 See Table 2-3: AC Electrical Characteristics for the PLL loop-bandwidth value set at each rate by each of these settings.

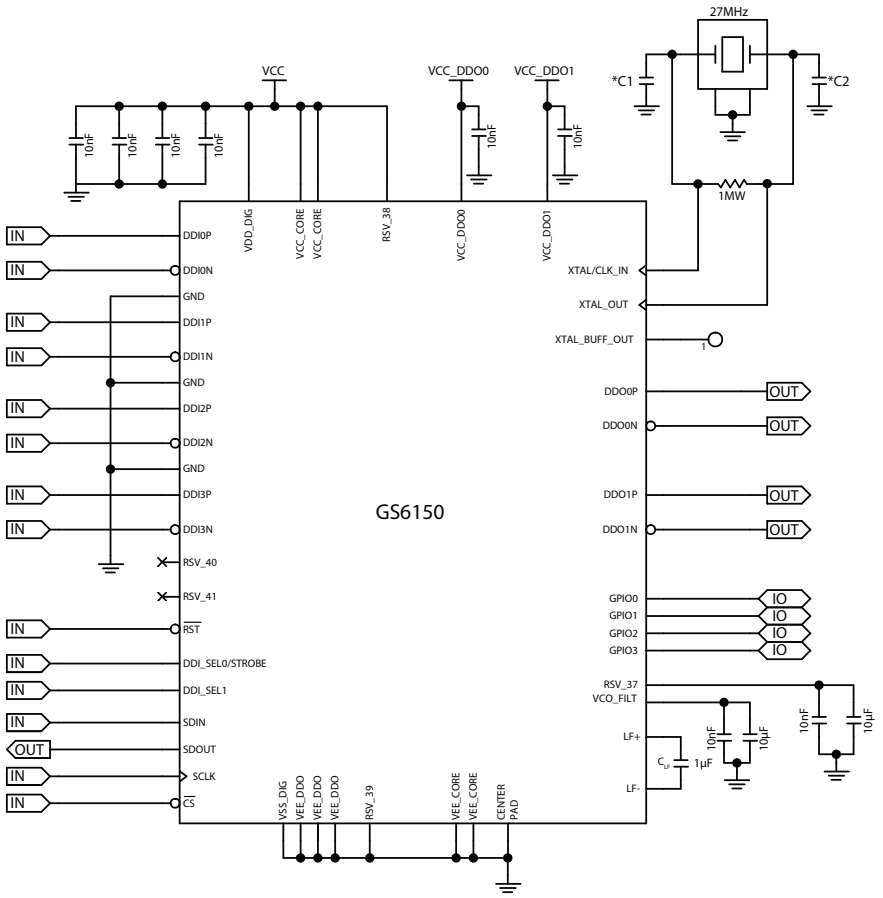
RW = Read/Write

RO = Read Only

ROCW = Read Only/ Clear on Write

ROSW = Read Only/ Set on Write

6. Typical Application Circuit

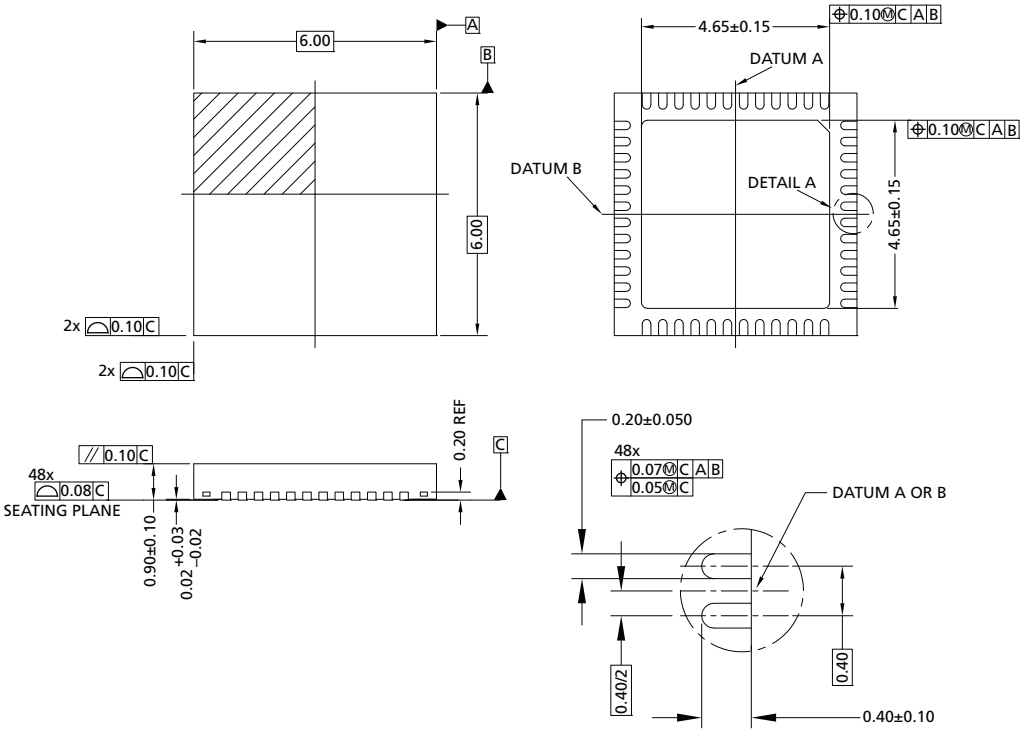


Notes:
VCC IS 1.8V
VCC_DDO0 AND VCC_DDO1 ARE IN THE RANGE +1.2V TO +2.5V
XTAL IS OPTIONAL
*VALUES FOR C1 AND C2 ARE CHOSEN BASED ON THE REQUIRED LOADING FOR THE SELECTED CRYSTAL
IF AC COUPLING IS REQUIRED ON THE HIGH-SPEED SERIAL INPUTS AND OUTPUTS BY THE APPLICATION, A CERAMIC CAPACITOR 4.7µF OR HIGHER WITH A STABLE DIELECTRIC IS RECOMMENDED

Figure 6-1: GS6150 Typical Application Circuit

7. Package and Ordering Information

7.1 Package Dimensions



DETAIL A (SCALE 3:1)

NOTES:
1. DIMENSIONS AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS OR IN DEGREES

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint

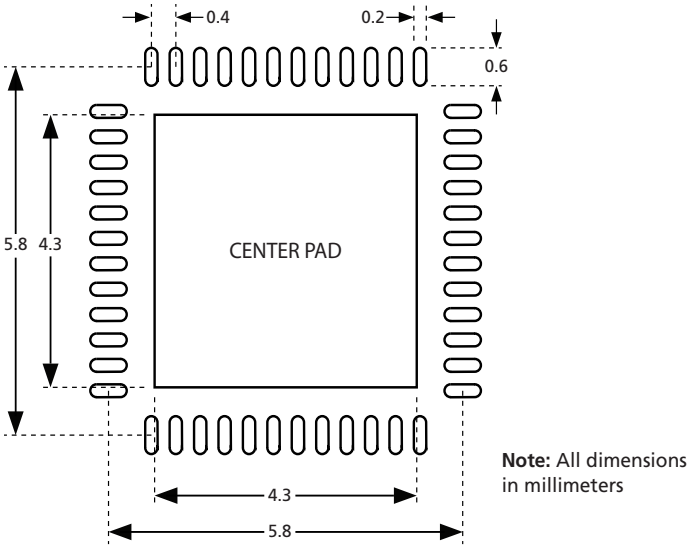


Figure 7-2: GS6150 PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	6mm x 6mm 48-pin QFN
Moisture Sensitivity Level (Note 1)	3
Junction to Case Thermal Resistance, θ_{j-c}	26.2°C/W
Junction to Air Thermal Resistance, θ_{j-a}	21.6°C/W
Junction to Board Thermal Resistance, θ_{j-b}	4.4°C/W
Psi, Ψ	0.2°C/W
Pb-free and RoHS Compliant	Yes

Note:

1. Value per JEDEC J-STD-020C

7.4 Marking Diagram

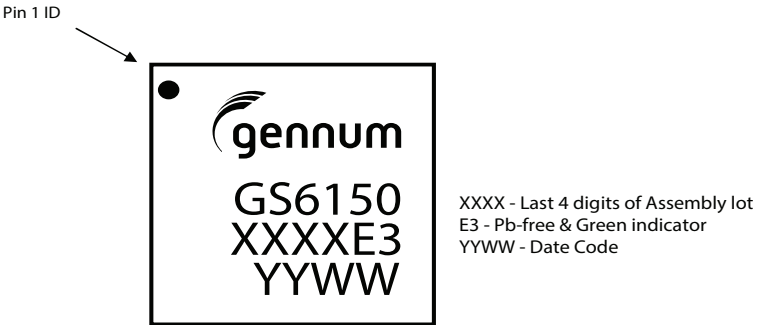


Figure 7-3: GS6150 Marking Diagram

7.5 Solder Reflow Profile

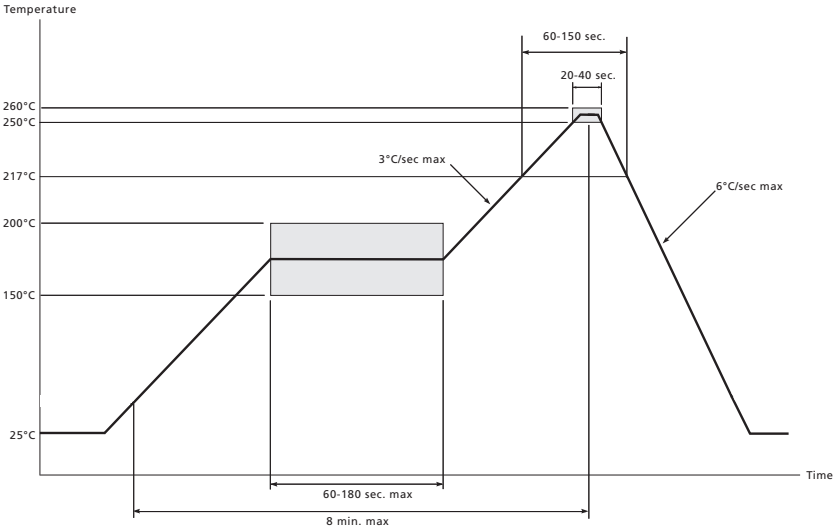


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Package	Temperature Range
GS6150-INE3	Pb-free 48-pin QFN	-40°C to 85°C
GS6150-INTE3	Pb-free 48-pin QFN (250pc. tape and reel)	-40°C to 85°C
GS6150-INTE3Z	Pb-free 48-pin QFN (2.5k tape and reel)	-40°C to 85°C

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