KAI-0330

648 (H) x 484 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAI−0330 Image Sensor is a high performance, low cost, progressive scan 648 (H) × 484 (V) (1/2″ optical format) Interline CCD Image Sensor designed specifically for demanding machine vision, surveillance, and computer input imaging applications.

Available in both single- and dual-output configurations, frame rates up to 120 Hz are available, providing the ability to design an image capture device that is up to 4× faster than traditional CCD image sensors. In addition, 9 μm square pixels with micolenses and anti-blooming structure provide high sensitivity and excellent specular reflection blooming control. Coupled with the additional benefits of electronic shutter, rapid clearing of horizontal lines for faster sub-region readout, and availability in color and monochrome configurations, this sensor is an ideal choice for challenging imaging applications.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CDD; Progressive Scan
Total Number of Pixels	680 (H) × 496 (V)
Number of Effective Pixels	648 (H) × 484 (V)
Number of Active Pixels	648 (H) × 484 (V)
Pixel Size	9.0 μm(H) × 9.0 μm (V)
Active Image Size	5.832 mm (H) × 4.356 mm (V), 7.28 mm (Diagonal), 1/2″ Optical Format
Aspect Ratio	4:3
Number of Outputs	1 or 2
Saturation Signal	30.000 e^-
Output Sensitivity	11.5 μV/e^-
Quantum Efficiency −ABA (490 nm) −CBA (620 nm, 530 nm, 460 nm)	 36% 25%, 26%, 32%
Total Sensor Noise	0.5 mV rms
Dynamic Range	57 dB
Dark Current	< 0.5 nA/cm^2
Dark Current Doubling Temperature	8°C
Charge Transfer Efficiency	0.99999
Smear	0.01%
Image Lag	Negligible
Maximum Data Rate	30 MHz
Package	20-Pin CERDIP
Cover Glass	Clear Glass

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

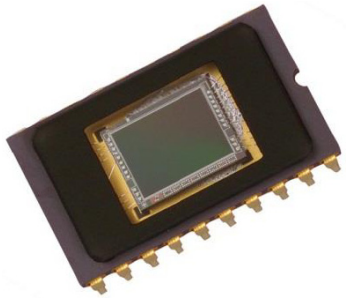


Figure 1. KAI−0330 Interline CCD Image Sensor

Features

- Front Illuminated Interline Architecture
- Progressive Scan
- Electronic Shutter
- Integral RGB Color Filter Array (Optional)
- On-Chip Dark Reference Pixels
- Low Dark Current
- Dual Output Shift Registers
- Anti-Blooming Protection
- Negligible Lag
- Low Smear

Applications

- Machine Vision

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−0330 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−0330−AAA−CP−BA−Dual Output	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade, Dual Output	KAI−0330D Serial Number
KAI−0330−AAA−CP−AE−Dual Output	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Grade, Dual Output	
KAI−0330−ABA−CB−AA−Single Output	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade, Single Output	KAI−0330SM Serial Number
KAI−0330−ABA−CB−BA−Dual Output	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade, Dual Output	KAI−0330DM Serial Number
KAI−0330−ABA−CB−AE−Dual Output	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Grade, Dual Output	
KAI−0330−CBA−CB−BA−Dual Output	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade, Dual Output	KAI−0330DCM Serial Number
KAI−0330−CBA−CB−AE−Dual Output	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Grade, Dual Output	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAI−0330−12−30−A−GEVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

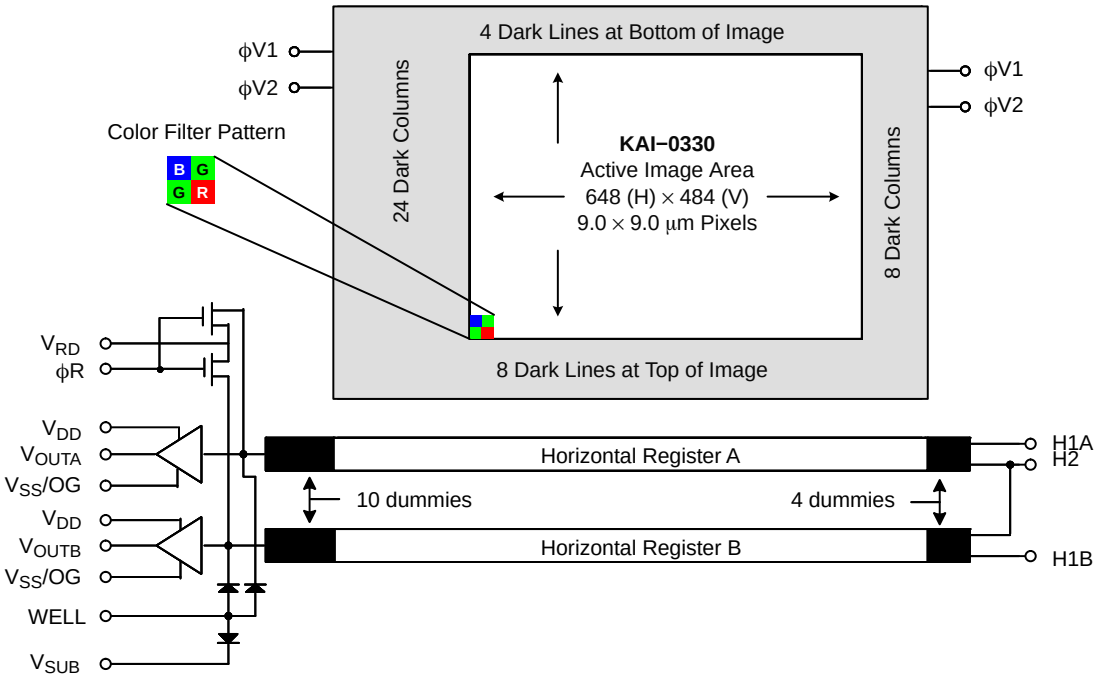


Figure 2. Functional Block Diagram

The KAI−0330 consists of 648 × 484 photodiodes, 680 vertical (parallel) CCD shift registers (VCCDs), and dual 496 pixel horizontal (serial) CCD shift registers (HCCDs) with independent output structures. The device can be operated in either single or dual line mode. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The active pixels are surrounded by an additional 32 columns and 12 rows of light-shielded dark reference pixels.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Charge Transport

The accumulated or integrated charge from each photodiode is transported to the output by a three-step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock (ϕV1). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock, ϕH2, these charge packets are dumped over the output gate (OG, Figure 3) onto the floating diffusion (FDA and FDB, Figure 3).

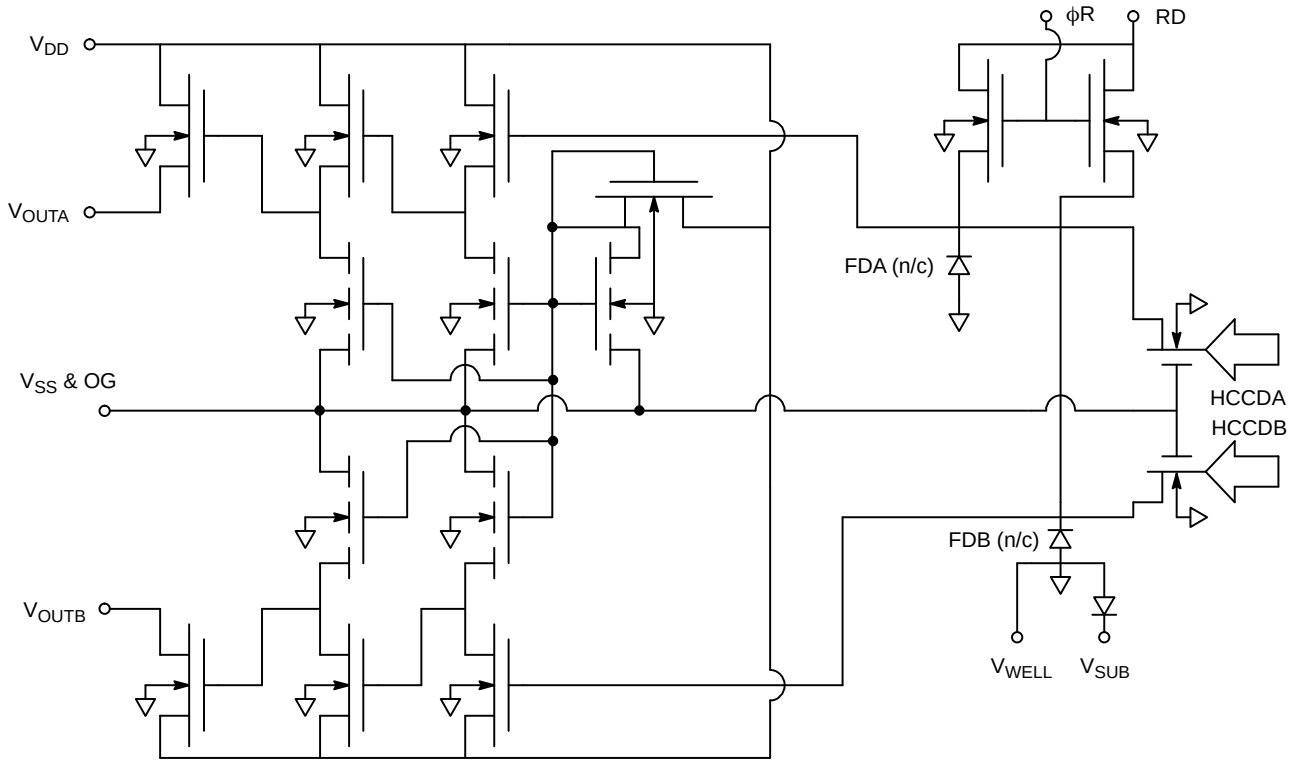
Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the HCCDs begins when ϕV2 is clocked high and then low (while holding ϕH1A high) causing charge to be transferred from ϕV1 to ϕV2 and subsequently into the A HCCD. The A register can now be read out in single line mode. If it is desired to operate the device in a dual line readout mode for higher frame rates, this line is transferred into the B HCCD by clocking ϕH1A to a low state, and ϕH1B to a high state while holding ϕH2 low. After ϕH1A is returned to a high state, the next line can be transferred into the A HCCD. After this clocking sequence, both HCCDs are read out in parallel.

The charge capacity of the horizontal CCDs is slightly more than twice that of the vertical CCDs. This feature allows the user to perform two-to-one line aggregation in the charge domain during V-to-H transfer. This device is also equipped with a fast dump feature that allows the user to selectively dump complete lines (or rows) of pixels at a time. This dump, or line clear, is also accomplished during the V-to-H transfer time by clocking the fast dump gate.

Output Structure

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression $\Delta V_{FD} = \Delta Q / C_{FD}$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain.

The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of μV/e⁻. After the signal has been sampled off-chip, the reset clock (ϕR) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage (V_{RD}).



NOTE: For the single output version, V_{OUTB} is not active.

Figure 3. Output Structure

Electronic Shutter

The KAI−0330 provides a structure for the prevention of blooming which may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD). This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse (VES ≈ 40 V) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on ϕV1. The integration time is then the time between the falling edges of the substrate shutter pulse and ϕV1. This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feed-through. The shutter pulse VES must be “hidden” in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Physical Description

Pin Description and Device Orientation

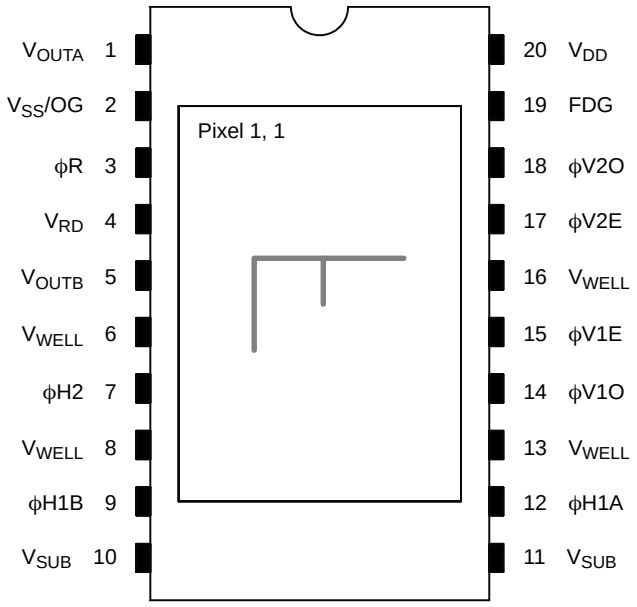


Figure 4. Pinout Diagram (Top View)

Table 4. PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{OUTA}	Video Output Channel A
2	V_{SS}/OG	Output Amplifier Return and OG
3	ϕR	Reset Clock
4	V_{RD}	Reset Drain
5	V_{OUTB}	Video Output Channel B (Note 1)
6, 8, 13, 16	V_{WELL}	P-Well (Ground)
7	ϕH2	A & B Horizontal CCD Clock − Phase 2
9	ϕH1B	B Horizontal CCD Clock − Phase 1
10, 11	V_{SUB}	Substrate
12	ϕH1A	A Horizontal CCD Clock − Phase 1
14	ϕV1O	Vertical CCD Clock − Phase 1, Odd Field (Note 2)
15	ϕV1E	Vertical CCD Clock − Phase 1, Even Field (Note 2)
17	ϕV2E	Vertical CCD Clock − Phase 2, Even Field (Note 3)
18	ϕV2O	Vertical CCD Clock − Phase 2, Odd Field (Note 3)
19	FDG	Fast Dump Gate
20	V_{DD}	Output Amplifier Supply

1. For the single output version, V_{OUTB} is not active.
2. Pins 14 and 15 must be connected together − only 1 Phase 1 clock driver is required.
3. Pins 17 and 18 must be connected together − only 1 Phase 2 clock driver is required.

IMAGING PERFORMANCE

All the following values were derived using nominal operating conditions using the recommended timing. Unless otherwise stated, readout time = 40 ms, integration time = 40 ms and sensor temperature = 40°C. Correlated double sampling of the output is assumed and recommended. Many units are expressed in electrons, to convert to voltage, multiply by the amplifier sensitivity.

Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

Table 5. ELECTRO-OPTICAL FOR KAI−0330−CBA

Parameter	Symbol	Min.	Nom.	Max.	Unit
Optical Fill Factor	F	−	55.0	−	%
Saturation Exposure (Note 1)	E_{SAT}	−	0.046	−	$\mu J/cm^2$
Red Peak Quantum Efficiency λ = 620 nm (Note 2)	QE_R	−	25	−	%
Green Peak Quantum Efficiency λ = 530 nm (Note 2)	QE_G	−	26	−	%
Blue Peak Quantum Efficiency λ = 460 nm (Note 2)	QE_B	−	32	−	%
Green Photoresponse Shading (Note 4)	R_{GS}	−	6	−	%
Photoresponse Non-Uniformity (Note 3)	PRNU	−	5.0	−	p-p %
Photoresponse Non-Linearity	PRNL	−	5.0	−	%
Amplifier Sensitivity	ΔV/ΔN	−	11.5	−	$\mu V/e^-$

1. For λ = 530 nm wavelength, and V_{SAT} = 350 mV.
2. Refer to typical values from Figure 5.
3. Under uniform illumination with output signal equal to 280 mV.
4. This is the global variation in chip output for green pixels across the entire chip.
5. It is recommended to use low-pass filter with $\lambda_{CUT\text{-}OFF}$ at ~ 680 nm for high performance.

Table 6. ELECTRO-OPTICAL FOR KAI−0330−ABA

Parameter	Symbol	Min.	Nom.	Max.	Unit
Optical Fill Factor	F	−	55.0	−	%
Saturation Exposure (Note 1)	E_{SAT}	−	0.037	−	$\mu J/cm^2$
Peak Quantum Efficiency (Note 2)	QE	−	36	−	%
Photoresponse Non-Uniformity (Note 3)	PRNU	−	5.0	−	p-p %
Photoresponse Non-Linearity	PRNL	−	5.0	−	%

1. For λ = 550 nm wavelength, and V_{SAT} = 350 mV.
2. Refer to typical values from Figure 6.
3. Under uniform illumination with output signal equal to 280 mV.

Table 7. CCD IMAGE SPECIFICATIONS

Parameter	Symbol	Min.	Nom.	Max.	Unit
Output Saturation Voltage (Notes 1, 2, 8)	V_{SAT}	−	350	−	mV
Dark Current	I_D	−	−	0.5	nA
Dark Current Doubling Temperature	DCDT	7	8	10	°C
Charge Transfer Efficiency (Notes 2, 3)	CTE	−	0.99999	−	
Horizontal CCD Frequency (Note 4)	f_H	−	−	30	MHz
Image Lag (Note 5)	IL	−	−	100	e^-
Blooming Margin (Notes 6, 8)	X_{AB}	−	100	−	
Vertical Smear (Note 7)	Smr	−	0.01	−	%

1. V_{SAT} is the green pixel mean value at saturation as measured at the output of the device with X_{AB} = 1. V_{SAT} can be varied by adjusting V_{SUB}.
2. Measured at sensor output.
3. With stray output load capacitance of C_L = 10 pF between the output and AC ground.
4. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
5. This is the first field decay lag measured by strobe illuminating the device at (H_{SAT},V_{SAT}), and by then measuring the subsequent frame's average pixel output in the dark.
6. X_{AB} represents the increase above the saturation-irradiance level (H_{SAT}) that the device can be exposed to before blooming of the vertical shift register will occur. It should also be noted that V_{OUT} rises above V_{SAT} for irradiance levels above H_{SAT}, as shown in Figure 8.
7. Measured under 10% (~100 lines) image height illumination with white light source and without electronic shutter operation and below V_{SAT}.
8. It should be noted that there is tradeoff between X_{AB} and V_{SAT}.

Table 8. OUTPUT AMPLIFIER @ V_{DD} = 15 V, V_{SS} = 0.0 V

Description	Symbol	Min.	Nom.	Max.	Unit
Output DC Offset (Notes 1, 2)	V_{ODC}	−	7	−	V
Power Dissipation (Note 3)	P_D	−	55	−	mW
Output Amplifier Bandwidth (Notes 1, 4)	f_{-3db}	−	140	−	MHz
Off-Chip Load	C_L	−	−	10	pF

1. Measured at sensor output with constant current load of I_{OUT} = 5 mA per output.
2. Measured with V_{RD} = 9 V during the floating-diffusion reset interval, (ϕR high), at the sensor output terminals.
3. Both channels.
4. With stray output load capacitance of C_L = 10 pF between the output and AC ground.

Table 9. GENERAL

Description	Symbol	Min.	Nom.	Max.	Unit
Total Sensor Noise (Note 1)	$V_{n-TOTAL}$	−	0.5	−	mV, rms
Dynamic Range (Note 2)	DR	−	−	58	dB

1. Includes amplifier noise and dark current shot noise at data rates of 10 MHz. The number is based on the full bandwidth of the amplifier. It can be reduced when a low pass filter is used.
2. Uses 20 Log (V_{SAT} / $V_{n-TOTAL}$) where V_{SAT} refers to the output saturation signal.

TYPICAL PERFORMANCE CURVES

Color with Microlens Quantum Efficiency

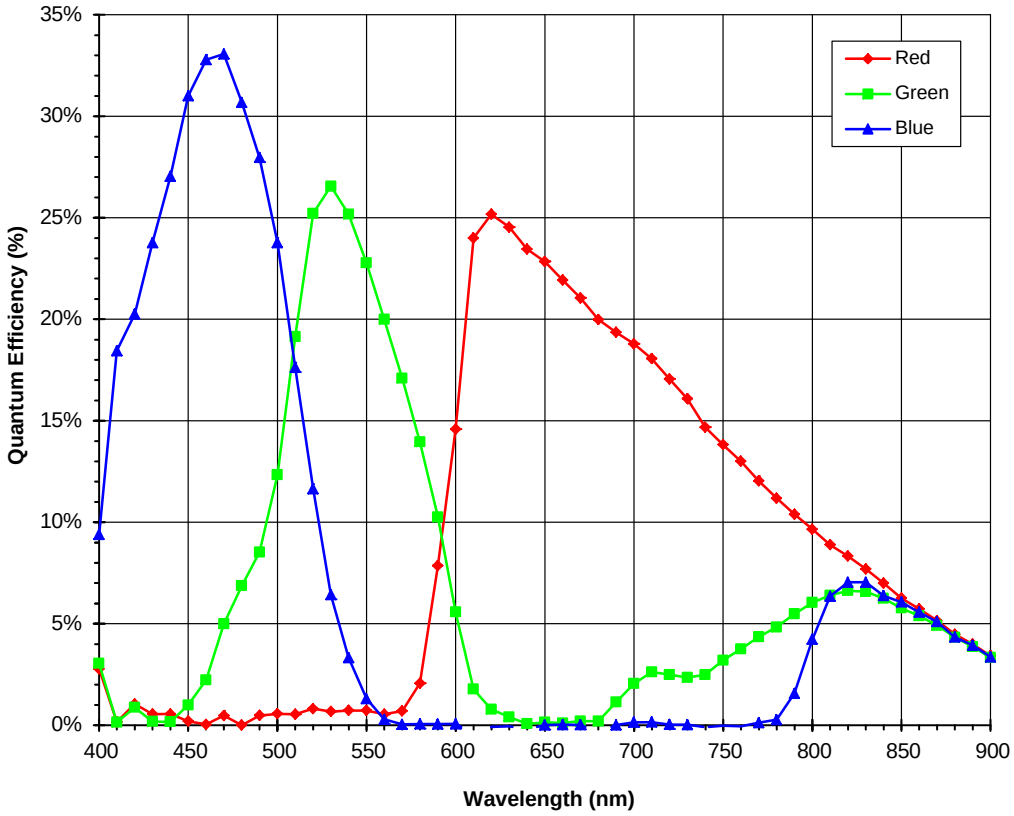


Figure 5. Nominal KAI−0330−CBA Spectral Response

Monochrome with Microlens Quantum Efficiency

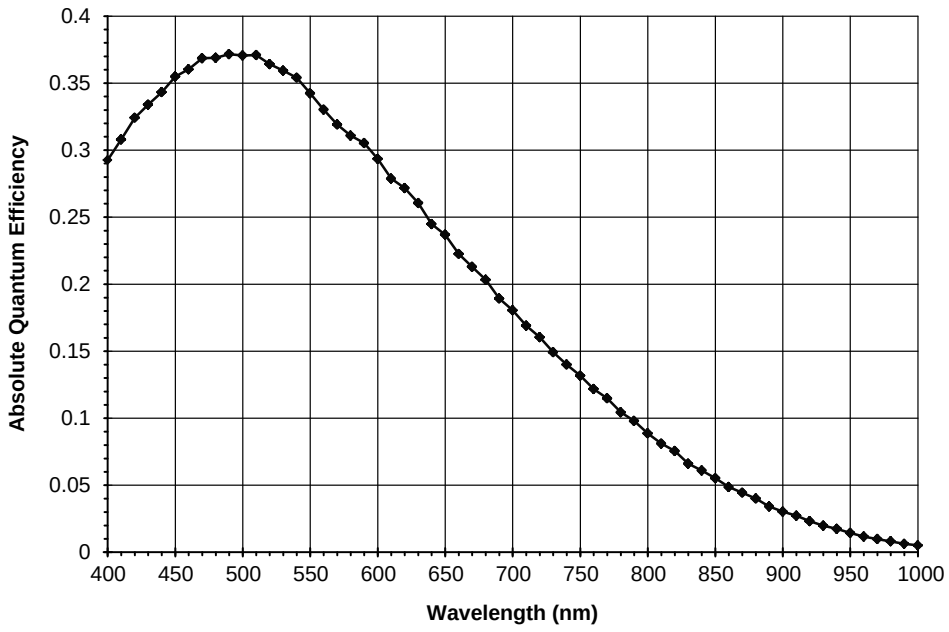


Figure 6. Nominal KAI−0330−ABA Spectral Response

Angular Quantum Efficiency

Monochrome with Microlens

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

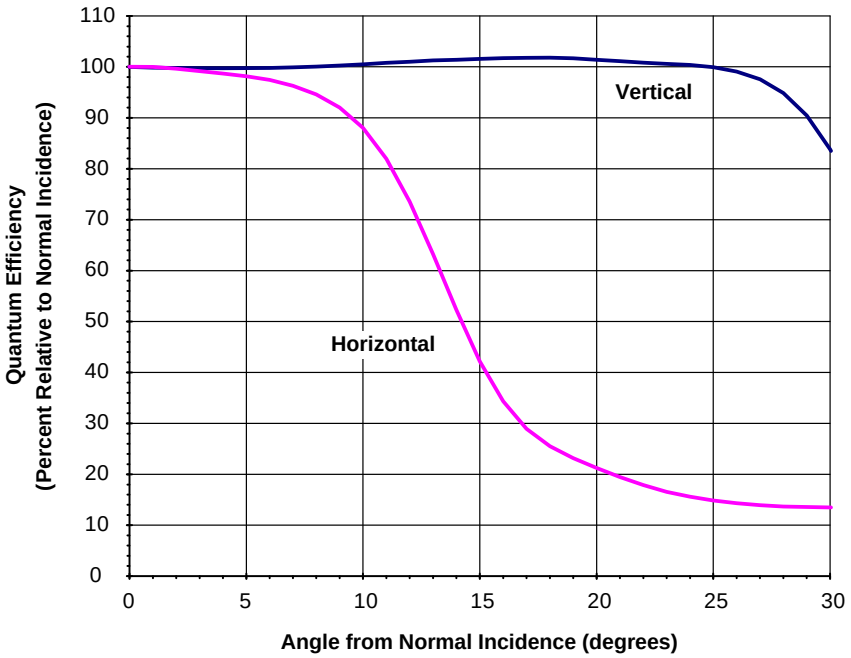


Figure 7. Angular Dependence on Quantum Efficiency

Typical Photoresponse

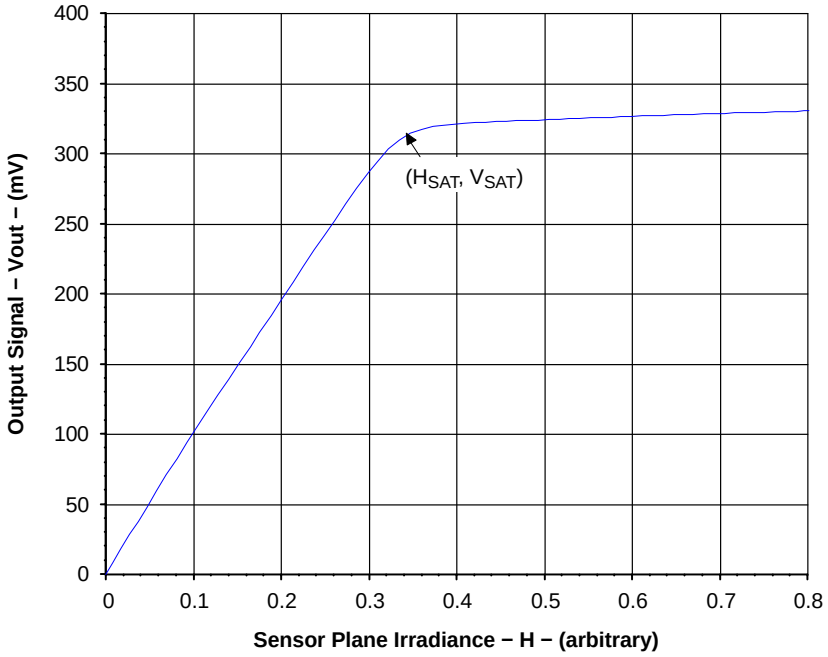


Figure 8. Typical KAI−0330 Photoresponse

Saturation Signal vs. Substrate Voltage

As V_{SUB} is decreased, V_{SAT} increases and anti-blooming protection decreases.
As V_{SUB} is increased, V_{SAT} decreases and anti-blooming protection increases.

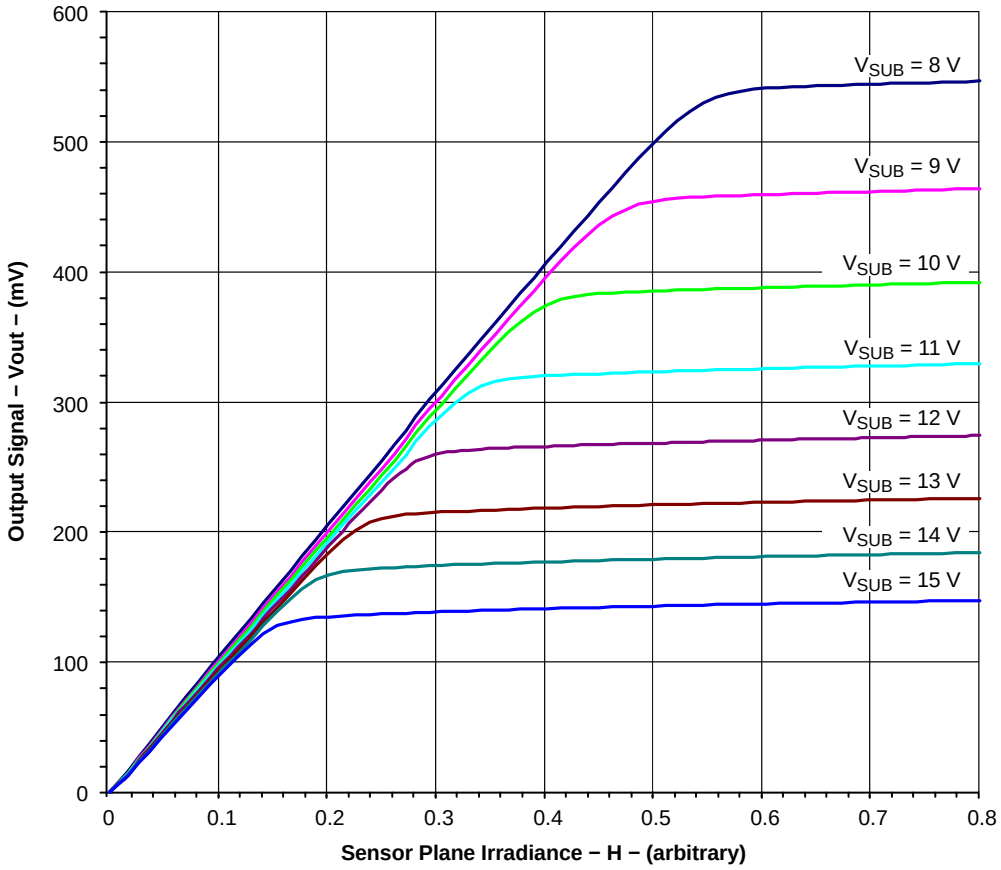


Figure 9. Example of V_{SAT} vs V_{SUB}

Frame Rate

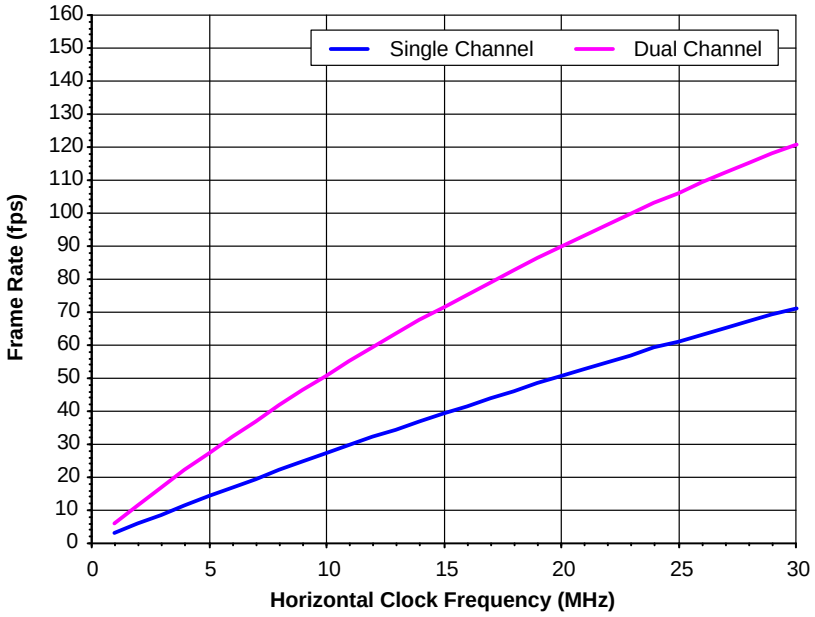


Figure 10. Frame Rate vs. Horizontal Clock Frequency

DEFECT DEFINITIONS

Table 10. OPERATIONAL CONDITIONS

Description	Symbol	Condition
Junction Temperature	T_J	40°C
Integration Time	t_{INT}	40 ms
Readout Rate	$t_{READOUT}$	40 ms

Table 11. SPECIFICATIONS

Point Defects (Major)	Point Defects (Minor)	Cluster Defects	Column Defects
≤ 2	≤ 15	0	0

Table 12. DEFECT DEFINITIONS

Defect Type	Defect Definition
Major Defective Pixel	A pixel whose signal deviates by more than 25 mV from the mean value of all active pixels under dark field condition or by more than 15% from the mean value of all active pixels under uniform illumination at 80% of saturation.
Minor Defective Pixel	A pixel whose signal deviates by more than 6 mV from the mean value of all active pixels under dark field condition.
Point Defect	An isolated defective pixel.
Cluster Defect	A group of 2 to 4 contiguous major defective pixels.
Column Defect	A group of more than 4 contiguous major defective pixels along a single column or row.

NOTE: No row defect are allowed.

OPERATION

Table 13. ABSOLUTE MAXIMUM RATINGS

Rating	Description	Min.	Max.	Unit	Notes
Temperature (@ 10% ±5%RH)	Operation Without Damage	−50	70	°C	
Voltage (Between Pins)	SUB−WELL	0	40	V	1, 5
	V_{RD}, V_{DD}, OG & V_{SS} − WELL	0	15	V	2
	V_{OUTA} & V_{OUTB} – WELL	0	15	V	2
	ϕV1 − ϕV2	−12	20	V	2
	ϕH1A, ϕH1B − ϕH2	−12	15	V	2
	ϕH1A, ϕH1B, ϕH2, FDG − ϕV2	−12	15	V	2
	ϕH2 − OG & V_{SS}	−12	15	V	2
	ϕR – SUB	−20	0	V	1, 2, 4
	All Clocks – WELL	−12	15	V	2
Current	Output Bias Current (I_{OUT})	−	10	mA	3

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Under normal operating conditions the substrate voltage should be above +7 V, but may be pulsed to 40 V for electronic shuttering.
2. Care must be taken in handling so as not to create static discharge which may permanently damage the device.
3. Per Output, I_{OUT} affects the band-width of the outputs.
4. ϕR should never be more positive than V_{SUB}.
5. Refer to Application Note *Using Interline CCD Image Sensors s in High Intensity Visible Lighting Conditions*.

DC Operating Conditions

Table 14. DC OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Pin Impedance
Reset Drain	V_{RD}	8.5	9	9.5	V	5 pF, > 1.2 MΩ
Reset Drain Current	I_{RD}	−	0.2	−	mA	
Output Amplifier Return & OG	V_{SS}	−	0	−	V	30 pF, > 1.2 MΩ
Output Amplifier Return Current	I_{SS}	−	5	−	mA	
Output Amplifier Supply	VDD	12	15.0	15.5	V	30 pF, > 1.2 MΩ
Output Bias Current (Note 4)	I_{OUT}	−	5	10	mA	
P-Well (Note 1)	WELL	−	0.0	−	V	Common
Ground (Note 1)	GND	−	0.0	−	V	
Fast Dump Gate (Note 2)	FDG	−5.5	−5.0	−4.5	V	20 pF, > 1.2 MΩ
Substrate (Notes 3, 7)	SUB	7	V_{SUB}	15	V	1 nF, > 1.2 MΩ

1. The WELL and GND pins should be connected to P-well ground.
2. The voltage level specified will disable the fast dump feature.
3. This pin may be pulsed to V_{ES} = 40 V for electronic shuttering.
4. Per output. Note also that I_{OUT} affects the bandwidth of the outputs.
5. Pins shown with impedance greater than 1.2 MΩ are expected resistances. These pins are only verified to 1.2 MΩ.
6. The operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
7. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

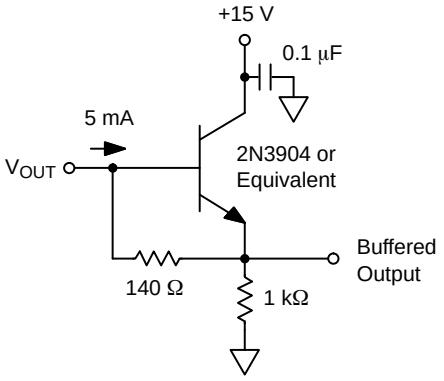


Figure 11. Recommended Output Structure Load Diagram

AC Clock Level Conditions

Table 15. CLOCK LEVELS

Description	Symbol	Level	Min.	Nom.	Max.	Unit	Pin Impedance
Vertical CCD Clock	ϕV1	Low	−10.0	−9.5	−9.0	V	25 nF, > 1.2 MΩ
		Mid	0.0	0.2	0.4	V	
		High	8.5	9.0	9.5	V	
Vertical CCD Clock	ϕV2	Low	−10.0	−9.5	−9.0	V	25 nF, > 1.2 MΩ
		High	0.0	0.2	0.4	V	
ϕ1 Horizontal CCD A Clock	ϕH1A	Low	−7.5	−7.0	−6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
ϕ1 Horizontal CCD B Clock (Single Register Mode) (Note 4)	ϕH1B	Low	−7.5	−7.0	−6.5	V	100 pF, > 1.2 MΩ
ϕ1 Horizontal CCD B Clock (Dual Register Mode) (Note 4)	ϕH1B	Low	−7.5	−7.0	−6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
ϕ2 Horizontal CCD Clock	ϕH2	Low	−7.5	−7.0	−6.5	V	125 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
Reset Clock	ϕR	Low	−6.5	−6.0	−5.5	V	5 pF, > 1.2 MΩ
		High	−0.5	0.0	0.5	V	
Fast Dump Gate Clock (Note 3)	ϕFDG	Low	−5.5	−5.0	−4.5	V	20 pF, > 1.2 MΩ
		High	4.5	5.0	5.5	V	

1. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
2. Pins shown with impedance greater than 1.2 MΩ are expected resistances. These pins are only verified to 1.2 MΩ.
3. When not used, refer to DC operating condition.
4. For single register mode, set ϕH1B to −7.0 V at all times rather than clocking it.

This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult ON Semiconductor in those situations in which operating conditions meet or exceed minimum or maximum levels.

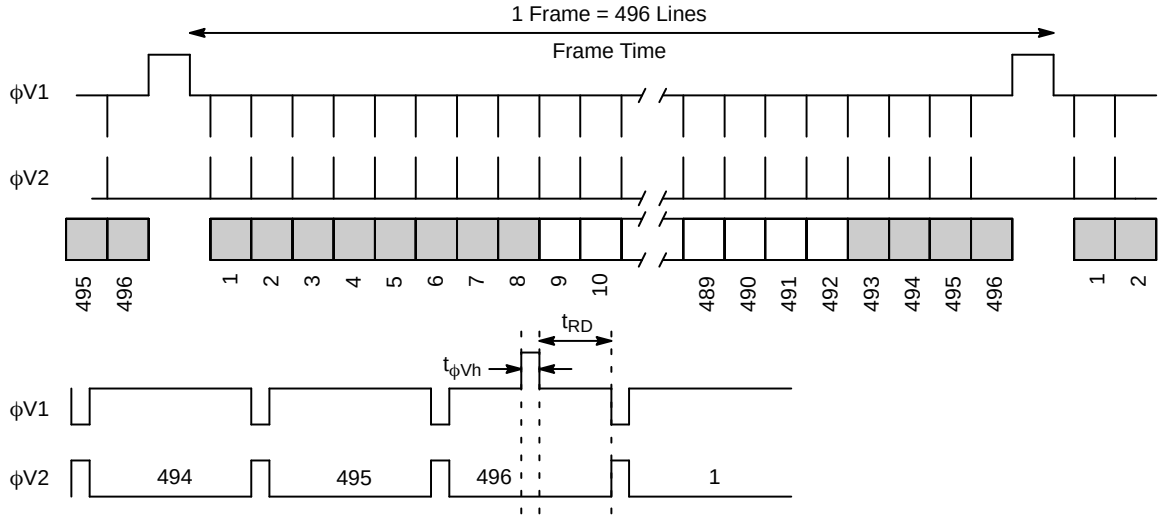
TIMING

Table 16. REQUIREMENTS AND CHARACTERISTICS (For 30 MHz Operation)

Description	Symbol	Min.	Nom.	Max.	Unit	Figure
Reset Pulse Width	$t_{\phi R}$	−	10	−	ns	Figure 14
Electronic Shutter Pulse Width	t_{ES}	10	25	−	μs	Figure 15
Integration Time (Note 1)	tI_{NT}	0.1	−	−	ms	Figure 15
Photodiode to VCCD Transfer Pulse Width (Note 2)	$t_{\phi Vh}$	4	5	−	μs	Figure 12
Clamp Delay	t_{CD}	−	15	−	ns	Figure 14
Clamp Pulse Width	t_{CP}	−	15	−	ns	Figure 14
Sample Delay	t_{SD}	−	35	−	ns	Figure 14
Sample Pulse Width	t_{SP}	−	15	−	ns	Figure 14
Vertical Readout Delay	t_{RD}	10	−	−	μs	Figure 12
ϕV1, ϕV2 Pulse Width	$t_{\phi V}$	2	2.5	−	μs	Figure 13
ϕH1A, ϕH1B, ϕH2	Clock Frequency $t_{\phi H}$	−	−	30	MHz	Figure 14
Line A to Line B Transfer Pulse Width	$t_{\phi AB}$	2	2.5	−	μs	Figure 17
Horizontal Delay	$t_{\phi Hd}$	2	2.5	−	μs	Figure 13
Vertical Delay	$t_{\phi Vd}$	25	−	−	ns	Figure 13
Horizontal Delay with Electronic Shutter	$t_{\phi HVES}$	1	−	−	μs	Figure 15

1. Integration time varies with shutter speed. It is to be noted that smear increases when integration time decreases below readout time (frame time). Photodiode dark current increases when integration time increases, while CCD dark current increases with readout time (frame time).
2. Anti-blooming function is off during photodiode to VCCD transfer.

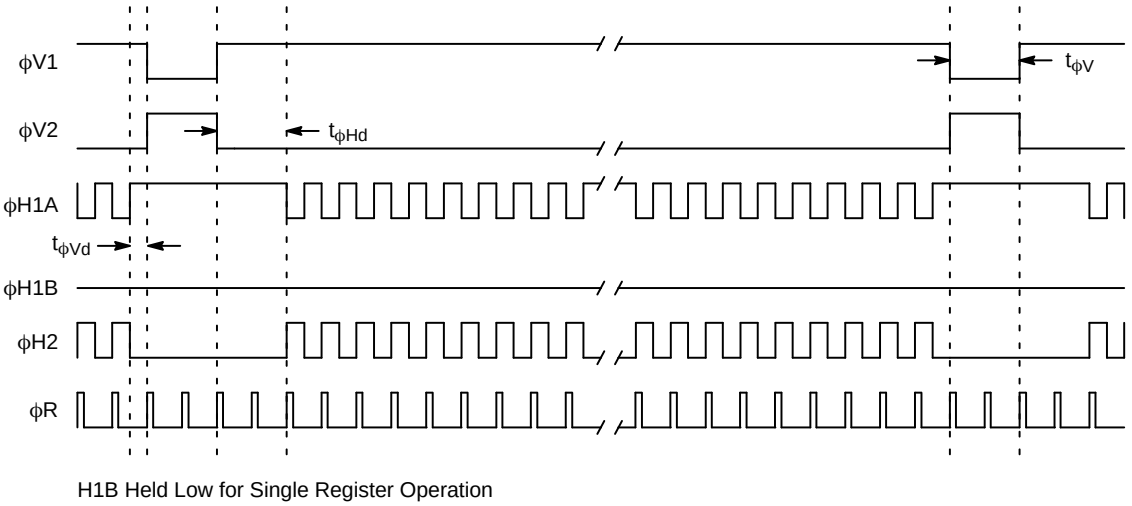
Frame Timing − Single Register Readout



NOTE: When no electronic shutter is used, the integration time is equal to the frame time.

Figure 12. Frame Timing Diagram − Single Register Readout

Line Timing − Single Register Readout



Line Content

Figure 13. Line Timing Diagram − Single Register Output

Pixel Timing − Single Register Readout

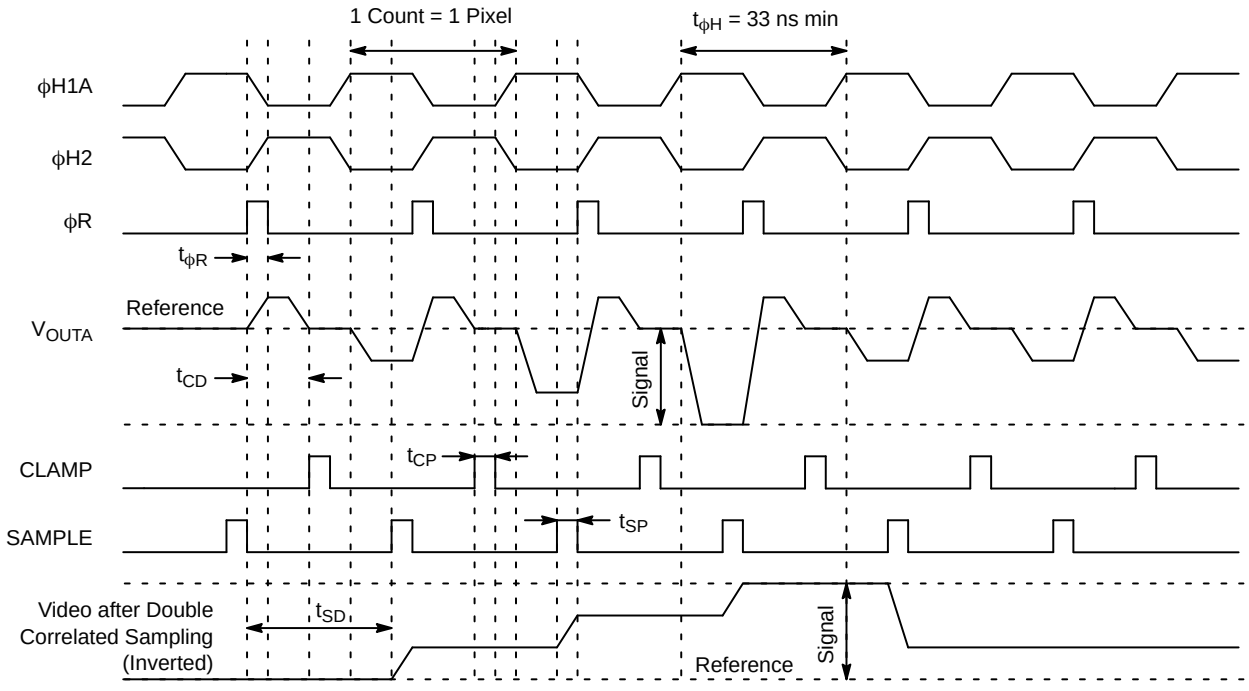
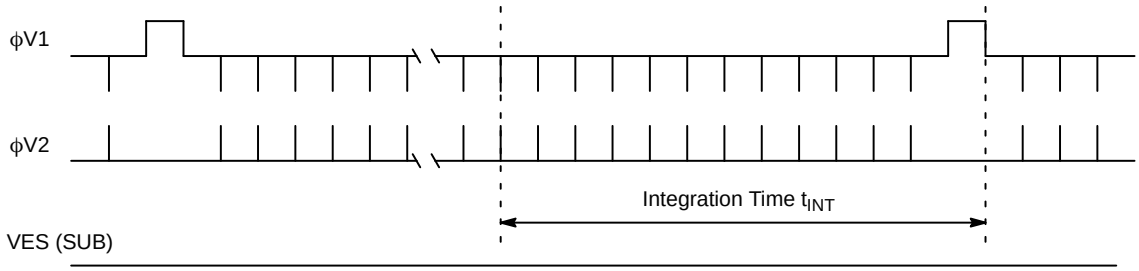


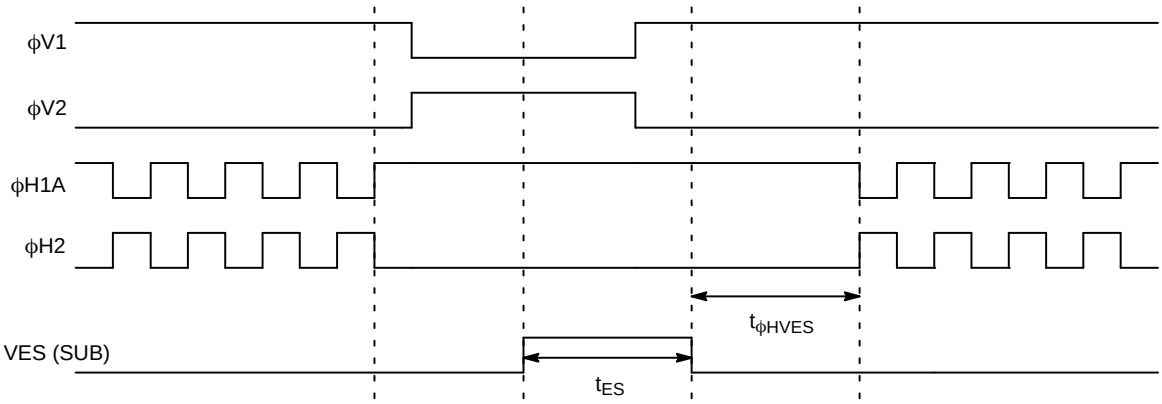
Figure 14. Pixel Timing Diagram − Single Register Readout

Electronic Shutter Timing − Single Regulator Readout

Frame Timing



Placement



Operating Voltages

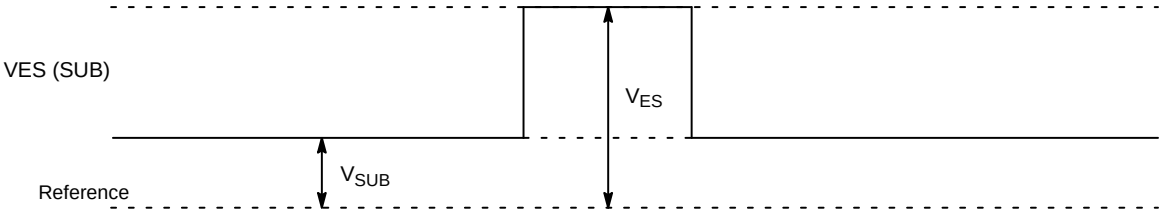
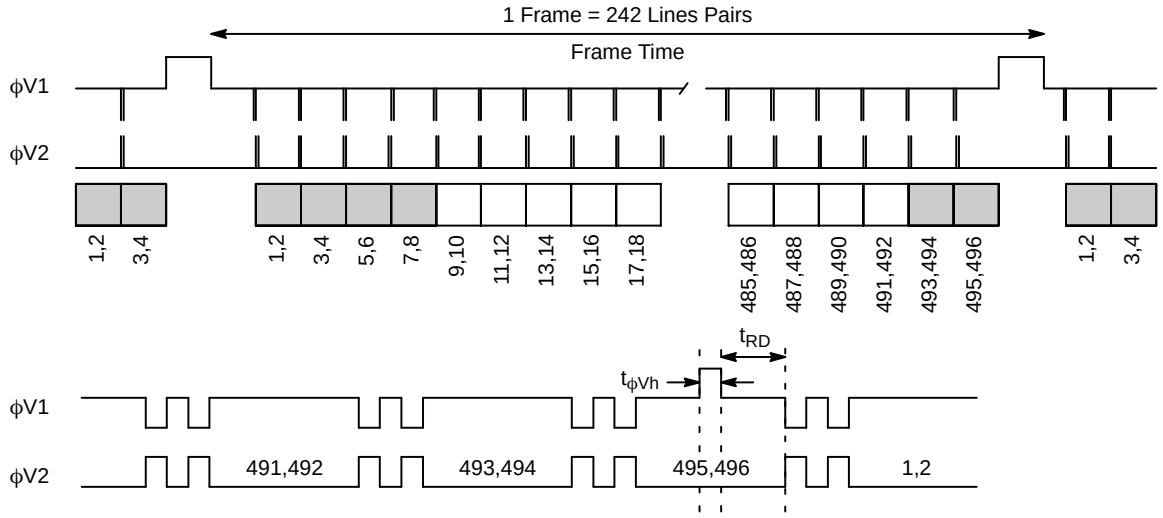


Figure 15. Electronic Shutter Timing Diagram − Single Register Readout

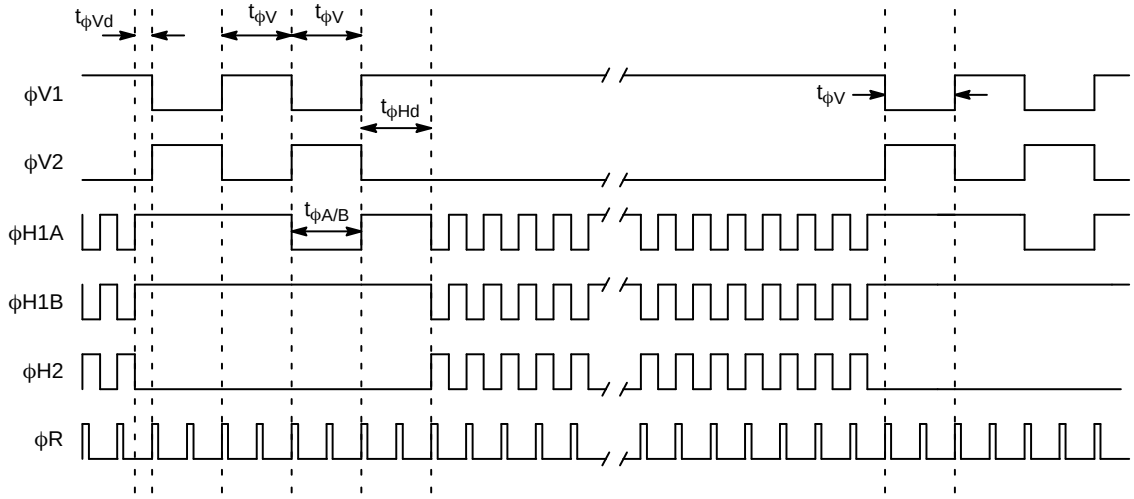
Frame Timing − Dual Register Readout



NOTE: When no electronic shutter is used, the integration time is equal to the frame time.

Figure 16. Frame Timing Diagram − Dual Register Readout

Line Timing − Dual Register Readout



Line Content

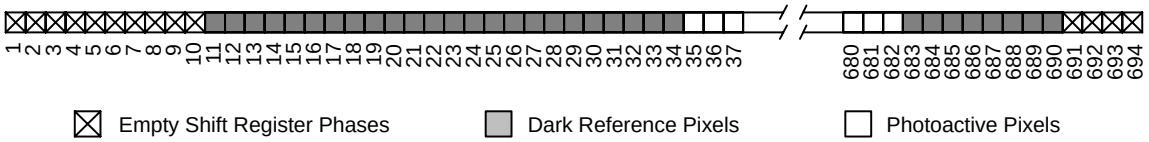


Figure 17. Line Timing Diagram − Dual Register Output

Pixel Timing − Dual Register Readout

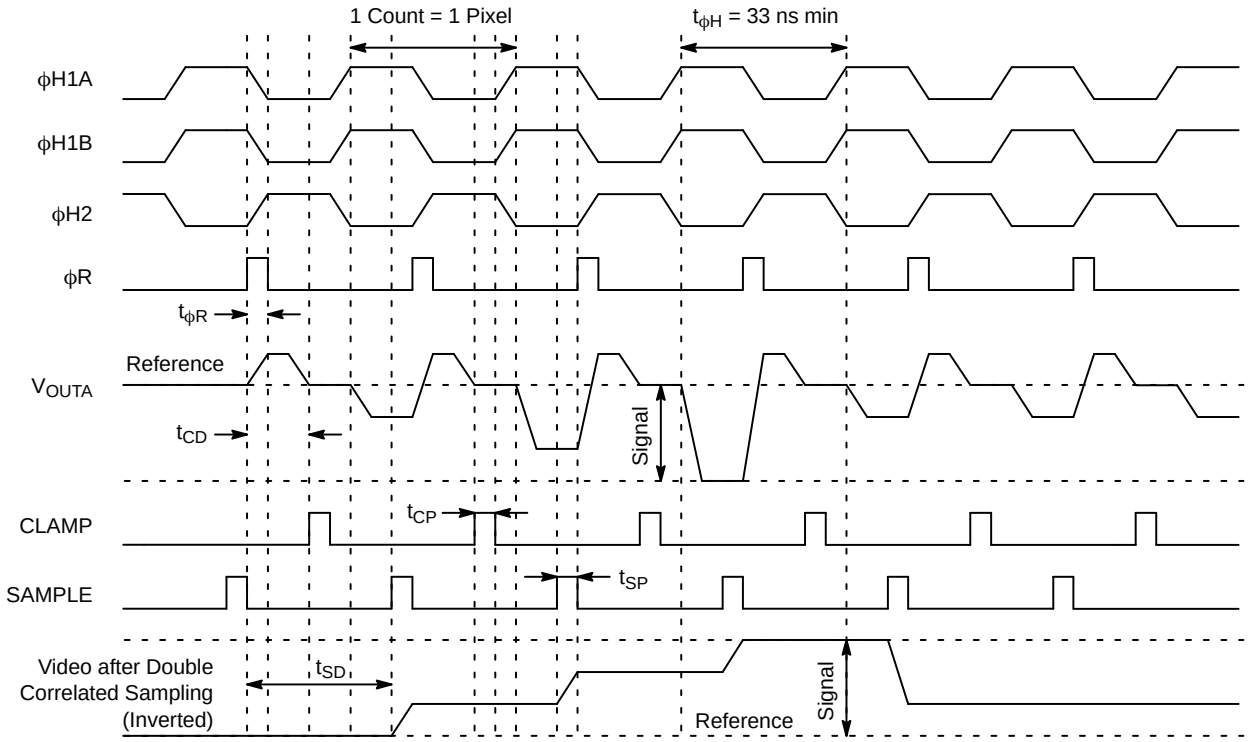


Figure 18. Pixel Timing Diagram − Dual Register Readout

Fast Line Dump Timing − Removing Four Lines

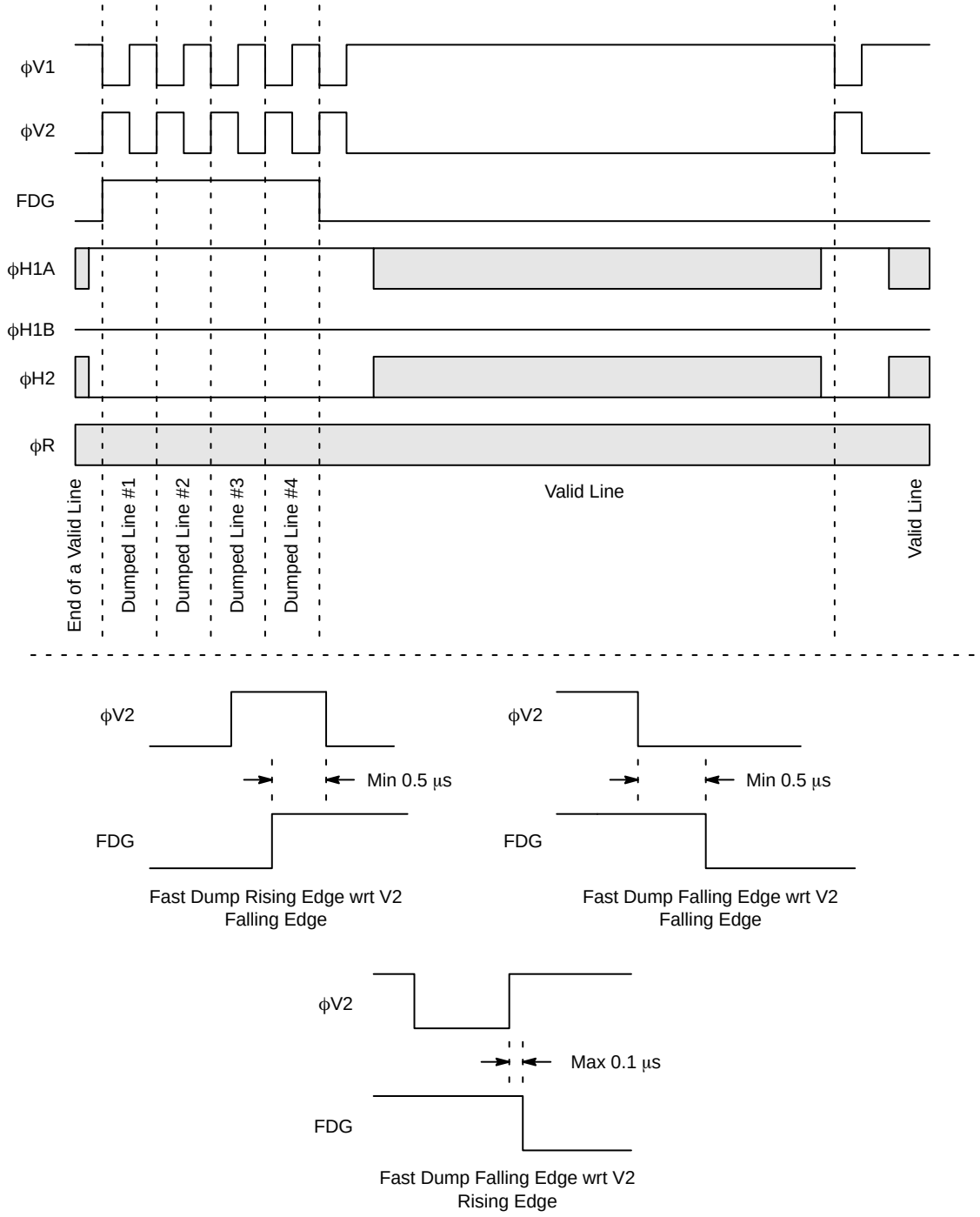


Figure 19. Fast Line Dump Timing − Removing Four Lines

Binning − Two to One Line Binning

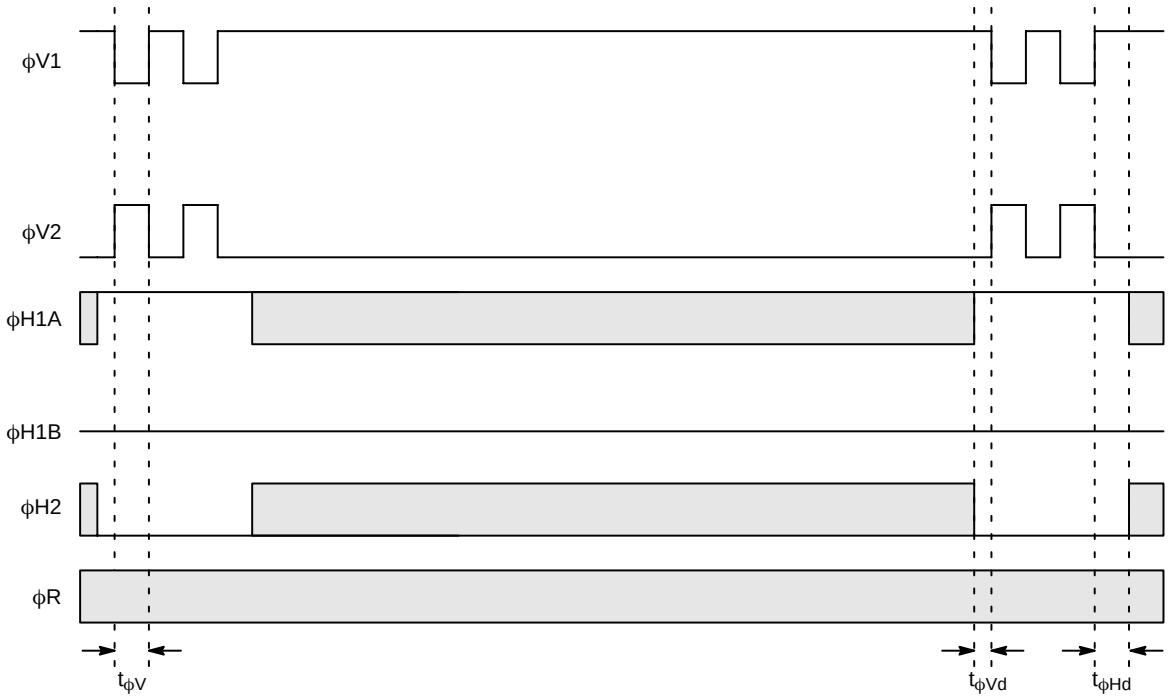


Figure 20. Binning − 2 to 1 Line Binning

Timing − Sample Video Waveform

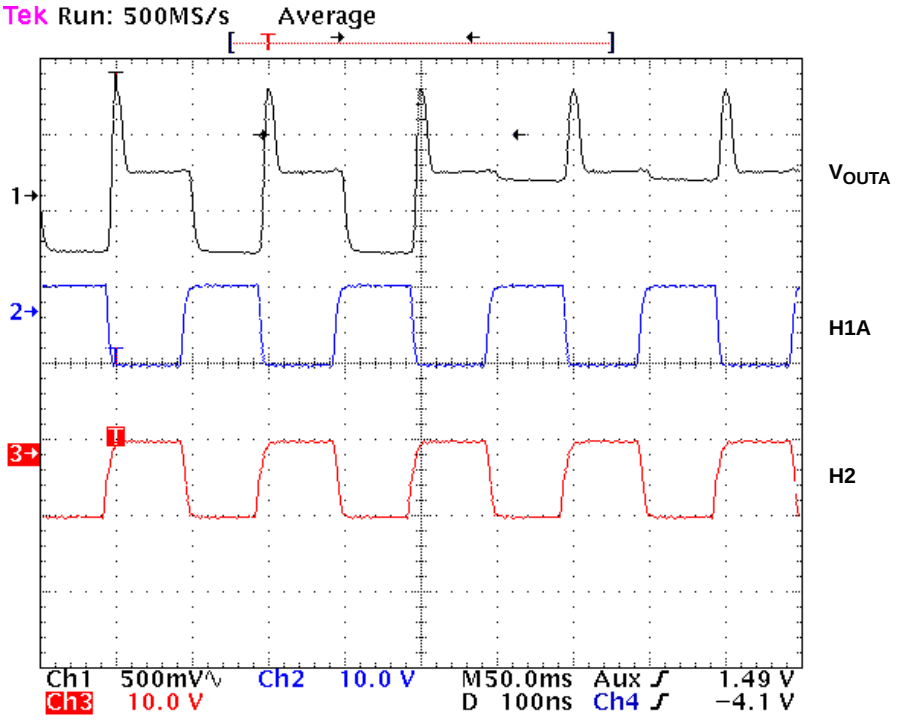


Figure 21. Sample Video Waveform at 5 MHz

STORAGE AND HANDLING

Table 17. CLIMATIC REQUIREMENTS

Item	Description	Min.	Max.	Units	Conditions	Notes
Operation to Specification	Temperature	−25	40	°C	@ 10% ±5% RH	1, 2
	Humidity	10±5	86±5	% RH	@ 36±2°C Temp.	1, 2
Storage	Temperature	−55	70	°C	@ 10% ±5% RH	2, 4
	Humidity	−	95±5	% RH	@ 49±2°C Temp.	2, 4

1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
3. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
4. The image sensor shall meet the specifications of this document after storage for 15 days at the specified conditions.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

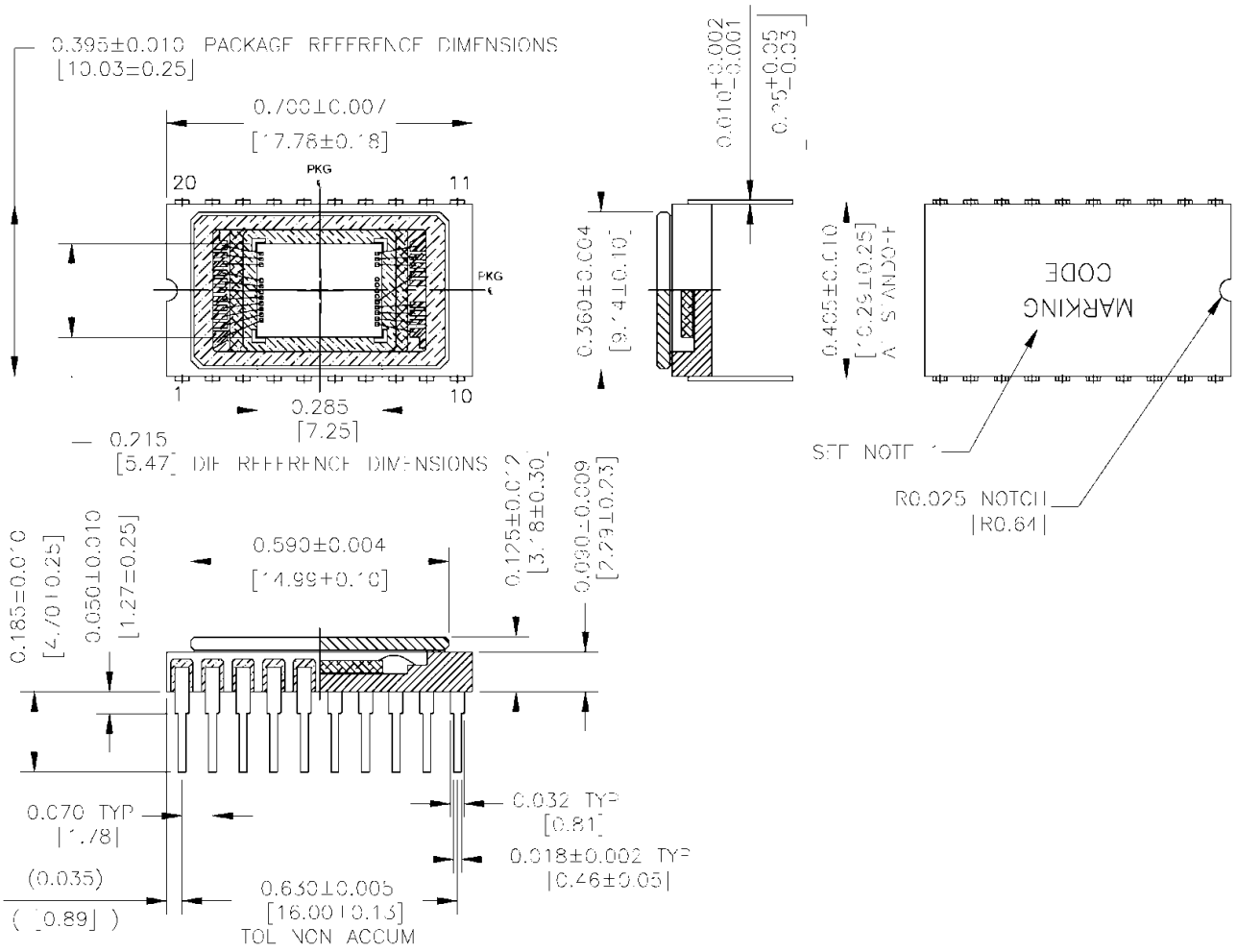
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

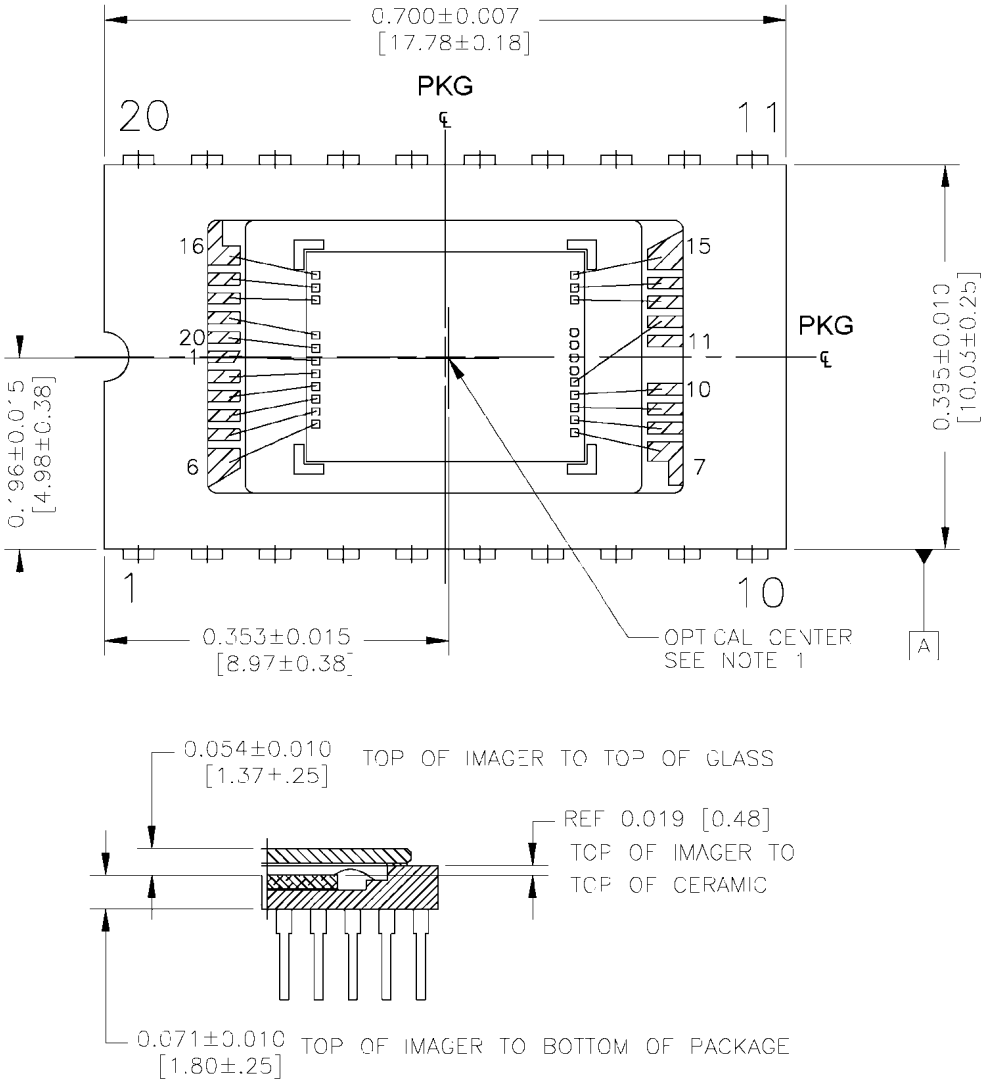
MECHANICAL INFORMATION

Completed Assembly



Notes:
1. See Ordering Information for Marking Code.
2. Cover Glass is visually aligned over die – location accuracy is not guaranteed.
3. Units: Inches [mm].

Figure 22. Completed Assembly (1 of 2)

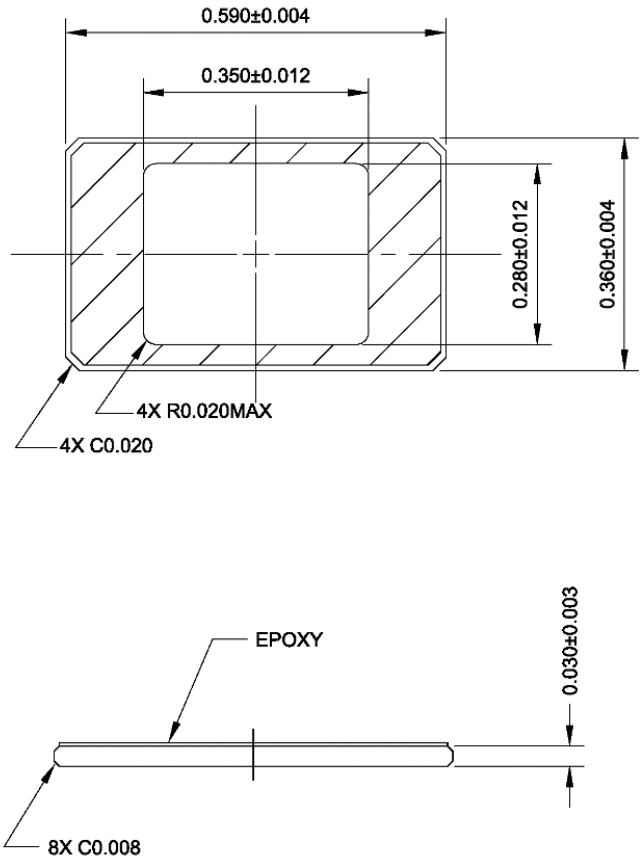


Notes:

1. Center of image area is offset from center of package by (0.08, −0.04) mm nominal.
2. Die is visually aligned within ±2° of datum A.
3. Units: Inches [mm].

Figure 23. Completed Assembly (2 of 2)

Cover Glass



Notes:
1. Dust/Scratch Count: 5 microns max
2. Units: Inches

Figure 24. Cover Glass Drawing

Cover Glass Transmission

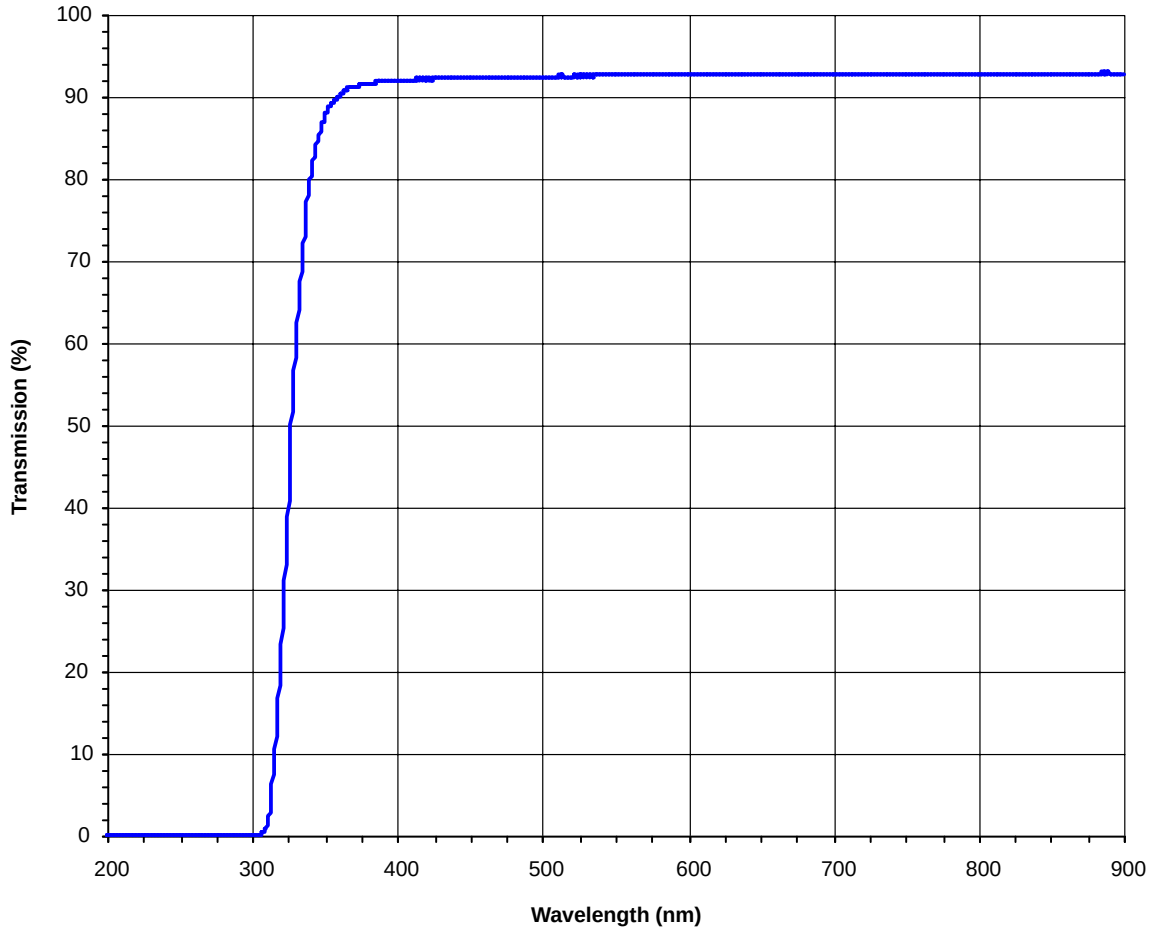


Figure 25. Cover Glass Transmission

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А